VECTRON INTERNATIONAL
A DOVER TECHNOLOGIES COMPANY

S-Type
Voltage Controlled Crystal Oscillator

The S-Type Voltage Controlled Crystal Oscillator

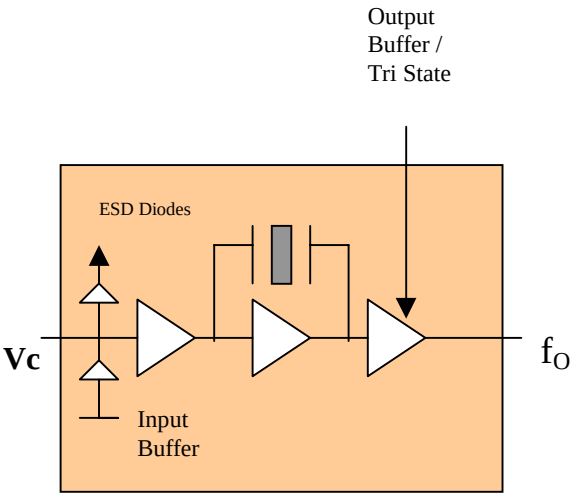


Figure 1

Features

- Output Frequencies to 65.536MHz
- 5 or 3.3 Vdc operation
- Tri-State Output
- Low jitter < 6pS rms (for freq >12MHz)
- VCXO with CMOS outputs
- 0/70 or –40/85 °C temperature range
- Hermetically sealed ceramic SMD package

Applications

- SONET/SDH
- xDSL
- Digital Video
- Low jitter PLL's

Description

The VI S-Type Voltage Controlled Crystal Oscillator (VCXO) is a quartz stabilized square wave generator with a CMOS output and is tested at CMOS (3.3 and 5V operation) and TTL (5 V operation) logic levels. Devices are tested for absolute pull range (APR) and start-up over the operating temperature range which insures the performance and reliability.

Performance Characteristics

Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Supply Voltage [1] (+5 or +3.3 V)	V_{DD}	0.9*V_{DD}		1.1*V_{DD}	V
Supply Current	I_{DD}	10mA +0.25mA/MHz			mA
Output Logic Levels Output Logic High[2] Output Logic Low[2]	 V_{OH} V_{OL}	 0.8*V_{DD}		 0.1V_{DD}	 V V
Transition Times Rise Time[2] Fall Time[2]	 t_R t_F			 5 5	 ns ns
Symmetry or Duty Cycle[3]	SYM			45/55	%
Nominal Output Frequency Options	f_O	1.024		65.536	MHz
Test Conditions for APR (+5V option)	V_C	0.5		4.5	V
Test Conditions for APR (+3.3V option)	V_C	0.3		3.0	V
Absolute Pull Range (*ordering option*)	APR	*50,80 or 100*			ppm
Gain Transfer		Positive			
Operating temperature (*ordering option*)		0/70 or –40/85			°C
Control Voltage Leakage Current	I_{VCXO}			±1	uA
Control Voltage Bandwidth (-3dB)	BW	10			KHz

1. A 0.01uF capacitor should be located as close to the supply as possible (to ground) and a 0.1uF is also recommended.
2. Figure 1 defines these parameters. Figure 2 illustrates the equivalent five gate TTL load and operating conditions under which these parameters are tested and specified.
3. Symmetry is defined as (ON TIME/PERIOD with Vs=-1.4 V for TTL and Vs=2.5 V for CMOS, 5 volt operation, and Vs=1.65V for 3.3 Volt operation. TTL/CMOS pin should be grounded for frequencies <12MHz.

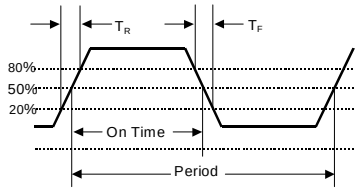


Figure 2. Output Waveform

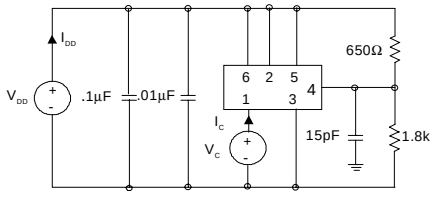


Figure 3. Output Test Conditions (25±5°C)

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	7	Vdc
Storage Temperature	Tstorage	-55/125	°C
Voltage Control Range	V_C	0 to V_{DD}	V

Qualification Conformance

The S-Type has undergone the following Mil-Std qualification.

Table 3. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883C 2002.3, TEST B
Mechanical Vibration	MIL-STD-883C 2007.1, TEST C
Solderability	MIL-STD-883C 2003.5
Gross and Fine Leak	MIL-STD-883C 1014.7, 100% Tested
Resistance to Solvents	MIL-STD-883C 2016

Handling Precautions

Although ESD protection circuitrry has been designed into the the S-Type, proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance=1.5Kohms and capacitance = 100pF is widely used and Therefore can be used for comparison purposes.

Table 4. ESD Ratings

Model	Minimum
Human Body Model	1500 V (Mil-STD-883D, Method 3015, Class 1)
Charged Device Model	1500 V

Absolute Pull Range (APR) Specification

The frequency deviation of the S-Type VCXO is specified in terms of Absolute Pull Range (APR). APR provides the user with a guaranteed specification for minimum available frequency deviation over all operating conditions. Operating conditions include operating temperature range, power supply variation, differences in output loading and changes due to aging.

An S-Type VCXO with an APR of +/-50 ppm will track a +/-50 ppm reference source over all operating conditions. The same device will typically demonstrate a Total Pull capability of 150 to 350 ppm. Absolute Pull Range (APR) is specified by the fourth character of the product code in Table 6. *Please see Vectron's web site, **www.vectron.com**, for the APR Application Note.*

Oscillator Aging

Quartz stabilized oscillators typically exhibit a small shift in output frequency during aging. The major factors which lead to this shift are changes in the mechanical stress on the crystal and mass-loading of foreign material on the crystal.

As the oscillator ages, relaxation of the crystal mounting stress or transfer of environmental stress through the package to the crystal mounting arrangement can lead to frequency variations. VI has minimized these two effects through the use of a miniature AT-Cut strip resonator crystal which allows a superior mounting arrangement and results in minimal relaxation and almost negligible environmental stress transfer.

Oscillator Aging

Mass-loading on the crystal generally results in a frequency decrease and is typically due to out-gassing of material within a hermetic package or from contamination by external material in a less than hermetic package. VI has minimized the impact of mass loading by ensuring hermetic integrity and minimizing out-gassing by limiting the number of internal components through the use of ASIC technology.

Under normal operating conditions with an operating temperature of 40°C, the S-Type will typically exhibit 2 ppm aging in the first year of operation. The device will then typically exhibit 1 ppm aging the following year with a logarithmic decline each year thereafter.

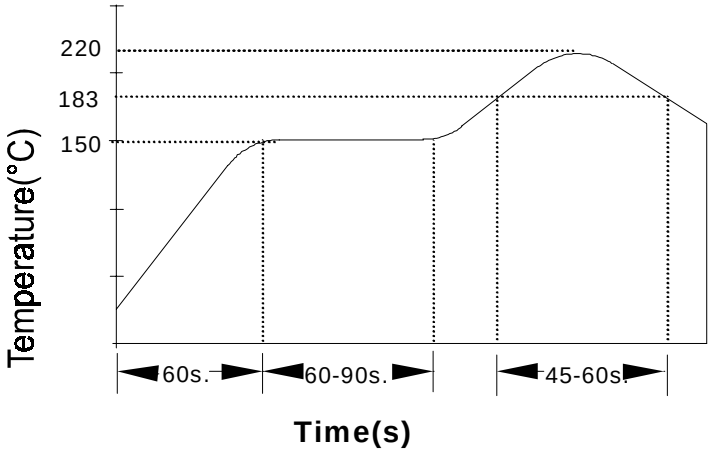


Figure 4. Suggested IR profile

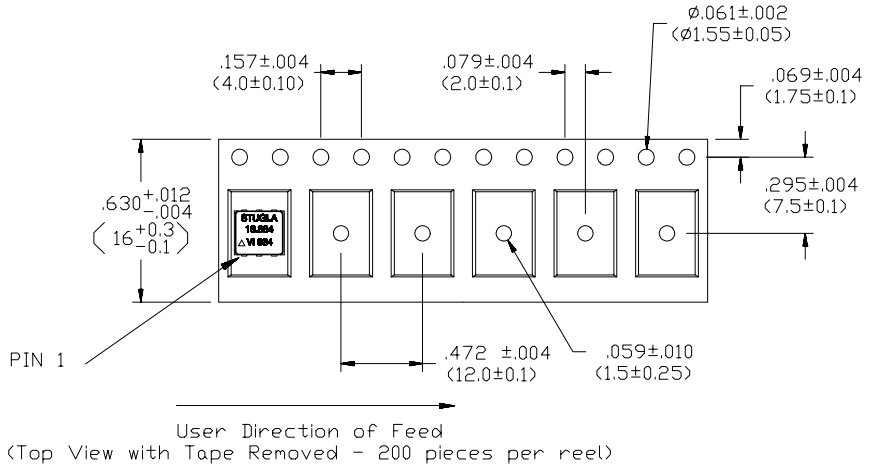


Figure 5. Tape and Reel

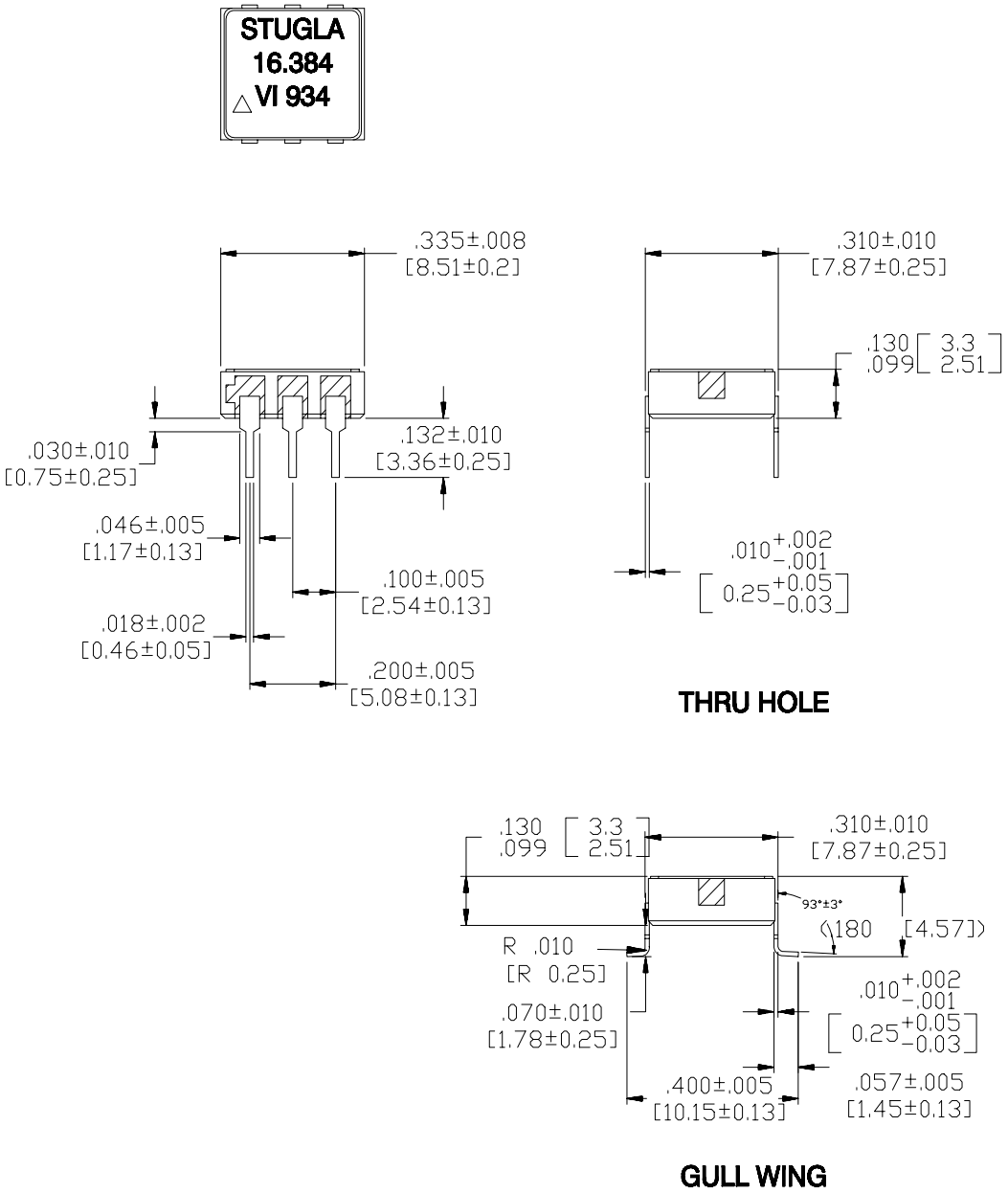
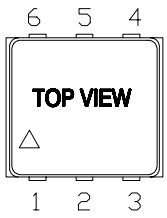


Figure 6. Outline Diagram

Table 5. Pin Function

Pin	Symbol	Function
1	V_C	VCXO Control Voltage
2	Tri-State	TTL Low to Disable Output. TTL High, or no connect, to Enable Output.
3	GND	Case Ground
4	Output	VCXO Output
5	TTL/CMOS	TTL Logic Low for CMOS optimized symmetry. TTL Logic High, or no connect, for TTL optimized symmetry.
6	V_{DD}	Power Supply Voltage (3.3 V ±10% or 5.0 V ±10%)



Ordering information

Table 6. Standard Frequencies

1.024	1.544	2.000	2.048	3.088	3.580	3.686	4.000	4.032	4.096
4.434	5.000	5.760	6.144	6.176	6.312	6.400	8.000	8.192	8.448
9.192	10.000	11.000	11.2896	11.290	12.000	12.288	12.352	12.900	13.000
13.500	14.318	15.360	15.440	16.000	16.123	16.384	17.734	18.432	19.440
19.985	20.000	20.480	24.000	24.576	24.704	27.000	30.000	32.000	32.768
34.368	35.328	38.880	40.000	40.960	44.736	50.000	51.840	52.000	

Other frequencies may be available upon request

Table 7. Part number ordering information

S G U G L A - 44.736 (frequency in MHz)

Package Size

S-Type

Supply Voltage

T: Thru hole

G: Gull Wing

Output, Symmetry

U: VCXO, +5V, standard linearity

L: VCXO, +5V, 10% linearity

D: VCXO, +3.3V, standard linearity

K: VCXO, +3.3V, 10% linearity

Symmetry

A: 45/55%

Temperature Range

C: 0 to 70°C

L: -40 to 85 °C

Absolute Pull Range (Stability XO)

G: ±50 ppm

N: ±80 ppm

H: ±100 ppm

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