PRELIMINARY PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

# LHF00L01

## Flash Memory

### 16M (2Mb × 8)

(Model No.: LHF00L01)

Spec No.: LHF00L01

Issue Date: August 5, 2003

SHARP

| Date | Aug. 5. 2003 |
|---|---|

PRELIMINARY DATASHEET

# DATASHEET

**PRODUCT :** 16M (x8) Flash Memory

**MODEL NO :** ***LHF00L01***

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

# LHF00L01
# 16Mbit (2Mbit×8)
# LPC Flash MEMORY

■ Conforms to Intel LPC Interface Specification 1.0

■ Optimized Array Blocking Architecture
- Thirty 64-KByte Uniform Blocks
- Eight 8-KByte Top Boot Sectors
- Sixteen 4-KByte Bottom Boot Sectors
- Top Boot Sector Data Protection for each 8-KByte sector
- Full Chip Erase for A/A Mode Only

■ $V_{CC}$=3.0V-3.6V Operation

■ Extended Cycling Capability
- Minimum 100,000 Block Erase Cycles

■ Low Power Consumption (LPC Interface)
- Standby Current : 15µA (Max.)
- Read Current : 15mA (Max.)
- Erase or Program Current : 25mA (Max.)

■ Erase or Program Operation
- Byte Program Time : 25µs (Typ.)
- Sector Erase Time : 0.6s (Typ.)
- Block Erase Time : 1.2s (Typ.)
- Full Chip Erase Time : 40s (Typ.)
- Sector Rewrite Time : 0.8s (Typ.)
- Block Rewrite Time : 2.8s (Typ.)

■ Operating Temperature 0°C to +85°C

■ CMOS Process (P-type silicon substrate)

■ Two Operational Modes
- Low Pin Count (LPC) Interface mode for In-System operation
- Address/Address Multiplexed Interface (A/A) Mode for production erasing and programming

■ LPC Interface Mode
- 5 signal communication interface supporting byte Read and Write
- 33MHz clock frequency operation
- WP# and TBL# pins provide hardware data protection for entire chip and/or top boot sector
- Status Polling and Toggle Bit for End-of-Write detection
- 5 GPI pins for system design flexibility
- ID pins for multi-chip selection

■ A/A Interface Mode
- 11 pin multiplexed address and 8-pin data I/O interface
- Supports fast In-System or PROM programming for manufacturing

■ CMOS and PCI I/O Compatibility

■ 32-Lead TSOP (Normal Bend)

■ ETOX$^{TM*}$ Flash Technology

■ Not designed or rated as radiation hardened

* ETOX is a trademark of Intel Corporation.

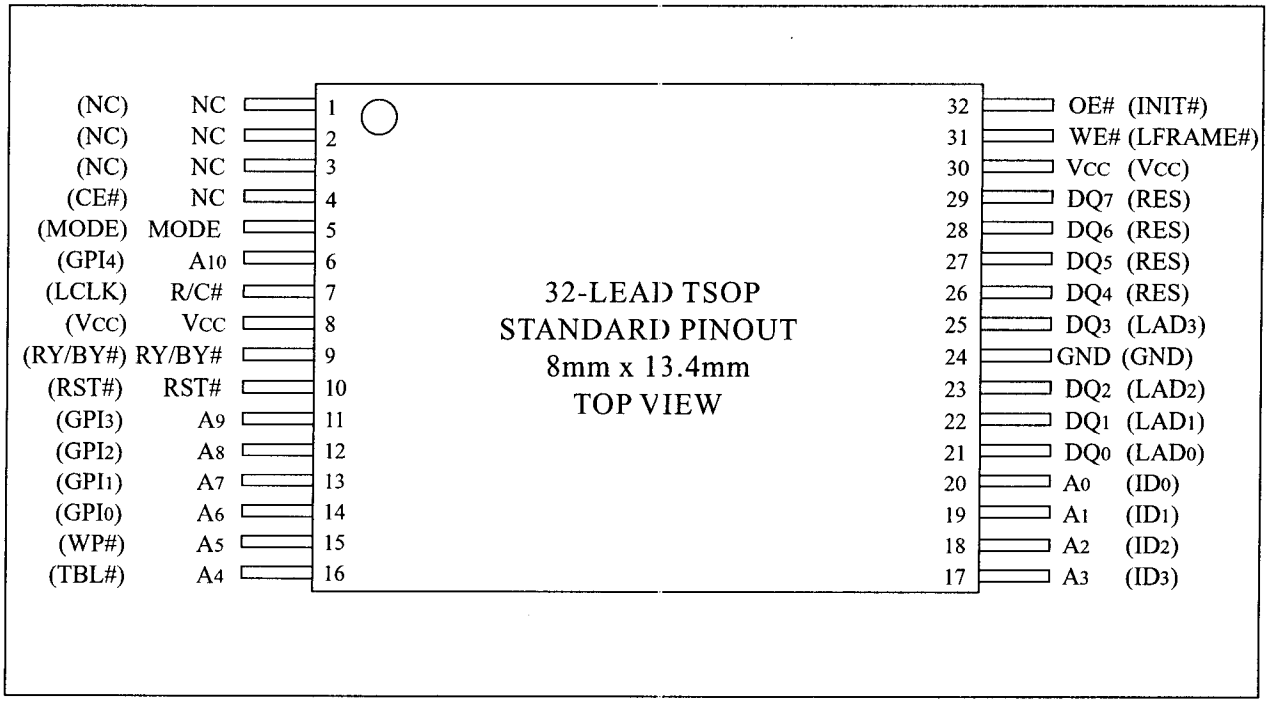



Figure 1. 32-Lead TSOP (Normal Bend) Pinout

Symbols inside ( ) are those for LPC mode.

## 1 Product Description

The product is offered in 32-Lead TSOP (Normal Bend) package. Refer to Figure 1 for pinouts and Table 1 for pin descriptions.

Table 1. Pin Descriptions

| Symbol | Type | Interface | | Name and Function |
|---|---|---|---|---|
| | | A/A | LPC | |
| RST# | INPUT | O | O | RESET: When low ($V_{IL}$), RST# resets internal automation and inhibits erase and program operations, which provides data protection. RST#-high ($V_{IH}$) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. |
| MODE | INPUT | O | O | MODE: This pin determines which interface is operational. This pin must be held high ($V_{IH}$) for A/A mode and low ($V_{IL}$) for LPC mode. This pin is internally pulled-down with a resistor between 20KΩ-100KΩ. |
| INIT# | INPUT | | O | INITIALIZE: This is the second reset pin for in-system use. This pin is internally combined with the RST# pin; If this pin or RST# pin is driven low, identical operation is exhibited. |
| CE# | INPUT | | O | CHIP ENABLE: This signal must be asserted to select the device. When CE# is low, the device is enabled. When CE# is high, the device is placed in low power standby mode. |
| LFRAME# | INPUT | | O | FRAME: To indicate start of a data transfer operation. This pin is also used to abort an LPC cycle in progress. |
| $LAD_3$-$LAD_0$ | INPUT/ OUTPUT | | O | ADDRESS AND DATA: To provide LPC control signals, as well as addresses and command Inputs data/Outputs data. |
| LCLK | INPUT | | O | CLOCK: To provide a clock input to the control unit. |
| $ID_3$-$ID_0$ | INPUT | | O | IDENTIFICATION INPUTS: These four pins are part of the mechanism that allows multiple parts to be attached to the same bus. The strapping of these pins is used to identify the component. These pins are internally pulled-down with a resistor between 20KΩ-100KΩ. |
| $GPI_4$-$GPI_0$ | INPUT | | O | GENERAL PURPOSE INPUTS: These individual inputs can be used for additional board flexibility. The state of these pins can be read through GPI registers. |
| TBL# | INPUT | | O | TOP BOOT LOCK: When low, prevents erasing and programming to the boot sectors at top (highest address) of memory. When TBL# is high, it disables hardware data protection for the top boot sectors. This pin cannot be left unconnected. |
| WP# | INPUT | | O | WRITE PROTECT: When low, prevents erasing and programming to all blocks other than top boot sector. When WP# is high, it disables hardware data protection for these blocks. This pin cannot be left unconnected. |
| RES | | | O | RESERVED: These pins must be left unconnected. |

Table 1. Pin Descriptions (Continued)

| Symbol | Type | Interface | | Name and Function |
|---|---|---|---|---|
| | | A/A | LPC | |
| OE# | INPUT | O | | OUTPUT ENABLE: Gates the device's outputs during a read cycle. |
| WE# | INPUT | O | | WRITE ENABLE: Controls writes to the memory array. Data is latched on the rising edge of WE#. |
| R/C# | INPUT | O | | ROW/COLUMN SELECT: For A/A interface mode, this pin determines whether the address pins are porting to the row address, or to the column address. |
| $A_{10}$-$A_0$ | INPUT | O | | ADDRESS INPUTS: Inputs for low-order addresses during read and write operations. Addresses are internally latched by R/C# during an erase or program cycle. These addresses share the same pins as the high-order address inputs. |
| $DQ_7$-$DQ_0$ | INPUT/ OUTPUT | O | | DATA INPUTS/OUTPUTS: Inputs data and commands during write cycles, outputs data during memory array, status register and identifier code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle. |
| RY/BY# | OPEN DRAIN OUTPUT | O | O | READY/BUSY#: This output pin is a reflection bit 7 in the status register. This pin is used to determine the erase or program completion. This pin must be pulled-up with an external resistor on board. |
| $V_{CC}$ | SUPPLY | O | O | DEVICE POWER SUPPLY (3.0V-3.6V): With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid $V_{CC}$ voltage (refer to DC Characteristics) produce spurious results and should not be attempted. |
| GND | SUPPLY | O | O | GROUND: Do not float any ground pins. |
| NC | | O | O | NO CONNECT: Lead is not internally connected; it may be driven or floated. |

# 2 Device Operation

## 2.1 Mode Selection

The product can operate in two distinct interface modes:

- The LPC interface mode for In-System erasing and programming
- Address/Address Multiplexed (A/A) interface mode for factory erasing and programming

The state of the device's MODE pin determines which interface is in use. If the MODE pin is set to logic high, the device is in A/A mode; while if the MODE pin is set low, the device is in the LPC mode. The MODE selection pin must be configured prior to device operation.

## 2.2 LPC Mode

The LPC mode uses a 5-signal communication interface, 4-bit address/data bus, $LAD_3$-$LAD_0$, and a control line, LFRAME#, to control operations of the product. Cycle type operations such as Memory Read and Memory Write are defined in Intel Low Pin Count Interface Specification, Rev.1.0. Erase and Program commands sequences are incorporated into the standard LPC memory cycles.

LPC signals are transmitted via the 4-bit Address/Data bus ($LAD_3$-$LAD_0$), and follow a particular sequence, depending on whether they are Read or Write operations. The standard LPC memory cycle is defined in Table 2 and Table 3.

### 2.2.1 CE#, LFRAME#

The CE# pin, enables and disables the product, controlling read and write access of the device. To enable the product, the CE# pin must be driven low one cycle prior to LFRAME# being driven low. For write (erase or program) cycles, the CE# pin must remain low during the internal operation. When CE# is high, the product is placed in standby mode.

The LFRAME# signifies the start of a frame or the termination of a broken frame. Asserting LFRAME# for one or more clock cycle and driving a valid "START" value on $LAD_3$-$LAD_0$ will initiate device operation. The device enters standby mode when LFRAME# and CE# are high and no internal operation is in progress.

### 2.2.2 Abort Mechanism

If LFRAME# is driven low for 4 clock cycles during a LPC cycle, the cycle will be terminated and the device will wait for the "ABORT" command. To return the device to the ready mode, the host must drive the $LAD_3$-$LAD_0$ with "1111b" ("ABORT" command) while LFRAME# is driven low, and $LAD_3$-$LAD_0$ must remain unchanged until LFRAME# goes to $V_{IH}$ (refer to Figure 21). When an abort procedure is performed between the two command write cycles, such as sector/block erase or byte program, the device turns the bus around to the host but the termination of command for the internal operation is not guaranteed. If the system needs to abort after the first command cycle, the host must write "FFH" and check the status register after performing the abort procedure. Status register indicates the termination of internal operation and error conditions. If abort occurs during the internal write cycle, the data may be incorrectly programmed or erased. It is required to wait for the write operation to complete prior to initiation of the abort command. It is recommended to check the write status with status polling ($DQ_7$) or toggle bit ($DQ_6$). One other option is to wait for the fixed write time to expire.

## 2.3 Status Polling $DQ_7$ (LPC Mode, A/A Mode)

When the product device is in the automatic internal operation (program, erase, etc.), WSM (Write State Machine) status bit $DQ_7$ (SR.7) will produce a "0". Once the internal operation is completed, $DQ_7$ will produce a "1". The SR.7 bit can be polled to find the end of the operation. The other status bits (SR.5-0) should not be checked until the WSM completes the operation and the status bit SR.7 is "1". Refer to Table 11 for the status register definition.

## 2.4 Toggle Bit $DQ_6$ (LPC Mode, A/A Mode)

During the automatic internal operation (program, erase, etc.), any consecutive attempts to read $DQ_6$ (SR.6) will produce alternating "0"s and "1"s, i.e., toggling between "0" and "1". When the internal operation is completed, the toggling will stop.

## 2.5 LPC Memory Cycle Field Definitions

Table 2. LPC Read Cycle Field Definitions

| Field | Clocks | $LAD_3$-$LAD_0$ Direction | Description |
|---|---|---|---|
| START | 1 | INPUT | Start of Cycle: "0000b" appears on LPC bus to indicate the start of cycle. |
| CYCTYPE | 1 | INPUT | Cycle Type: Indicates the type of cycle. $LAD_3$-$LAD_2$ must be "01b" for memory cycle. $LAD_1$ indicates the direction of the transfer: "0b" for read. $LAD_0$ is reserved for future implementation. |
| ADDR | 8 | INPUT | Address Phase for Memory Cycle: LPC supports the 32-bit address protocol. It is transferred most significant nibble first. All the values of $A_{31}$-$A_{24}$ must be set to "1". For $A_{23}$-$A_{21}$ values, refer to Table 4. |
| TAR | 2 | INPUT then High Z | Turn-Around: It indicates a turn-around cycle to drive $LAD_3$-$LAD_0$ to "1111b" during the first clock and to drive $LAD_3$-$LAD_0$ to High Z during the second clock by the host. |
| Sync | 1 | OUTPUT | Sync: The product only supports "0000b" Ready sync. |
| Data | 2 | OUTPUT | Data Phase: The data byte is transferred least significant nibble first. ($DQ_3$-$DQ_0$ on $LAD_3$-$LAD_0$ first, $DQ_7$-$DQ_4$ on $LAD_3$-$LAD_0$ last.) |
| TAR | 2 | OUTPUT then High Z | Turn-Around: It indicates a turn-around cycle to drive $LAD_3$-$LAD_0$ to "1111b" during the first clock and to drive $LAD_3$-$LAD_0$ to High Z during the second clock by the Flash Memory. |

Table 3. LPC Write Cycle Field Definitions

| Field | Clocks | $LAD_3$-$LAD_0$ Direction | Description |
|---|---|---|---|
| START | 1 | INPUT | Start of Cycle: "0000b" appears on LPC bus to indicate the start of cycle. |
| CYCTYPE | 1 | INPUT | Cycle Type: Indicates the type of cycle. $LAD_3$-$LAD_2$ must be "01b" for memory cycle. $LAD_1$ indicates the direction of the transfer: "1b" for write. $LAD_0$ is reserved for future implementation. |
| ADDR | 8 | INPUT | Address Phase for Memory Cycle: LPC supports the 32-bit address protocol. It is transferred most significant nibble first. All the values of $A_{31}$-$A_{24}$ must be set to "1". For $A_{23}$-$A_{21}$ values, refer to Table 4. |
| Data | 2 | INPUT | Data Phase: The data byte is transferred least significant nibble first. ($DQ_3$-$DQ_0$ on $LAD_3$-$LAD_0$ first, $DQ_7$-$DQ_4$ on $LAD_3$-$LAD_0$ last.) |
| TAR | 2 | INPUT then High Z | Turn-Around: It indicates a turn-around cycle to drive $LAD_3$-$LAD_0$ to "1111b" during the first clock and to drive $LAD_3$-$LAD_0$ to High Z during the second clock by the last components driving $LAD_3$-$LAD_0$. |
| Sync | 1 | OUTPUT | Sync: The product only supports "0000b" Ready sync. |
| TAR | 2 | OUTPUT then High Z | Turn-Around: It indicates a turn-around cycle to drive $LAD_3$-$LAD_0$ to "1111b" during the first clock and to drive $LAD_3$-$LAD_0$ to High Z during the second clock by the Flash Memory. |

## 2.6 Multiple Device Selection (LPC Mode)

Multiple LPC Flash devices may be strapped to increase memory densities in a system. LPC protocol of the product supports up to 4 LPC Flash devices.

The four ID pins, $ID_3$-$ID_0$, allow up to 4 devices to be attached to the same bus by using different ID strapping in a system. If the product is used as a boot device, $ID_3$-$ID_0$ must be strapped as "0000", all subsequent devices should use a sequential up-count strapping (i.e., "0000", "0100", "1000", "1100", etc.). $ID_1$-$ID_0$ are not used and may be either "0" or "1".

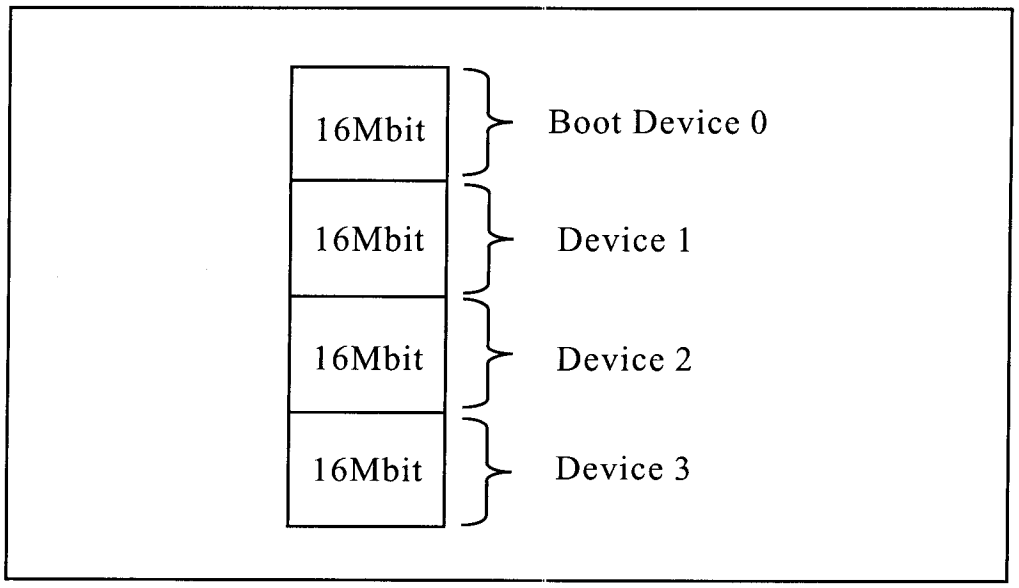



Figure 2. Multiple LPC Device Mapping

Table 4. ID Strapping Values (LPC Mode)

| Device No. | $ID_3$-$ID_0$ | $A_{23}$ | $A_{22}$ | $A_{21}$ |
|---|---|---|---|---|
| 0 (Boot device) | 00xx | | Read: | 1 |
| 1 | 01xx | | 1 = Memory Read<br>0 = Register Read | 0 |
| 2 | 10xx | 0 | Write: | 1 |
| 3 | 11xx | 0 | 0 or 1 = Memory Write | 0 |

## 2.7 General Purpose Inputs (GPI) Register (LPC Mode)

The GPI_REG (General Purpose Inputs Register) reads the status of the $GPI_4$-$GPI_0$ pins on the product. Since this is a pass-through register, there is no default value, only the state of the pins at power-up. The pins must have stable data from before the start of the cycle that reads the GPI_REG until after the cycle is complete. These pins must not be left to float and they should be driven $V_{IL}$ or $V_{IH}$.

Refer to Table 5 for the GPI_REG bits and function, and Table 6 for memory address location for its respective device strapping. If this address is input, GPI_REG can be read also on read identifier codes mode, read status register mode or read array mode.

Table 5. General Purpose Input Register

| Bit | Function |
|---|---|
| 7:5 | Reserved for future implementation. |
| 4 | $GPI_4$ : Reads status of general-purpose input pin (Pin 6) |
| 3 | $GPI_3$ : Reads status of general-purpose input pin (Pin 11) |
| 2 | $GPI_2$ : Reads status of general-purpose input pin (Pin 12) |
| 1 | $GPI_1$ : Reads status of general-purpose input pin (Pin 13) |
| 0 | $GPI_0$ : Reads status of general-purpose input pin (Pin 14) |

Table 6. Memory Map for General Purpose Input Register Addresses

| Device No. | GPI_REG |
|---|---|
| 0 (Boot device) | FFBC0100H |
| 1 | FF9C0100H |
| 2 | FF3C0100H |
| 3 | FF1C0100H |

## 2.8 Product Identifier Codes (LPC Mode, A/A Mode)

The product identifier codes identify the device as the product and manufacturer as SHARP.

• In LPC mode:

The Read Identifier Codes command is unnecessary and only an address shown in Table 7 is required. However, $A_{22}$ must be "0" in this operation. The operation by the command is also possible if the Read Identifier Codes command is written. Any command is acceptable not only when $A_{22}$="1" but also when $A_{22}$="0".

• In A/A mode:

The Read Identifier Codes command is necessary. Refer to Table 10 for the command definitions.

Table 7. Identifier Codes (3)

| Code | | Address [$A_{20}$-$A_0$] (1) | Data [$DQ_7$-$DQ_0$] | Notes |
|---|---|---|---|---|
| Manufacturer Code | | 000000H | B0H | |
| Device Code | | 000001H | CAH | |
| Block Lock Configuration Code | Top Boot Lock Bit is Cleared. | Block Address + 2 | $DQ_0$ = 0 | 2 |
| | Top Boot Lock Bit is Set. | | $DQ_0$ = 1 | 2 |
| | Whole Block Lock Bit is Cleared. | | $DQ_1$ = 0 | 2 |
| | Whole Block Lock Bit is Set. | | $DQ_1$ = 1 | 2 |

NOTES:
1. $A_{22}$ must be "0" when the identifier codes are read in LPC mode.
2. $DQ_7$-$DQ_2$ are reserved for future implementation.
3. The identifier codes must not be read while the WSM is busy.

## 2.9 A/A Mode

Commands are used to initiate the memory operation functions of the device. The data portion of the software command sequence is latched on the rising edge of WE#.

During the software command sequence, the row address is latched on the falling edge of R/C# and the column address is latched on the rising edge of R/C#.

Table 8. Operation Modes Selection (1)

| Mode | Notes | RST# | OE# | WE# | Address | DQ (2) |
|---|---|---|---|---|---|---|
| Read Array | 6 | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $A_{IN}$ | $D_{OUT}$ |
| Output Disable | | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | X | High Z |
| Standby | | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | X | High Z |
| Reset | 3 | $V_{IL}$ | X | X | X | High Z |
| Read Identifier Codes | 6 | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | Refer to Table 7 | Refer to Table 7 |
| Read Status Register | 6 | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $A_{IN}$ | $D_{OUT}$ |
| Write | 4, 5, 6 | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | $A_{IN}$ | $D_{IN}$ |

NOTES:
1. X can be $V_{IL}$ or $V_{IH}$ for control pins and addresses.
2. DQ refers to $DQ_7$-$DQ_0$.
3. RST# at GND±0.2V ensures the lowest power consumption.
4. Command writes involving sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set top boot lock bit and clear top boot lock bits are reliably executed when $V_{CC}$=3.0V-3.6V.
5. Refer to Table 10 for valid $D_{IN}$ during a write operation.
6. Never hold OE# low and WE# low at the same timing.

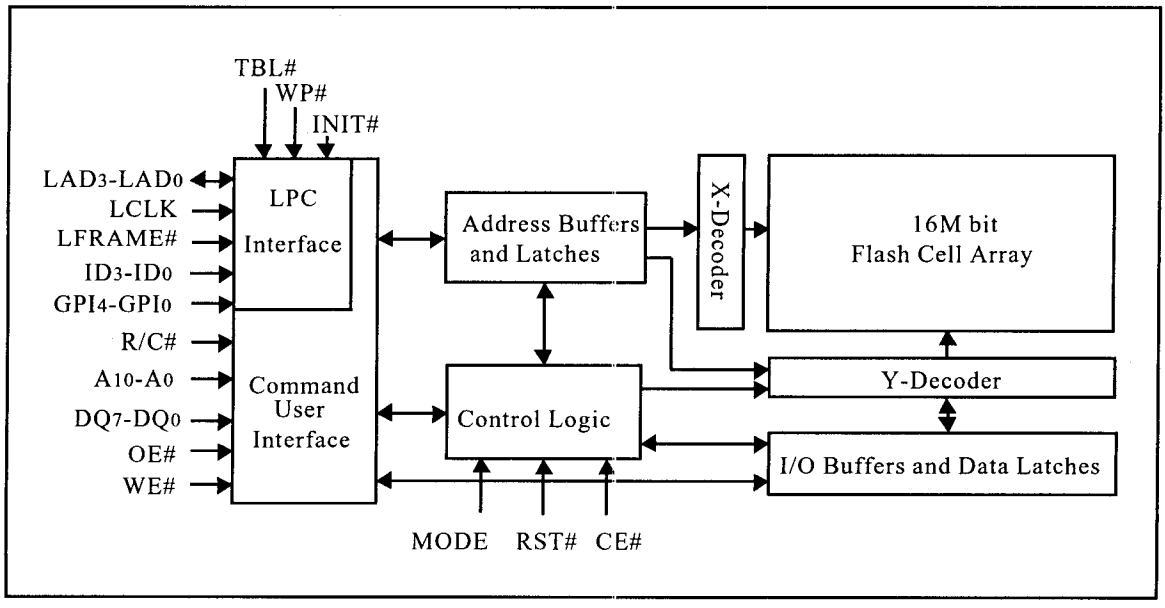



Figure 3. Block Diagram

## 2.10 Write Protection

### 2.10.1 TBL# and WP# Hardware Write Protection (LPC Mode)

The top boot lock (TBL#) and write protect (WP#) pins are provided for hardware write protection of the memory area in the product. TBL# pin is used to write protection of 8 boot sectors (8Kbytes) at the highest memory address range for the product. WP# pin is used for the remaining blocks in the flash memory.

An active low signal at the TBL# pin prevents erase and program operations of the top boot sectors. TBL# protection is effective only to the sector to which the top boot lock bit is set. When TBL# pin is held high, the write protection of the top boot sectors is disabled. The WP# pin serves the same function for the remaining blocks of the memory array. The TBL# and WP# pins write protection functions operate independently of one another.

Both TBL# and WP# pins must be set to their required protection states prior to starting an erase or program operation. A logic level change occurring at the TBL# or WP# pin during an erase or program operation could cause unpredictable results.

### 2.10.2 Whole Block Lock Software Write Protection (LPC Mode, A/A Mode)

The whole block lock is provided for software write protection of the memory area in the product. Whole block lock protects all sectors and blocks in the device by lock bit. The lock bit is set to locked state in an initial state after power-up or reset operation. The lock bit must be cleared to unlocked state before starting erase or program operation. The lock bit is cleared by clear whole block lock bit operation. After erase or program operation is finished, the memory array can be protected by set whole block lock bit operation.

Table 9. Write Protection Alternatives

| Operation | Whole Block Lock Bit (1) | TBL# | Top Boot Lock Bit (1) | WP# | Effect |
|---|---|---|---|---|---|
| Sector Erase or Block Erase or Full Chip Erase or Byte Program | 1 | X | X | X | All sectors and blocks are Locked. |
| | 0 | $V_{IL}$ | 1 | X | Top boot sector is Locked. |
| | | $V_{IL}$ | 0 | X | Top boot sector is Unlocked. |
| | | $V_{IH}$ | X | X | All top boot sectors are Unlocked |
| | | $V_{IH}$ | X | $V_{IL}$ | The remaining blocks other than top boot sectors are Locked |
| | | $V_{IH}$ | X | $V_{IH}$ | All sectors and blocks are Unlocked |

NOTES:
1. Lock Bit : "1" = Locked State, "0" = Unlocked State

## 2.11 Command Definitions

Table 10. Command Definitions [12]

| Command | Interface | | Bus Cycles Req'd | Notes | First Bus Cycle | | | Second Bus Cycle | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | A/A | LPC | | | Oper[1] | Addr[2] | Data | Oper[1] | Addr[2] | Data[3] |
| Read Array | O | O | 1 | 4 | Write | X | FFH | | | |
| Read Identifier Codes | O | O | ≥2 | 5 | Write | X | 90H | Read | IA | ID |
| Read Status Register | O | O | 2 | | Write | X | 70H | Read | X | SRD |
| Clear Status Register | O | O | 1 | 4 | Write | X | 50H | | | |
| Sector/Block Erase | O | O | 2 | 6,7 | Write | BA | 20H | Write | BA | D0H |
| Full Chip Erase | O | | 2 | 6,7,8 | Write | X | 30H | Write | X | D0H |
| Byte Program | O | O | 2 | 6,7,9 | Write | X | 40H or 10H | Write | WA | WD |
| Set Whole Block Lock Bit | O | O | 2 | | Write | X | 60H | Write | X | BBH |
| Clear Whole Block Lock Bit | O | O | 2 | 7 | Write | X | 60H | Write | X | DBH |
| Set Top Boot Lock Bit | O | O | 2 | 10 | Write | X | 60H | Write | SA | 01H |
| Clear Top Boot Lock Bits | O | O | 2 | 11 | Write | X | 60H | Write | SA | D0H |

NOTES:

1. Bus operations are defined in Table 8.
2. Any command is acceptable not only when $A_{22}$="1" but also when $A_{22}$="0" in LPC mode.
   X=Any valid address within the device.
   IA=Identifier codes address (Refer to Table 7).
   BA=Address within the sector/block for sector/block erase.
   WA=Address of memory location for program.
   SA=Address within the top boot sector for set top boot lock bit.
3. ID=Data to be read from identifier codes. (Refer to Table 7).
   SRD=Data to be read from status register. Refer to Table 11 for a description of the status register bits.
   WD=Data to be programmed at location WA.
4. The device returns to the read array mode even after Clear Status Register command or reset operation by RST#/INIT#.
5. Following the Read Identifier Codes command, read operations access manufacturer code, device code and block lock configuration code (Refer to Table 7). The identifier codes must not be read while the WSM is busy.
6. Sector/block erase, full chip erase and byte program operations cannot be executed to top boot sector when TBL# goes to $V_{IL}$. Sector/block erase, full chip erase and byte program operations cannot be executed to blocks other than top boot sector when WP# goes to $V_{IL}$.
7. Whole block lock bit must be cleared when executing sector/block erase, full chip erase and byte program operations. Sector/block erase, full chip erase and byte program operations cannot be executed if whole block lock bit is set.
8. Supported in A/A Mode only. Any top boot sector which is locked by top boot lock bit is protected from alteration. Top boot lock bit should be cleared before performing an erase operation.
9. Either 40H or 10H are recognized as the program first bus cycle command.
10. Lock bit can be set to each sector within the top block (block 31). Since this lock bit is non-volatility, it holds the lock state even after power-off or reset.
11. All top boot lock bits of each sector are cleared at a time.
    SA=Address within the top boot sector (1F0000H-1FFFFFH).
12. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

### 2.11.1 Read Array Command

The Read Array command places the device to read array mode. The device remains enabled for read array mode until another valid command is written. When RST# is at $V_{IH}$, the Read Array command is valid. Once the internal WSM (Write State Machine) has started sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set top boot lock bit or clear top boot lock bits operation, the device will not recognize the Read Array command until the WSM completes its operation. Upon initial device power-up or after reset mode, the product defaults to read array mode.

### 2.11.2 Read Identifier Codes Command

The read identifier codes mode is initiated by writing the Read Identifier Codes command (90H). After writing the command, read operations output the identifier codes. To terminate the operation, write another valid command. In this mode, the manufacturer code, device code and block lock configuration codes can be read on the addresses shown in Table 7. Once the internal WSM has started sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set top boot lock bit or clear top boot lock bits operation, the device will not recognize the Read Identifier Codes command until the WSM completes its operation. The Read Identifier Codes command is valid when RST# is at $V_{IH}$.

### 2.11.3 Read Status Register Command

The status register may be read to determine when sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set top boot lock bit or clear top boot lock bits operation has been completed and whether the operation has been successfully completed or not (refer to Table 11). The status register can be read at any time by writing the Read Status Register command (70H). Subsequent read operations output the status register data until another valid command is written. The Read Status Register command is valid when RST# is at $V_{IH}$.

### 2.11.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 and SR.1 that have been set to "1"s by the WSM can only be cleared by writing the Clear Status Register command (50H). RST# must be at $V_{IH}$. To clear the status register, write the Clear Status Register command to the CUI. After executing the Clear Status Register command, the device returns to read array mode.

Status register bits SR.5, SR.4, SR.3 and SR.1 indicate various error conditions occurring after writing commands (refer to Table 11). When erasing multiple sectors/blocks or programming several bytes in sequence, clear these bits before starting each operation. The status register bits indicate an error for during the sequence.

### 2.11.5 Sector/Block Erase Command

The two-cycle Sector/Block Erase command initiates one sector/block erase at the addressed sector/block. After writing the command, read operations output the status register data. At the first cycle, command (20H) and an address within the sector/block to be erased is written to the CUI, and command (D0H) and the same address as the first cycle is written at the second cycle. Once the Sector/Block Erase command is successfully written, the WSM automatically starts erase and verification processes. The data in the selected sector/block are erased (becomes "FFH"). The system CPU can detect the sector/block erase completion by analyzing the output data of the status register bit SR.7. The device remains in read status register mode after the completion of the sector/block erase operation until another command is written to the CUI. Figure 4 shows a flowchart of the sector/block erase operation.

Check the status register bit SR.5 at the end of sector/block erase. If a sector/block erase error is detected, the status register should be cleared before system software attempts corrective actions. The device remains in read status register mode until a new command is written.

This two-cycle command sequence ensures that sector/block contents are not accidentally erased. An invalid Sector/Block Erase command sequence will result in status register bits SR.5 and SR.4 being set to "1" and the operation will be aborted.

For reliable sector/block erase operation, apply the specified voltage on $V_{CC}$. In the absence of this voltage, sector/block erase operations are not guaranteed. Also, successful sector/block erase requires that the selected sector/block is unlocked. When sector/block erase is attempted to the locked sector/block, bits SR.5 and SR.1 will be set to "1".

### 2.11.6 Full Chip Erase Command

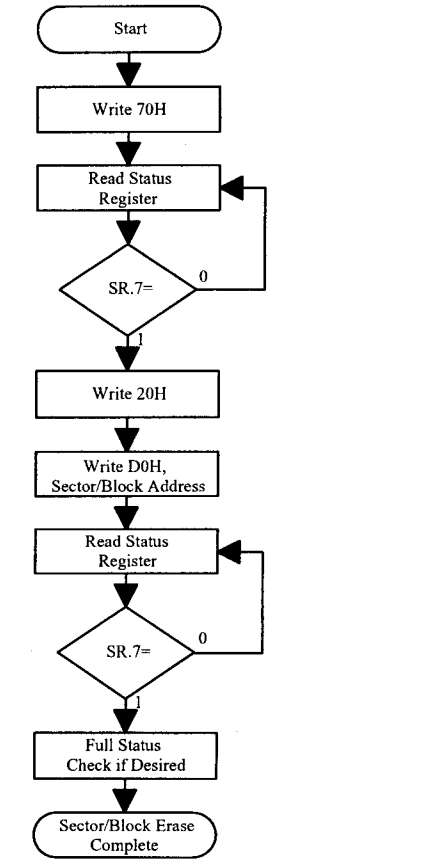
The two-cycle Full Chip Erase command erases all of the unlocked sectors/blocks. At the first cycle, command (30H) is written to the CUI, and command (D0H) is written at the second cycle. After writing the command, the device outputs the status register data when any address within the device is selected. The WSM automatically starts the erase operation for all unlocked sectors/blocks, skipping the locked sectors/blocks. The system CPU can detect the full chip erase completion by analyzing the output data of the status register bit SR.7. The device remains in the read status register mode after the completion of the full chip erase operation until another command is written to the CUI. Figure 5 shows a flowchart of the full chip erase operation.

The WSM aborts the operation upon encountering an error during the full chip erase operation and leaves the remaining sectors/blocks not erased. After the full chip erase operation, check the status register bit SR.5. When a full chip erase error is detected, SR5 will be set to "1". The status register should be cleared before system software attempts corrective actions. After that, retry the Full Chip Erase command or erase sector/block by sector/block using the Sector/Block Erase command.

This two-cycle command sequence ensures that sector/block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in status register bits SR.5 and SR.4 being set to "1" and the operation will be aborted.

For reliable full chip erase operation, apply the specified voltage on $V_{CC}$. In the absence of this voltage, full chip erase operations are not guaranteed.

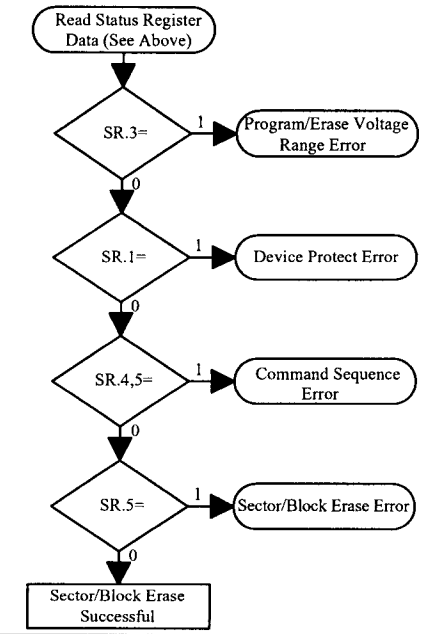
As previously mentioned, the Full Chip Erase command erases all sectors/blocks except for the locked sectors/blocks. Unlike the sector/block erase, the status register bits SR.5 and SR.1 are not set to "1" even if the locked sector/block is included. However, when all sectors/blocks are locked, the bits SR.5 and SR.1 are set to "1" and the operation will not be executed.




| Bus Operation | Command | Comments |
|---|---|---|
| Write | Read Status Register | Data=70H<br>Addr=X |
| Read | | Status Register Data |
| Standby | | Check SR.7<br>1=WSM Ready<br>0=WSM Busy |
| Write | Sector/Block Erase | Data=20H<br>Addr=X |
| Write | Sector/Block Erase | Data=D0H<br>Addr=Within Sector/Block to be Erased |
| Read | | Status Register Data |
| Standby | | Check SR.7<br>1=WSM Ready<br>0=WSM Busy |

When subsequently erasing a sector/block, repeat the above sequence.
Full status check can be done after each sector/block erase or after a sequence of sector/block erasures.
Write FFH after a sequence of sector/block erasures to place device in read array mode.

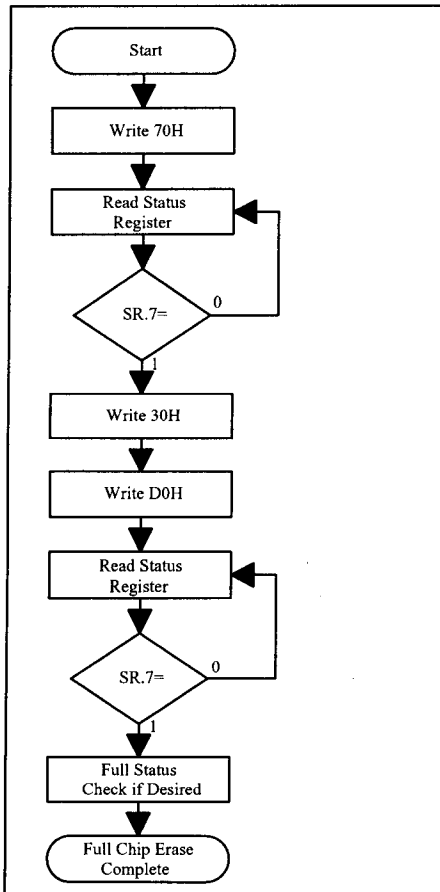
FULL STATUS CHECK PROCEDURE




| Bus Operation | Command | Comments |
|---|---|---|
| Standby | | Check SR.3<br>1=Program/Erase Voltage Error Detect |
| Standby | | Check SR.1<br>1=Device Protect Detect |
| Standby | | Check SR.4, 5<br>Both 1=Command Sequence Error |
| Standby | | Check SR.5<br>1=Sector/Block Erase Error |

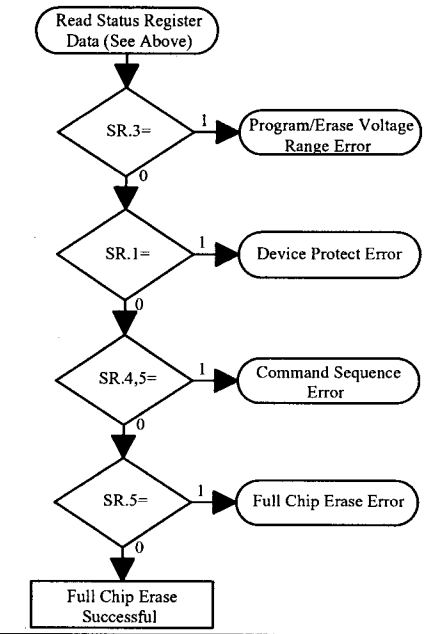
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple sectors/blocks are erased before full status is checked.
If an error is detected, clear the status register before attempting retry or other error recovery.

Figure 4. Sector/Block Erase Flowchart




| Bus Operation | Command | Comments |
|---|---|---|
| Write | Read Status Register | Data=70H<br>Addr=X |
| Read | | Status Register Data |
| Standby | | Check SR.7<br>1=WSM Ready<br>0=WSM Busy |
| Write | Full Chip Erase | Data=30H<br>Addr=X |
| Write | Full Chip Erase | Data=D0H<br>Addr=X |
| Read | | Status Register Data |
| Standby | | Check SR.7<br>1=WSM Ready<br>0=WSM Busy |
| Check the status after full chip erase.<br>Write FFH after the full chip erase to place device in read array mode. | | |

FULL STATUS CHECK PROCEDURE




| Bus Operation | Command | Comments |
|---|---|---|
| Standby | | Check SR.3<br>Program/Erase Voltage Error Detect |
| Standby | | Check SR.1<br>1=Device Protect Detect |
| Standby | | Check SR.4, 5<br>Both 1=Command Sequence Error |
| Standby | | Check SR.5<br>1=Full Chip Erase Error |
| SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery. | | |

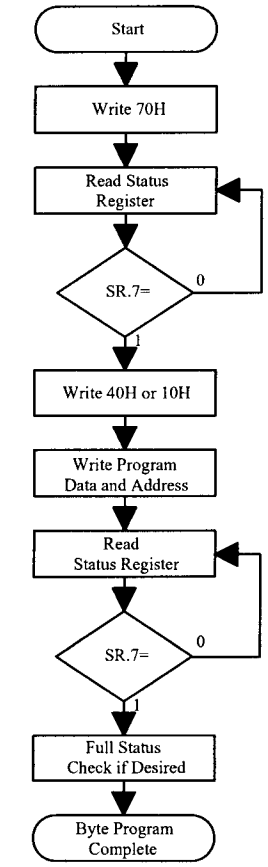
Figure 5. Full Chip Erase Flowchart

### 2.11.7 Byte Program Command

A two-cycle command sequence initiates one-byte program operation. Read operations output the status register data until another valid command is written. At the first cycle, write command (standard 40H or alternate 10H), followed by the second write that specifies the address and data to be programmed. The WSM then takes over, controlling the internal program algorithm. The system CPU can detect the byte program completion by analyzing the output data of the status register bit SR.7. Figure 6 shows a byte program flowchart.

The internal WSM verify only detects errors for "1"s that are not successfully programmed to "0"s. Check the status register bit SR.4 at the end of byte program. If a program error is detected, the status register should be cleared before system software attempts corrective actions. The device remains in read status register mode until it receives another command.

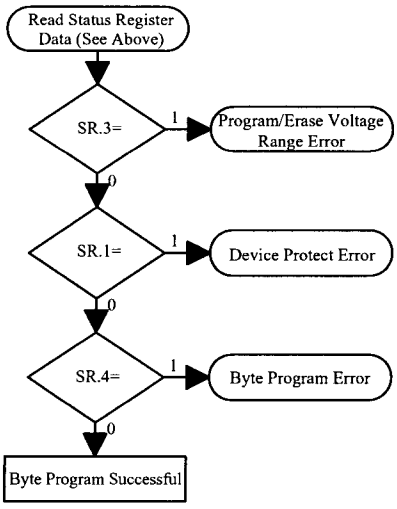
For reliable byte program operation, apply the specified voltage on $V_{CC}$. In the absence of this voltage, byte program operations are not guaranteed. Also, successful byte program requires that the selected sector/block is unlocked. When byte program is attempted to the locked sector/block, bits SR.4 and SR.1 will be set to "1".




| Bus Operation | Command | Comments |
|---|---|---|
| Write | Read Status Register | Data=70H<br>Addr=X |
| Read | | Status Register Data |
| Standby | | Check SR.7<br>1=WSM Ready<br>0=WSM Busy |
| Write | Byte Program | Data=40H or 10H<br>Addr=X |
| Write | Byte Program | Data=Data to be Programmed<br>Addr=Location to be Programmed |
| Read | | Status Register Data |
| Standby | | Check SR.7<br>1=WSM Ready<br>0=WSM Busy |

Repeat the above sequence for the subsequent byte programs.
Full status check can be done after each byte program, or after a sequence of byte programs.
Write FFH after a sequence of byte programs to place device in read array mode.

FULL STATUS CHECK PROCEDURE




| Bus Operation | Command | Comments |
|---|---|---|
| Standby | | Check SR.3<br>1= Program/Erase Voltage Error Detect |
| Standby | | Check SR.1<br>1=Device Protect Detect |
| Standby | | Check SR.4<br>1=Byte Program Error |

SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple locations are programmed before full status is checked.
If an error is detected, clear the status register before attempting retry or other error recovery.

Figure 6. Byte Program Flowchart

### 2.11.8 Set Whole Block Lock Bit, Set Top Boot Lock Bit Command

The product is provided with a lock bit. Refer to "2.10 Write Protection" for the features of set lock bit.

The Set Whole Block Lock Bit command and Set Top Boot Lock Bit command is a two-cycle command. At the first cycle, command (60H) is written. At the second cycle, command (BBH) (set whole block lock bit), or command (01H) and an address within the sector to be locked (set top boot lock bit) is written. Once the command is successfully written, the internal WSM then controls the set whole block lock bit or set top boot lock bit algorithm. After the two-cycle command is written, the device outputs the status register data. The CPU can detect the completion of the set whole block lock bit or set top boot lock bit operation by analyzing the data of the status register bit SR.7. Figure 7 shows set whole block lock bit, set top boot lock bit flowchart.

The two-cycle command sequence ensures that block is not accidentally locked. An invalid Set Whole Block Lock Bit or Set Top Boot Lock Bit command sequence will result in both status register bits SR.5 and SR.4 being set to "1" and the operation will not be executed.

For reliable set whole block lock bit and set top boot lock bit operation, apply the specified voltage on $V_{CC}$.

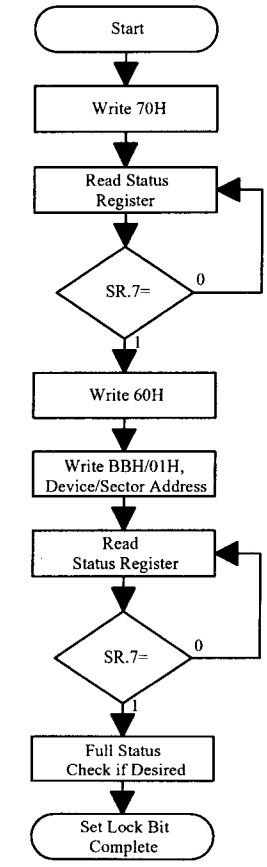
### 2.11.9 Clear Whole Block Lock Bit, Clear Top Boot Lock Bits Command

A locked block can be unlocked by writing the Clear Whole Block Lock Bit or Clear Top Boot Lock Bits command. Refer to "2.10 Write Protection" for the features of clear lock bit.

The Clear Whole Block Lock Bit and Clear Top Boot Lock Bits command is a two-cycle command. At the first cycle, command (60H) is written. At the second cycle, command (DBH) (clear whole block lock bit), or command (D0H) and an address within the sector to be unlocked (clear top boot lock bits) is written. Once the command is successfully written, the internal WSM then controls the clear whole block lock bit or clear top boot lock bits algorithm. After the two-cycle command is written, the device outputs the status register data. The CPU can detect the completion of the clear whole block lock bit or clear top boot lock bits operation by analyzing the data of the status register bit SR.7. Figure 8 shows clear whole block lock bit, clear top boot lock bits flowchart.

The two-cycle command sequence ensures that block is not accidentally unlocked. An invalid Clear Whole Block Lock Bit or Clear Top Boot Lock Bits command sequence will result in both status register bits SR.5 and SR.4 being set to "1" and the operation will not be executed.

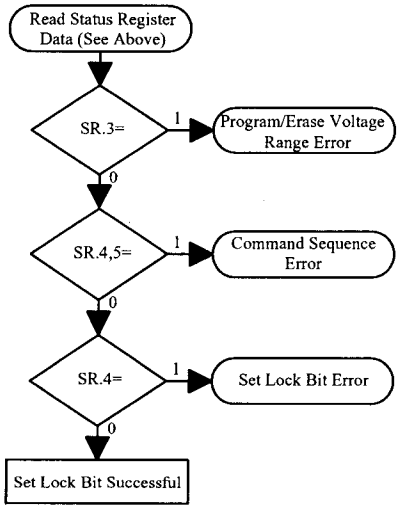
For reliable clear whole block lock bit and clear top boot lock bits operation, apply the specified voltage on $V_{CC}$.




| Bus Operation | Command | Comments |
|---|---|---|
| Write | Read Status Register | Data=70H<br>Addr=X |
| Read | | Status Register Data |
| Standby | | Check SR.7<br>1=WSM Ready<br>0=WSM Busy |
| Write | Set Whole Block Lock Bit,<br>Set Boot Lock Bit | Data=60H<br>Addr=X |
| Write | Set Whole Block Lock Bit,<br>Set Boot Lock Bit | Data=BBH (Whole Block),<br>01H (Boot)<br>Addr=X (Whole Block),<br>Sector Address (Boot) |
| Read | | Status Register Data |
| Standby | | Check SR.7<br>1=WSM Ready<br>0=WSM Busy |

Repeat for the subsequent set lock bit.
Full status check can be done after each set lock bit operation or after a sequence of set lock bit operations.
Write FFH after a sequence of set lock bit operations to place device in read array mode.

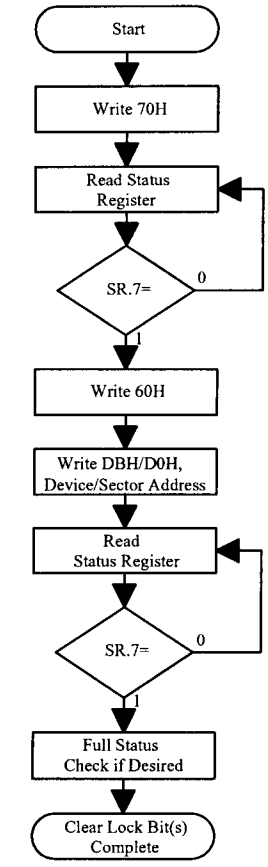
FULL STATUS CHECK PROCEDURE




| Bus Operation | Command | Comments |
|---|---|---|
| Standby | | Check SR.3<br>Program/Erase Voltage Error Detect |
| Standby | | Check SR.4, 5<br>Both 1=Command Sequence Error |
| Standby | | Check SR.4<br>1=Set Lock Bit Error |

SR.5, SR.4 and SR.3 are only cleared by the Clear Status Register Command in cases where multiple lock bits are set before full status is checked.
If an error is detected, clear the status register before attempting retry or other error recovery.

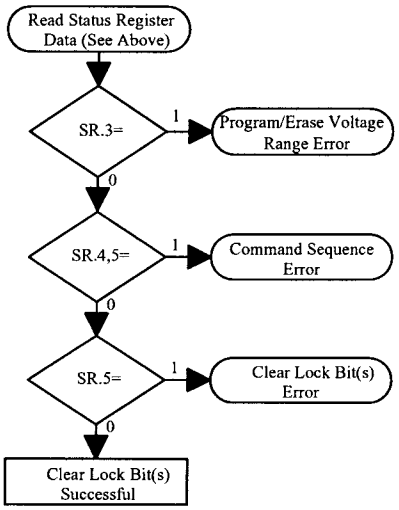
Figure 7. Set Whole Block Lock Bit, Set Top Boot Lock Bit Flowchart




| Bus Operation | Command | Comments |
|---|---|---|
| Write | Read Status Register | Data=70H<br>Addr=X |
| Read | | Status Register Data |
| Standby | | Check SR.7<br>1=WSM Ready<br>0=WSM Busy |
| Write | Clear Whole Block Lock Bit,<br>Clear Boot Lock Bits | Data=60H<br>Addr=X |
| Write | Clear Whole Block Lock Bit,<br>Clear Boot Lock Bits | Data=DBH (Whole Block),<br>D0H (Boot)<br>Addr=X (Whole Block),<br>Sector Address (Boot) |
| Read | | Status Register Data |
| Standby | | Check SR.7<br>1=WSM Ready<br>0=WSM Busy |

Repeat for the subsequent clear lock bit(s).
Full status check can be done after each clear lock bit(s) operation or after a sequence of clear lock bit(s) operations.
Write FFH after a sequence of clear lock bit(s) operations to place device in read array mode.

FULL STATUS CHECK PROCEDURE




| Bus Operation | Command | Comments |
|---|---|---|
| Standby | | Check SR.3<br>1=Program/Erase Voltage Error Detect |
| Standby | | Check SR.4, 5<br>Both 1=Command Sequence Error |
| Standby | | Check SR.5<br>1=Clear Lock Bit(s) Error |

SR.5, SR.4 and SR.3 are only cleared by the Clear Status Register Command in cases where multiple lock bits are cleared before full status is checked.
If an error is detected, clear the status register before attempting retry or other error recovery.

Figure 8. Clear Whole Block Lock Bit, Clear Top Boot Lock Bits Flowchart

## 2.12 Status Register Definition

Table 11. Status Register Definition

| WSMS | TB | ECLS | PSLS | PVEVS | R | DPS | R |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| | NOTES: |
|---|---|
| SR.7 = WRITE STATE MACHINE STATUS (WSMS)<br>1 = Ready<br>0 = Busy | Check SR.7 or SR.6 or RY/BY# to determine sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set top boot lock bit or clear top boot lock bits completion. SR.5, SR.4, SR.3 and SR.1 are invalid while SR.7="0". |
| SR.6 = TOGGLE BIT (TB)<br>Toggling between "0" and "1" during the erase or program operation. | |
| SR.5 = SECTOR/BLOCK ERASE, FULL CHIP ERASE AND CLEAR TOP BOOT LOCK BITS STATUS (ECLS)<br>1 = Error in Sector/Block Erase, Full Chip Erase or Clear Top Boot Lock Bits<br>0 = Successful Sector/Block Erase, Full Chip Erase or Clear Top Boot Lock Bits | If both SR.5 and SR.4 are "1"s after a sector/block erase, full chip erase, set whole block lock bit, clear whole block lock bit, set top boot lock bit and clear top boot lock bits attempt, an improper command sequence was entered. |
| SR.4 = BYTE PROGRAM AND SET TOP BOOT LOCK BIT STATUS (PSLS)<br>1 = Error in Byte Program or Set Top Boot Lock Bit<br>0 = Successful Byte Program or Set Top Boot Lock Bit | SR.3 indicates the program or erase voltage conditions. The program or erase voltage is the internal voltage which is used for the program or erase operation in the flash memory. SR.3 does not provide a continuous indication of the program or erase voltage level. The WSM interrogates and indicates the program or erase voltage level only after Sector/Block Erase, Full Chip Erase, Byte Program, Set Top Boot Lock Bit and Clear Top Boot Lock Bits command sequences. |
| SR.3 = PROGRAM VOLTAGE OR ERASE VOLTAGE STATUS (PVEVS)<br>1 = Invalid Program or Erase Voltage Detect, Operation Abort<br>0 = Program or Erase Voltage OK | |
| SR.2 = RESERVED FOR FUTURE ENHANCEMENTS (R) | |
| SR.1 = DEVICE PROTECT STATUS (DPS)<br>1 = Erase or Program Attempted on a Locked Block by TBL#, WP# or Block Lock Bit, Operation Abort<br>0 = Unlocked | SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates TBL#, WP# or block lock bit only after Sector/Block Erase, Full Chip Erase or Byte Program command sequences. It informs the system, depending on the attempted operation, if the block is locked. |
| SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R) | SR.2 and SR.0 are reserved for future use and should be masked out when polling the status register. |

## 2.13 Memory Map

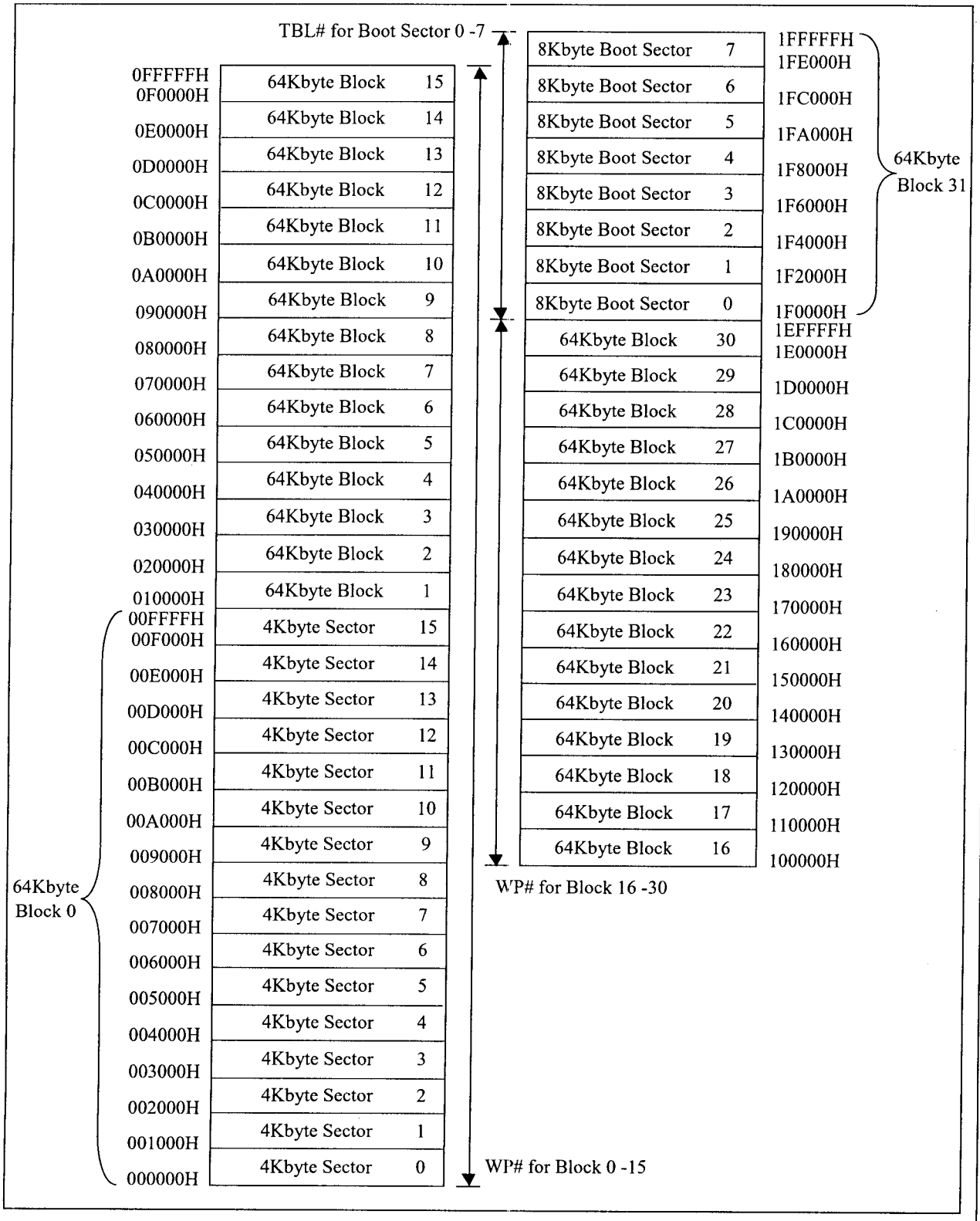



Figure 9. Memory Map

# 3 Design Considerations

## 3.1 Power Supply Decoupling

Flash memory's power switching characteristics require careful device decoupling for eliminating noises to the system power lines. System designers should consider standby current levels ($I_{CCS}$), active current levels ($I_{CCR}$) and transient peaks produced by falling and rising edges of control signals. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1µF ceramic capacitor connected between each $V_{CC}$ and GND. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads. Additionally, for every eight devices, a 4.7µF electrolytic capacitor should be placed at the array's power supply connection between $V_{CC}$ and GND. These capacitors will overcome voltage slumps caused by circuit board trace inductance.

## 3.2 $V_{CC}$, RST# Transitions

If RST# is not at $V_{IH}$, sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set top boot lock bit and clear top boot lock bits operation are not guaranteed. If RST# transitions to $V_{IL}$ during the sector/block erase, full chip erase or byte program operation, the status register bit SR.7 will remain "0" until reset operation has been completed. Then, the attempted operation will be aborted and the device will enter reset mode after the completion of the reset sequence. If RST# is taken $V_{IL}$ during a sector/block erase, full chip erase or byte program operation, the memory contents at the aborted location are no longer valid. Therefore, the proper command must be written again after RST# is driven $V_{IH}$. And also, if $V_{CC}$ transitions to lower than $V_{LKO}$ during a sector/block erase, full chip erase or byte program operation, the attempted operation will be aborted and the memory contents at the aborted location are no longer valid. Write the proper command again after $V_{CC}$ transitions above $V_{LKO}$.

## 3.3 Power-Up/Down Protection

The product is designed to offer protection against accidental sector/block erase, full chip erase and byte program due to noises during power transitions. When the device power-up, holding RST# to GND until $V_{CC}$ has reached the specified level and in stable. For additional information, please refer to the AP-007-SW-E *RST#, $V_{PP}$ Electric Potential Switching Circuit*. After power-up, the product defaults to the read array mode.

The block locking scheme prevents the accidental data alteration. The device is also disabled until RST# is brought to $V_{IH}$, regardless of the state of its control inputs. By holding the device in reset during power-up/down, invalid bus conditions can be masked, providing yet another level of memory protection.

## 3.4 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. The nonvolatility of the product increases usable battery life because data is retained when system power is removed.

## 3.5 Reset Operation

During power-up/down or transitions of power supply voltage, hold the RST# pin at $V_{IL}$ to protect data against noises which are caused by invalid bus conditions and initialize the internal circuitry in flash memory. Bringing RST# to $V_{IL}$ resets the internal WSM (Write State Machine) and sets the status register to "80H".

After return from reset, a wait time is required until the device is ready. After this wake-up interval, normal operation is restored.

## 3.6 WSM (Write State Machine) Polling

The status register bit SR.7 provides a software method of detecting sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set top boot lock bit or clear top boot lock bits completion. After the Sector/Block Erase, Full Chip Erase, Byte Program, Set Whole Block Lock Bit, Clear Whole Block Lock Bit, Set Top Boot Lock Bit or Clear Top Boot Lock Bits command is written to the CUI (Command User Interface), SR.7 goes to "0". It will return to "1" when the WSM (Write State Machine) has completed the internal algorithm.

## 3.7 Attention to Program Operation

Do not *re*-program "0" data for the bit in which "0" has been already programmed. This *re*-program operation may generate the bit which cannot be erased.

To change the data from "1" to "0", take the following steps.

- Program "0" for the bit in which you want to change the data from "1" to "0".
- Program "1" for the bit in which "0" has been already programmed.
  (When "1" is programmed, erase/program operations are not executed onto the memory cell in flash memory.)

For example, changing the data from "10111101" to "10111100" requires "11111110" programmed.

# 4 Electrical Specifications

## 4.1 Absolute Maximum Ratings*

Operating Temperature

During Read, Erase and Program ..... 0°C to +85°C (1)

Storage Temperature

During under Bias..... -10°C to +85°C

During non Bias..... -65°C to +125°C

Voltage On Any Pin

(except $V_{CC}$)..... -0.5V to $V_{CC}$+0.5V (2)

$V_{CC}$ Supply Voltage ..... -0.2V to +3.9V (2)

Output Short Circuit Current..... 100mA (3)

**WARNING:* Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:

1. Operating temperature is for commercial temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on $V_{CC}$ pin. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is $V_{CC}$+0.5V which, during transitions, may overshoot to $V_{CC}$+2.0V for periods <20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

## 4.2 Operating Conditions

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $T_A$ | Operating Temperature | | 0 | +25 | +85 | °C | Ambient Temperature |
| $V_{CC}$ | $V_{CC}$ Supply Voltage | 1 | 3.0 | 3.3 | 3.6 | V | |
| | Sector/Block Erase Cycling | | 100,000 | | | Cycles | |

NOTES:

1. Refer to DC Characteristics tables for voltage range-specific specification.

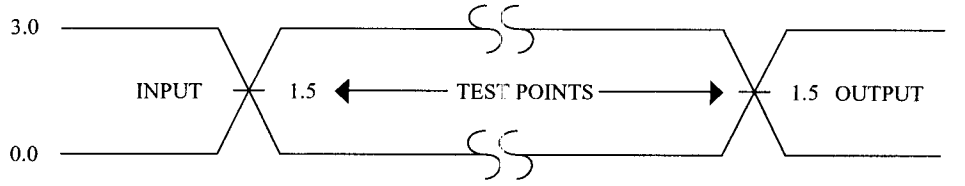
### 4.2.1 Capacitance (1) ($T_A$=+25°C, f=1MHz)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 7 | 10 | pF | $V_{IN}$=0.0V |
| $C_{I/O}$ | Input / Output Capacitance | | 9 | 12 | pF | $V_{I/O}$=0.0V |

NOTE:

1. Sampled, not 100% tested.

### 4.2.2 AC Input/Output Test Conditions




AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0".
Input timing begins and output timing ends at 1.5V. Input rise and fall times (10% to 90%) < 5ns.

Figure 10. Transient Input/Output Reference Waveform for $V_{CC}$=3.0V-3.6V

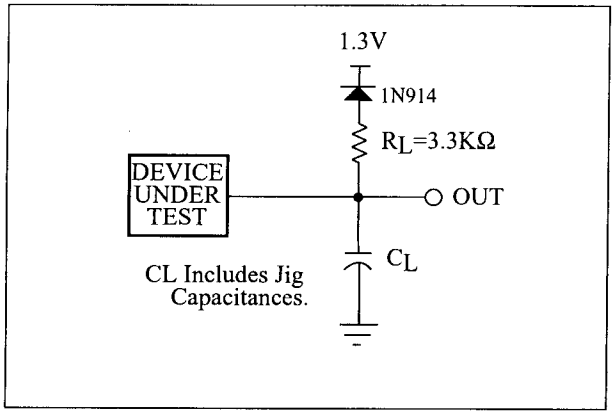



Figure 11. Transient Equivalent Testing Load Circuit

Table 12. Configuration Capacitance Loading Value

| Test Configuration | $C_L$ (pF) |
|---|---|
| $V_{CC}$=3.0V-3.6V | 30 |

### 4.2.3 DC Characteristics

$V_{CC}$=3.0V-3.6V

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | 1 | -1 | | +1 | µA | $V_{CC}=V_{CC}$Max., $V_{IN}/V_{OUT}=V_{CC}$ or GND |
| $I_{LID}$ | Input Load Current for MODE, $ID_3$-$ID_0$ pins | 1 | -200 | | +200 | µA | |
| $I_{LO}$ | Output Leakage Current | 1 | -1 | | +1 | µA | |
| $I_{CCS1}$ | $V_{CC}$ Standby Current (LPC Interface) | 1, 2, 5 | | 5 | 15 | µA | CMOS Inputs, $V_{CC}=V_{CC}$Max., CE#=$V_{IH}$, RST#=$V_{CC}$±0.2V |
| $I_{CCS2}$ | $V_{CC}$ Standby Current (LPC Interface) | 1, 2, 5 | | 5 | 15 | µA | CMOS Inputs, $V_{CC}=V_{CC}$Max., CE#=$V_{IL}$, f(CLK)=33MHz LFRAME#=$V_{IH}$, RST#=$V_{CC}$±0.2V |
| $I_{CCRY}$ | $V_{CC}$ Ready Mode Current (LPC Interface) | 1, 2, 5 | | 5 | 8 | mA | CMOS Inputs, $V_{CC}=V_{CC}$Max., CE#=$V_{IL}$, f(CLK)=33MHz LFRAME#=$V_{IL}$, RST#=$V_{CC}$±0.2V |
| $I_{CCS3}$ | $V_{CC}$ Standby Current (A/A Interface) | 1, 2, 5 | | 5 | 8 | mA | CMOS Inputs, $V_{CC}=V_{CC}$Max., RST#=$V_{CC}$±0.2V, R/C#=OE#=WE#=$V_{IH}$ |
| $I_{CCD}$ | $V_{CC}$ Reset Current | 1 | | 5 | 15 | µA | RST#=GND±0.2V, $I_{OUT}$ (RY/BY#)=0mA |
| $I_{CCR1}$ | $V_{CC}$ Read Current (LPC Interface) | 1, 2 | | | 15 | mA | CMOS Inputs, $V_{CC}=V_{CC}$Max., CE#=LFRAME#=$V_{IL}$, f(CLK)=33MHz, $I_{OUT}$=0mA |
| $I_{CCR2}$ | $V_{CC}$ Read Current (A/A Interface) | 1, 2 | | | 15 | mA | CMOS Inputs, $V_{CC}=V_{CC}$Max., f=4MHz, $I_{OUT}$=0mA |
| $I_{CCW}$ | $V_{CC}$ Byte Program, Set Top Boot Lock Bit Current | 1, 2, 4 | | | 25 | mA | CMOS Inputs, $V_{CC}=V_{CC}$Max. |
| $I_{CCE}$ | $V_{CC}$ Sector/Block Erase, Full Chip Erase, Clear Top Boot Lock Bits Current | 1, 2, 4 | | | 25 | mA | CMOS Inputs, $V_{CC}=V_{CC}$Max. |

DC Characteristics (Continued)

$V_{CC}$=3.0V-3.6V

| Symbol | Parameter | Notes | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 4 | 0.5× $V_{CC}$ | $V_{CC}$ + 0.5 | V | $V_{CC}$=$V_{CC}$Max., |
| $V_{IL}$ | Input Low Voltage | 4 | -0.5 | 0.3× $V_{CC}$ | V | $V_{CC}$=$V_{CC}$Min., |
| $V_{OH}$ | Output High Voltage | 4 | 0.9× $V_{CC}$ | | V | $V_{CC}$=$V_{CC}$Min., $I_{OH}$=-0.5mA |
| $V_{OL}$ | Output Low Voltage | 4, 5 | | 0.1× $V_{CC}$ | V | $V_{CC}$=$V_{CC}$Min., $I_{OL}$=1.5mA |
| $V_{LKO}$ | $V_{CC}$ Lockout Voltage | 3 | 2.0 | | V | |

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values are the reference values at $V_{CC}$=3.3V and $T_A$=+25°C unless $V_{CC}$ is specified.
2. CMOS inputs are either $V_{CC}$±0.2V or GND±0.2V.
3. Sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set top boot lock bit and clear top boot lock bits operations are inhibited when $V_{CC} \leq V_{LKO}$. These operations are not guaranteed outside the specified voltage ($V_{CC}$=3.0V-3.6V).
4. Sampled, not 100% tested.
5. Includes RY/BY#.

### 4.2.4 AC Characteristics (LPC Mode) (1)

AC Characteristics (LPC Mode)

$V_{CC}$=3.0V~3.6V, $T_A$=0°C~+85°C

| Symbol | Parameter | Notes | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{CYC}$ | Clock Cycle Time | | 30 | | | ns |
| $t_{HIGH}$ | LCLK High Time | | 11 | | | ns |
| $t_{LOW}$ | LCLK Low Time | | 11 | | | ns |
| | LCLK Slew Rate (peak-to-peak) | | 1 | | 4 | V/ns |
| $t_{SU}$ | Data Set-up Time to Clock Rising | | 9 | | | ns |
| $t_{DH}$ | Data Hold Time from Clock Rising | | 0 | | | ns |
| $t_{FSU}$ | LFRAME# Set-up Time to Clock Rising | | 18 | | | ns |
| $t_{FDH}$ | LFRAME# Hold Time from Clock Rising | | 2 | | | ns |
| $t_{VAL}$ | Clock Rising to Data Valid | | 2 | | 15 | ns |
| $t_{ON}$ | Clock Rising to Output in Low Z | 3 | 2 | | | ns |
| $t_{OFF}$ | Clock Rising to Output in High Z | 3 | | | 28 | ns |
| $t_{WQV1}$ | Byte Program Time | 3, 4 | | 25 | 200 | µs |
| $t_{WQV2}$ | Sector Erase Time | 3, 4 | | 0.6 | 5 | s |
| $t_{WQV3}$ | Block Erase Time | 3, 4 | | 1.2 | 6 | s |
| $t_{WQV4}$ | Full Chip Erase Time | 3, 4 | | 40 | 200 | s |
| $t_{SWBL}$ | Set Whole Block Lock Bit Time | 3, 4 | | 5 | 10 | µs |
| $t_{CWBL}$ | Clear Whole Block Lock Bit Time | 3, 4 | | 5 | 10 | µs |
| $t_{STBL}$ | Set Top Boot Lock Bit Time | 3, 4 | | 35 | 200 | µs |
| $t_{CTBL}$ | Clear Top Boot Lock Bits Time | 3, 4 | | 0.4 | 5 | s |

NOTES:
1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. Typical values measured at $V_{CC}$=3.3V and $T_A$=+25°C. Assumes TBL#, WP# and corresponding lock bits are not set. Subject to change based on device characterization.
3. Sampled, not 100% tested.
4. Excludes external system-level overhead.

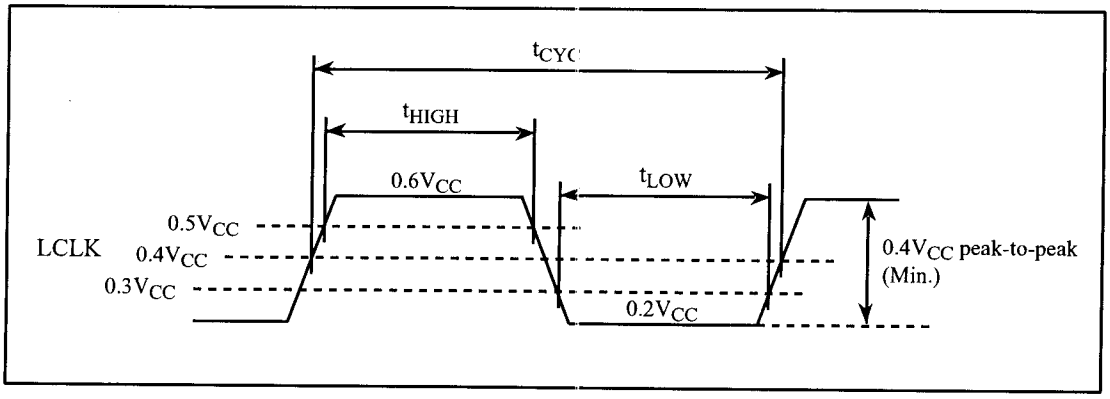



Figure 12. LCLK Waveform

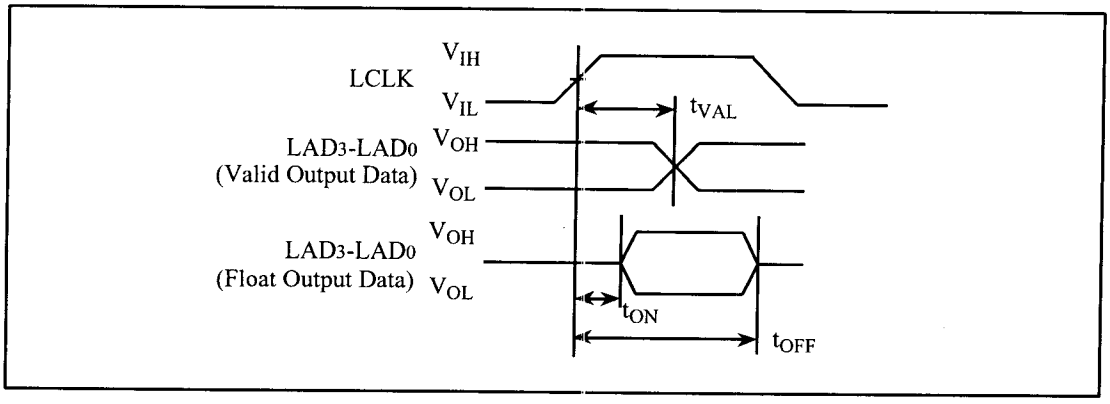



Figure 13. Output Timing Parameters

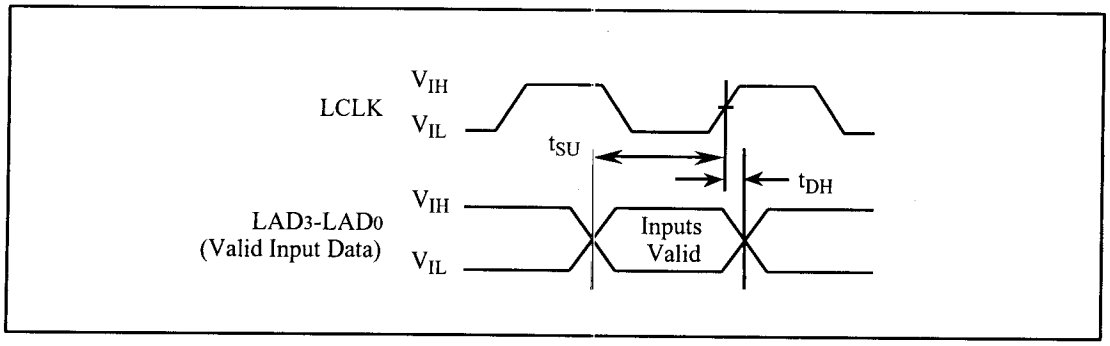



Figure 14. Input Timing Parameters

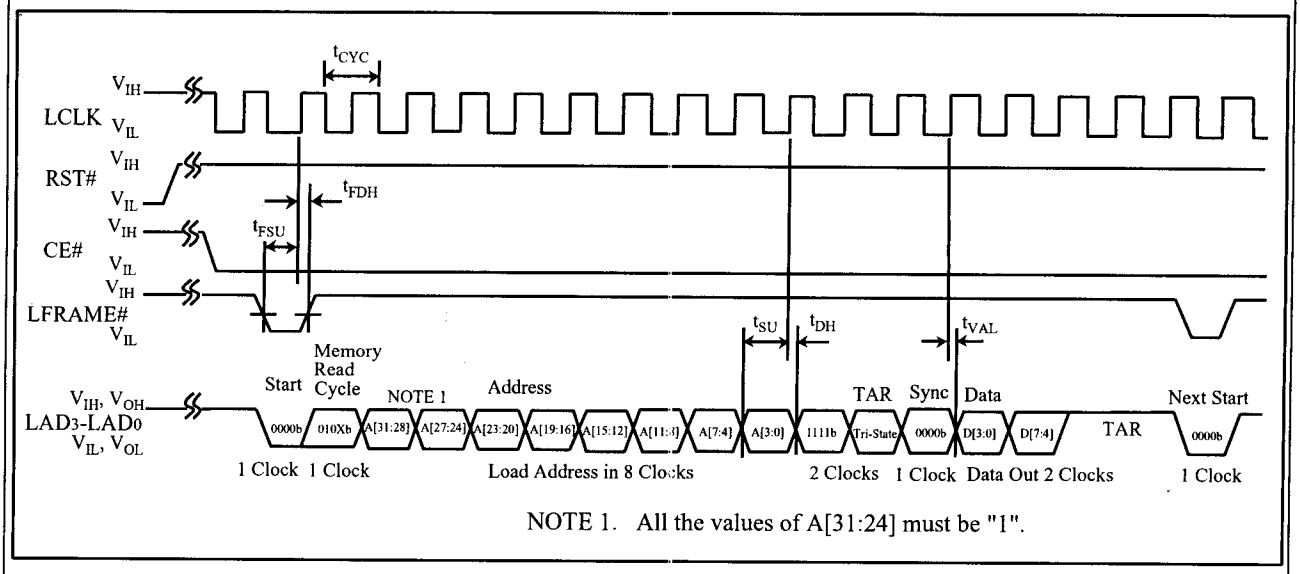



Figure 15. Read Cycle Timing Diagram (LPC Mode)

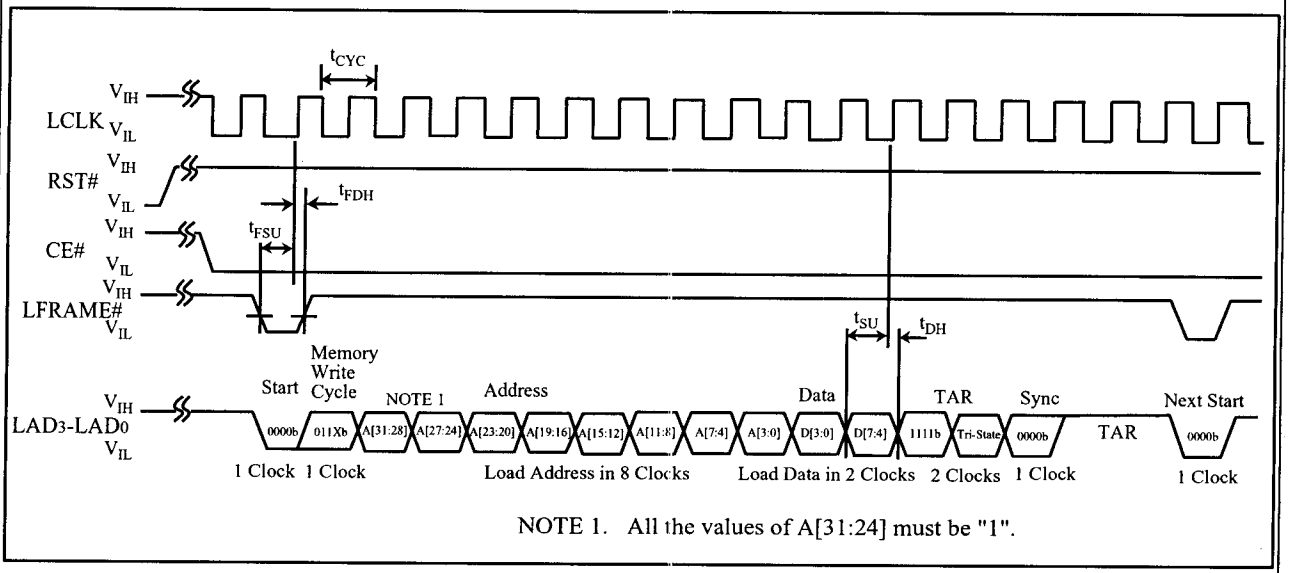
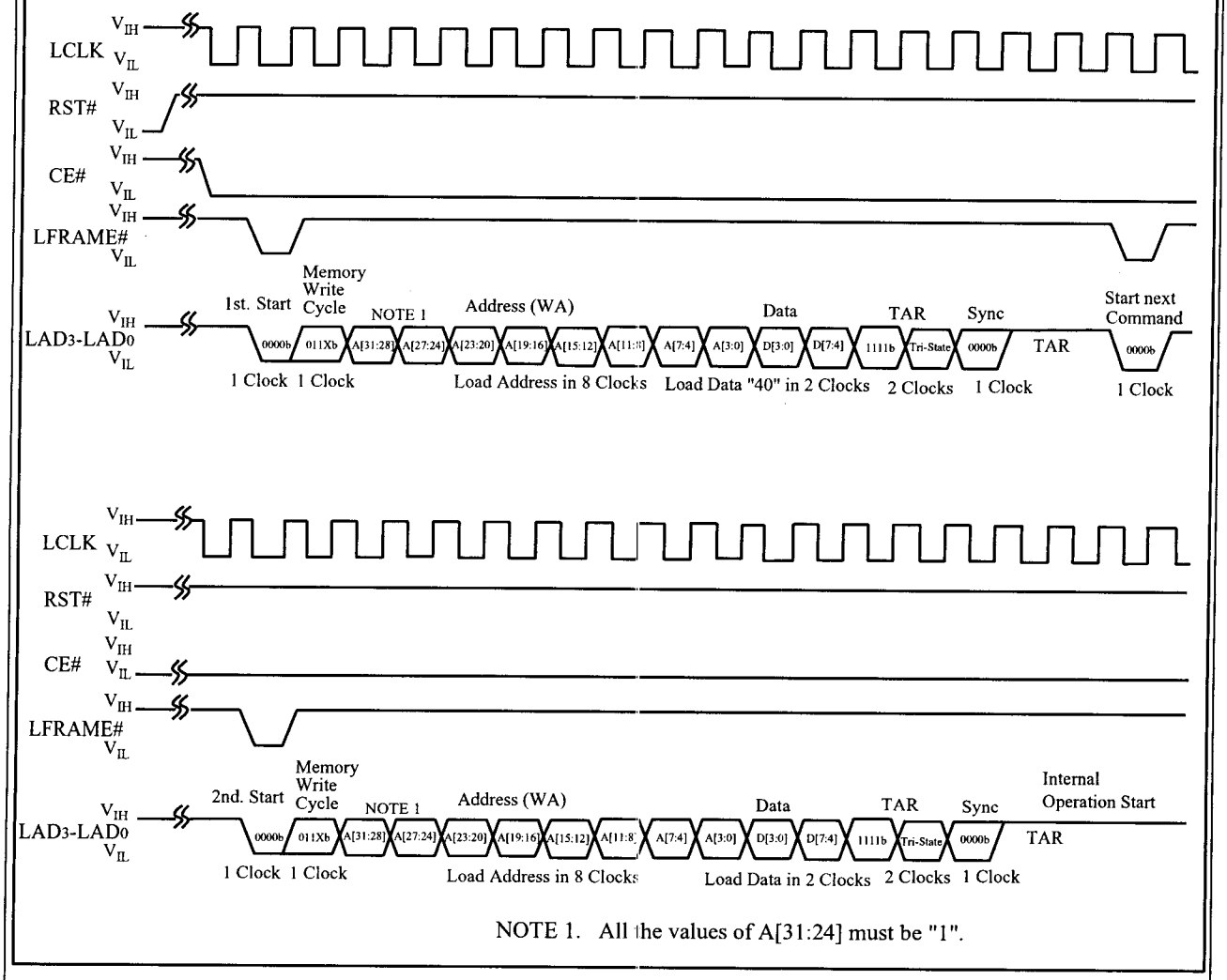



Figure 16. Write Cycle Timing Diagram (LPC Mode)




NOTE 1. All the values of A[31:24] must be "1".

Figure 17. Byte Program Cycle Timing Diagram (LPC Mode)

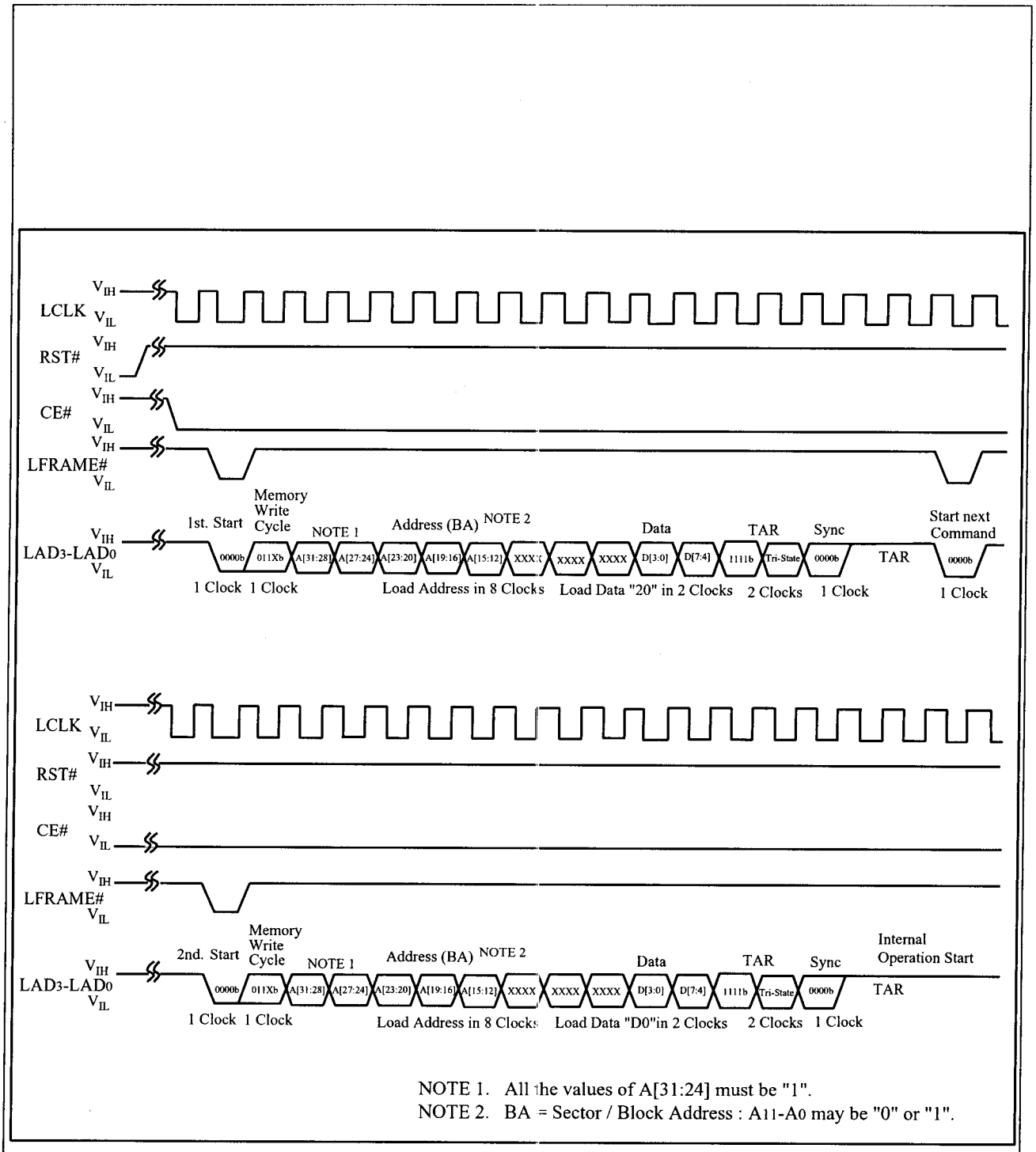



Figure 18. Sector/Block Erase Cycle Timing Diagram (LPC Mode)

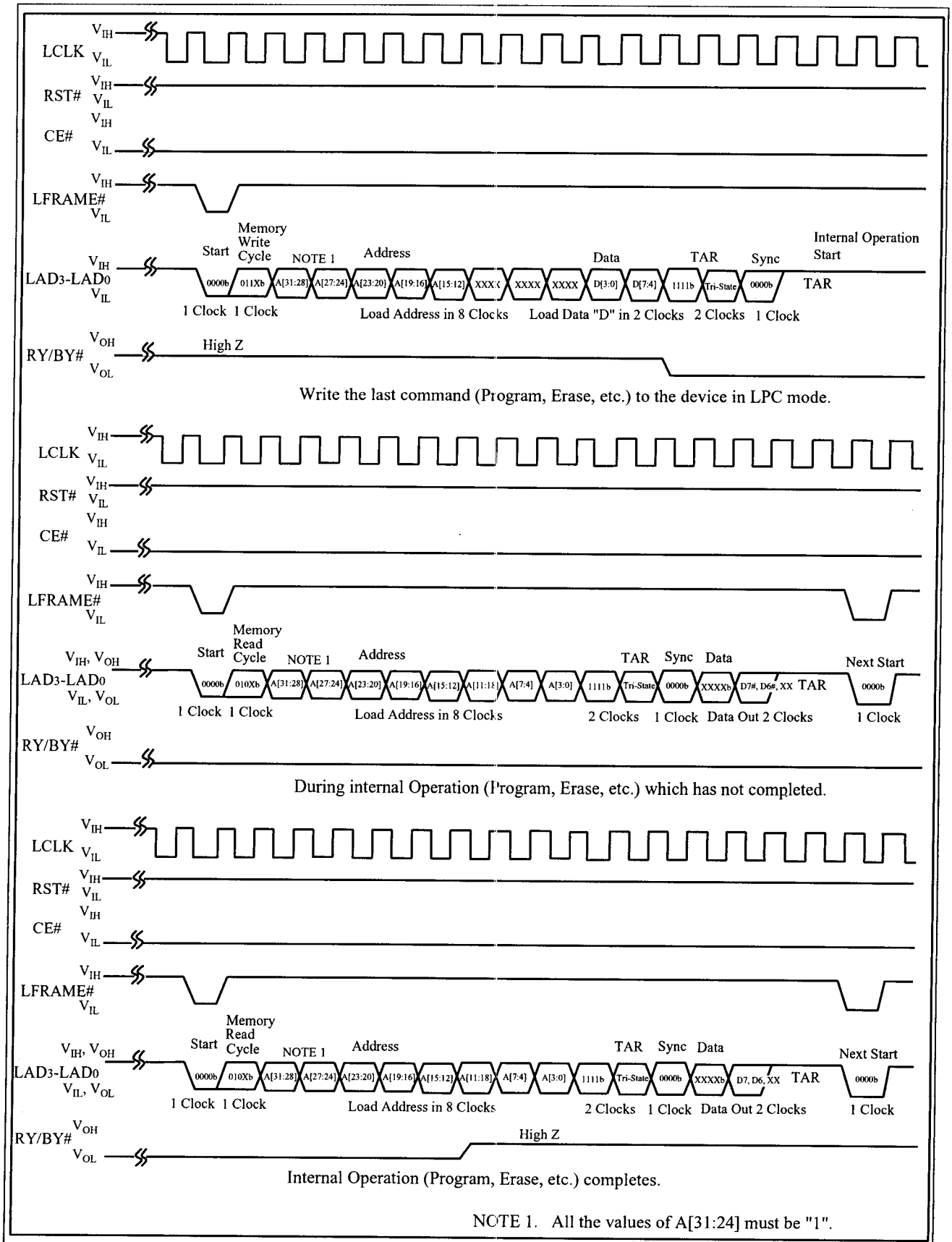



Figure 19. Status Polling, Toggle Bit Timing Diagram (LPC Mode)

### 4.2.5 Reset and Abort Operations (LPC Mode)

Reset and Abort Characteristics (LPC Mode)

$V_{CC}$=3.0V~3.6V, $T_A$=0°C~+85°C

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{PRSTH}$ | $V_{CC}$ 3.0V stable to RST#/INIT# High | 2 | 100 | | ns |
| $t_{PRSTL}$ | $V_{CC}$ 3.0V stable to RST#/INIT# Low | 2 | 1 | | ms |
| $t_{KRST}$ | Clock stable to RST#/INIT# Low | 2 | 100 | | µs |
| $t_{RSTP}$ | RST#/INIT# Pulse Width Low | 1, 2 | 100 | | ns |
| | RST#/INIT# Slew Rate | 2 | 50 | | mV/ns |
| $t_{RSTF}$ | RST#/INIT# Low to Output in High Z | 2 | | 48 | ns |
| $t_{RSTL}$ | RST#/INIT# High to LFRAME# Low | 2, 3 | 1 | | µs |
| $t_{ABTL}$ | Abort Command to LFRAME# Low | 2 | 60 | | ns |
| $t_{RSTE}$ | RST#/INIT# Low to Reset during internal operation | 2, 4 | | 30 | µs |

NOTES:
1. The device may reset if $t_{RSTP}$ < 100ns, but this is not guaranteed.
2. Sampled, not 100% tested.
3. There will be a latency of $t_{RSTE}$ if a reset/abort procedure is performed during an internal operation.
4. If RST#/INIT# asserted while a sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set top boot lock bit and clear top boot lock bits operations are not executing, the reset will complete within 100ns.

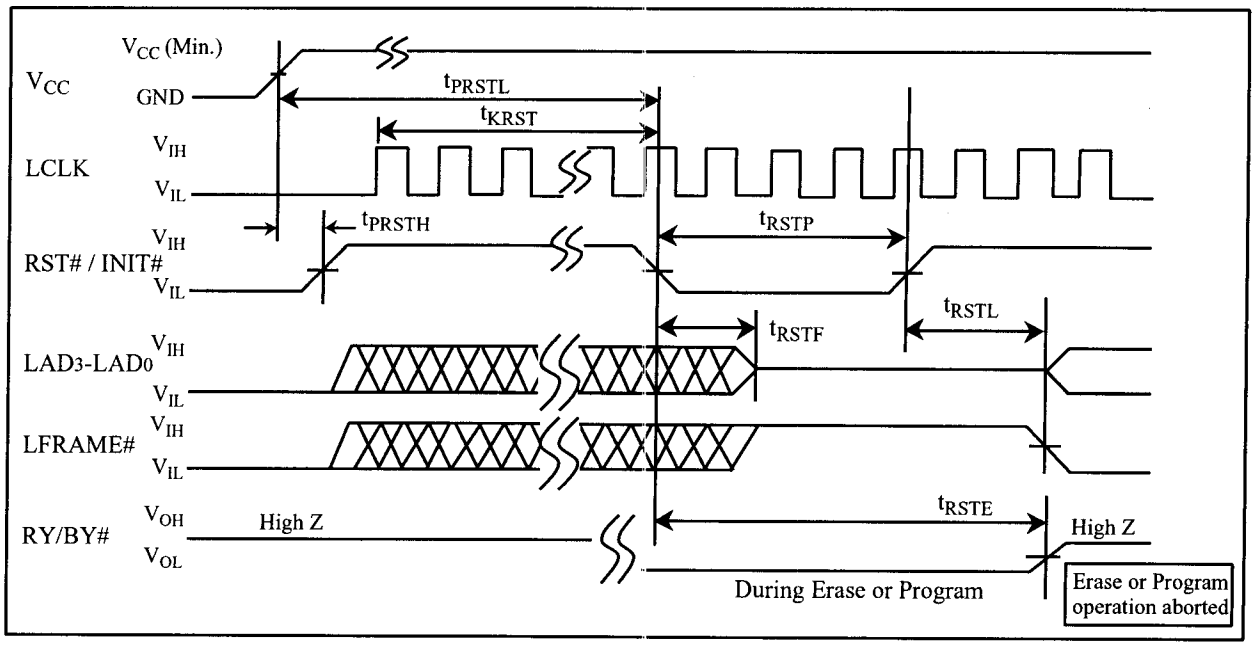



Figure 20. Reset Operation by RST#/INIT# Timing Diagram (LPC Mode)

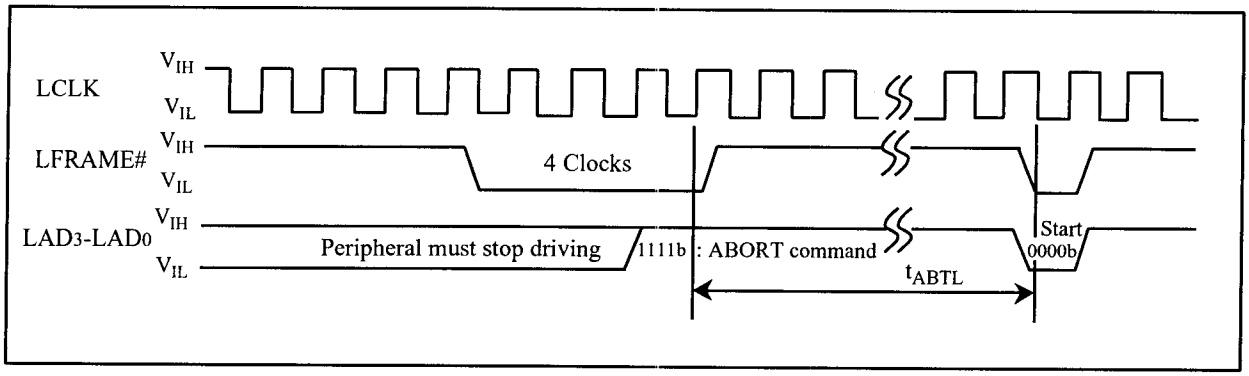



Figure 21. Abort Operation Timing Diagram (LPC Mode)

### 4.2.6 AC Characteristics (A/A Mode) (1)

Read Characteristics (A/A Mode)

$V_{CC}$=3.0V~3.6V, $T_A$=0°C~+85°C

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle Time | | 250 | | ns |
| $t_{RSTA}$ | RST# High Recovery to Row Address | | 1 | | µs |
| $t_{AS}$ | Address Setup to R/C# | | 50 | | ns |
| $t_{AH}$ | Address Hold from R/C# | | 50 | | ns |
| $t_{AA}$ | Address to Output Delay | 2 | | 100 | ns |
| $t_{OE}$ | OE# to Output Delay | 2 | | 60 | ns |
| $t_{OLZ}$ | OE# to Output in Low Z | 3 | 0 | | ns |
| $t_{OHZ}$ | OE# to Output in High Z | 3 | | 35 | ns |
| $t_{OH}$ | Output Hold from Address | 3 | 0 | | ns |

NOTES:
1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. OE# may be delayed up to $t_{AA} - t_{OE}$ after the rising edge of R/C# without impact to $t_{AA}$.
3. Sampled, not 100% tested.

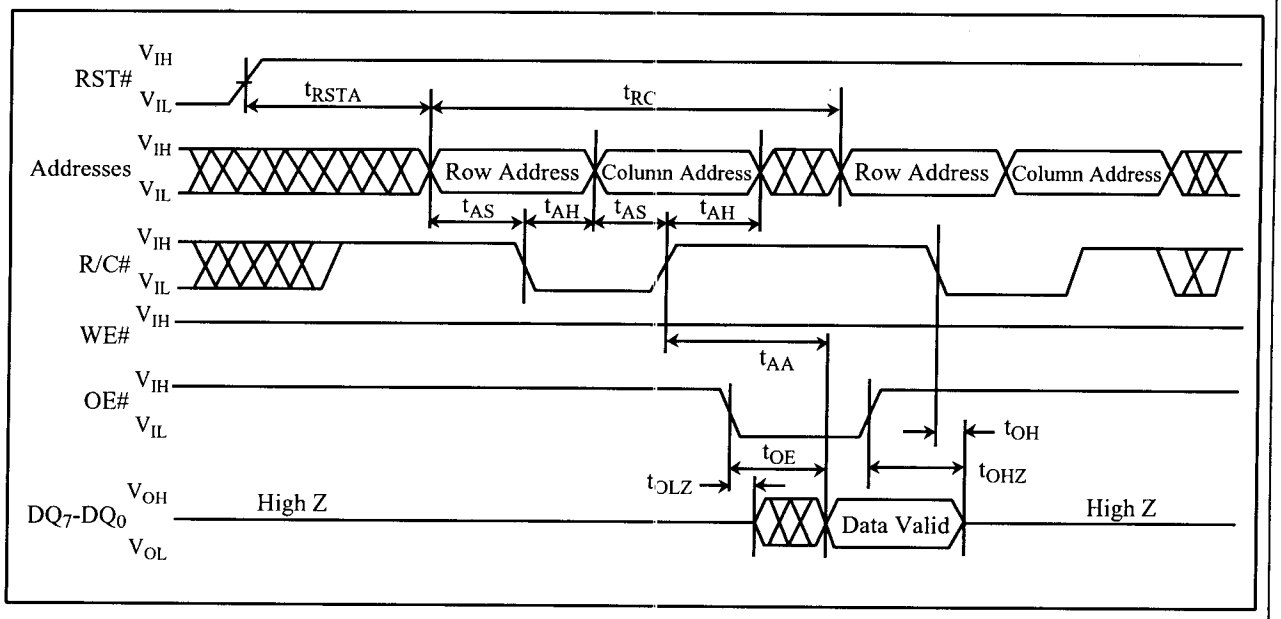



Figure 22. Read Cycle Timing Diagram (A/A Mode)

Write Characteristics (A/A Mode)

$V_{CC}$=3.0V~3.6V, $T_A$=0°C~+85°C

| Symbol | Parameter | Notes | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{WC}$ | Write Cycle Time | | 200 | | | ns |
| $t_{RSTA}$ | RST# High Recovery to Row Address | | 30 | | | µs |
| $t_{AS}$ | Address Setup to R/C# | 4 | 50 | | | ns |
| $t_{AH}$ | Address Hold from R/C# | | 50 | | | ns |
| $t_{CWH}$ | R/C# to WE# High Time | | 50 | | | ns |
| $t_{OES}$ | OE# High Setup Time | | 20 | | | ns |
| $t_{OEH}$ | OE# High Hold Time | | 20 | | | ns |
| $t_{OEP}$ | OE# to Status Polling Delay | 2 | | | 40 | ns |
| $t_{OET}$ | OE# to Toggle Bit Delay | 2 | | | 40 | ns |
| $t_{WP}$ | WE# Pulse Width Low | | 100 | | | ns |
| $t_{WPH}$ | WE# Pulse Width High | | 100 | | | ns |
| $t_{DS}$ | Data Setup to WE# High | 4 | 50 | | | ns |
| $t_{DH}$ | Data Hold from WE# High | | 10 | | | ns |
| $t_{IDA}$ | ID Access Time | | | | 150 | ns |
| $t_{RB}$ | WE# High to RY/BY# going Low | 3 | | | 100 | ns |
| $t_{WQV1}$ | Byte Program Time | 3, 5 | | 25 | 200 | µs |
| $t_{WQV2}$ | Sector Erase Time | 3, 5 | | 0.6 | 5 | s |
| $t_{WQV3}$ | Block Erase Time | 3, 5 | | 1.2 | 6 | s |
| $t_{WQV4}$ | Full Chip Erase Time | 3, 5 | | 40 | 200 | s |
| $t_{SWBL}$ | Set Whole Block Lock Bit Time | 3, 5 | | 5 | 10 | µs |
| $t_{CWBL}$ | Clear Whole Block Lock Bit Time | 3, 5 | | 5 | 10 | µs |
| $t_{STBL}$ | Set Top Boot Lock Bit Time | 3, 5 | | 35 | 200 | µs |
| $t_{CTBL}$ | Clear Top Boot Lock Bits Time | 3, 5 | | 0.4 | 5 | s |

NOTES:

1. Typical values measured at $V_{CC}$=3.3V and $T_A$=+25°C. Assumes TBL#, WP# and corresponding lock bits are not set. Subject to change based on device characterization.
2. The timing characteristics for reading the status register during sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set top boot lock bit and clear top boot lock bits operations are the same as during read-only operations. Refer to Read Characteristics (A/A Mode) for read-only operations.
3. Sampled, not 100% tested.
4. Refer to Table 10 for valid address and data for sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set top boot lock bit and clear top boot lock bits.
5. Excludes external system-level overhead.

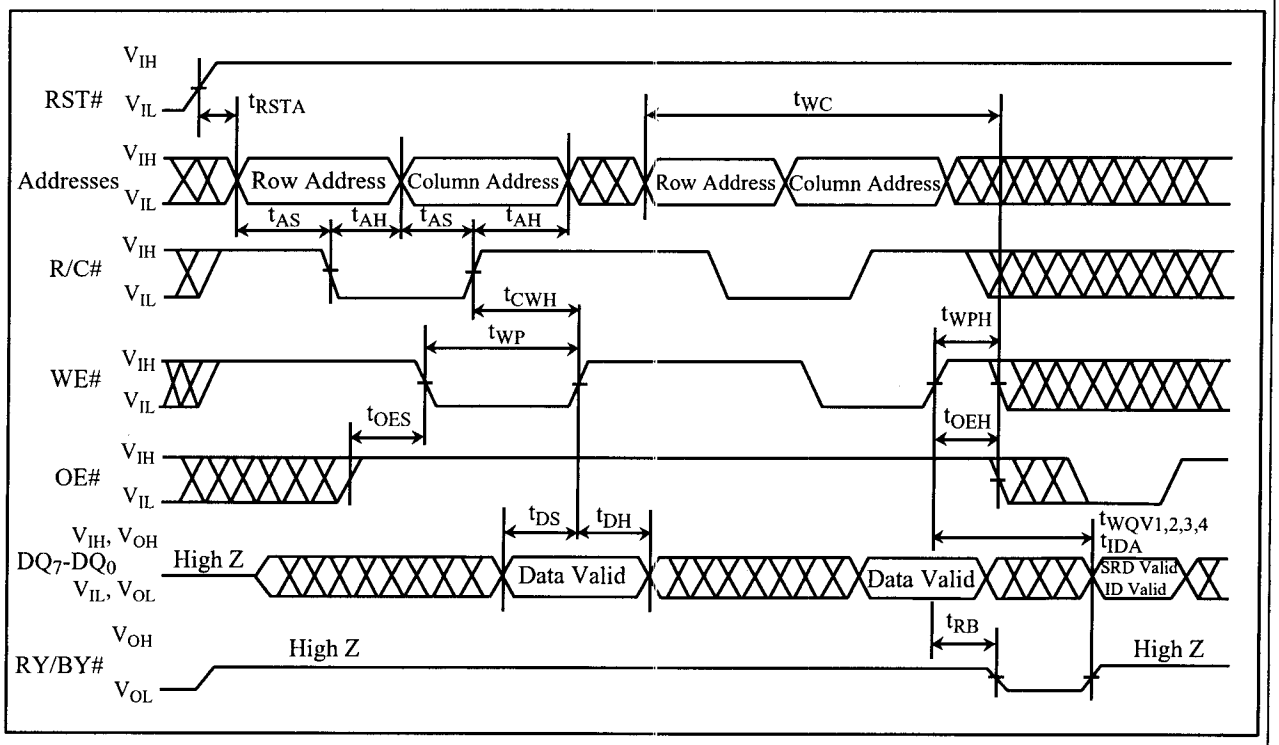



Figure 23. Write Cycle Timing Diagram (A/A Mode)

### 4.2.7 Reset Operations (A/A Mode)

Reset Characteristics (A/A Mode)

$V_{CC}$=3.0V~3.6V, $T_A$=0°C~+85°C

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{PRSTH}$ | $V_{CC}$ 3.0V stable to RST# High | 2 | 100 | | ns |
| $t_{PRSTL}$ | $V_{CC}$ 3.0V stable to RST# Low | 2 | 1 | | ms |
| $t_{RSTP}$ | RST# Pulse Width Low | 1, 2 | 100 | | ns |
| | RST# Slew Rate | 2 | 50 | | mV/ns |
| $t_{RSTF}$ | RST# Low to Output in High Z | 2 | | 48 | ns |
| $t_{RSTA}$ | RST# High to Row Address Valid | 2, 3 | 1 | | µs |
| $t_{RSTE}$ | RST# Low to Reset during erase or program operation | 2, 4 | | 30 | µs |

NOTES:
1. The device may reset if $t_{RSTP}$ < 100ns, but this is not guaranteed.
2. Sampled, not 100% tested.
3. There will be a latency of $t_{RSTE}$ if a reset procedure is performed during an internal operation.
4. If RST# asserted while a sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set top boot lock bit and clear top boot lock bits operations are not executing, the reset will complete within 100ns.

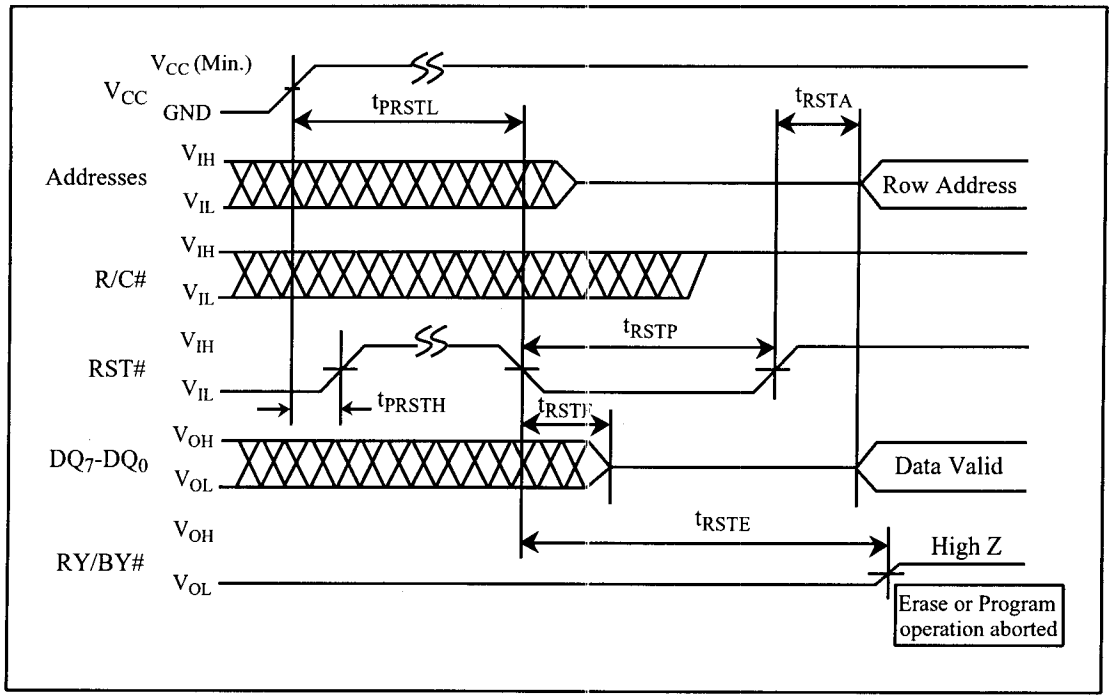
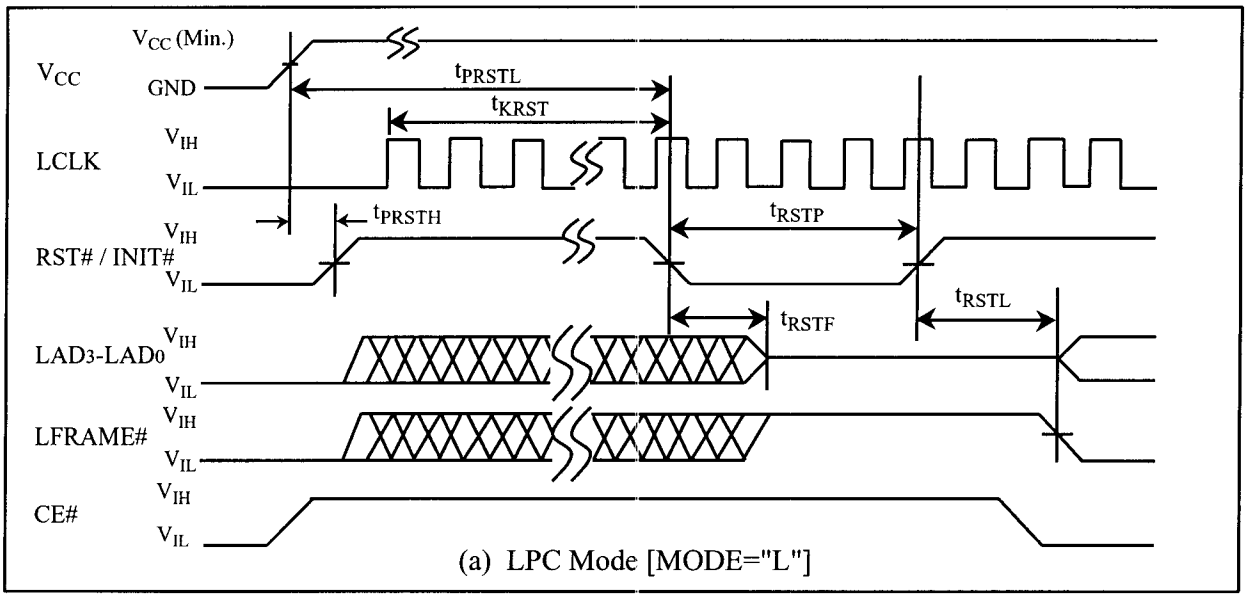



Figure 24. Reset Operation Timing Diagram (A/A Mode)

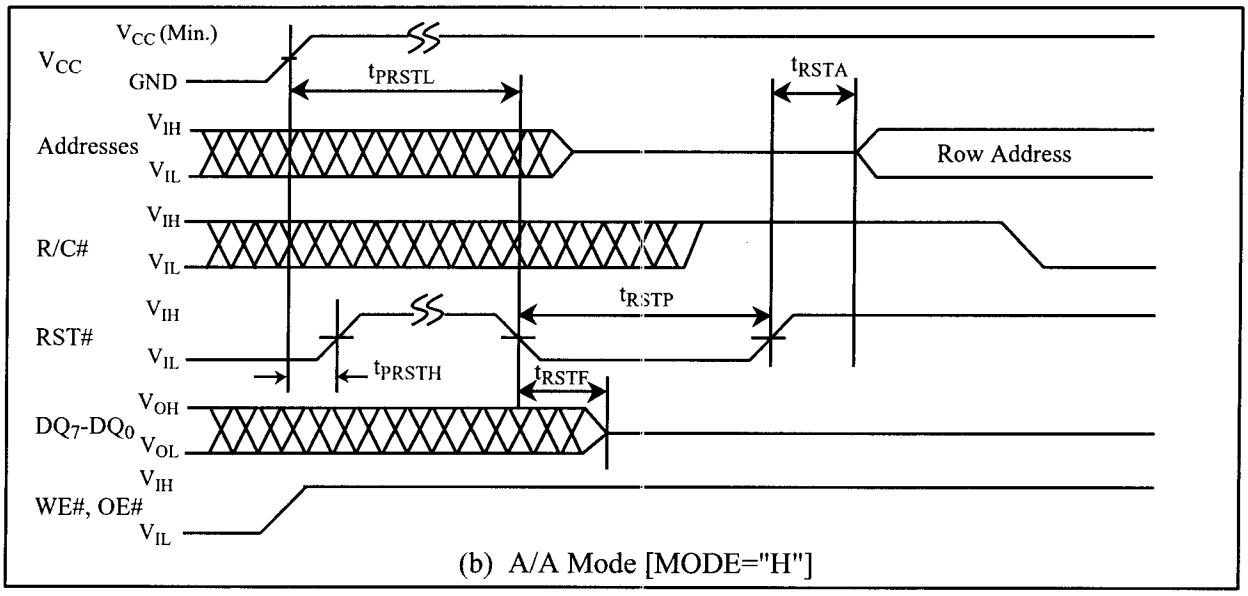
## A-1 RECOMMENDED OPERATING CONDITIONS

### A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.




(a) LPC Mode [MODE="L"]




(b) A/A Mode [MODE="H"]

Figure A-1. AC Timing at Device Power-Up

See the "ELECTRICAL SPECIFICATIONS" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

### A-1.1.1 Rise and Fall Time

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{VR}$ | $V_{CC}$ Rise Time | 1 | 0.5 | 30000 | µs/V |
| $t_R$ | Input Signal Rise Time | 1, 2 | | 1 | µs/V |
| $t_F$ | Input Signal Fall Time | 1, 2 | | 1 | µs/V |

NOTES:
1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.
   $t_R$(Max.) and $t_F$(Max.) for RST# (INIT#) are 100µs/V

## A-1.2 Glitch Noises

Do not input the glitch noises which are below $V_{IH}$ (Min.) or above $V_{IL}$ (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

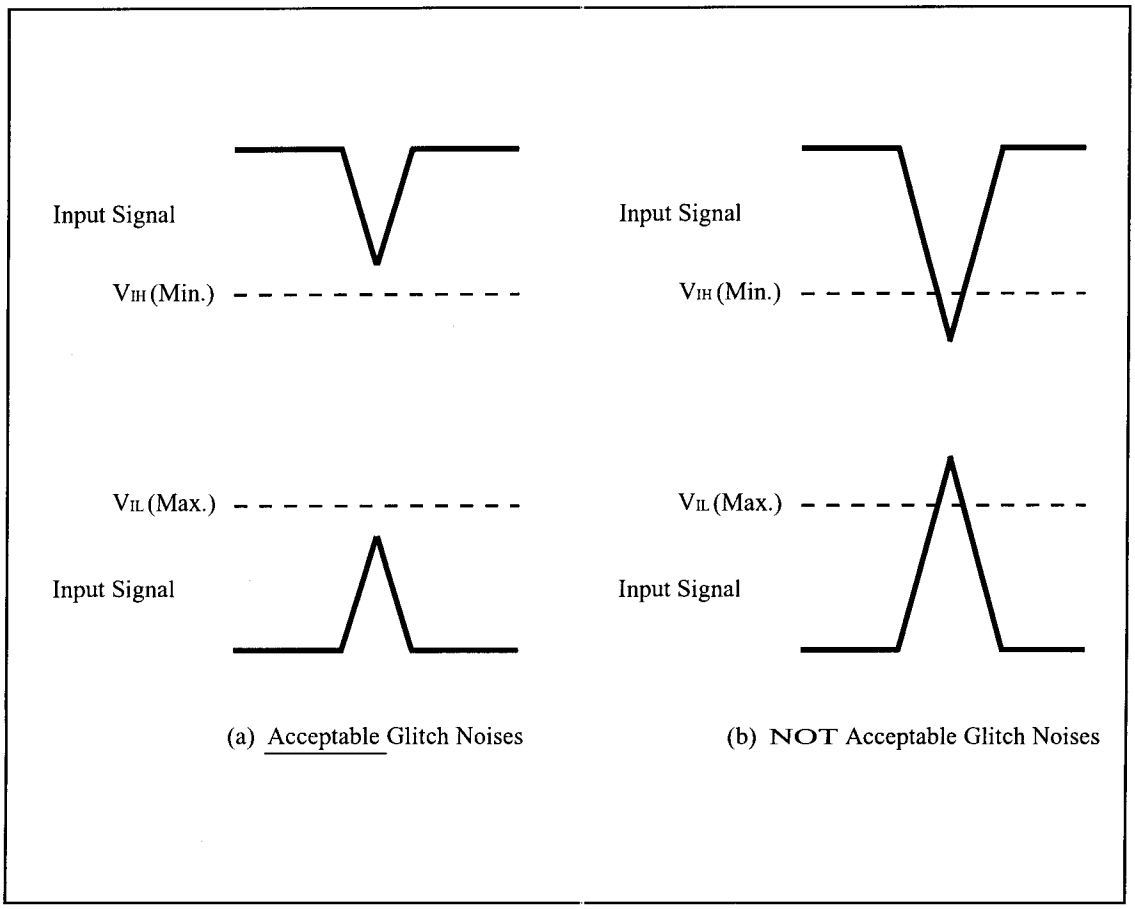



Figure A-2. Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for $V_{IH}$ (Min.) and $V_{IL}$ (Max.).

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