Frequently Asked Questions About TSWC0x622/TSYN0x622 Devices

1 General

Question 1. Where can I find more information on the TSWC0x622 and TSYN0x622 devices?

Answer: More information, including data sheets and application notes are located on the Agere Systems website:
http://www.agere.com/enterprise_metro_access/system_timing_devices.html

Question 2. Are evaluation boards available for the TSWC0x622 and the TSYN0x622 devices?

Answer: Yes, please contact the Agere Systems sales person or FAE.

Question 3. What are the differences between the TSWC0x622 and TSYN0x622 products?

Answer: The different TSWC/TSYN products are targeted at the following applications.

Device	Application
TSWC01622	General hitless protection switch with PDH and SONET/SDH outputs for OC-48/OC-192 systems.
TSWC02622	Hitless protection switch with only 155.52 MHz and 622.08 MHz SONET/SDH outputs for OC-48/OC-192 systems.
TSWC03622	General hitless protection switch with PDH and SONET/SDH outputs for PDH/OC-3/OC-12 systems.
TSYN01622	Clock synthesis device with PDH and SONET/SDH outputs for OC-48/OC-192 systems (no hitless protection switch).
TSYN03622	Clock synthesis device with PDH and SONET/SDH outputs for PDH/OC-3/OC-12 systems (no hitless protection switch).

Question 4. What is the correct ordering information for the TSWC0x622 and TSYN0x622 devices?

Answer: The ordering information is shown in the table below.

Device	Full Part Number	Comcode
TSWC01622	TSWC01622-3-BAL-DB	108696386
TSWC02622	TSWC02622-3-BAL-DB	700021310
TSWC03622	TSWC03622-3-BAL-DB	700021311
TSYN01622	TSYN01622-3-BAL-DB	700034203
TSYN03622	TSYN03622-3-BAL-DB	700049132

Question 5. Is information available for interfacing the TSWC/TSYN devices to other Agere Systems devices?

Answer: Yes, please see the website listed above for current application notes. If an application note for the desired device is not on that site, please contact the local FAE.

2 Loop Filters

Question 1. Are there recommended loop filters for the TSWC0x622/TSYN0x622 devices?

Answer: Yes, recommended loop filters for the TSWC/TSYN devices can be found in the data sheets. Two loop filters are required, one for the low-speed PLL and one for the high-speed PLL. The low-speed PLL loop filter can be configured in two different ways, depending on how large the maximum phase offset will be between clock A and clock B (see the respective data sheet for more information).

Question 2. Are there recommended components for the VCXO, high-value capacitors, and inductors?

Answer: Yes, please see the *TSWC01622/TSYN01622 Loop Filters: Compatible Components* application note for details.

3 CKPDHx Programmable Outputs

Question 1. What is the frequency range of the programmable outputs?

Answer: CKPDH1–3 have a range of 607.5 kHz—65.536 MHz. CKPDH4–5 have a range of 151.875 kHz—38.88 MHz.

4 Fanout

Question 1. How can I get increased fanout?

Answer: There are several ways to increase fanout on the device including using external fanout buffers and using a single output to drive multiple loads. An application note has been written to discuss alternatives. Please contact the local FAE for more information.

Question 2. How do I get programmable clock rates above the maximum output of the TSWC0x622/TSYN0x622?

Answer: One solution is to program the TSWC0x622/TSYN0x622 to a submultiple of the desired frequency and then multiply it externally to achieve the desired rate. Agere Systems has several frequency multipliers available, i.e., LCK4950, LCK4972, LCK4973, LCK4993, and LCK4994.

5 Board Layout Considerations

Question 1. Which inputs need pull-ups or pull-downs?

Answer: No inputs need pull-ups or pull-downs. All inputs are internally tied through 50 kΩ resistors, either to V$_{DD}$ or GND.

Question 2. Which unused outputs need to be terminated?

Answer: No unused outputs need to be terminated. All outputs are internally tied to either V$_{DD}$ or to GND.

Question 3. How are used outputs terminated?

Answer: CMOS and LVDS outputs can be directly connected to their target. LVPECL outputs need to be terminated with 50 Ω to V$_{DD}$ – 2.0 V.

Question 4. What considerations should be taken to power supply filtering and grouping?

Answer: Please see application note *TSWC01622 Power Supply Grouping and Filtering* for details.

Question 5. How should SDH_HW, TSTMODE, and TSTCLKP/N be configured?

Answer: These inputs are for factory test only. They can be left open or tied low.

Question 6. Are there any suggested considerations for board design and layout?

Answer: Yes, please see application note: *Helpful Hints for a Successful TSYN TSWC0x622 Schematic*.

6 Jitter, Phase Noise, and MTIE Performance

Question 1. Do the TSWC0x622 devices meet the ITU and the *Telcordia* ® standard MTIE requirements?

Answer: Yes, the TSWC0x622 devices meet transient and nontransient MTIE (maximum time interval error) requirements for all input and output clock rate combinations.

Question 2. What is the jitter/phase noise performance of the TSWC01622 and the TSYN01622 devices?

Answer: Typical measurements for the 155 MHz and 622 MHz outputs show about 1.7 ps of phase noise. This performance is good for most OC-48 applications. Recommendations are available for using the TSWC01622/TSYN01622 in an OC-192 application, please contact the FAE.

7 Holdover

Question 1. Do the TSWC0x622/TSYN0x622 devices support holdover?

Answer: Standalone, the TSWC/TSYN devices do not implement holdover. The devices can support limited holdover (tens to hundreds of milliseconds) for typical applications. (An application note is available with more detailed information.) True standards compatible holdover can be implemented externally. This external solution is under consideration, please contact the FAE for more information.

Question 2. Do the TSWC0x622/TSYN0x622 devices support stratum 3 or stratum 3E?

Answer: Stratum 2/3/3E/4 compliancy is a system spec, therefore designers are free to do as they may. Historically, the major component costs for system timing card switching solutions are at least several hundred dollars, and major component costs for a line card solution are less than half of that cost. One reason why customers generally just put the stratum compliancy guarantee on the system timing card is cost. There are some systems with 1500 line cards, but even with ordinary systems consisting of 20—30 line cards, it makes a lot more fiscal sense to put all the stringent requirements just on the 2 system timing cards and put as little as possible on the line card. (Smaller systems with just a few cards tend to do a hybrid mix of requirements, if they choose to meet them at all.) When using a TSWC0x622/TSYN0x622, as long as the TSWC0x622/TSYN0x622 has a stratum reference clock valid on its A or B input, the clock on the output will still be stratum traceable and have exactly the same accuracy as the clock on its input. One of the major features that is required for stratum 3/3E support is holdover. Standalone, the TSWC0x622/TSYN0x622 devices do not implement holdover. Holdover can be implemented externally. This external solution is under consideration, please contact the FAE for more information.

8 Serial Interface

Question 1. What can be accomplished through the serial interface vs. external pins?

Answer: The serial interface has all control of the external pins and adds more flexibility. Some of the added flexibility include:

- Ability to program each individual CKPDHx output to any desired frequency (within range) through fractional synthesis.

- Ability to enable or disable each clock and sync output individually.

- Ability to program sync offset over the entire 8 kHz period.

- Ability to control exact duty cycle of sync outputs.

Question 2. Is the serial interface on the TSWC0x622/TSYN0x622 devices compatible with any industry standard?

Answer: No, the serial interface on the TSWC/TSYN devices is a simple interface containing an asynchronous clock, data (I/O), and enable. The data line is composed of a start bit, an 8-bit address, a 6-bit read/write sequence, and a 16-bit data word.

Question 3. Is FPGA/CPLD code available to interface to the TSWC/TSYN serial interface?

Answer: Yes, some VHDL code is available to go from the serial interface to a parallel interface within an FPGA/CPLD. Also drivers are available for a GPIO port, please contact the FAE.

Question 4. Can a script be provided for programming the internal registers?

Answer: Yes, the evaluation board software is capable of creating a script based on the configuration input into the program. Please consult the software manual, please contact the FAE.

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