DS5130 ISSUE 3 February 1999

Features

- Full duplex transmission over a single twisted pair
- Selectable 80 or 160 kbit/s line rate
- Adaptive echo cancellation
- Up to 3km (9171) and 4 km (9172)
- ISDN compatible (2B+D) data format
- Transparent modem capability
- Frame synchronization and clock extraction
- Zarlink ST-BUS compatible
- Low power (typically 50 mW), single 5V supply

Applications

- Digital subscriber lines
- High speed data transmission over twisted wires
- Digital PABX line cards and telephone sets
- 80 or 160 kbit/s single chip modem

Ordering Information

MT9171AE	22 Pin Plastic DIP (400 mil)
MT9171AN	24 Pin SSOP
MT9171AP	28 Pin PLCC
MT9172AE	22 Pin Plastic DIP (400 mil)
MT9172AN	24 Pin SSOP
MT9172AP	28 Pin PLCC

-40°C to +85°C

Description

The MT9171 (DSIC) and MT9172 (DNIC) are pin for pin compatible replacements for the MT8971 and MT8972, respectively. They are multi-function devices capable of providing high speed, full duplex digital transmission up to 160 kbit/s over a twisted wire pair. They use adaptive echo-cancelling techniques and transfer data in (2B+D) format compatible to the ISDN basic rate. Several modes of operation allow an easy interface to digital telecommunication networks including use as a high speed limited distance modem with data rates up to 160 kbit/s. Both devices function identically but with the DSIC having a shorter maximum loop reach specification. The generic "DNIC" will be used to reference both devices unless otherwise noted.

The MT9171/72 is fabricated in Zarlink's ISO^2-CMOS process.

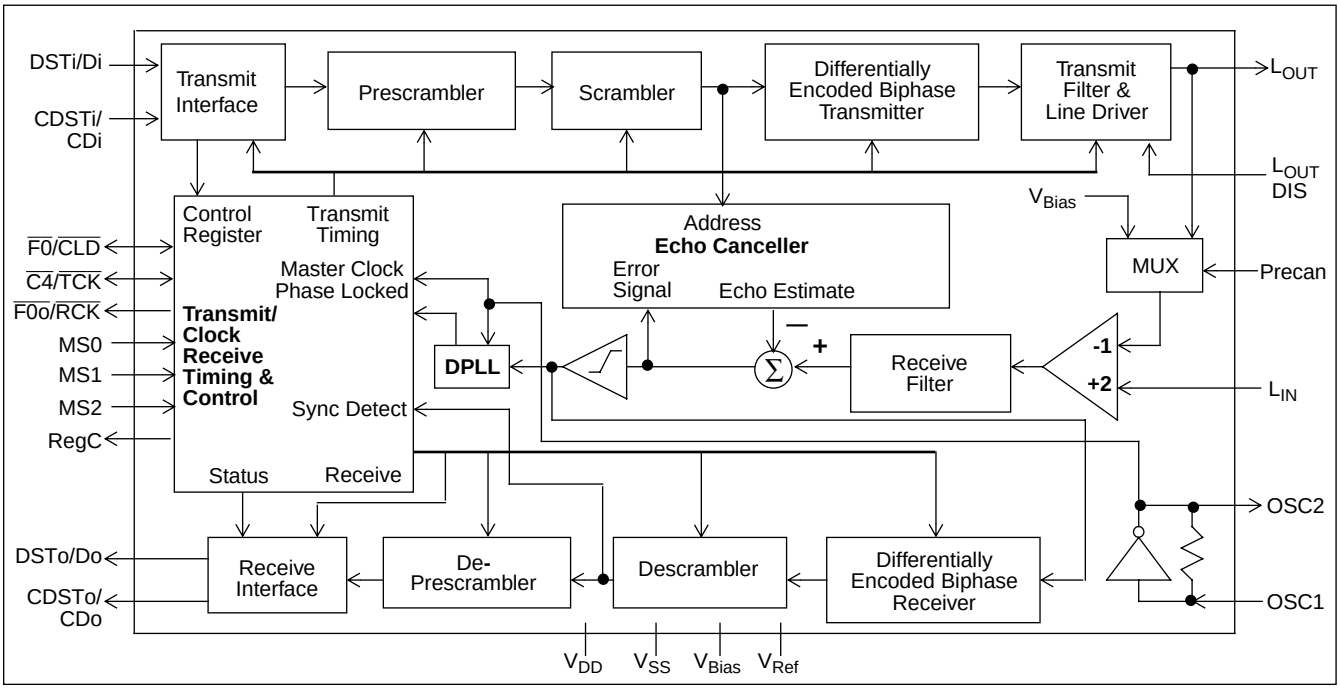


Figure 1 - Functional Block Diagram

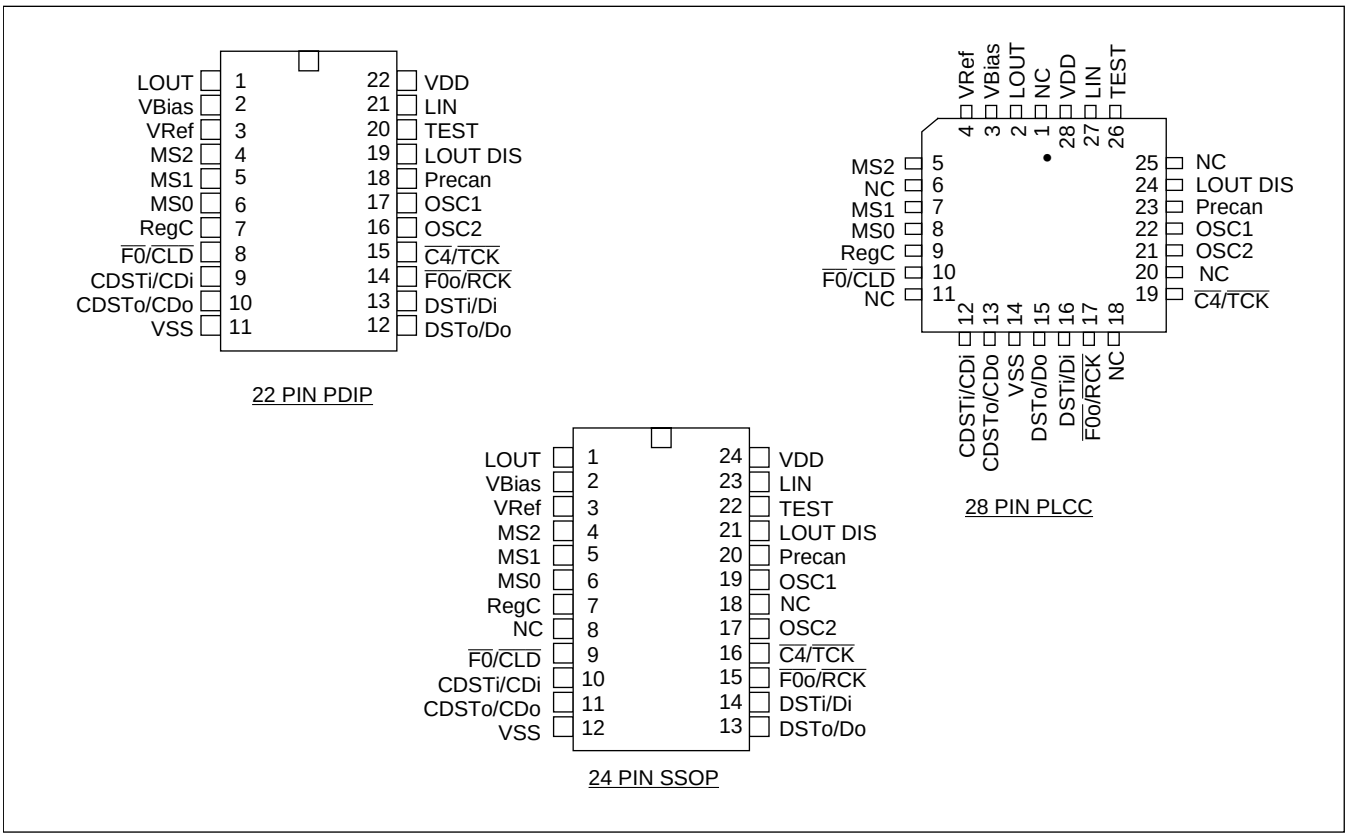


Figure 2 - Pin Connections

Pin Description

Pin #			Name	Description
22	24	28		
1	1	2	L_{OUT}	**Line Out.** Transmit Signal output (Analog). Referenced to V_{Bias}.
2	2	3	V_{Bias}	**Internal Bias Voltage** output. Connect via 0.33 µF decoupling capacitor to V_{DD}.
3	3	4	V_{Ref}	**Internal Reference Voltage** output. Connect via 0.33 µF decoupling capacitor to V_{DD}.
4,5, 6	4,5, 6	5,7, 8	MS2-MS0	**Mode Select** inputs (Digital). The logic levels present on these pins select the various operating modes for a particular application. See Table 1 for the operating modes.
7	7	9	RegC	**Regulator Control** output (Digital). A 512 kHz clock used for switch mode power supplies. Unused in MAS/MOD mode and should be left open circuit.
8	9	10	$\overline{F0}/\overline{CLD}$	**Frame Pulse/C-Channel Load** (Digital). In DN mode a 244 ns wide negative pulse input for the MASTER indicating the start of the active channel times of the device. Output for the SLAVE indicating the start of the active channel times of the device. Output in MOD mode providing a pulse indicating the start of the C-channel.
9	10	12	CDSTi/ CDi	**Control/Data ST-BUS In/Control/Data In** (Digital). A 2.048 Mbit/s serial control & signalling input in DN mode. In MOD mode this is a continuous bit stream at the bit rate selected.
10	11	13	CDSTo/ CDo	**Control/Data ST-BUS Out/Control/Data Out** (Digital). A 2.048 Mbit/s serial control & signalling output in DN mode. In MOD mode this is a continuous bit stream at the bit rate selected.
11	12	14	V_{SS}	**Negative Power Supply** (0V).
12	13	15	DSTo/Do	**Data ST-BUS Out/Data Out** (Digital). A 2.048 Mbit/s serial PCM/data output in DN mode. In MOD mode this is a continuous bit stream at the bit rate selected.

Pin Description (continued)

Pin #			Name	Description
22	24	28		
13	14	16	DSTi/Di	**Data ST-BUS In/Data In** (Digital). A 2.048 Mbit/s serial PCM/data input in DN mode. In MOD mode this is a continuous bit stream at the bit rate selected.
14	15	17	$\overline{F0o}/\overline{RCK}$	**Frame Pulse Out/Receive Bit Rate Clock** output (Digital). In DN mode a 244 ns wide negative pulse indicating the end of the active channel times of the device to allow daisy chaining. In MOD mode provides the receive bit rate clock to the system.
15	16	19	$\overline{C4}/\overline{TCK}$	**Data Clock/Transmit Baud Rate Clock** (Digital). A 4.096 MHz TTL compatible clock input for the MASTER and output for the SLAVE in DN mode. For MOD mode this pin provides the transmit bit rate clock to the system.
16	17	21	OSC2	**Oscillator Output**. CMOS Output.
17	19	22	OSC1	**Oscillator Input**. CMOS Input. D.C. couple signals to this pin. Refer to D.C. Electrical Characteristics for OSC1 input requirements.
18	20	23	Precan	**Precanceller Disable.** When held to Logic '1', the internal path from L_{OUT} to the precanceller is forced to V_{Bias} thus bypassing the precanceller section. When logic '0', the L_{OUT} to the precanceller path is enabled and functions normally. An internal pulldown (50 kΩ) is provided on this pin.
	8, 18	1,6, 11, 18, 20, 25	NC	**No Connection.** Leave open circuit
19	21	24	L_{OUT} DIS	**L_{OUT} Disable.** When held to logic "1", L_{OUT} is disabled (i.e., output = V_{Bias}). When logic "0", L_{OUT} functions normally. An internal pulldown (50 kΩ) is provided on this pin.
20	22	26	TEST	**Test Pin.** Connect to V_{SS}.
21	23	27	L_{IN}	**Receive Signal** input (Analog).
22	24	28	V_{DD}	**Positive Power Supply** (+5V) input.

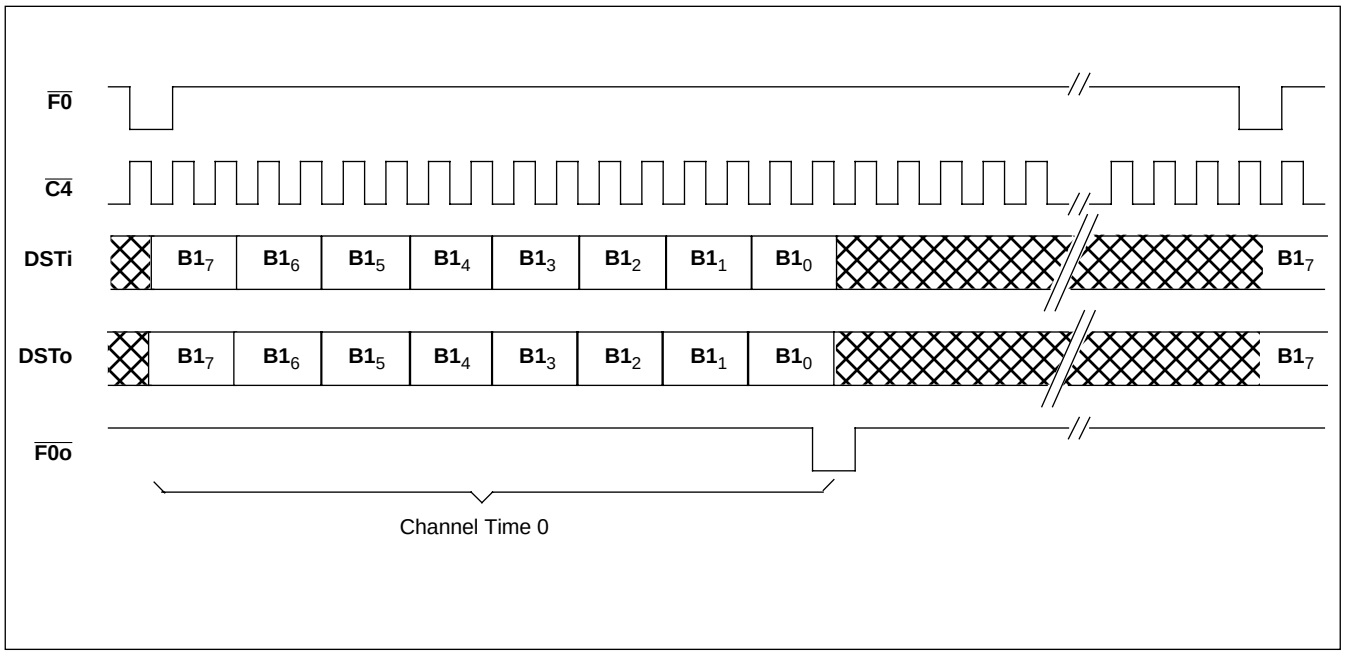


Figure 3 - DV Port - 80 kbit/s (Modes 2, 3, 6)

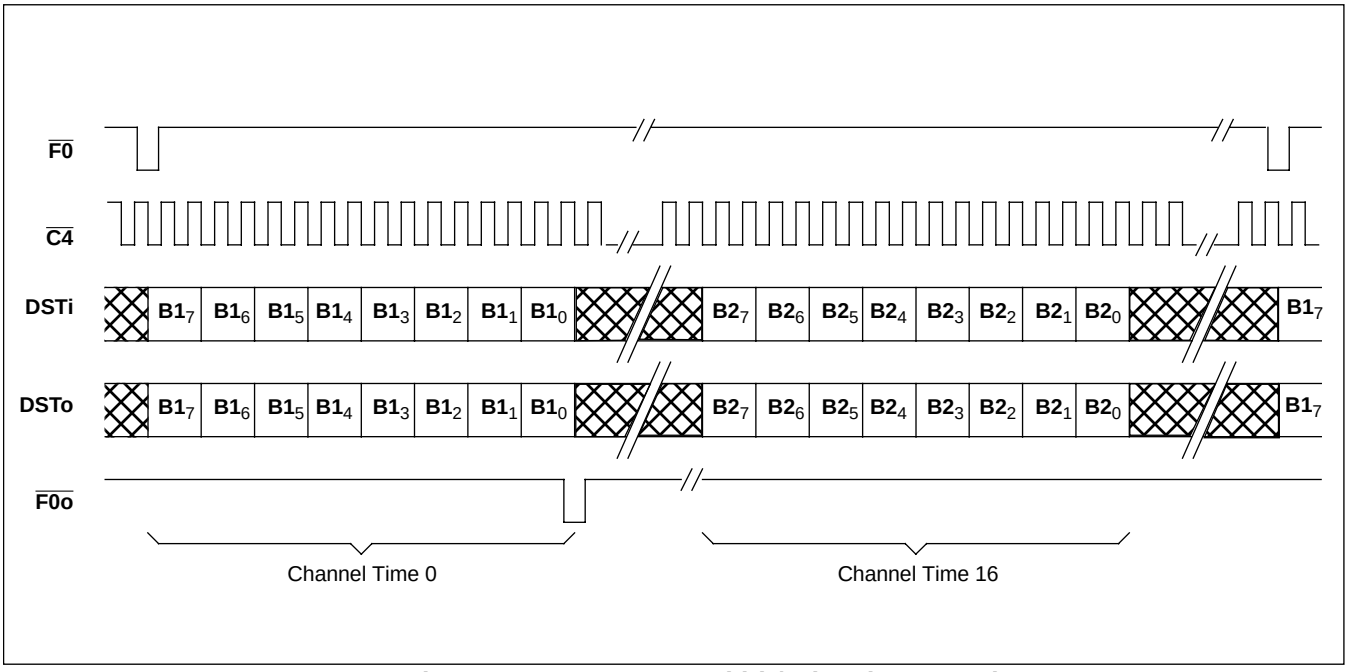


Figure 4 - DV Port - 160 kbit/s (Modes 2, 3, 6)

Functional Description

The MT9171/72 is a device which may be used in practically any application that requires high speed data transmission over two wires, including smart telephone sets, workstations, data terminals and computers. The device supports the 2B+D channel format (two 64 kbit/s B-channels and one 16 kbit/s D-channel) over two wires as recommended by the CCITT. The line data is converted to and from the ST-BUS format on the system side of the network to allow for easy interfacing with other components such as the S-interface device in an NT1 arrangement, or to digital PABX components.

Smart telephone sets with data and voice capability can be easily implemented using the MT9171/72 as a line interface. The device's high bandwidth and long loop length capability allows its use in a wide variety of sets. This can be extended to provide full data and voice capability to the private subscriber by the installation of equipment in both the home and central office or remote concentration equipment. Within the subscriber equipment the MT9171/72 would terminate the line and encode/ decode the data and voice for transmission while additional electronics could provide interfaces for a standard telephone set and any number of data ports supporting standard data rates for such things as computer communications and telemetry for remote meter reading. Digital workstations with a high degree of networking capability can be designed using the DNIC for the line interface, offering up to 160 kbit/s data transmission over existing telephone lines. The MT9171/72 could also be valuable within existing computer networks for connecting a large number of terminals to a computer or for intercomputer links. With the DNIC, this can be accomplished at up to 160 kbit/s at a very low cost per line for terminal to computer links and in many cases this bandwidth would be sufficient for computer to computer links.

Figure 1 shows the block diagram of the MT9171/72. The DNIC provides a bidirectional interface between the DV (data/voice) port and a full duplex line operating at 80 or 160 kbit/s over a single pair of twisted wires. The DNIC has three serial ports. The DV port (DSTi/Di, DSTo/Do), the CD (control/data) port (CDSTi/CDi, CDSTo/CDo) and a line port (L_{IN}, L_{OUT}). The data on the line is made up of information from the DV and CD ports. The DNIC must combine information received from both the DV and CD ports and put it onto the line. At the same time, the data received from the line must be split into the various channels and directed to the proper ports. The usable data rates are 72 and 144 kbit/s as required for the basic rate interface in ISDN. Full duplex transmission is made possible through on board adaptive echo cancellation.

The DNIC has various modes of operation which are selected through the mode select pins MS0-2. The two major modes of operation are the MODEM (MOD) and DIGITAL NETWORK (DN) modes. MOD mode is a transparent 80 or 160 kbit/s modem. In DN mode the line carries the B and D channels formatted for the ISDN at either 80 or 160 kbit/s. In the DN mode the DV and CD ports are standard ST-BUS and in MOD mode they are transparent serial data streams at 80 or 160 kbit/s. Other modes include: MASTER (MAS) or SLAVE (SLV) mode, where the timebase and frame synchronization are provided externally or are extracted from the line and DUAL or SINGLE (SINGL) port modes, where both the DV and CD ports are active or where the CD port is inactive and all information is passed through the DV port. For a detailed description of the modes see "Operating Modes" section.

In DIGITAL NETWORK (DN) mode there are three channels transferred by the DV and CD ports. They are the B, C and D channels. The B1 and B2 channels each have a bandwidth of 64 kbit/s and are used for carrying PCM encoded voice or data. These channels are always transmitted and received through the DV port (Figures 3, 4, 5, 6). The C-channel, having a bandwidth of 64 kbit/s, provides a means for the system to control the DNIC and for the DNIC to pass status information back to the system. The C-channel has a Housekeeping (HK) bit which is the only bit of the C-channel transmitted and received on the line. The 2B+D channel bits and the HK bit are double-buffered. The D-channel can be transmitted or received on the line with either an 8, 16 or 64 kbit/s bandwidth depending on the DNIC's mode of operation. Both the HK bit and the D-channel can be used for end-to-end signalling or low speed data transfer. In DUAL port mode the C and D channels are accessed via the CD port (Figure 7) while in SINGL port mode they are transferred through the DV port (Figures 5, 6) along with the B1 and B2 channels.

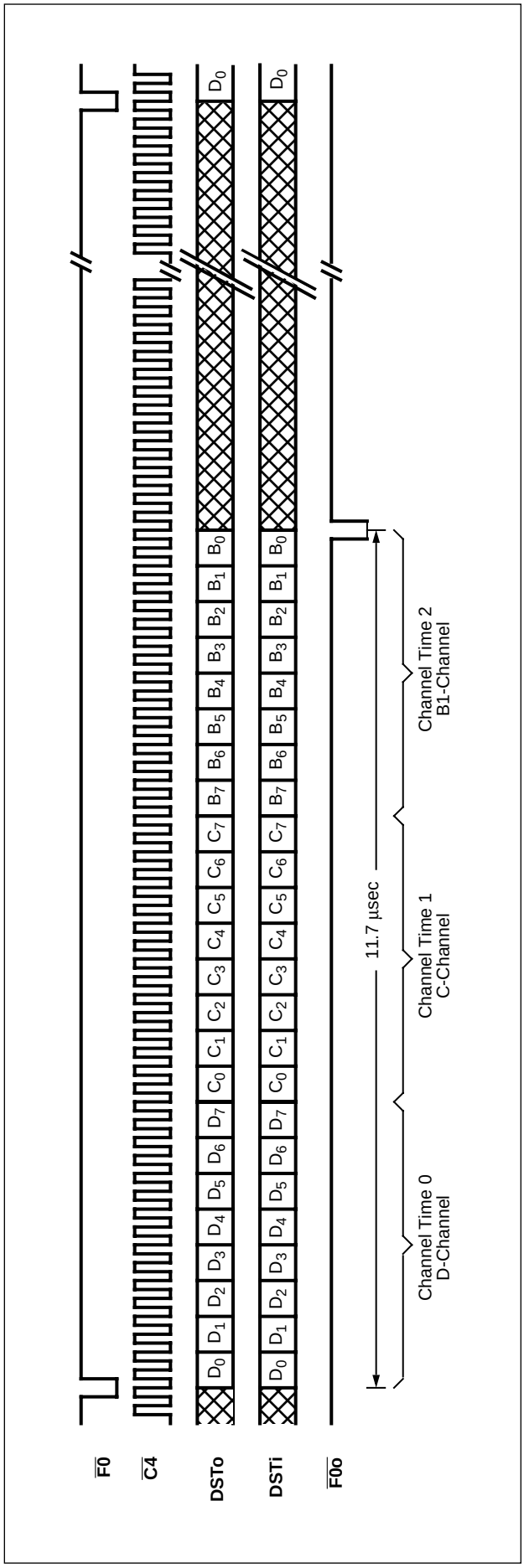


Figure 5 - DV Port - 80 kbit/s (Modes 0,4)

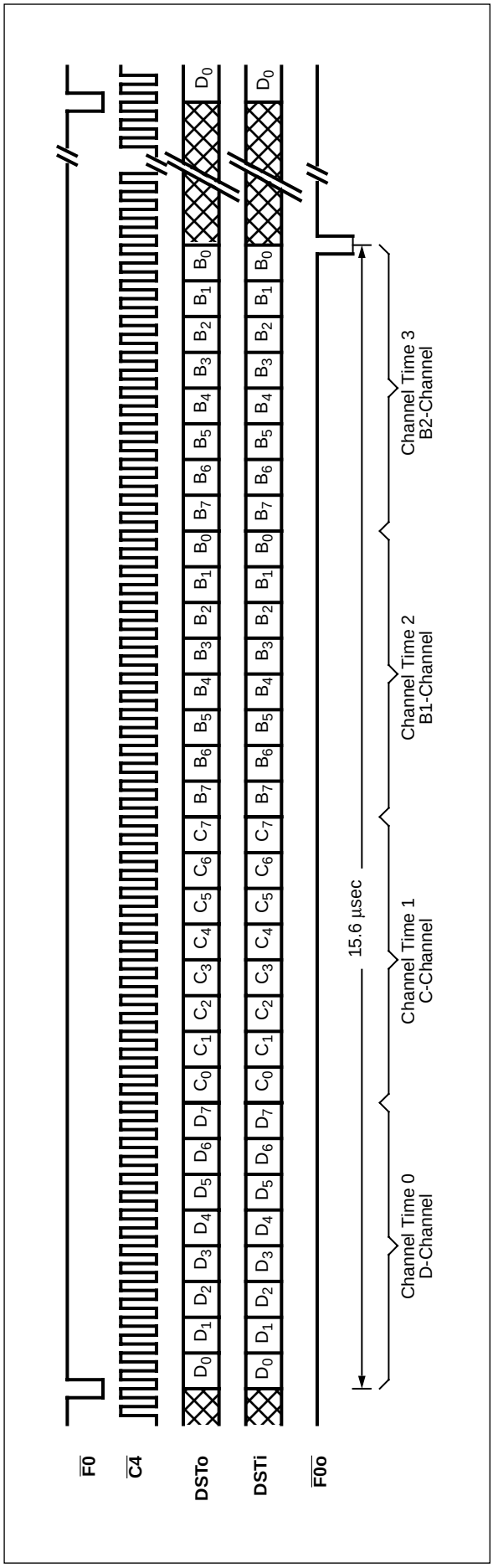


Figure 6 - DV Port - 160 kbit/s (Modes 0,4)

In DIGITAL NETWORK (DN) mode, upon entering the DNIC from the DV and CD ports, the B-channel data, D-channel D0 (and D1 for 160 kbit/s), the HK bit of the C-channel (160kbit/s only) and a SYNC bit are combined in a serial format to be sent out on the line by the Transmit Interface (Figures 11, 12). The SYNC bit produces an alternating 1-0 pattern each frame in order for the remote end to extract the frame alignment from the line. It is possible for the remote end to lock on to a data bit pattern which simulates this alternating 1-0 pattern that is not the true SYNC. To decrease the probability of this happening the DNIC may be programmed to put the data through a prescrambler that scrambles the data according to a predetermined polynomial with respect to the SYNC bit. This greatly decreases the probability that the SYNC pattern can be reproduced by any data on the line. In order for the echo canceller to function correctly, a dedicated scrambler is used with a scrambling algorithm which is different for the SLV and MAS modes. These algorithms are calculated in such a way as to provide orthogonality between the near and far end data streams such that the correlation between the two signals is very low.

For any two DNICs on a link, one must be in SLV mode with the other in MAS mode. The scrambled data is differentially encoded which serves to make the data on the line polarity-independent. It is then biphase encoded as shown in Figure 10. See “Line Interface” section for more details on the encoding. Before leaving the DNIC the differentially encoded biphase data is passed through a pulse-shaping bandpass transmit filter that filters out the high and low frequency components and conditions the signal for transmission on the line.

The composite transmit and receive signal is received at L_{IN}. On entering the DNIC this signal passes through a Precanceller which is a summing amplifier and lowpass filter that partially cancels the near-end signal and provides first order antialiasing for the received signal. Internal, partial cancellation

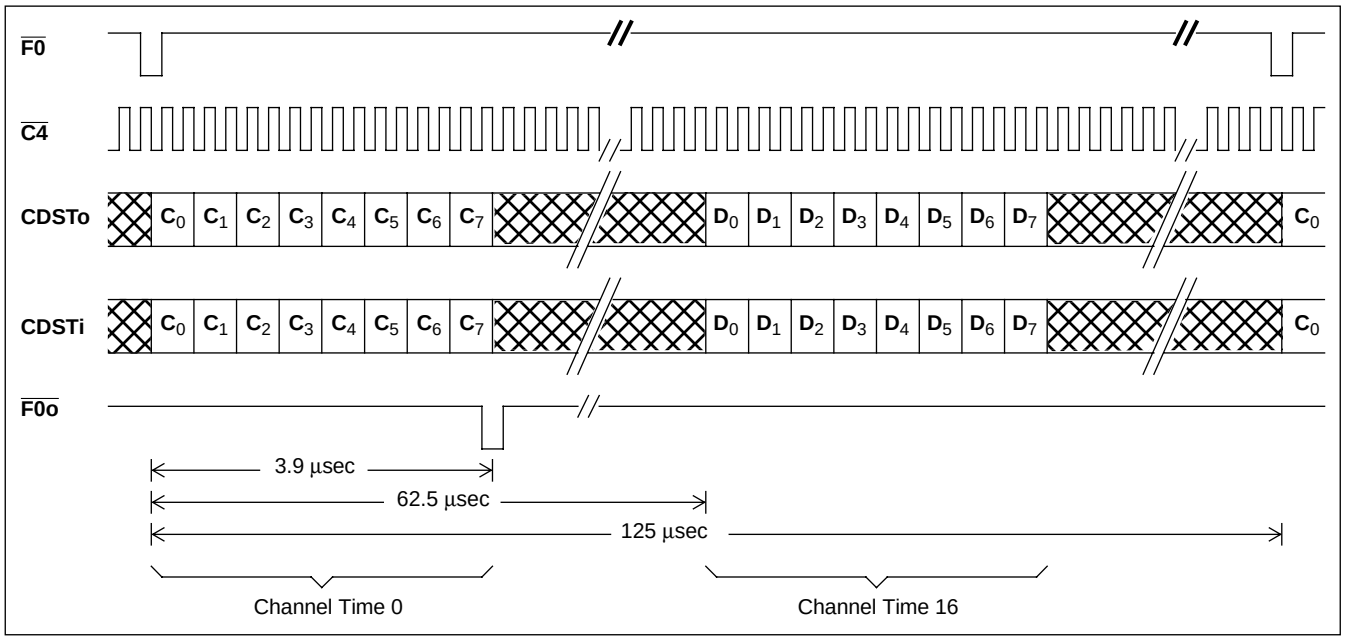


Figure 7 - CD Port (Modes 2,6)

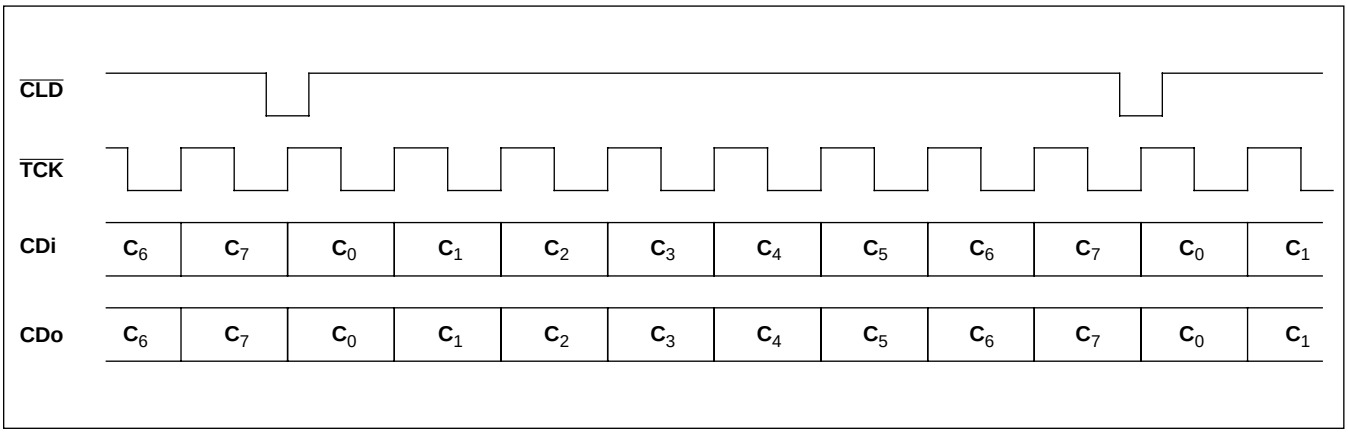


Figure 8 - CD Port (Modes 1,5)

of the near end signal may be disabled by holding the Precan pin high. This mode simplifies the design of external line transceivers used for loop extension applications. The Precan pin features an internal pull-down which allows this pin to be left unconnected in applications where this function is not required. The resultant signal passes through a receive filter to bandlimit and equalize it. At this point, the echo estimate from the echo canceller is subtracted from the precancelled received signal. This difference signal is then input to the echo canceller as an error signal and also squared up by a comparator and passed to the biphase receiver. Within the echo canceller, the sign of this error signal is determined. Depending on the sign, the echo estimate is either incremented or decremented and this new estimate is stored back in RAM.

The timebase in both SLV and MAS modes (generated internally in SLV mode and externally in MAS mode) is phase-locked to the received data stream. This phase-locked clock operates the Biphase Decoder, Descrambler and Deprescrambler in MAS mode and the entire chip in SLV mode. The Biphase Decoder decodes the received encoded bit stream resulting in the original NRZ data which is passed onto the Descrambler and Deprescrambler where the data is restored to its original content by performing the reverse polynomials. The SYNC bits are extracted and the Receive Interface separates the channels and outputs them to the proper ports in the proper channel times. The destination of the various channels is the same as that received on the input DV and CD ports.

The Transmit/Receive Timing and Control block generates all the clocks for the transmit and receive functions and controls the entire chip according to the control register. In order that more than one DNIC may be connected to the same DV and CD ports an $\overline{F0o}$ signal is generated which signals the next device in a daisy chain that its channel times are now active. In this arrangement only the first DNIC in the chain receives the system $\overline{F0}$ with the following devices receiving its predecessor's $\overline{F0o}$.

In MOD mode, all the ports have a different format. The line port again operates at 80 or 160 kbit/s, however, there is no synchronization overhead, only transparent data. The DV and CD ports carry serial data at 80 or 160 kbit/s with the DV port transferring all the data for the line and the CD port carrying the C-channel only. In this mode the transfer of data at both ports is synchronized to the $\overline{TCK}$ and $\overline{RCK}$ clocks for transmit and receive data, respectively.

The $\overline{CLD}$ signal goes low to indicate the start of the C-channel data on the CD port. It is used to load and latch the input and output C-channel but has no relationship to the data on the DV port.

Operating Modes (MS0-2)

The logic levels present on the mode select pins MS0, MS1 and MS2 program the DNIC for different operating modes and configure the DV and CD ports accordingly. Table 1 shows the modes corresponding to the state of MS0-2. These pins select the DNIC to operate as a MASTER or SLAVE, in DUAL or SINGLE port operation, in MODEM or DIGITAL NETWORK mode and the order of the C and D channels on the CD port. Table 2 provides a description of each mode and Table 3 gives a pin configuration according to the mode selected for all pins that have variable functions. These functions vary depending on whether it is in MAS or SLV, and whether DN or MOD mode is used.

The overall mode of operation of the DNIC can be programmed to be either a baseband modem (MOD mode) or a digital network transceiver (DN mode). As a baseband modem, transmit/receive data is passed transparently through the device at 80 or 160 kbit/s by the DV port. The CD port transfers

Mode Select Pins			Mode	Operating Mode								
MS2	MS1	MS0		SLV	MAS	DUAL	SINGL	MOD	DN	D-C	C-D	ODE
0	0	0	0		E		E		E	E		E
0	0	1	1		E	E		E		X	X	E
0	1	0	2		E	E			E		E	E
0	1	1	3		E	E			E	E		E
1	0	0	4	E			E		E	E		E
1	0	1	5	E		E		E		X	X	E
1	1	0	6	E		E			E		E	E
1	1	1	7		E	E			E	E		

Table 1. Mode Select Pins

E=Enabled X=Not Applicable
Blanks are disabled

the C-channel and D-Channel also at 80 or 160 kbit/s.

In DN mode, both the DV and CD ports operate as ST-BUS streams at 2.048 Mbit/s. The DV port transfers data over pins DSTi and DSTo while on the CD port, the CDSTi and CDSTo pins are used. The SINGL port option only exists in DN mode.

In MOD mode, DUAL port operation must be used and the D, B1 and B2 channel designations no longer exist. The selection of SLV or MAS will determine which of the DNICs is using the externally supplied clock and which is phase locking to the data on the line. Due to jitter and end to end delay, one end must be the master to generate all the timing for the link and the other must extract the timing from the receive data and synchronize itself to this timing in order to recover the synchronous data. DUAL port mode allows the user to use two separate serial busses: the DV port for PCM/data (B channels) and the CD port for control and signalling information (C and D channels). In the SINGL port mode, all four channels are concatenated into one serial stream and input to the DNIC via the DV port. The order of the C and D channels may be changed only in DN/DUAL mode. The DNIC may be configured to transfer the D-channel in channel 0 and the C-channel in

Mode	Function
SLV	**SLAVE** - The chip timebase is extracted from the received line data and the external 10.24 MHz crystal is phase locked to it to provide clocks for the entire device and are output for the external system to synchronize to.
MAS	**MASTER -** The timebase is derived from the externally supplied data clocks and 10.24 MHz clock which must be frequency locked. The transmit data is synchronized to the system timing with the receive data recovered by a clock extracted from the receive data and resynchronized to the system timing.
DUAL	**DUAL PORT -** Both the CD and DV ports are active with the CD port transferring the C&D channels and the DV port transferring the B1& B2 channels.
SINGL	**SINGLE PORT -** The B1& B2, C and D channels are all transferred through the DV port. The CD port is disabled and CDSTi should be pulled high.
MOD	**MODEM -** Baseband operation at 80 or 160 kbits/s. The line data is received and transmitted through the DV port at the baud rate selected. The C-channel is transferred through the CD port also at the baud rate and is synchronized to the $\overline{CLD}$ output.
DN	**DIGITAL NETWORK -** Intended for use in the digital network with the DV and CD ports operating at 2.048 Mbits/s and the line at 80 or 160 kbits/s configured according to the applicable ISDN recommendation.
D-C	**D BEFORE C-CHANNEL -** The D-channel is transferred before the C-channel following $\overline{F0}$.
C-D	**C BEFORE D-CHANNEL -** The C-channel is transferred before the D-channel following $\overline{F0}$.
ODE	**OUTPUT DATA ENABLE -** When mode 7 is selected, the DV and CD ports are put in high impedance state. This is intended for power-up reset to avoid bus contention and possible damage to the device during the initial random state in a daisy chain configuration of DNICs. In all the other modes of operation DV and CD ports are enabled during the appropriate channel times.

Table 2. Mode Definitions

Mode #	$\overline{F0}/\overline{CLD}$		$\overline{F0o}/\overline{RCK}$		$\overline{C4}/\overline{TCK}$	
	Name	Input/Output	Name	Input/Output	Name	Input/Output
0	$\overline{F0}$	Input	$\overline{F0o}$	Output	$\overline{C4}$	Input
1	$\overline{CLD}$	Output	$\overline{RCK}$	Output	$\overline{TCK}$	Output
2	$\overline{F0}$	Input	$\overline{F0o}$	Output	$\overline{C4}$	Input
3	$\overline{F0}$	Input	$\overline{F0o}$	Output	$\overline{C4}$	Input
4	$\overline{F0}$	Output	$\overline{F0o}$	Output	$\overline{C4}$	Output
5	$\overline{CLD}$	Output	$\overline{RCK}$	Output	$\overline{TCK}$	Output
6	$\overline{F0}$	Output	$\overline{F0o}$	Output	$\overline{C4}$	Output
7	$\overline{F0}$	Input	$\overline{F0o}$	Output	$\overline{C4}$	Input

Table 3. Pin Configurations

channel 16 or vice versa. One other feature exists; ODE, where both the DV and CD ports are tristated in order that no devices are damaged due to excessive loading while all DNICs are in a random state on power up in a daisy chain arrangement.

DV Port (DSTi/Di, DSTo/Do)

The DV port transfers data or PCM encoded voice to and from the line according to the particular mode selected by the mode select pins. The modes affecting the configuration of the DV port are MOD or DN and DUAL or SINGL. In DN mode the DV port operates as an ST-BUS at 2.048 Mbit/s with 32, 8 bit channels per frame as shown in Figure 9. In this mode the DV port channel configuration depends upon whether DUAL or SINGL port is selected. When DUAL port mode is used, the C and D channels are passed through the CD port and the B1 and B2 channels are passed through the DV port. At 80 kbit/s only one channel of the available 32 at the DV port is utilized, this being channel 0 which carries the B1-channel. This is shown in Figure 3. At 160 kbit/s, two channels are used, these being 0 and 16 carrying the B1 and B2 channels, respectively. This is shown in Figure 4. When SINGL port mode is used, channels B1, B2, C and D are all passed via the DV port and the CD port is disabled. See CD port description for an explanation of the C and D channels.

The D-channel is always passed during channel time 0 followed by the C and B1 channels in channel times 1 and 2, respectively for 80 kbit/s. See Figure 5. For 160 kbit/s the B2 channel is added and occupies channel time 3 of the DV port. See Figure 6. For all of the various configurations the bit orders are shown by the respective diagram. In MOD mode the DV and CD ports no longer operate at 2.048 Mbits/s but are continuous serial bit streams operating at the bit rate selected of 80 or 160 kbit/s.

While in the MOD mode only DUAL port operation can be used.

In order for more than one DNIC to be connected to any one DV and CD port, making more efficient use of the busses, the DSTo and CDSTo outputs are put into high impedance during the inactive channel times of the DNIC. This allows additional DNICs to be cascaded onto the same DV and CD ports. When used in this way a signal called $\overline{F0o}$ is used as an indication to the next DNIC in a daisy chain that its channel time is now active. Only the first DNIC in the chain receives the system frame pulse and all others receive the $\overline{F0o}$ from its predecessor in the chain. This allows up to 16 DNICs to be cascaded.

CD Port (CDSTi/CDi, CDSTo/CDo)

The CD port is a serial bidirectional port used only in DUAL port mode. It is a means by which the DNIC receives its control information for things such as setting the bit rate, enabling internal loopback tests, sending status information back to the system and transferring low speed signalling data to and from the line.

The CD port is composed of the C and D-Channels. The C-channel is used for transferring control and status information between the DNIC and the system. The D-channel is used for sending and receiving signalling information and lower speed data between the line and the system. In DN/DUAL mode the DNIC receives a C-channel on CDSTi while transmitting a C-channel on CDSTo. Fifteen channel times later (halfway through the frame) a D-channel is received on CDSTi while a D-channel is transmitted on CDSTo. This is shown in Figure 7. The order of the C and D bytes in DUAL port mode can be reversed by the mode select pins. See Table 1 for a listing of the byte orientations.

The D-channel exists only in DN mode and may be used for transferring low speed data or signalling information over the line at 8, 16 or 64 kbit/s (by using the DINB feature). The information passes

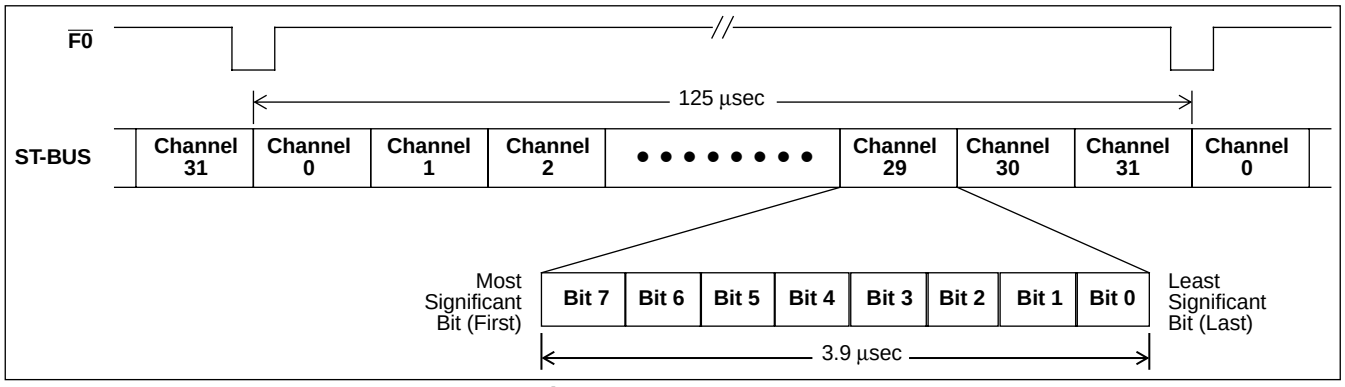


Figure 9 - ST-BUS Format

transparently through the DNIC and is transmitted to or received from the line at the bit rate selected in the Control Register.

If the bit rate is 80 kbit/s, only D0 is transmitted and received. At 160 kbit/s, D0 and D1 are transmitted and received. When the DINB bit is set in the Control Register the entire D-channel is transmitted and received in the B1-channel timeslot.

The C-channel is used for transferring control and status information between the DNIC and the system. The Control and Diagnostics Registers are accessed through the C-channel. They contain information to control the DNIC and carry out the diagnostics as well as the HK bit to be transmitted on the line as described in Tables 4 and 5. Bits 0 and 1 of the C-channel select between the Control and Diagnostics Register. If these bits are 0, 0 then the C-channel information is written to the Control Register (Table 4). If they are 0, 1 the C-Channel is written to the Diagnostics Register (Table 5).

The Diagnostics Register Reset bit (bit 2) of the Control Register determines the reset state of the Diagnostics Register. If, on writing to the Control Register, this bit is set to logic “0”, the Diagnostics Register will be reset coincident with the frame pulse. When this bit is logic “1”, the Diagnostics Register will not be reset. In order to use the diagnostic features, the Diagnostics Register must be continuously written to. The output C-channel sends status information from the Status Register to the system along with the received HK bit as shown in Table 6.

In MOD mode, the CD port is no longer an ST-BUS but is a serial bit stream operating at the bit rate selected. It continues to transfer the C-channel but the D-channel and the HK bit no longer exist. DUAL

bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
Reg Sel-1	Reg Sel-2	DRR	BRS	DINB	PSEN	ATTACK	TxHK
				Default Mode Selection (Refer to Table 4a)			

Bit	Name	Description
0	Reg Sel-1	Register Select-1. Must be set to ’0’ to select the Control Register.
1	Reg Sel-2	Register Select-2. Must be set to ’0’ to select the Control Register.
2	DRR	Diagnostics Register Reset. Writing a "0" to this bit will cause a diagnostics register reset to occur coincident with the next frame pulse as in the MT8972A. When this bit is a logic "1", the Diagnostics Register will not be reset.
3	BRS	Bit Rate Select. When set to ’0’ selects 80 kbit/s. When set to ’1’, selects 160 kbit/s.
4	DINB②	D-Channel in B Timeslot. When ’0’, the D-channel bits (D0 or D0 and D1) corresponding to the selected bit rate (80 or 160 kbit/s) are transmitted during the normal D-channel bit times. When set to ’1’, the entire D-channel (D0-D7) is transmitted during the B1-channel timeslot on the line providing a 64 kbit/s D-channel link.
5	PSEN②	Prescrambler/Deprescrambler Enable. When set to ’1’, the data prescrambler and deprescrambler are enabled. When set to ’0’, the data prescrambler and deprescrambler are disabled.
6	ATTACK②	Convergence Speedup. When set to ’1’, the echo canceller will converge to the reflection coefficient much faster. Used on power-up for fast convergence.① When ’0’, the echo canceller will require the normal amount of time to converge to a reflection coefficient.
7	TxHK②	Transmit Housekeeping. When set to ’0’, logic zero is transmitted over the line as Housekeeping Bit. When set to ’1’, logic one is transmitted over the line as Housekeeping Bit.

Table 4. Control Register

Notes:
① Suggested use of ATTACK:
-At 160 kbit/s full convergence requires 850 ms with ATTACK held high for the first 240 frames or 30 ms.
-At 80 kbit/s full convergence requires 1.75 s with ATTACK held high for the first 480 frames or 60 ms.
② When bits 4-7 of the Control Register are all set to one, the DNIC operates in one of the default modes as defined in Table 4a, depending upon the status of bit-3.

C-Channel (Bit 0-7)	Internal Control Register	Internal Diagnostic Register	Description
XXX01111	00000000	01000000	Default Mode-1③: Bit rate is 80 kbit/s. ATTACK, PSEN, DINB, DRR and all diagnostics are disabled. TxHK=0.
XXX11111	00010000	01000000	Default Mode-2④ Bit rate is 160 kbit/s. ATTACK, PSEN, DINB, DRR and all diagnostics are disabled. TxHK=0.

Table 4a. Default Mode Selection

Notes:
③ Default Mode 1 can also be selected by tying CDSTi/CDi pin low when DNIC is operating in dual mode.
④ Default Mode 2 can also be selected by tying CDSTi/CDi pin high when DNIC is operating in dual mode.

bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
Reg Sel-1	Reg Sel-2	Loopback		FUN	PSWAP	DLO	Not Used
				Default Mode Selection (Refer to Table 4a)			

Bit	Name	Description
0	Reg Sel-1	Register Select-1. Must be set to '0' to select the Diagnostic Register.
1	Reg Sel-2	Register Select-2. Must be set to '1' to select the Diagnostic Register.
2,3	Loopback	Bit 2 Bit 3 0 0 All loopback testing functions disabled. Normal operation. 0 1 DSTi internally looped back into DSTo for system diagnostics. 1 0 L_{OUT} is internally looped back into L_{IN} for system diagnostics.② 1 1 DSTo is internally looped back into DSTi for end-to-end testing.③
4	FUN①	Force Unsync. When set to '1', the DNIC is forced out-of-sync to test the SYNC recovery circuitry. When set to '0', the operation continues in synchronization.
5	PSWAP①	Polynomial Swap. When set to '1', the scrambling and descrambling polynomials are interchanged (use for MAS mode only). When set to '0', the polynomials retain their normal designations.
6	DLO①	Disable Line Out. When set to '1', the signal on L_{OUT} is set set to V_{Bias}. When set to '0', L_{OUT} pin functions normally.
7	Not Used	Must be set to '0' for normal operation.

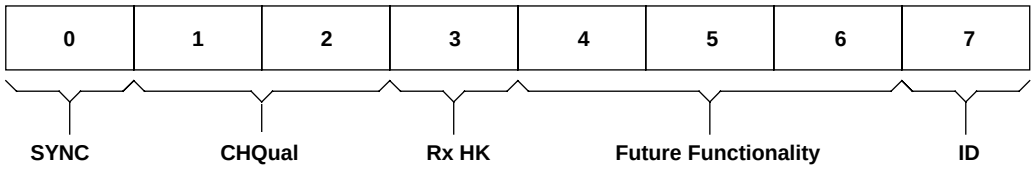
Table 5. Diagnostic Register

Notes:
① When bits 4-7 of the Diagnostic Register are all set to one, the DNIC operates in one of the default modes as defined in Table 4a, depending upon the status of bit-3.
② Do not use L_{OUT} to L_{IN} loopback in DN/SLV mode.
③ Do not use DSTo to DSTi loopback in MOD/MAS mode.

port operation must be used in MOD mode. The C-channel is clocked in and out of the CD port by $\overline{TCK}$ and $\overline{CLD}$ with $\overline{TCK}$ defining the bits and $\overline{CLD}$ the channel boundaries of the data stream as shown in Figure 8.

Line Port (L_{IN}, L_{OUT})

The line interface is made up of L_{OUT} and L_{IN} with L_{OUT} driving the transmit signal onto the line and L_{IN} receiving the composite transmit and receive signal from the line. The line code used in the DNIC is Biphase and is shown in Figure 10. The scrambled NRZ data is differentially encoded meaning the previous differential encoded output is XOR'd with the current data bit which produces the current output. This is then biphase encoded where transitions occur midway through the bit cell with a



Status Register	Name	Function
0	**SYNC**	**Synchronization** - When set this bit indicates that synchronization to the received line data sync pattern has been acquired. For DN mode only.
1-2	**CHQual**	**Channel Quality -** These bits provide an estimate of the receiver's margin against noise. The farther this 2 bit value is from 0 the better the SNR.
3	**Rx HK**	**Housekeeping -** This bit is the received housekeeping (HK) bit from the far end.
4-6	**Future**	**Future Functionality.** These bits return Logic 1 when read.
7	**ID**	This bit provides a hardware identifier for the DNIC revision. The MT9171/72 will return a logic "0" for this bit. (Logic "1" returned for MT8972A.)

Table 6. Status Register

negative going transition indicating a logic "0" and a positive going transition indicating a logic "1".

There are some major reasons for using a biphase line code. The power density is concentrated in a spectral region that minimizes dispersion and differential attenuation. This can shorten the line response and reduce the intersymbol interference which are critical for adaptive echo cancellation. There are regular zero crossings halfway through every bit cell or baud which allows simple clock extraction at the receiving end. There is no D.C. content in the code so that phantom power feed may be applied to the line and simple transformer coupling may be used with no effect on the data. It is bipolar, making data reception simple and providing a high signal to noise ratio. The signal is then passed through a bandpass filter which conditions the signal for the line by limiting the spectral content from $0.2f_{Baud}$ to $1.6f_{Baud}$ and on to a line driver where it is made available to be put onto the line biased at V_{Bias}. The resulting transmit signal will have a distributed spectrum with a peak at $3/4f_{Baud}$. The transmit signal (L_{OUT}) may be disabled by holding the L_{OUT} DIS pin high or by writing DLO (bit 6) of the Diagnostics Register to logic "1". When disabled, L_{OUT} is forced to the V_{Bias} level. L_{OUT} DIS has an internal pull-down to allow this pin to be left not connected in applications where this function is not required. The receive signal is the above transmit signal superimposed on the signal from the remote end and any reflections or delayed symbols of the near end signal.

The frame format of the transmit data on the line is shown in Figures 11 and 12 for the DN mode at 80 and 160 kbit/s. At 80 kbit/s a SYNC bit for frame recovery, one bit of the D-channel and the B1-channel are transmitted. At 160 kbit/s a SYNC bit, the HK bit, two bits of the D-channel and both B1 and B2 channels are transmitted.

If the DINB bit of the Control Register is set, the entire D-channel is transmitted during the B1-channel timeslot. In MOD mode the SYNC, HK and D-channel bits are not transmitted or received but rather a continuous data stream at 80 or 160 kbit/s is present. No frame recovery information is present on the line in MOD mode.

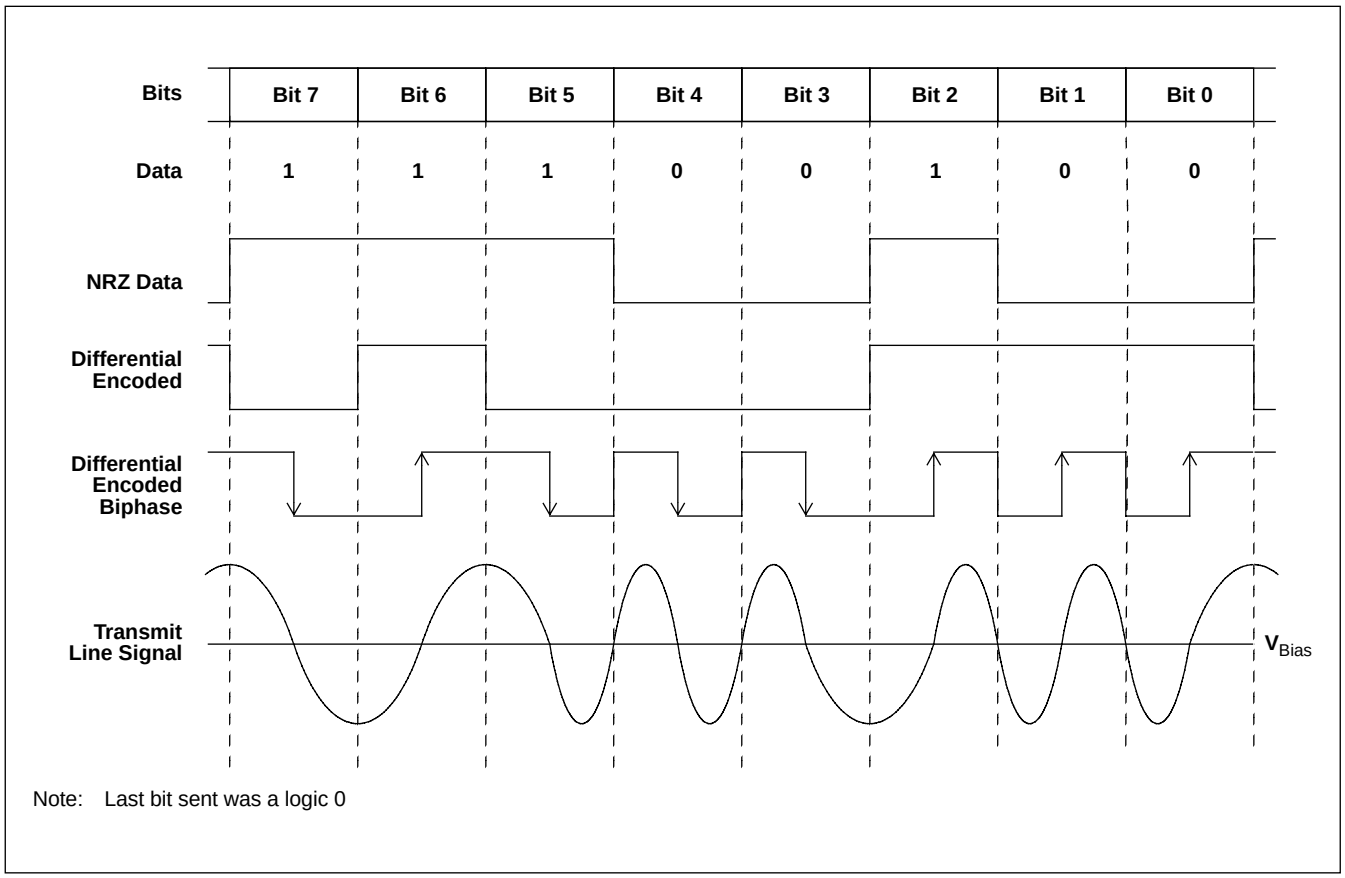


Figure 10 - Data & Line Encoding

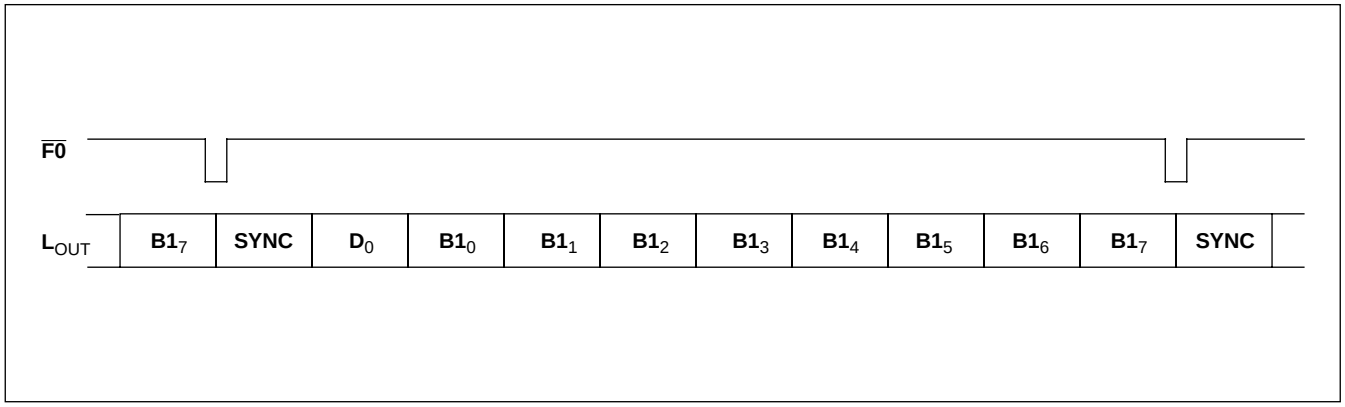


Figure 11 - Frame Format - 80 kbit/s (Modes 0, 2, 3, 4, 6)

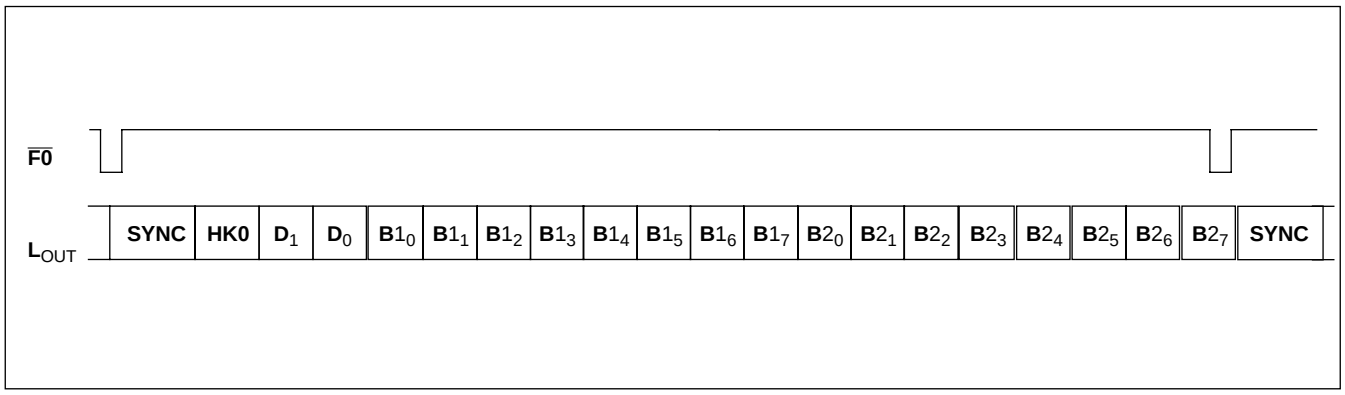


Figure 12 - Frame Format - 160 kbit/s (Modes 0, 2, 3, 4, 6)

Applications

Typical connection diagrams are shown in Figures 13 and 14 for the DN mode as a MASTER and SLAVE, respectively. L_{OUT} is connected to the coupling transformer through a resistor R2 and capacitors C2 and C2' to match the line characteristic impedance. Suggested values of R2, C2 and C2' for 80 and 160 kbit/s operation are provided in Figures 13 and 14. Overvoltage protection is provided by R1, D1 and D2. C1 is present to properly bias the received line signal for the L_{IN} input. A 2:1 coupling transformer is used to couple to the line with a secondary center tap for optional phantom power feed. Varistors have been shown for surge protection against such things as lightning strikes.

If the scramblers power up with all zeros in them, they are not capable of randomizing all-zeros data sequence. This increases the correlation between the transmit and receive data which may cause loss of convergence in the echo canceller and high bit error rates.

In DN mode the insertion of the SYNC pattern will provide enough pseudo-random activity to maintain convergence. In MOD mode the SYNC pattern is not inserted. For this reason, at least on "1" must be fed into the DNIC on power up to ensure that the scramblers will randomize any subsequent all-zeros sequence.

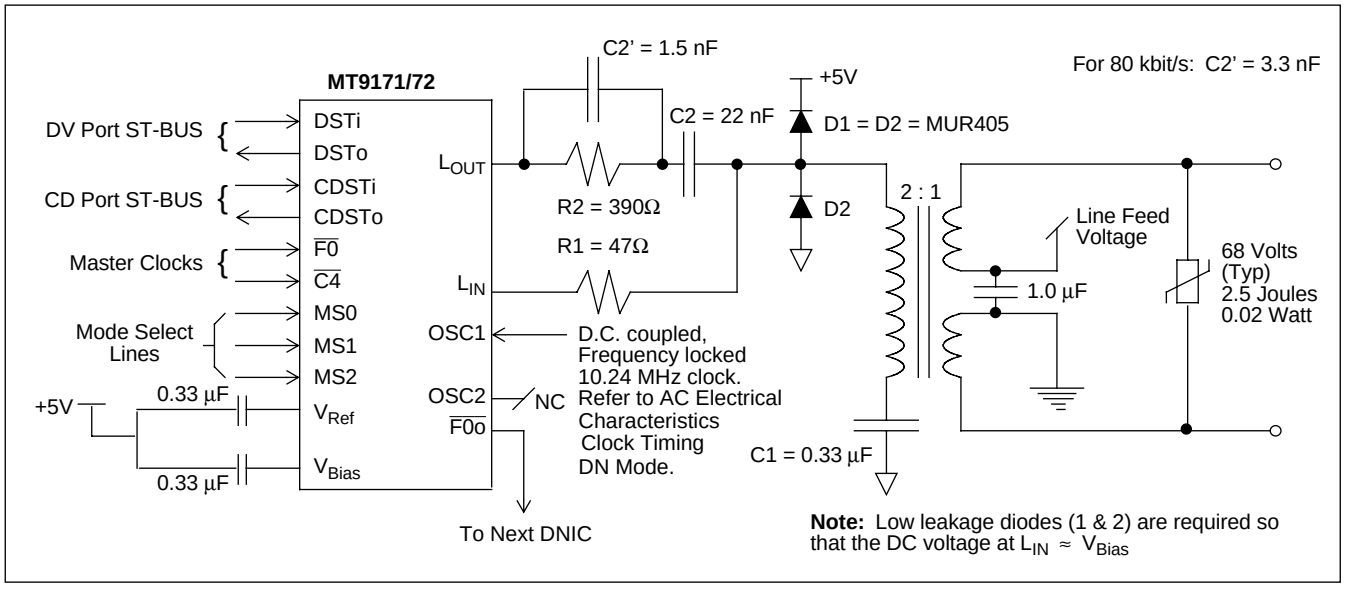


Figure 13 - Typical Connection Diagram - MAS/DN Mode, 160 kbit/s

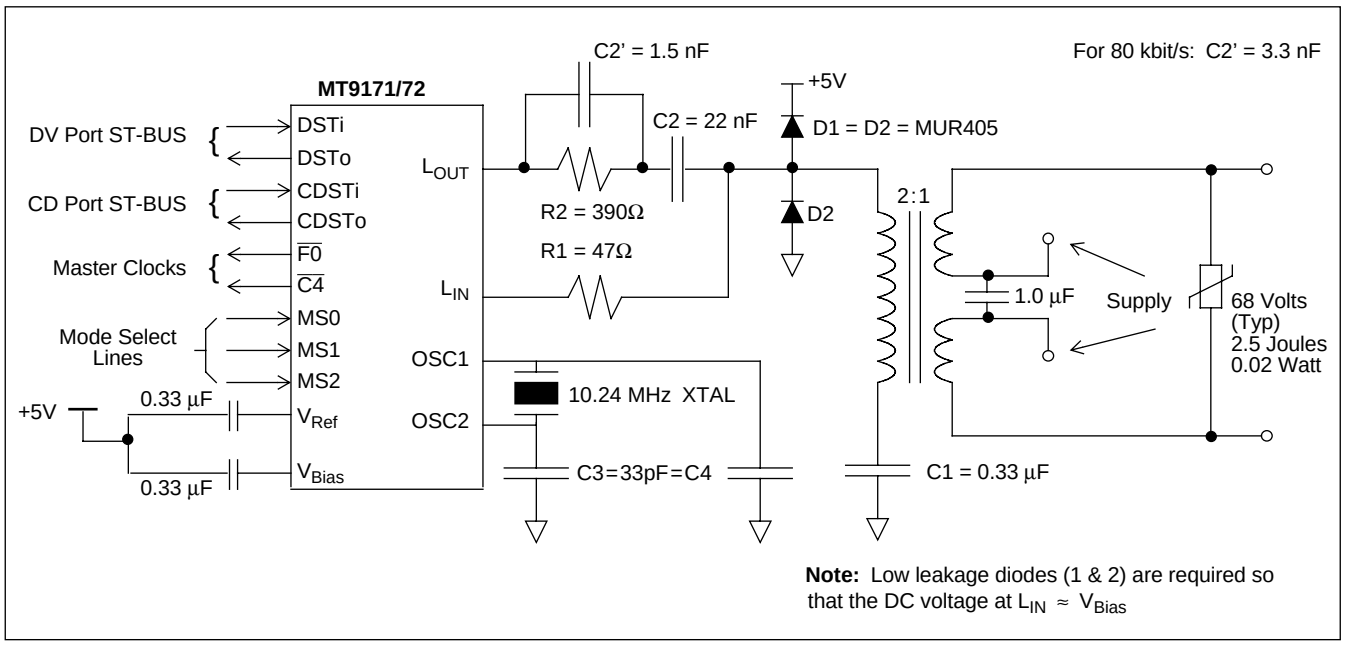


Figure 14 - Typical Connection Diagram - SLV/DN Mode, 160 kbit/s

Absolute Maximum Ratings** - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.3	7	V
2	Voltage on any pin (other than supply)	V_{Max}	-0.3	V_{DD}+0.3	V
3	Current on any pin (other than supply)	I_{Max}		40	mA
4	Storage Temperature	T_{ST}	-65	+150	°C
5	Package Power Dissipation (Derate 16mW/°C above 75°C)	P_{Diss}		750	mW

** Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Operating Supply Voltage	V_{DD}	4.75	5.00	5.25	V	
2	Operating Temperature	T_{OP}	-40		+85	°C	
3	Input High Voltage (except OSC1)	V_{IH}	2.4		V_{DD}	V	for 400 mV noise margin
4	Input Low Voltage (except OSC1)	V_{IL}	0		0.4	V	for 400 mV noise margin

* Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
† Parameters over recommended temperature & power supply voltage ranges.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	OUTPUTS	Operating Supply Current	I_{DD}		10		mA	
2		Output High Voltage (ex OSC2)	V_{OH}	2.4			V	I_{OH}=10mA
3		Output High Current (except OSC2)	I_{OH}	10			mA	Source current. V_{OH}=2.4V
4		Output High Current - OSC2	I_{OH}	10			µA	Source current V_{OH}=3.5V
5		Output Low Voltage (ex OSC2)	V_{OL}			0.4	V	I_{OL}=5mA
6		Output Low Current (except OSC2)	I_{OL}	5	7.5		mA	Sink current. V_{OL}=0.4V
7		Output Low Current - OSC2	I_{OL}	10			µA	Sink current. V_{OL}=1.5V
8		High Imped. Output Leakage	I_{OZ}			10	µA	V_{IN}=V_{SS} to V_{DD}
9		Output Voltage (V_{Ref})	V_O		V_{Bias}-1.8		V	
10		(V_{Bias})			V_{DD}/2		V	
11	INPUTS	Input High Voltage (ex OSC1)	V_{IH}	2.0			V	
12		Input Low Voltage (ex OSC1)	V_{IL}			0.8	V	
13		Input High Voltage (OSC1)	V_{IHo}	4.0			V	
14		Input Low Voltage (OSC1)	V_{ILo}			1.0	V	
15		Input Leakage Current	I_{IL}			10	µA	V_{IN}=V_{SS} to V_{DD}
16		Input Pulldown Impedance L_{OUT} DIS and Precan	Z_{PD}		50		kΩ	
17		Input Leakage Current for OSC1 Input	I_{IOSC}		20		µA	

* Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
† Parameters over recommended temperature & power supply voltage ranges.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	INPUTS	Input Voltage (L_{IN})	V_{IN}			5.0	V_{pp}	
2		Input Impedance (L_{IN})	Z_{IN}	20			kΩ	f_{Baud}=160 kHz
3		Crystal/Clock Frequency	f_C		10.24		MHz	
4		Crystal/Clock Tolerance	T_C	-100	0	+100	ppm	
5a		Crystal/Clock Duty Cycle ①	DC_C	40	50	60	%	Normal temp. & V_{DD}
5b		Crystal/Clock Duty Cycle ①	DC_C	45	50	55	%	Recommended at max./ min. temp. & V_{DD}
6		Crystal/Clock Loading	C_L		33	50	pF	From OSC1 & OSC2 to V_{SS}.
7	OUTPUTS	Output Capacitance (L_{OUT})	C_o		8		pF	
8		Load Resistance (L_{OUT}) (V_{Bias}, V_{Ref})	R_{Lout}		500 100		Ω kΩ	
9		Load Capacitance (L_{OUT}) (V_{Bias}, V_{Ref})	C_{Lout}	 0.1		20	pF µF	Capacitance to V_{Bias}.
10		Output Voltage (L_{OUT})	V_o	3.2	4.3	4.6	V_{pp}	R_{Lout} = 500Ω, C_{Lout} = 20pF

† Timing is over recommended temperature & power supply voltages.
* Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
① Duty cycle is measured at $V_{DD}/2$ volts.

AC Electrical Characteristics† - Clock Timing - DN Mode (Figures 16 & 17)

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	$\overline{C4}$ Clock Period	t_{C4P}		244		ns	
2	$\overline{C4}$ Clock Width High or Low	t_{C4W}		122		ns	In Master Mode - Note 1
3	Frame Pulse Setup Time	t_{F0S}	50			ns	
4	Frame Pulse Hold Time	t_{F0H}	50			ns	
5	Frame Pulse Width	t_{F0W}		244		ns	
6	10.24 MHz Clock Jitter (wrt $\overline{C4}$)	J_C		±15		ns	Note 2

† Timing is over recommended temperature & power supply voltages.
* Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Notes: 1) When operating as a SLAVE the C4 clock has a 40% duty cycle.
2) When operating in MAS/DN Mode, the $\overline{C4}$ and Oscillator clocks must be externally frequency-locked (i.e., F_C=2.5xf_{C4}). The relative phase between these two clocks (Φ in Fig. 17) is not critical and may vary from 0 ns to t_{C4P} . However, the relative jitter must be less than J_C (see Figure 17).

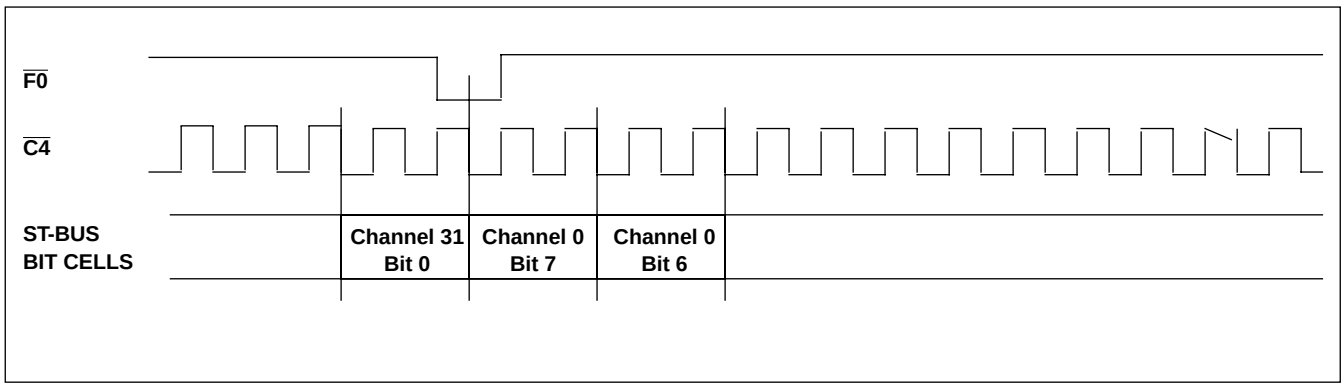


Figure 15 - $\overline{C4}$ Clock & Frame Pulse Alignment for ST-BUS Streams

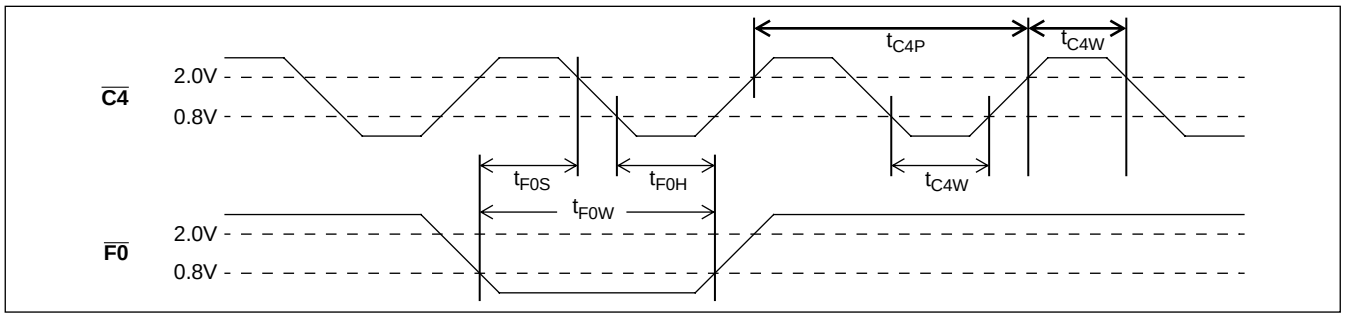


Figure 16 - $\overline{C4}$ Clock & Frame Pulse Alignment for ST-BUS Streams in DN Mode

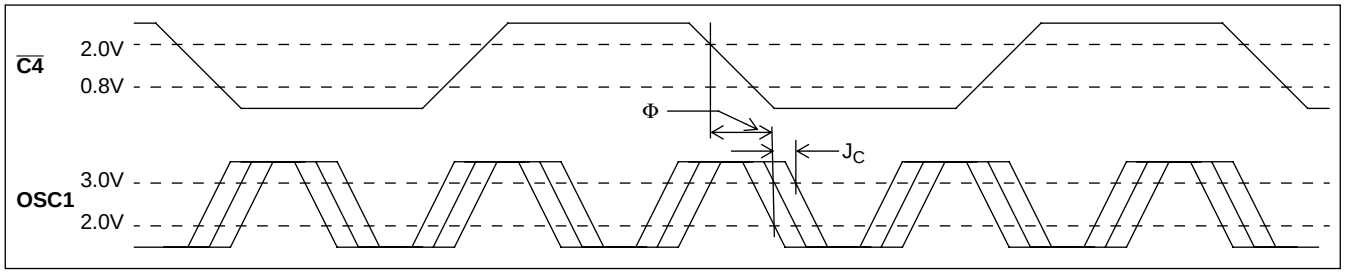
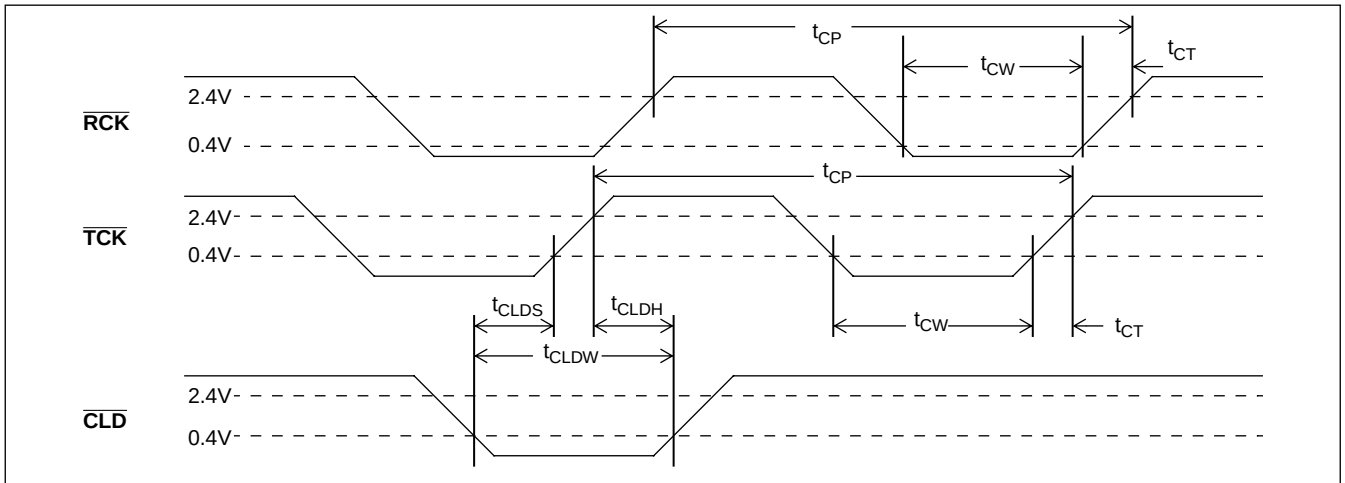


Figure 17 - Frequency Locking for the $\overline{C4}$ and OSC1 Clocks in MAS/DN Mode

AC Electrical Characteristics† - Clock Timing - MOD Mode (Figure 18)

	Characteristics	Sym	80 kbit/s			160 kbit/s			Units	Test Conditions
			Min	Typ*	Max	Min	Typ*	Max		
1	$\overline{TCK}$/$\overline{RCK}$ Clock Period	t_{CP}		12.5			6.25		µs	
2	$\overline{TCK}$/$\overline{RCK}$ Clock Width	t_{CW}		6.25			3.125		µs	
3	$\overline{TCK}$/$\overline{RCK}$ Clock Transition Time	t_{CT}		20			20		ns	C_L=40pF
4	$\overline{CLD}$ to $\overline{TCK}$ Setup Time	t_{CLDS}		3.125			1.56		µs	
5	$\overline{CLD}$ to $\overline{TCK}$ Hold Time	t_{CLDH}		3.125			1.56		µs	
6	$\overline{CLD}$ Width Low	t_{CLDW}		6.05			2.925		µs	
7	$\overline{CLD}$ Period	t_{CLDP}		8xt_{CP}			8xt_{CP}		µs	

† Timing is over recommended temperature & power supply voltage ranges.
* Typical figures are at 25°C, for design aid only: not guaranteed and not subject to production testing.



Note 1: $\overline{TCK}$ and $\overline{CLD}$ are generated on chip and provide the data clocks for the CD port and the transmit section of the DV port. $\overline{RCK}$, also generated on chip, is extracted from the receive data and only clocks out the data at the D_0 output and may be skewed with respect to $\overline{TCK}$ due to end-to-end delay.
Note 2: At the slave end $\overline{TCK}$ is phase locked to $\overline{RCK}$.
The rising edge of $\overline{TCK}$ will lead the rising edge of $\overline{RCK}$ by approximately 90°.

Figure 18 - $\overline{RCK}$, $\overline{TCK}$ & $\overline{CLD}$ Timing For MOD Mode

AC Electrical Characteristics† - Data Timing - DN Mode (Figure 19)

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	DSTi/CDSTi Data Setup Time	t_{RS}	30			ns	
2	DSTi/CDSTi Data Hold Time	t_{RH}	50			ns	
3a	DSTo/CDSTo Data Delay	t_{TD}			120	ns	C_L=40pF
3b	DSTo/CDSTo High Z to Data Delay	t_{ZTD}			140	ns	C_L=40pF

† Timing is over recommended temperature & power supply voltage ranges.

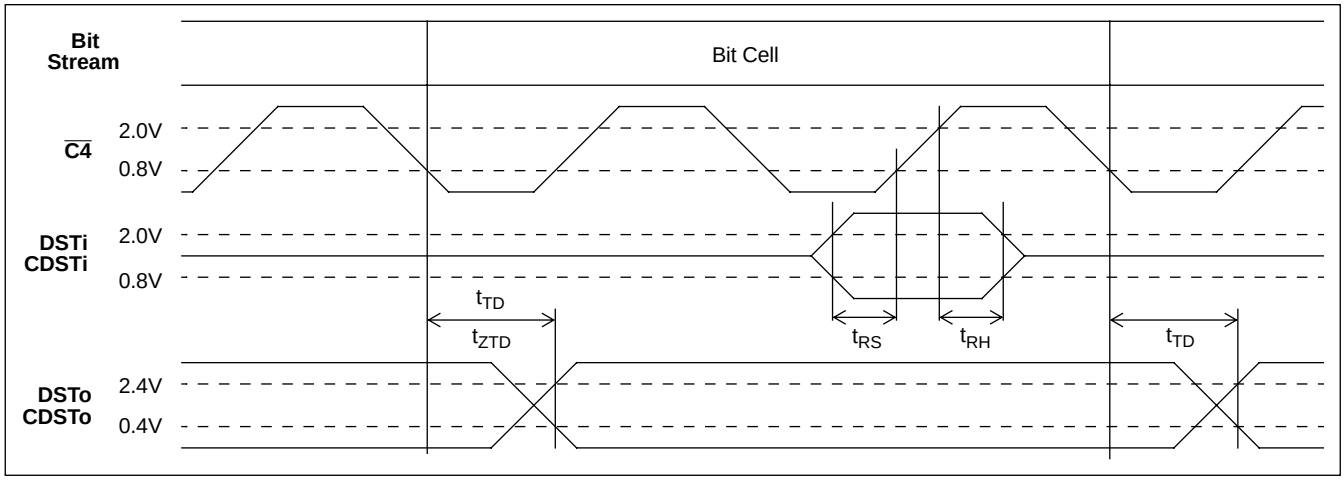


Figure 19 - Data Timing For DN Mode

AC Electrical Characteristics† - Data Timing - MOD Mode (Figure 20)

	Characteristics	Sym	80 kbit/s		160 kbit/s			Units	Test Conditions
			Min	Typ*	Max	Min	Typ*	Max		
1	Di/CDi Data Setup Time	t_{DS}	150			150			ns	
2	Di/CDi Data Hold Time	t_{DH}	4.5			2.5			µs	
3	Do Data Delay Time	t_{RD}		70			70		ns	C_L=40pF
4	CDo Data Delay Time	t_{TD}		70			70		ns	C_L=40pF

† Timing is over recommended temperature & power supply voltage ranges.
* Typical figures are at 25°C, for design aid only: not guaranteed and not subject to production testing.

Performance Characteristics of the MT9171 DSIC

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Allowable Attenuation for Bit Error Rate of 10^{-6} (Note 1)	A_{fb}	0	30	25	dB	SNR≥16.5dB (300kHz bandlimited noise)
2	Line Length at 80 kbit/s -24 AWG -26 AWG	L_{80}		3.0 2.2		km	attenuation - 6.9 dB/km attenuation - 10.0 dB/km
3	Line Length at 160 kbit/s -24 AWG -26 AWG	L_{160}		3.0 2.2		km	attenuation - 8.0 dB/km attenuation - 11.5 dB/km

Performance Characteristics of the MT9172 DNIC

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Allowable Attenuation for Bit Error Rate of 10^{-6} (Note 1)	A_{fb}	0	40	33	dB	SNR≥16.5dB (300kHz bandlimited noise)
2	Line Length at 80 kbit/s -24 AWG -26 AWG	L_{80}		5.0 3.4		km	attenuation - 6.9 dB/km attenuation - 10.0 dB/km
3	Line Length at 160 kbit/s -24 AWG -26 AWG	L_{160}		4.0 3.0		km	attenuation - 8.0 dB/km attenuation - 11.5 dB/km

Note 1: Attenuation measured from Master L_{OUT} to Slave L_{IN} at 3/4baud frequency.
* Typical figures are at 25°C, for design aid only: not guaranteed and not subject to production testing.

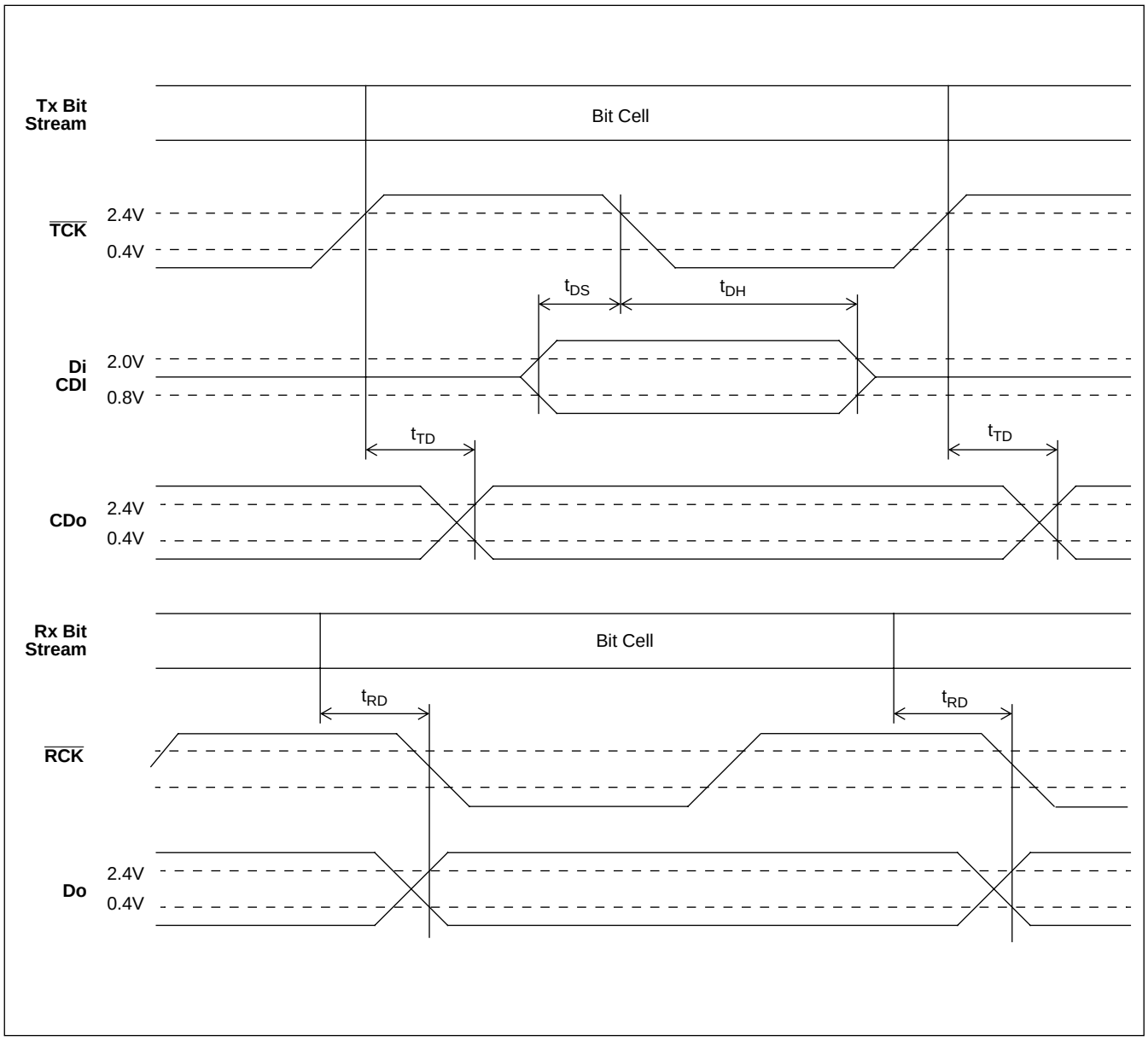


Figure 20 - Data Timing for Master Modem Mode

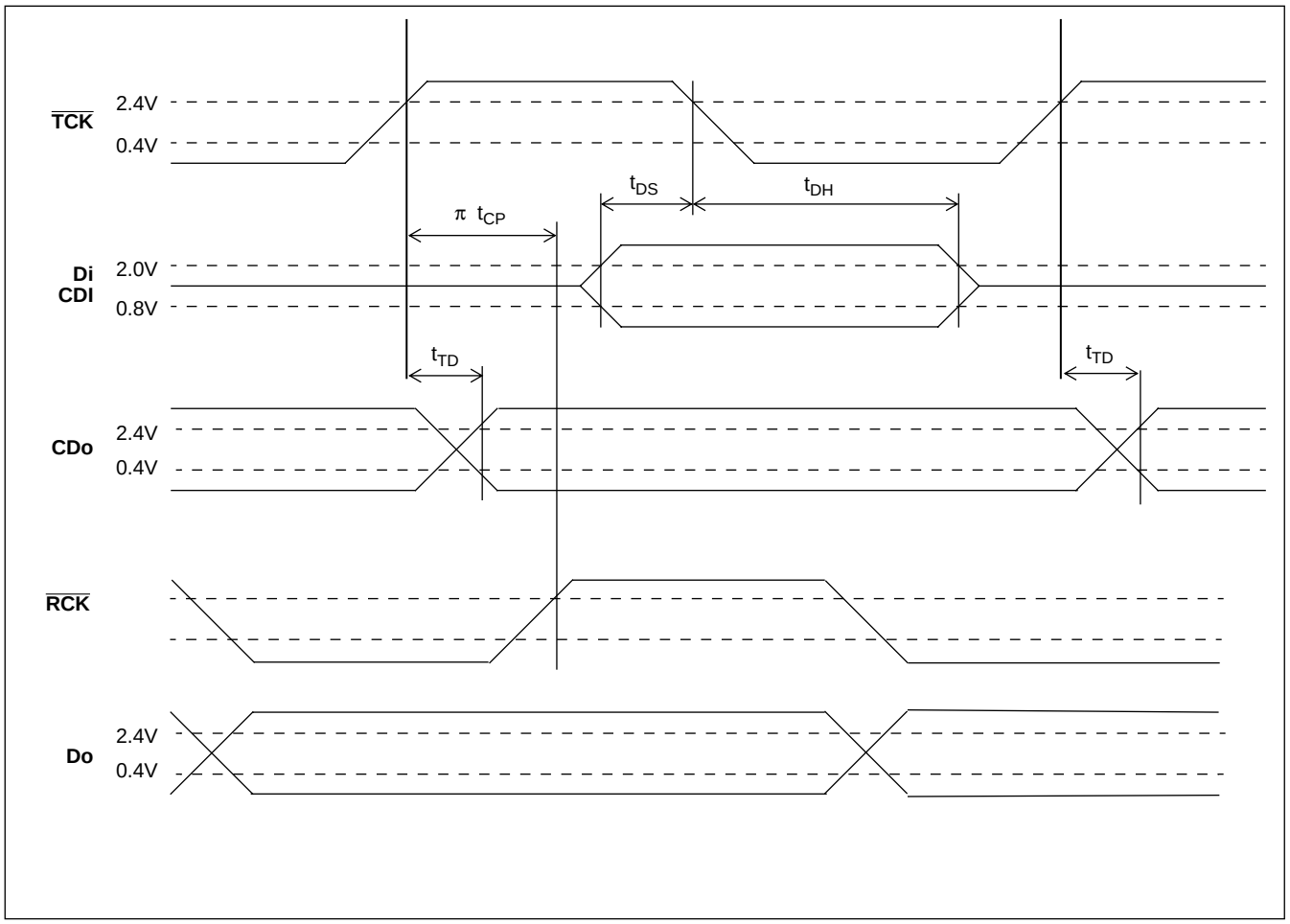
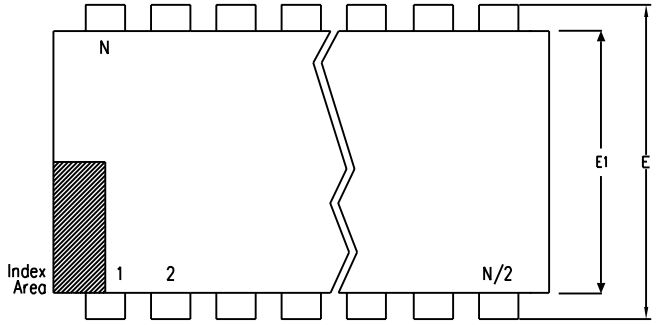
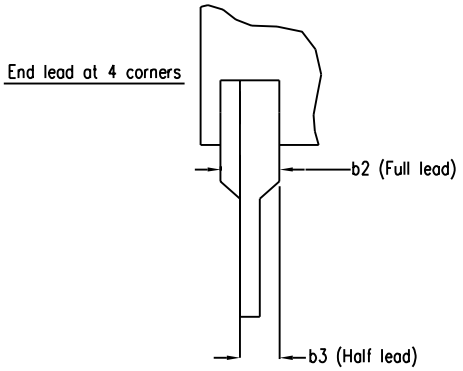
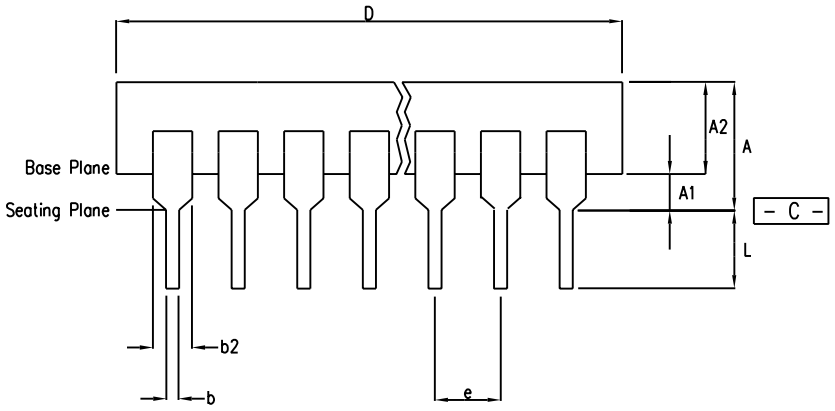
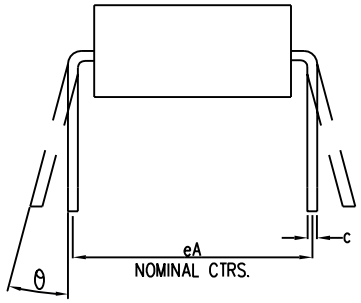


Figure 21 - Data Timing for Slave Modem Mode









SYMBOL	Min mm	Max mm	Min Inches	Max Inches
A		5.08		0.200
A1	0.51		0.020	
A2	3.81		0.150	
b	0.38	0.61	0.015	0.024
b2	1.14	1.65	0.045	0.065
b3	——		——	
c	0.23	0.41	0.009	0.016
D	30.48		1.200	
E	10.16	10.80	0.400	0.425
E1	8.38	9.65	0.330	0.380
e	2.54 BSC		0.100 BSC	
eA	10.16 BSC		0.400 BSC	
θ		15°		15°
L	3.05		0.120	
N	22		22	

Notes:

1. Dimensions D, D1 & E1 do not include mould flash or protrusions.
2. Dimensions E & eA are measured with leads constrained to be perpendicular to datum - C -
3. Angle θ is measured with the leads unconstrained
4. Controlling dimensions are Inches. Millimeter conversions are not necessarily exact.
5. N is the maximum of terminal positions.

This drawing supersedes: –
UK drawing # 418/ED/39502/006

ISSUE	1	2	3	
ACN	202564	208557	213108	
DATE	9Jun97	22Mar00	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

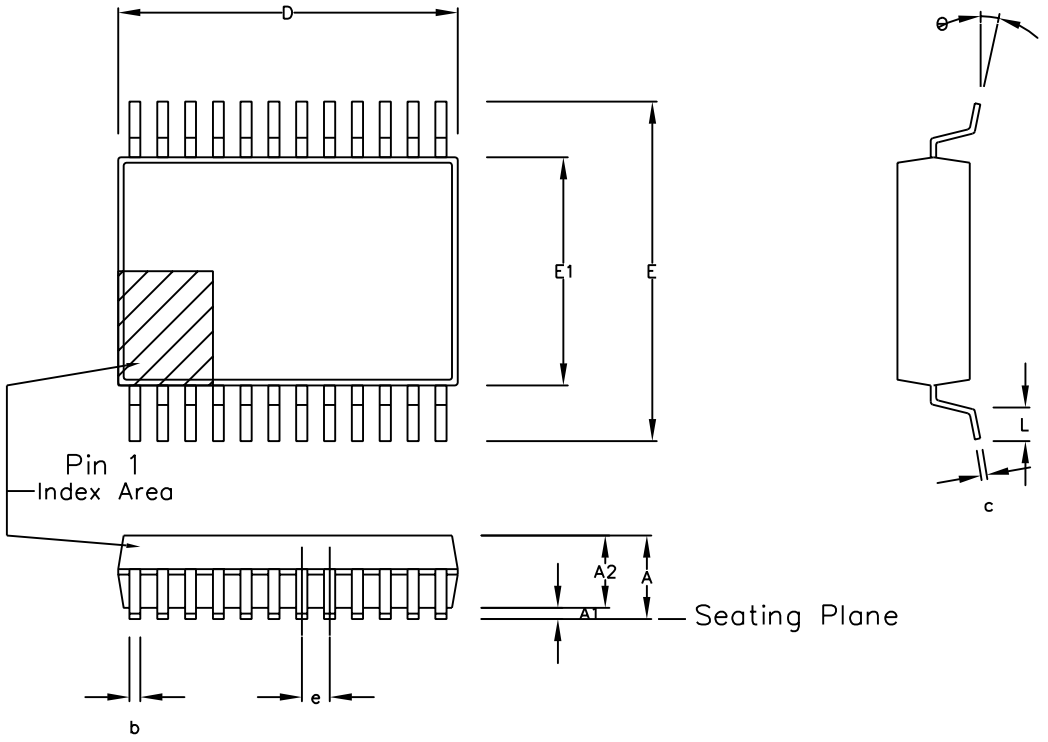
Previous package codes

DP / E

Package Code DA

Package Outline for 22 lead PDIP

GPD00349



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	7.90		8.50		0.311		0.335
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
θ	0°		8°		0°		8°
	Pin features						
N	24						
Conforms to JEDEC MO-150 AG Iss. B							

This drawing supersedes:-
418/ED/51481/003 (UK)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protrusion. Mould flash or protrusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

ISSUE	1	2	3	
ACN	201934	205233	213104	
DATE	27Feb97	25Sep98	15Jul02	
APPRD.				

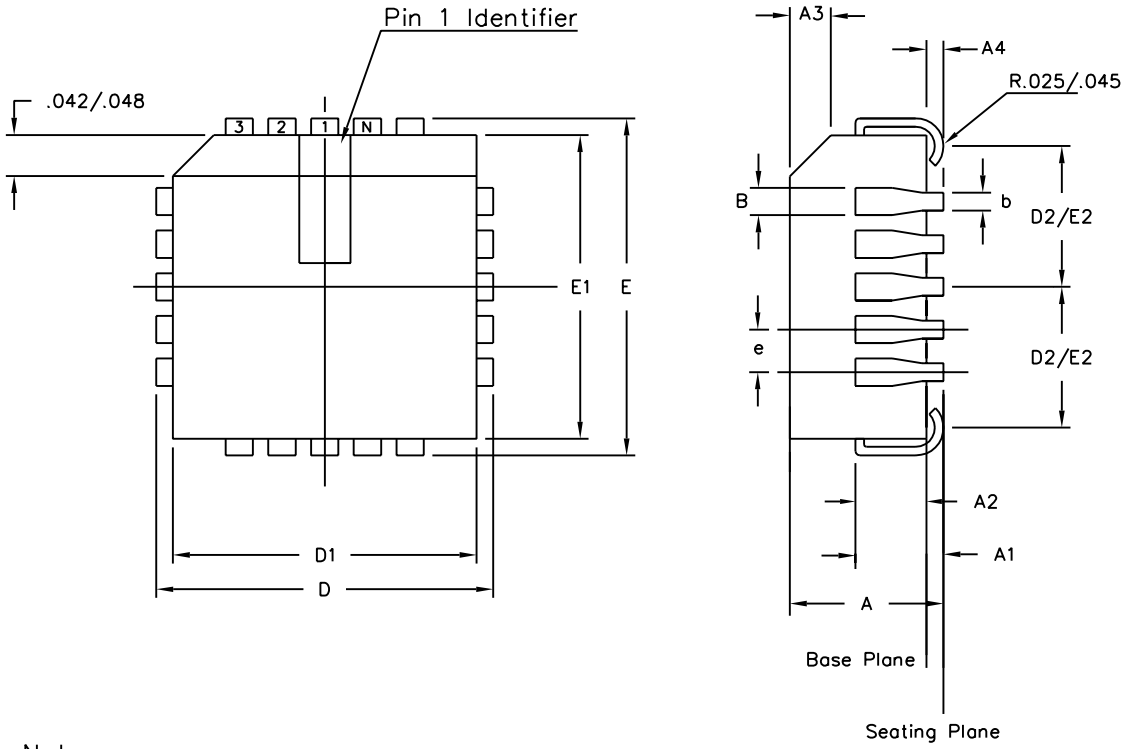
ZARLINK SEMICONDUCTOR

Previous package codes
NP / N

Package Code DD

Package Outline for
24 lead SSOP
(5.3mm Body Width)

GPD00295



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.485	0.495	12.32	12.57
D1	0.450	0.456	11.43	11.58
D2	0.191	0.219	4.85	5.56
E	0.485	0.495	12.32	12.57
E1	0.450	0.456	11.43	11.58
E2	0.191	0.219	4.85	5.56
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	7			
NE	7			
N	28			
Note	Square			
Conforms to JEDEC MS-018AB Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207469	212422	
DATE	15Aug94	10Sep99	22Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

HP / P

Package Code QA

Package Outline for 28 lead PLCC

GPD00002

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visit our Web Site at

www.zarlink.com