XC7236A
36-Macrocell CMOS CPLD

June 1, 1996 (Version 1.0)

Product Specification

Features

- Second-Generation High Density Programmable Logic Device
- UV-erasable CMOS EPROM technology
- 36 macrocells, grouped into four Function Blocks(FBs), interconnected by a programmable Universal Interconnect Matrix
- Each FB contains a programmable AND-array with 24 complementary inputs, providing up to 17 product terms per macrocell
- Enhanced logic features:
  - 2-input Arithmetic Logic Unit in each macrocell
  - Dedicated fast carry network between macrocells
  - Wide AND capability in the Universal Interconnect Matrix
- Identical timing for all interconnect paths and for all macrocell logic paths
- 36 signal pins
  - 30 I/Os, 2 inputs, 4 outputs
- Each input is programmable
  - Direct, latched, or registered
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ± 0.3 V
- Three high-speed, low-skew global clock inputs
- Available in 44-pin PLCC and CLCC packages

General Description

The XC7236A combines the classical features of the PAL-like CPLD architecture with innovative systems-oriented logic enhancements. This favors the implementation of fast state machines, large synchronous counters and fast arithmetic, as well as multi-level general-purpose logic. Performance, measured in achievable system clock rate and critical delays, is not only predictable, but independent of physical logic mapping, interconnect routing, and resource utilization. Performance, therefore, remains invariant between design iterations. The propagation delay through interconnect and logic is constant for any function implemented in any one of the output macrocells.

The functional versatility of the traditional programmable logic array architecture is enhanced through additional gating and control functions available in an Arithmetic Logic Unit (ALU) in each macrocell. Dedicated fast arithmetic carry lines running directly between adjacent macrocells and FBs support fast adders, subtractors and comparators of any length up to 36 bits.

This additional ALU in each macrocell can generate any combinatorial function of two sums of products, and it can generate and propagate arithmetic-carry signals between adjacent macrocells and FBs.

The Universal Interconnect Matrix (UIM) facilitates unrestricted, fixed-delay interconnects from all device inputs and macrocell outputs to any FB AND-array input. The UIM can also perform a logical AND across any number of its incoming signals on the way to any FB, adding another level of logic without additional delay. This supports bidirectional loadable synchronous counters of any size up to 36 bits, operating at the specified maximum device frequency

As a result of these logic enhancements, the XC7236A can deliver high performance even in designs that combine large numbers of product terms per output, or need more layers of logic than AND-OR, or need a wide AND function in some of the product terms, or perform wide arithmetic functions.

Architectural Overview

Figure 1 shows the XC7236A structure. Four Function Blocks(FBs) are all interconnected by a central UIM. Each FB receives 21 signals from the UIM and each FB produces nine signals back into the UIM. All device inputs are also routed via the UIM to all FBs. Each FB contains nine output macrocells that draw from a programmable AND array driven by the 21 signals from the UIM. Most macrocells drive a 3-state chip output. All feed back into the UIM.

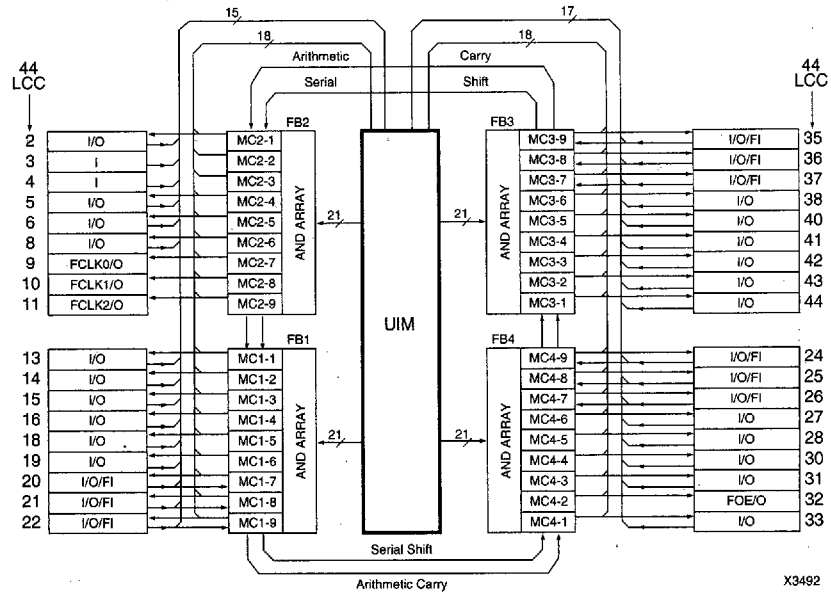


Figure 1: XC7236A Architecture

FBs and macrocells

The XC7236A contains 36 macrocells with identical structure, grouped into four FBs of nine macrocells each. Figure 2 shows the macrocell structure. Each macrocell is driven by product terms derived from a programmable AND array in the FB. The AND array in each FB receives 21 signals and their complements from the UIM. In three FBs, the AND array receives three additional inputs and their complements directly from FastInput (FI) pins, thus offering faster logic paths.

Five product terms are private to each macrocell; an additional 12 product terms are shared among the nine macrocells in each FB. Four of the private product terms can be selectively ORed together with up to four of the shared product terms, and drive the D1 input to the ALU. The other input, D2, to the ALU is driven by the OR of the fifth private product term and up to eight of the remaining shared product terms.

As a programmable option, four of the private product terms can be used for other purposes. One of the private product terms can be used as a dedicated clock for the flip-flop in the macrocell. (See the subsequent description of other clocking options.) Another one of the private product terms can be the asynchronous active-High Reset of the macrocell flip-flop, another one can be the asynchronous active-High Set of the macrocell flip-flop, and another one can be the Output Enable signal.

As a configuration option, the macrocell output can be fed back and ORed into the D2 input to the ALU after being ANDed with three of the shared product terms to implement counters and toggle flip-flops.

The ALU has two programmable modes. In the logic mode, it is a 2-input function generator, a 4-bit look-up table, that can be programmed to generate any Boolean function of its two inputs. It can OR them, widening the OR function to 17 inputs; it can AND them, which means that one sum of products can be used to mask the other; it can XOR them, toggling the flip-flop or comparing the two sums of products. Either or both of the sum-of-product inputs to the ALU can be inverted and either or both can be ignored. The ALU can implement one additional layer of logic without any speed penalty.

In the arithmetic mode, the ALU block in each macrocell can be programmed to generate the arithmetic sum or difference of two operands, combined with a carry signal coming from the next lower macrocell. It also feeds a carry output to the next higher macrocell. This carry propagation chain crosses the boundaries between FBs. This dedicated carry chain overcomes the inherent speed and density problems of the traditional CPLD architecture when trying to perform arithmetic functions.

The ALU output drives the D input of the macrocell flip-flop. Each flip-flop has several programmable options. One option is to eliminate the flip-flop by making it transparent, which makes the Q output identical with the D input, independent of the clock. Otherwise, the flip-flop operates in the

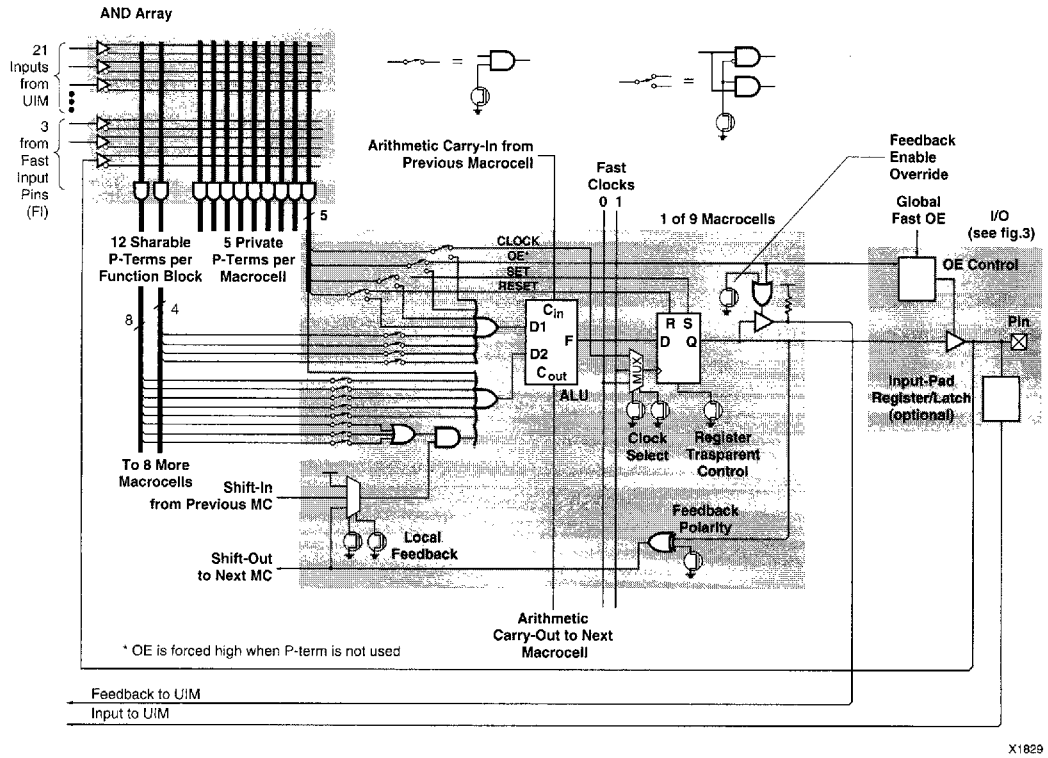


Figure 2: FB and macrocell Schematic

conventional manner, triggered by the rising edge on its clock input.

The clock source is programmable and is either the dedicated product term mentioned earlier, or one of two global FastCLK signals (FLCK0 or FLCK1) that are distributed with short delay and minimal skew over the whole chip.

The asynchronous Set and Reset (Clear) inputs override the clocked operation. If both asynchronous inputs are active simultaneously, Reset overrides Set. Upon power-up, each macrocell flip-flop can be preloaded with either 0 or 1.

In addition to driving a chip output pin, the macrocell output is also routed back as an input to the UIM. One private product term can be configured to control the Output Enable of the output pin driver and/or the feedback to the UIM. If configured to control UIM feedback, when the OE product-term is de-asserted, the UIM feedback line is forced High and thus disabled.

Universal Interconnect Matrix

The UIM receives 68 inputs: 36 from the macrocell feedbacks, 30 from bidirectional I/O pins, and 2 from dedicated input pins. Acting as an unrestricted crossbar switch, the UIM generates 84 output signals, 21 to each FB.

Any one of the 68 inputs can be programmed to be connected to any number of the 84 outputs. The delay through the array is constant, independent of the apparent routing distance, the fan-out, fan-in, or routing complexity.

Routability is not an issue in that any UIM input can drive any UIM output or multiple outputs without additional delay.

When multiple inputs are programmed to be connected to the same output, this output becomes the AND of the input signals if the levels are interpreted as active High. By choosing the appropriate signal inversion at the input pin, macrocell outputs and FB AND-array input, this AND-logic can also be used to implement a NAND, OR, or NOR function. This offers an additional level of logic without any speed penalty.

A macrocell feedback signal that is disabled by the output enable product term represents a High input to the UIM. Several such macrocell outputs programmed onto the same UIM output emulate a 3-state bus line. If one of the macrocell outputs is enabled, the UIM output assumes that same level.

Outputs

Thirty-four of the 36 macrocell drive chip outputs directly through individually programmable inverters followed by 3-state output buffers; each can be individually controlled by the Output Enable product term mentioned above. An additional configuration option disables the output permanently. One dedicated FastOE input also can be configured to control any of the chip outputs instead of, or in conjunction with, the individual OE product term.

Inputs

Each signal input to the chip is programmable as either direct, latched, or registered in a flip flop. The latch and flip-flop can be programmed with either of two FastCLK signals as latch enable or clock. The two FastCLK signals are FCLK0 and a global choice of either FCLK1 or FCLK2. Latches are transparent when FastCLK is High, and flip-flops clock on the rising edge of FastCLK. Registered inputs allow high system clock rates by pipelining the inputs before they incur the combinatorial delay in the device, provided the one-clock-period pipeline latency is acceptable.

The direct, latched, or registered inputs then drive the UIM. There is no propagation-delay difference between pure inputs and I/O inputs.

3.3 V or 5 V Interface configuration

The XC7236A can be used in systems with two different supply voltages, 5 V and 3.3 V. The device has separate V_{CC} connections to the internal logic and input buffers (V_{CCINT}) and to the I/O output drivers (V_{CCIO}). V_{CCINT} is always connected to a nominal +5 V supply, but V_{CCIO} may be connected to either +5 V or +3.3 V, depending on the output interface requirement.

When V_{CCIO} is connected to +5 V, the input thresholds are TTL levels, and thus compatible with 5 V or 3.3 V logic, and the output high levels are compatible with 5 V systems. When V_{CCIO} is connected to 3.3 V, the input thresholds are still TTL levels, and the outputs pull up to the 3.3 V rail. This makes the XC7236A ideal for interfacing directly to 3.3 V components. In addition, the output structure is designed such that the I/O can also safely interface to a mixed 3.3-V and 5-V bus.

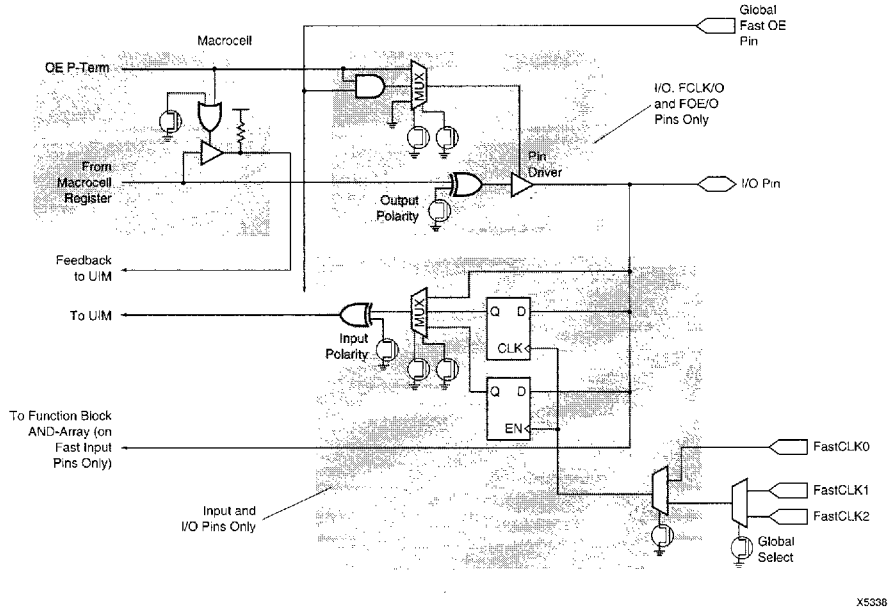


Figure 3: Input/Output Schematic

Programming and Using the XC7236A

The features and capabilities described above are used by the Xilinx development software to program the device according to the specification given either through schematic entry, or through a behavioral description expressed in Boolean equations.

The user can specify a security bit that prevents any reading of the programming bit map after the device has been programmed and verified.

The device is programmed in a manner similar to an EPROM (ultra-violet light erasable read-only memory) using the Intel Hex format. Programming support is available from a number of programmer manufacturers. The UIM connections and FB AND-array connections are made directly by non-volatile EPROM cells. Other control bits are read out of the EPROM array and stored into latches just after power-up. This method, common among EPLD devices, requires application of a master-reset signal delayed at least until V_{CC} has reached the required operating voltage. This can be achieved using a simple capacitor and pull-up resistor on the MR pin (the RC product should be larger than twice the V_{CC} rise time). The power-up or reset signal initiates a self-timed configuration period lasting about 350 µs (t_{RESET}), during which all device outputs remain disabled and programmed preload state values are loaded into the macrocell registers.

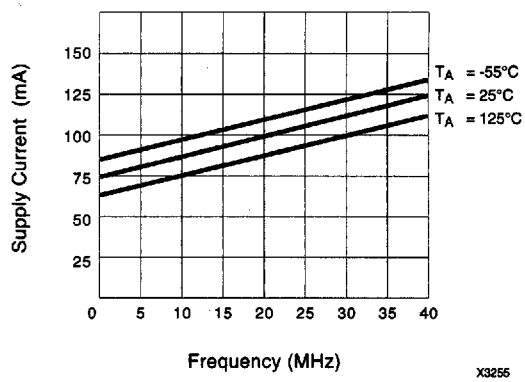


Figure 4: Typical I_{CC} vs. Frequency for XC7236A configured as sixteen 4-bit counters
(V_{CC} = +5.0 V, V_{IN} = V_{CC} or GND, all outputs open)

Unused input and I/O pins should be tied to ground or Vcc or some valid logic level. This is common practice for all CMOS devices to avoid dissipating excess current through the input pad circuitry.

The recommended decoupling capacitance on the three V_{CC} pins should total 1 µF using high-speed (tantalum or ceramic) capacitors.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT}/ V_{CCIO}	Supply voltage relative to GND Commercial T_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND Industrial T_A = –40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND Military T_A = –55°C to T_C + 125°C	4.5	5.5	V
V_{CCIO}	I/O supply voltage 3.3 V	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V TTL Low-level output voltage	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 24 mA V_{CC} = Min		0.4	V
I_{CC}	Supply current	V_{IN} = 0 V V_{CC} = Max f = 0 MHz	126 Typ		mA
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}	-10	+10	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_O = GND or V_{CCIO}	-100	+100	µA
C_{IN}	Input capacitance (sample tested)	V_{IN} = GND f = 1.0 MHz		10	pF

AC Timing Requirements

Symbol	Parameter	Fig.	XC7236A-25		XC7236A-20		XC7236A-16 (Com/Ind only)		Units
			Min	Max	Min	Max	Min	Max	
f_{CYC} (Note 1)	Max sequential toggle frequency (with feedback) using FastCLK	6	40		50		60		MHz
f_{CYC1} (Note 1)	Max sequential toggle frequency (with feedback) using a Product-Term Clock	6	40		50		60		MHz
f_{CYC4} (Note 2)	Max macrocell toggle frequency using local feedback and FastCLK		50		50		60		MHz
f_{CLK} (Note 2)	Max macrocell register transmission frequency (without feedback) using FastCLK		45		50		60		MHz
f_{CLK1} (Note 2)	Max macrocell register transmission frequency (without feedback) using a Product-Term Clock		42		50		60		MHz
f_{CLK2} (Note 2)	Max input register transmission frequency (without feedback) using FastCLK		50		50		60		MHz
f_{CLK3} (Note 1)	Max input register to macrocell register pipeline frequency using FastCLK	7	33		40		60		MHz
t_W	FastCLK pulse width (High/Low)	11	10		8		6		ns
f_{TOG}	Export Control Max. flip-flop toggle rate			50		62		83	MHz
t_{W1}	Product-term clock pulse width (active/inactive)	11	12		9		7		ns
t_{SU}	Input to macrocell register set-up time before FastCLK	9	29		24		18		ns
t_H	Input to macrocell register hold time after FastCLK	9	-7		-4		-4		ns
t_{SU1} (Note 1)	Input to macrocell register set-up time before Product-term clock	8	16		14		10		ns
t_{H1}	Input to macrocell register hold time after Product-term clock	8	0		0		0		ns
t_{SU2}	Input to register/latch set-up time before FastLCK	10	8		8		6		ns
t_{H2}	Input to register/latch hold time after FastLCK	10	0		0		0		ns
t_{SU5}	FastInput to macrocell register set-up time before FastCLK		20		18		15		ns
t_{H5}	FastInput to macrocell register hold time after FastCLK		0		0		0		ns
t_{WA}	Set/Reset pulse width (active)	11	12		12		10		ns
t_{RA}	Set/Reset input recovery set-up time before FastCLK	11	30		25		20		ns
t_{HA}	Set/Reset input hold time after FastCLK	11	-5		0		0		ns
t_{RA1}	Set/Reset input recovery set-up time before Product-term clock	11	15		15		12		ns
t_{HA1}	Set/Reset input hold time after Product-term clock	11	9		9		8		ns
t_{HRS}	Product-term clock width (active/inactive)		10		10		8		ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms and the ALU.
2. Not tested but derived from appropriate pulse-widths, set-up time and hold-time measurements.

Propagation Delays

Symbol	Parameter	Fig.	XC7236A-25		XC7236A-20		XC7236A-16 (Com/Ind only)		Units
			Min	Max	Min	Max	Min	Max	
t_{CO}	FastCLK input to registered output delay	11	5	14	3	13	3	10	ns
t_{CO1}	P-term clock input to registered output delay	11	10	30	5	24	5	20	ns
t_{AO}	Set/Reset input to registered output delay	11	10	40	5	32	5	25	ns
t_{PD} (Note 1)	Input to non-registered output delay	11	10	40	5	32	5	25	ns
t_{OE}	Input to output enable	11	10	32	5	25	5	20	ns
t_{OD}	Input to output disable	11	10	32	5	25	5	20	ns
t_{PD5}	FastInput to non-registered macrocell output delay		10	31	5	25	5	20	ns
t_{OE5}	FastInput to output enable		5	23	3	20	3	15	ns
t_{OD5}	FastInput to output disable		5	23	3	20	3	15	ns
t_{FOE}	FOE input to output enable		5	15	3	14	3	12	ns
t_{FOD}	FOD input to output disable		5	15	3	14	3	12	ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms and the ALU.

Incremental Parameters

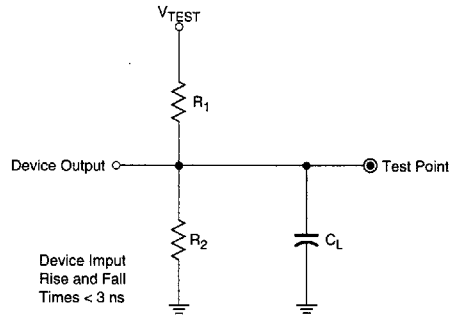
Symbol	Parameter	Fig.	XC7236A-25		XC7236A-20		XC7236A-16 (Com/Ind only)		Units
			Min	Max	Min	Max	Min	Max	
t_{PDT1} (Note 2)	Arithmetic carry delay between adjacent macrocells	12		1.2		1.2		1	ns
t_{PDT8} (Note 2)	Arithmetic carry delay through 9 adjacent macrocells in a FB	12		6		5		3	ns
t_{PDT9} (Note 2)	Arithmetic carry delay through 10 macrocells from macrocell #n to macrocell #n in next FB	12		9		6		4	ns
t_{COF1}	Incremental delay from UIM-input (for P-term clock) to registered macrocell feedback	13		12		7		5	ns
t_{COF2} (Note 3)	Incremental delay from FastCLK net to latched/registered UIM-input	13		1		1		1	ns
t_{PDF} (Note 1)	Incremental delay from UIM-input to non-registered macrocell feedback	13		22		14		10	ns
t_{AOF}	Incremental delay from UIM-input (Set/Reset) to registered macrocell feedback	13		22		14		10	ns
t_{OEF} t_{ODF}	Incremental delay from UIM-input (used as output-enable/disable) to macrocell feedback	13		14		7		5	ns
$t_{IN} + t_{OUT}$ (Note 4)	Propagation delay through unregistered input pad (to UIM) plus output pad driver (from macrocell)	13		18		18		15	ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms and the ALU.
2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent macrocell(s) for an adder with registered outputs.
3. Parameter t_{COF2} is derived as the difference between the clock period for pipelining input-to-macrocell registers ($1/f_{CLK3}$) and the non-registered input set-up time (t_{SU}).
4. Parameter t_{IN} represents the delay from an input or I/O pin to a UIM-input (or from a FastCLK pin to the Fast CLK net); t_{OUT} represents the delay from a macrocell output (feedback point) to an output or I/O pin. Only the sum of $t_{IN} + t_{OUT}$ can be derived from measurements, e.g., $t_{IN} + t_{OUT} = t_{SU} + t_{CO} - 1/f_{CYC}$.

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{rVCC}	V_{CC} rise time (if MR not used for power-up)			5	µs
t_{RESET}	Configuration completion time (to outputs operational)		350	1000	µs

Note: Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, V_{CC} rise *must be* monotonic. Following reset, the Clock, Reset and Set inputs must not be asserted until all applicable input and feedback set-up times are met.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
O	5.0 V	5.0 V	310 Ω	195 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X3489

Figure 5: AC Load Circuit

Timing and Delay Path Specifications

The delay path consists of three blocks that can be connected in series:

- Input Buffer and associated latch or register
- Logic Resource (UIM, AND-array and macrocell)
- Three-state Output Buffer

All inputs have the same delay, regardless of fan-out or location. All logic resources have the same delay, regardless of logic complexity, interconnect topology or location on the chip. All outputs have the same delay. The achievable clock rate is, therefore, determined only by the input method (direct, latched or registered) and the number of times a signal passes through the combinatorial logic.

Timing and Delay Path Descriptions

Figure 6 defines the maximum clock frequency (with feedback). Any macrocell output can be fed back to the UIM as an input for the next clock cycle. Figure 6 shows the relevant delay path. The parameters f_{CYC} and f_{CYC1} specify the maximum operating frequency for FastCLK and product-term clock operation respectively.

Figure 7 specifies the max operating frequency (f_{CLK3}) for pipelined operation between the input registers and the macrocell registers, using FastCLK.

Figure 8 defines the set-up and hold times from the data inputs to the product-term clock used by the output register.

Figure 9 defines the set-up and hold times from the data inputs to the FastCLK used by the output register.

Figure 10 defines the set-up and hold times from the data input to the FastCLK used in an input register.

Figure 11 shows the waveforms for the macrocell and control paths

Figure 12 defines the carry propagation delays between macrocells and between FBs. The parameters describe the delay from the C_{IN}, D1 and D2 inputs of a macrocell ALU to the C_{IN} input of the adjacent macrocell ALU. These delays must be added to the standard macrocell delay path (t_{PD} or t_{SU}) to determine the performance of an arithmetic function.

Figure 13 defines the incremental parameters for the standard macrocell logic paths. These incremental parameters are used in conjunction with pin-to-pin parameters when calculating compound logic path timing. Incremental parameters are derived indirectly from other pin-to-pin measurement.

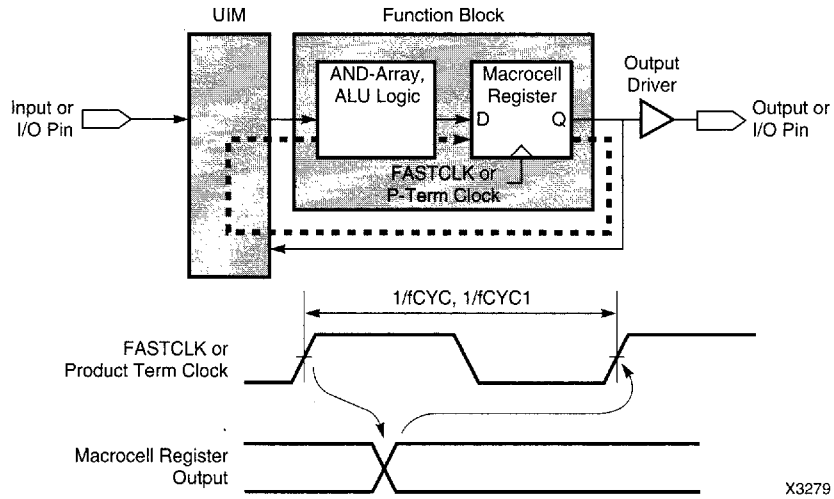


Figure 6: Delay Path Specification for f_{CYC} and f_{CYC1}

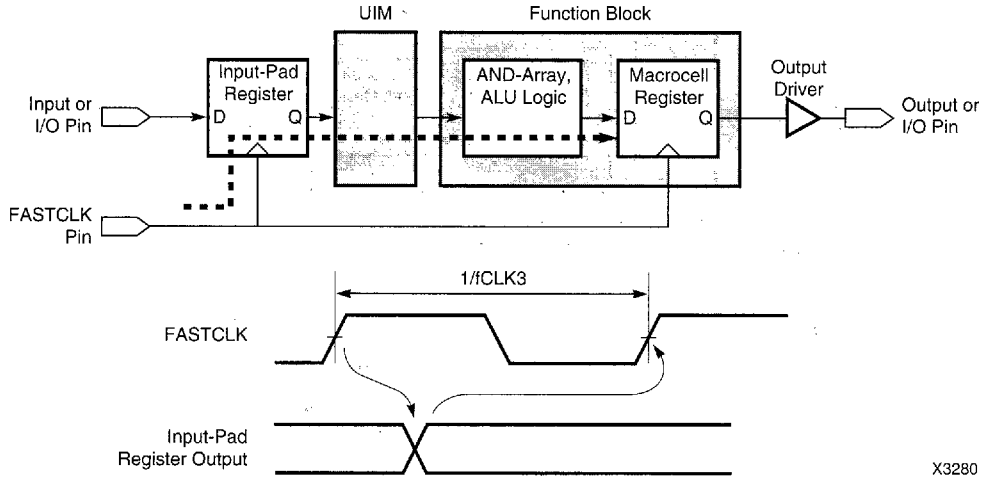


Figure 7: Delay Path Specification for f_{CLK3}

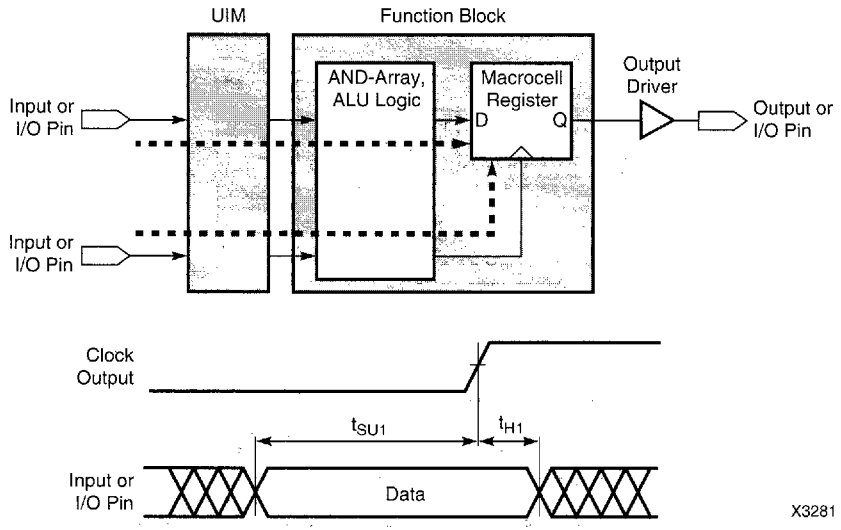


Figure 8: Delay Path Specification for f_{SU1} and f_{H1}

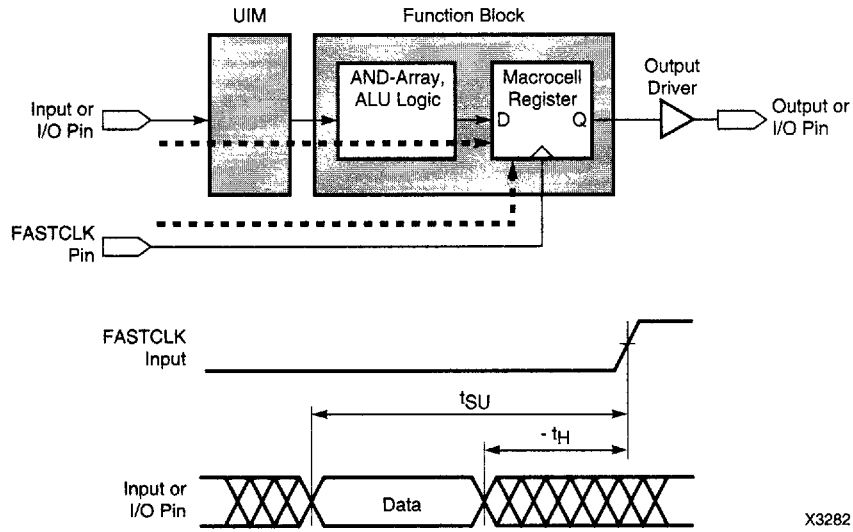


Figure 9: Delay Path Specification for f_{SU} and f_H

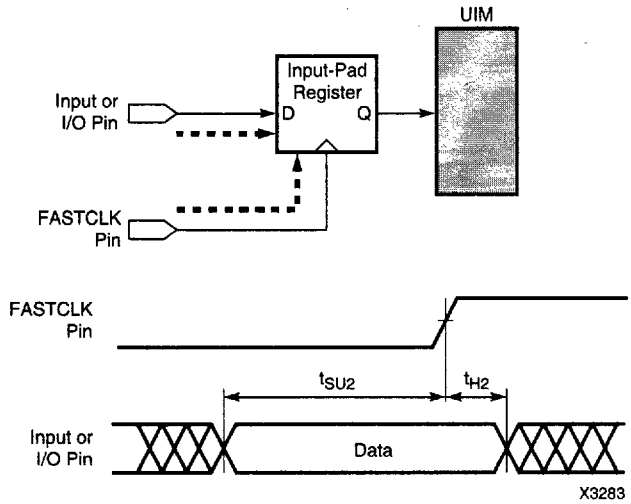


Figure 10: Delay Path Specification for f_{SU2} and f_{H2}

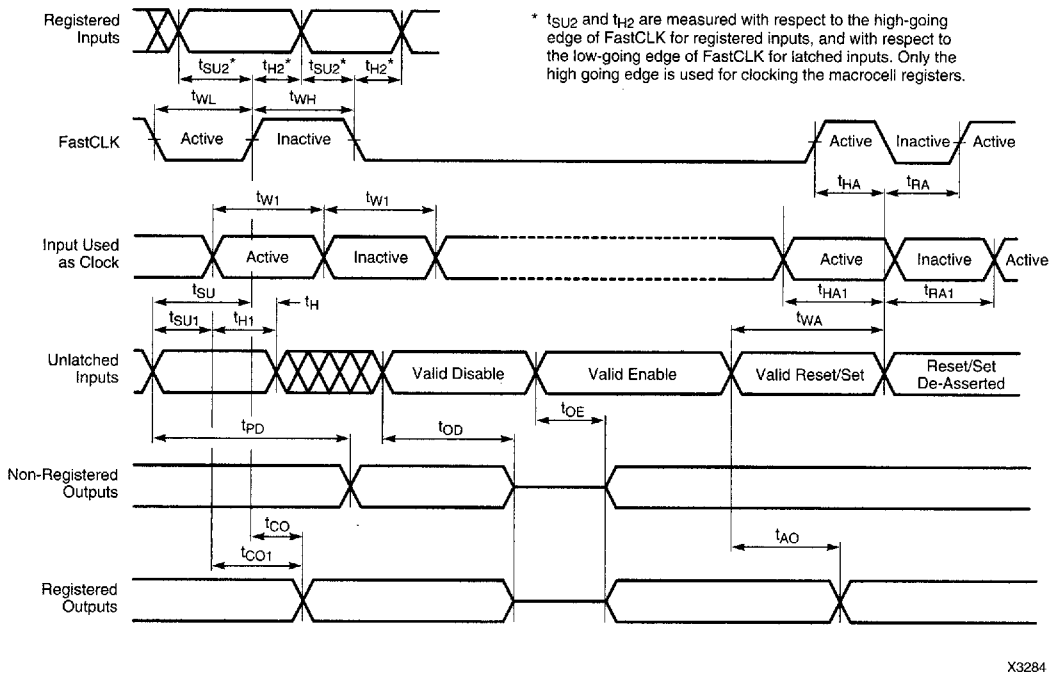


Figure 11: Principal Pin-to-Pin Measurements

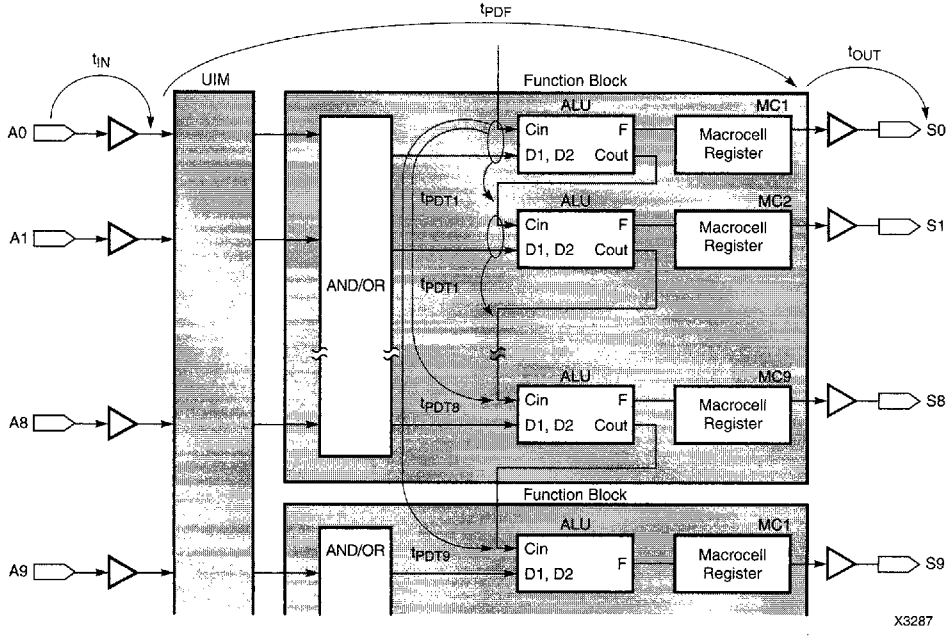


Figure 12: Arithmetic Timing Parameters

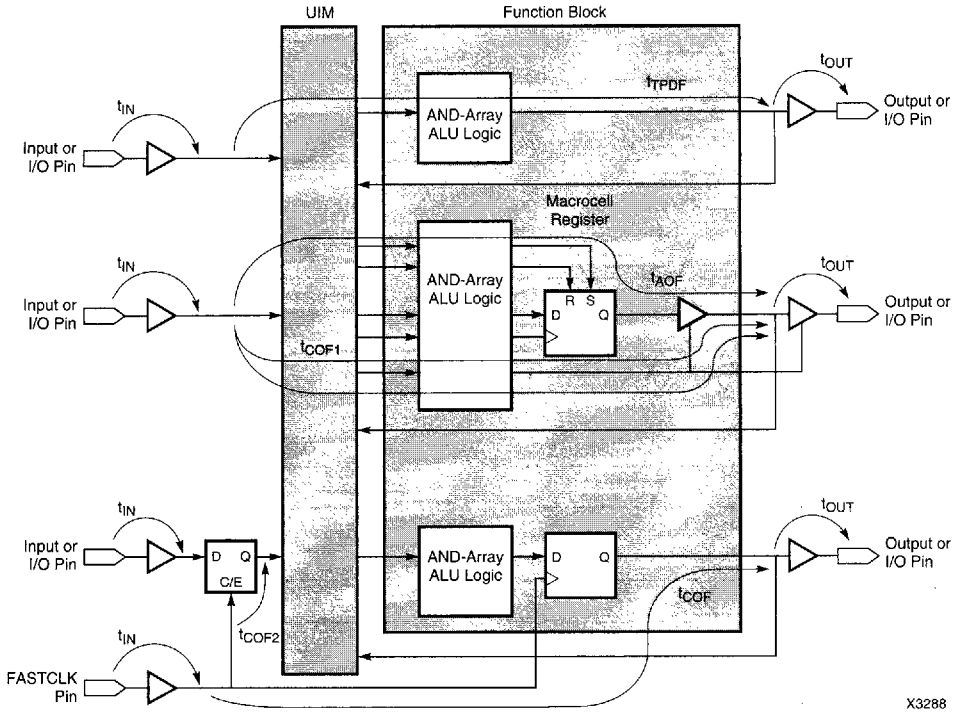


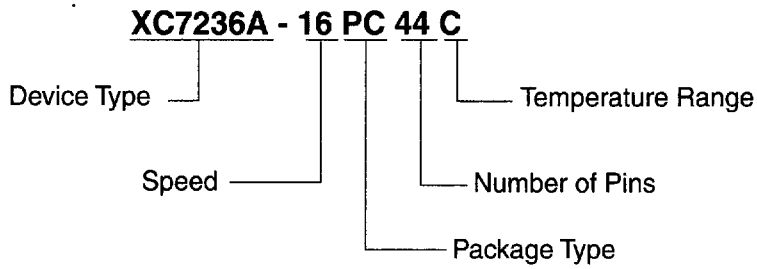
Figure 13: Incremental Timing Parameters

XC7372 Pinouts

Pin #	Input	Output
1	Master Reset VPP	
2	Input	MC2-1
3	Input	
4	Input	
5	Input	MC2-4
6	Input	MC2-5
7	GND	
8	Input	MC2-6
9	FastCLK0	MC2-7
10	FastCLK1	MC2-8
11	FastCLK2	MC2-9
12	VCCIO	
13	Input	MC1-1
14	Input	MC1-2
15	Input	MC1-3
16	Input	MC1-4
17	GND	
18	Input	MC1-5
19	Input	MC1-6
20	Input/FI	MC1-7
21	Input/FI	MC1-8
22	Input/FI	MC1-9

Pin #	Input	Output
23	VCCIO	
24	Input/FI	MC4-9
25	Input/FI	MC4-8
26	Input/FI	MC4-7
27	Input	MC4-6
28	Input	MC4-5
29	GND	
30	Input	MC4-4
31	Input	MC4-3
32	FastOE	MC4-2
33	Input	MC4-1
34	VCCINT	
35	Input/FI	MC3-9
36	Input/FI	MC3-8
37	Input/FI	MC3-7
38	Input	MC3-6
39	GND	
40	Input	MC3-5
41	Input	MC3-4
42	Input	MC3-3
43	Input	MC3-2
44	Input	MC3-1

Ordering Information



Speed Options

-25	25 ns (40 MHz) sequential cycle time
-20	20 ns (50 MHz) sequential cycle time
-16	16 ns (60 MHz) sequential cycle time (commercial/industrial only)

Packaging Options

PC44	44-Pin Plastic Leaded Chip Carrier
WC44	44-Pin Windowed Ceramic Leaded Chip Carrier

Temperature Options

C	Commercial0°C to 70°C
I	Industrial -40°C to 85°C
M	Military -55°C (Ambient) to 125°C (Case)

Component Availability

Pins		44	
Type		Plastic PLCC	Ceramic CLCC
Code		PC44	WC44
XC7236A	-25	CI	CIM
	-20	CI	CIM
	-16	CI	CI

C = Commercial = 0° to +70°C I = Industrial = –40° to 85°C M = Military = –55°C(A) to 125°C (C)