XC1700E, XC1700EL, and XC1700L Series Configuration PROMs

DS027 (v3.2) September 7, 2004 **Product Specification**

Features

- One-time programmable (OTP) read-only memory designed to store configuration bitstreams of Xilinx FPGA devices
- Simple interface to the FPGA; requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- XC17128E/EL, XC17256E/EL, XC1701 and XC1700L series support fast configuration
- Low-power CMOS Floating Gate process
- XC1700E series are available in 5V and 3.3V versions
- XC1700L series are available in 3.3V only
- Available in compact plastic packages: 8-pin SOIC, 8-pin VOIC, 8-pin PDIP, 20-pin SOIC, 20-pin PLCC, 44-pin PLCC or 44-pin VQFP.
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.
- Guaranteed 20 year life data retention

Description

The XC1700 family of configuration PROMs provides an easy-to-use, cost-effective method for storing large Xilinx FPGA configuration bitstreams. See Figure 1 for a simplified block diagram.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the FPGA D_{IN} pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. After configured, it disables the PROM. When the FPGA is in Slave Serial mode, the PROM and the FPGA must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

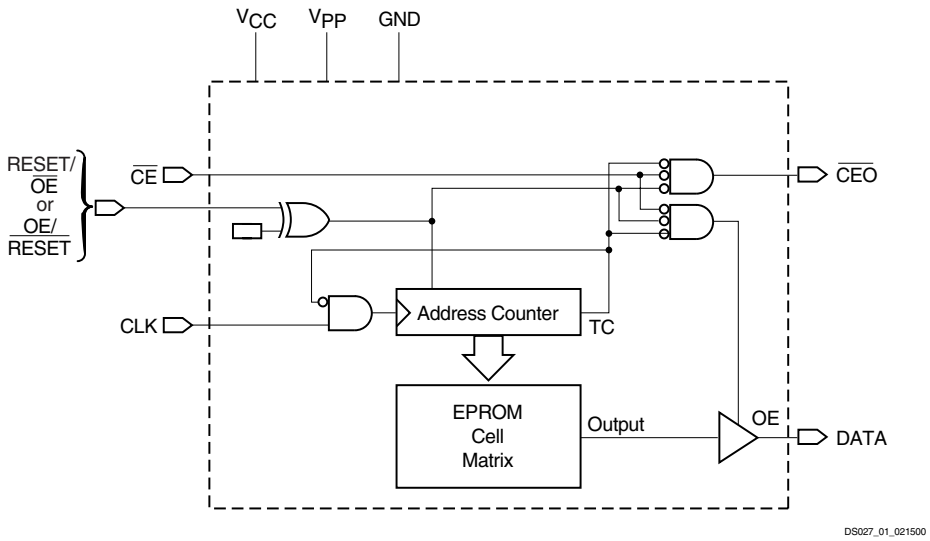


Figure 1: **Simplified Block Diagram (does not show programming circuit)**

For device programming, either the Xilinx Alliance or Foundation series development system compiles the FPGA design file into a standard Hex format, which is then transferred to most commercial PROM programmers.

Pin Description

DATA

Data output is in a high-impedance state when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

CLK

Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.

RESET/$\overline{OE}$

When High, this input holds the address counter reset and puts the DATA output in a high-impedance state. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/RESET. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at "0", and puts the DATA output in a high-impedance state. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be driven by the FPGAs INIT pin.

The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 Programmer. Third-party programmers have different methods to invert this pin.

$\overline{CE}$

When High, this pin disables the internal address counter, puts the DATA output in a high-impedance state, and forces the device into low-I_{CC} standby mode.

$\overline{CEO}$

Chip Enable output, to be connected to the $\overline{CE}$ input of the next PROM in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, $\overline{CEO}$ will follow $\overline{CE}$ as long as $\overline{OE}$ is active. When $\overline{OE}$ goes inactive, $\overline{CEO}$ stays High until the PROM is reset. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

V_{PP}

Programming voltage. No overshoot above the specified max voltage is permitted on this pin. For normal read operation, this pin must be connected to V_{CC}. Failure to do so may lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging. Do not leave V_{PP} floating!

V_{CC} and GND

Positive supply and ground pins.

PROM Pinouts

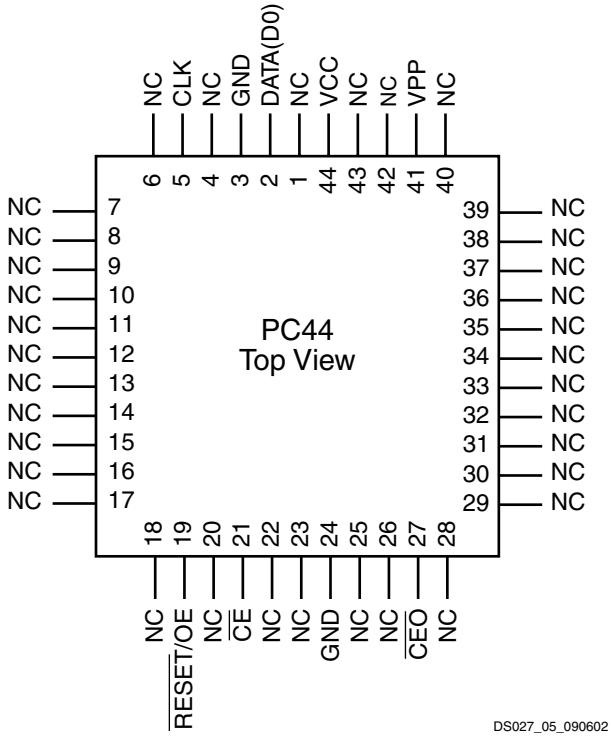
Pins not listed are "no connects."

Pin Name	8-pin PDIP (PD8) SOIC (SO8) VOIC (VO8)	20-pin SOIC (SO20)	20-pin PLCC (PC20)	44-pin VQFP (VQ44)	44-pin PLCC (PC44)
DATA	1	1	2	40	2
CLK	2	3	4	43	5
RESET/$\overline{OE}$ (OE/RESET)	3	8	6	13	19
$\overline{CE}$	4	10	8	15	21
GND	5	11	10	18, 41	24, 3
$\overline{CEO}$	6	13	14	21	27
V_{PP}	7	18	17	35	41
V_{CC}	8	20	20	38	44

Capacity

Devices	Configuration Bits
XC1704L	4,194,304
XC1702L	2,097,152
XC1701/L	1,048,576
XC17512L	524,288
XC1736E	36,288
XC1765E/EL	65,536
XC17128E/EL	131,072
XC17256E/EL	262,144

Pinout Diagrams



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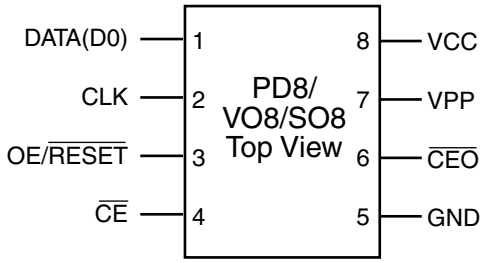

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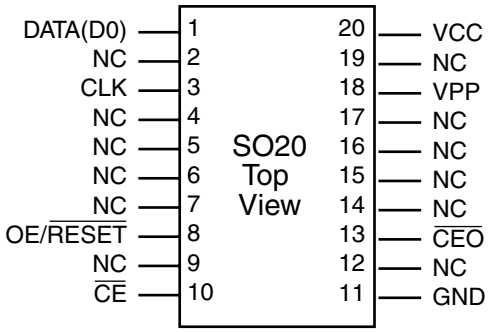

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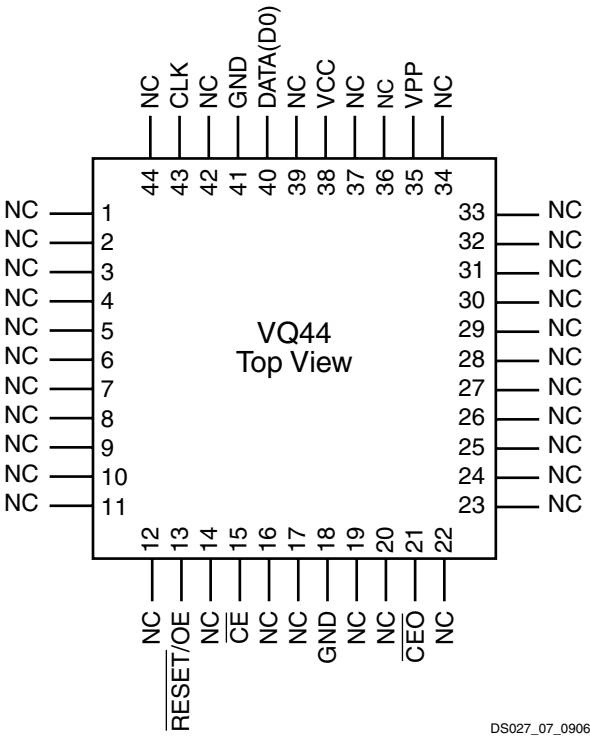

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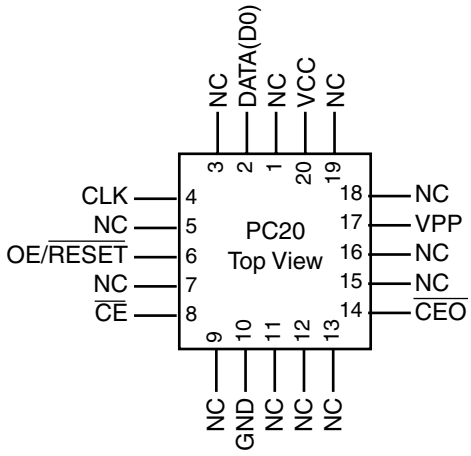


DS027_09_110102

Xilinx FPGAs and Compatible PROMs

Device	Configuration Bits	PROM
XC4003E	53,984	XC17128E(1)
XC4005E	95,008	XC17128E
XC4006E	119,840	XC17128E
XC4008E	147,552	XC17256E
XC4010E	178,144	XC17256E
XC4013E	247,968	XC17256E
XC4020E	329,312	XC1701
XC4025E	422,176	XC1701
XC4002XL	61,100	XC17128EL(1)
XC4005XL	151,960	XC17256EL
XC4010XL	283,424	XC17512L
XC4013XL/XLA	393,632	XC17512L
XC4020XL/XLA	521,880	XC17512L
XC4028XL/XLA	668,184	XC1701L
XC4028EX	668,184	XC1701
XC4036EX/XL/XLA	832,528	XC1701L
XC4036EX	832,528	XC1701
XC4044XL/XLA	1,014,928	XC1701L
XC4052XL/XLA	1,215,368	XC1702L
XC4062XL/XLA	1,433,864	XC1702L
XC4085XL/XLA	1,924,992	XC1702L
XC40110XV	2,686,136	XC1704L
XC40150XV	3,373,448	XC1704L
XC40200XV	4,551,056	XC1704L + XC17512L
XC40250XV	5,433,888	XC1704L+ XC1702L
XC5202	42,416	XC1765E
XC5204	70,704	XC17128E
XC5206	106,288	XC17128E
XC5210	165,488	XC17256E
XC5215	237,744	XC17256E
XCV50	559,200	XC1701L
XCV100	781,216	XC1701L
XCV150	1,040,096	XC1701L
XCV200	1,335,840	XC1702L
XCV300	1,751,808	XC1702L
XCV400	2,546,048	XC1704L
XCV600	3,607,968	XC1704L
XCV800	4,715,616	XC1704L + XC1701L
XCV1000	6,127,744	XC1704L + XC1702L
XCV50E	630,048	XC1701L
XCV100E	863,840	XC1701L
XCV200E	1,442,016	XC1702L
XCV300E	1,875,648	XC1702L
XCV400E	2,693,440	XC1704L
XCV405E	3,340,400	XC1704L
XCV600E	3,961,632	XC1704L
XCV812E	6,519,648	2 of XC1704L
XCV1000E	6,587,520	2 of XC1704L
XCV1600E	8,308,992	2 of XC1704L
XCV2000E	10,159,648	3 of XC1704L
XCV2600E	12,922,336	4 of XC1704L
XCV3200E	16,283,712	4 of XC1704L

Notes:

1. The suggested PROM is determined by compatibility with the higher configuration frequency of the Xilinx FPGA CCLK. Designers using the default slow configuration frequency (CCLK) can use the XC1765E or XC1765EL for the noted FPGA devices.

Controlling PROMs

Connecting the FPGA device with the PROM.

- The DATA output(s) of the of the PROM(s) drives the D_{IN} input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s).
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The $\overline{RESET}$/OE input of all PROMs is best driven by the $\overline{INIT}$ output of the lead FPGA device. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch. Other methods—such as driving $\overline{RESET}$/OE from $\overline{LDC}$ or system reset—assume the PROM internal

power-on-reset is always in step with the FPGA's internal power-on-reset. This may not be a safe assumption.

- The PROM $\overline{CE}$ input can be driven from either the $\overline{LDC}$ or DONE pins. Using $\overline{LDC}$ avoids potential contention on the D_{IN} pin.
- The $\overline{CE}$ input of the lead (or only) PROM is driven by the DONE output of the lead FPGA device, provided that DONE is not permanently grounded. Otherwise, $\overline{LDC}$ can be used to drive $\overline{CE}$, but must then be unconditionally High during user operation. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. The Xilinx PROMs have been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an FPGA. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function D_{IN} pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. The Xilinx FPGA families take care of this automatically with an on-chip default pull-up resistor.

Programming the FPGA With Counters Unchanged Upon Completion

When multiple FPGA-configurations for a single FPGA are stored in a PROM, the $\overline{OE}$ pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{OE}$ pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

This method fails if a user applies $\overline{RESET}$ during the FPGA configuration process. The FPGA aborts the configuration and then restarts a new configuration, as intended, but the PROM does not reset its address counter, since it never saw a High level on its $\overline{OE}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the FPGA is the master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and DONE goes High. However, the FPGA configuration will be completely wrong, with potential contentions inside the FPGA and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

Cascading Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded PROMs provide additional memory. After the last bit from the first PROM is read, the next clock signal to the PROM asserts its CEO output Low and disables its DATA line. The second PROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 2.

After configuration is complete, the address counters of all cascaded PROMs are reset if the FPGA $\overline{RESET}$ pin goes Low, assuming the PROM reset polarity option has been inverted.

To reprogram the FPGA with another program, the DONE line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of D_{IN}.

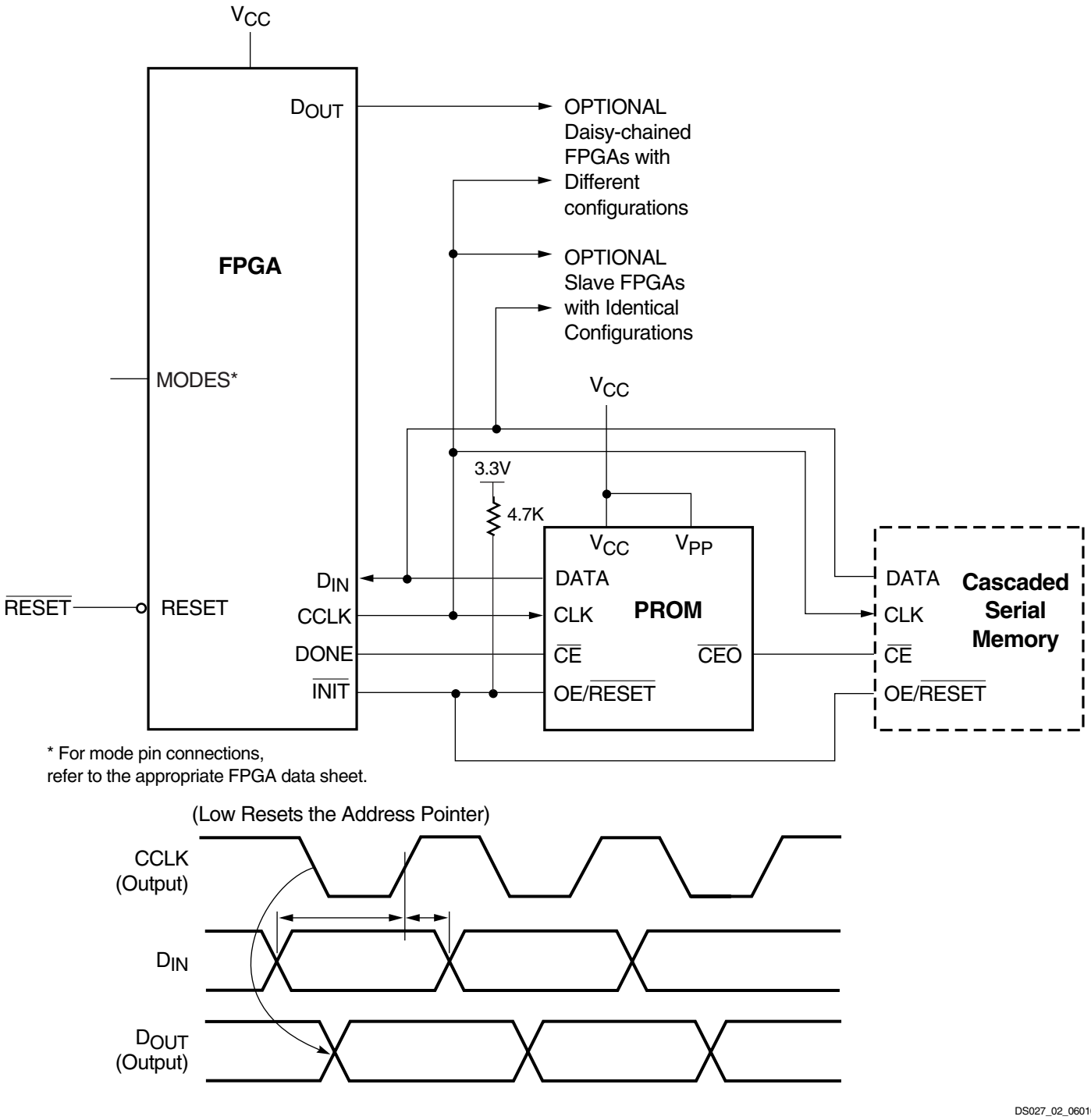


Figure 2: **Master Serial Mode.** The one-time-programmable PROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional FPGAs. An early DONE inhibits the PROM data output one CCLK cycle before the FPGA I/Os become active.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

Programming

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

Table 1: **Truth Table for XC1700 Control Inputs**

Control Inputs		Internal Address	Outputs		
RESET	**CE**		**DATA**	**CEO**	**I_{CC}**
Inactive	Low	If address ≤ TC(1): increment If address > TC(2): don't change	Active High-Z	High Low	Active Reduced
Active	Low	Held reset	High-Z	High	Active
Inactive	High	Not changing	High-Z	High	Standby
Active	High	Held reset	High-Z	High	Standby

Notes:
1. The XC1700 RESET input has programmable polarity
2. TC = Terminal Count = highest address value. TC + 1 = address 0.

XC1701, XC1736E, XC1765E, XC17128E and XC17256E

Absolute Maximum Ratings

Symbol	Description	Conditions	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{PP}	Supply voltage relative to GND	–0.5 to +12.5	V
V_{IN}	Input voltage relative to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to High-Z output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in.)	+260	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions (5V Supply)

Symbol	Description		Min	Max	Units
V_{CC}(1)	Supply voltage relative to GND (T_A = 0°C to +70°C)	Commercial	4.750	5.25	V
	Supply voltage relative to GND (T_A = –40°C to +85°C)	Industrial	4.50	5.50	V

Notes:
1. During normal read operation V_{PP} MUST be connect to V_{CC}.

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –4 mA)	Commercial	3.86	-	V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)		-	0.32	V
V_{OH}	High-level output voltage (I_{OH} = –4 mA)	Industrial	3.76	-	V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)		-	0.37	V
I_{CCA}	Supply current, active mode (at maximum frequency)		-	10	mA
I_{CCS}	Supply current, standby mode		-	50	µA
I_{CCS}	Supply current, standby mode (XC1701)		-	100	µA
I_L	Input or output leakage current		–10	10	µA
C_{IN}	Input capacitance (V_{IN} = GND, f = 1.0 MHz)		-	10	pF
C_{OUT}	Output capacitance (V_{IN} = GND, f = 1.0 MHz)		-	10	pF

XC1704L, XC1702L, XC1701L, XC17512L, XC1765EL, XC17128EL and XC17256EL

Absolute Maximum Ratings

Symbol	Description	Conditions	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{PP}	Supply voltage relative to GND	–0.5 to +12.5	V
V_{IN}	Input voltage relative to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to High-Z output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in.)	+260	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions (3V Supply)

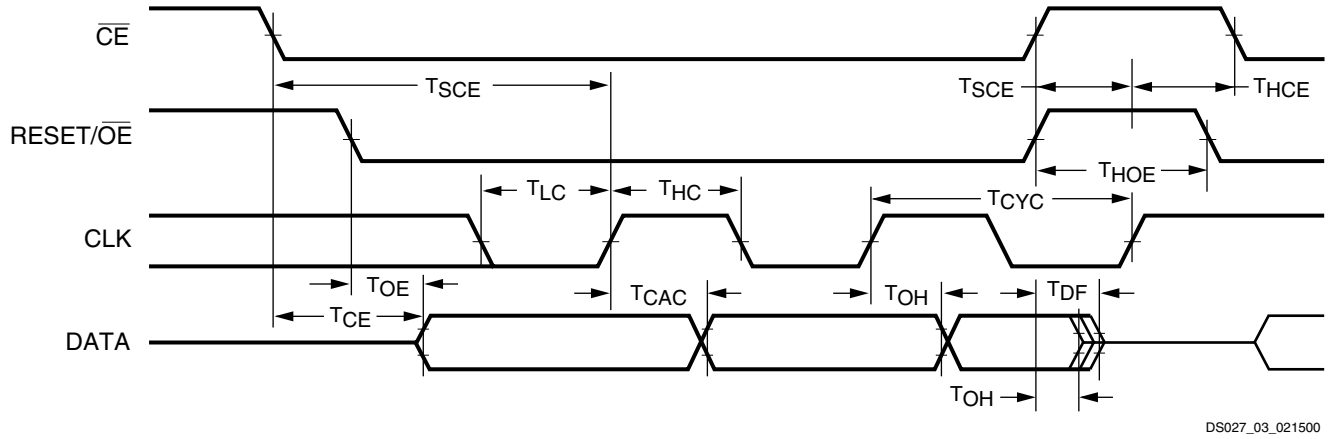
Symbol	Description		Min	Max	Units
V_{CC}(1)	Supply voltage relative to GND (T_A = 0°C to +70°C)	Commercial	3.0	3.6	V
	Supply voltage relative to GND (T_A = –40°C to +85°C)	Industrial	3.0	3.6	V

Notes:
1. During normal read operation V_{PP} MUST be connect to V_{CC}.

DC Characteristics Over Operating Condition

Symbol	Description	Min	Max	Units
V_{IH}	High-level input voltage	2	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –3 mA)	2.4	-	V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)	-	0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency) (XC1700L)	-	10	mA
I_{CCA}	Supply current, active mode (at maximum frequency) (XC1765EL, XC17128EL, XC17256EL)	-	5	mA
I_{CCS}	Supply current, standby mode (XC1701L, XC17512L, XC17256L, X1765EL, XC17128EL)	-	50	µA
I_{CCS}	Supply current, standby mode (XC1702L, XC1704L)	-	350	µA
I_L	Input or output leakage current	–10	10	µA
C_{IN}	Input capacitance (V_{IN} = GND, f = 1.0 MHz)	-	10	pF
C_{OUT}	Output capacitance (V_{IN} = GND, f = 1.0 MHz)	-	10	pF

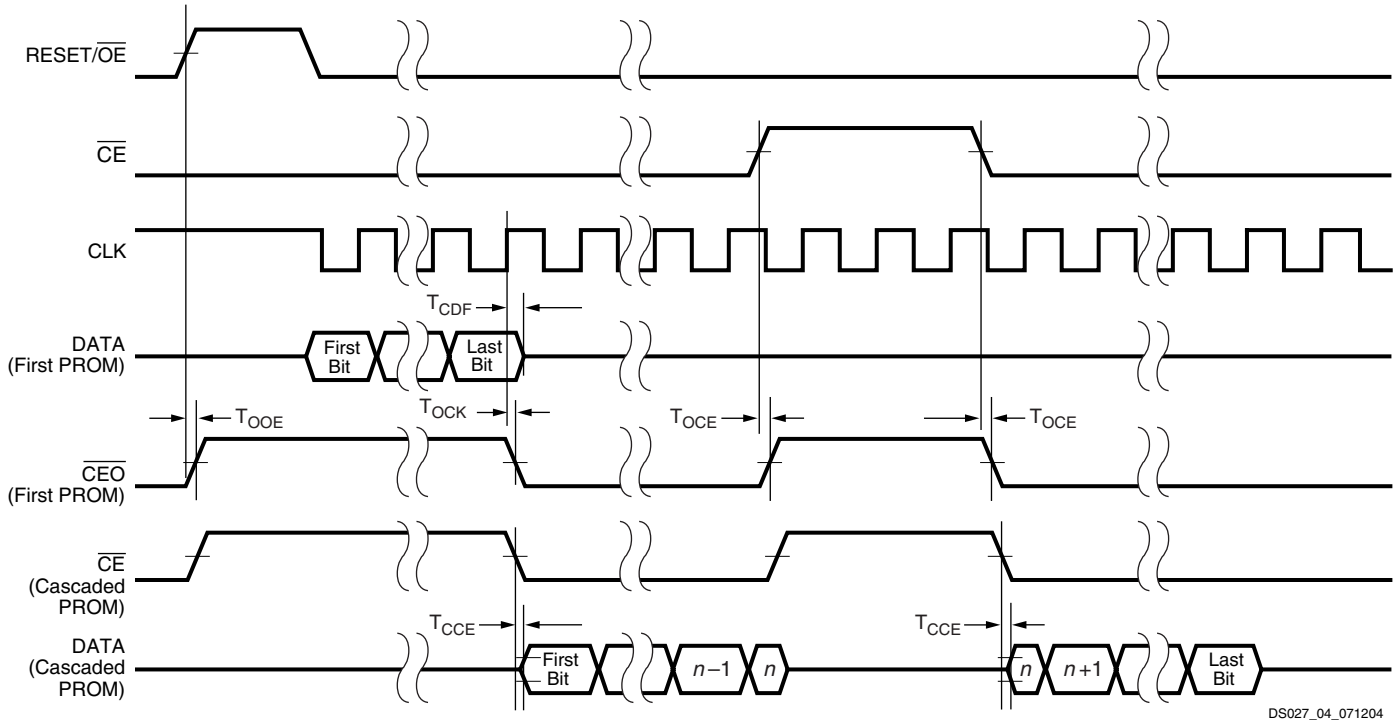
AC Characteristics Over Operating Condition



Symbol	Description	XC1701, XC17128E, XC17256E		XC17128EL, XC17256EL, XC1704L, XC1702L, XC1701L, XC17512L		XC1736E, XC1765E		XC1765EL		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{OE}	$\overline{OE}$ to data delay	-	25	-	30	-	45	-	40	ns
T_{CE}	$\overline{CE}$ to data delay	-	45	-	45	-	60	-	60	ns
T_{CAC}	CLK to data delay	-	45	-	45	-	80	-	200	ns
T_{DF}	$\overline{CE}$ or $\overline{OE}$ to data float delay(2,3)	-	50	-	50	-	50	-	50	ns
T_{OH}	Data hold from $\overline{CE}$, $\overline{OE}$, or CLK(3)	0	-	0	-	0	-	0	-	ns
T_{CYC}	Clock periods	67	-	67	-	100	-	400	-	ns
T_{LC}	CLK Low time(3)	20	-	25	-	50	-	100	-	ns
T_{HC}	CLK High time(3)	20	-	25	-	50	-	100	-	ns
T_{SCE}	$\overline{CE}$ setup time to CLK (to guarantee proper counting)	20	-	25	-	25	-	40	-	ns
T_{HCE}	$\overline{CE}$ hold time to CLK (to guarantee proper counting)	0	-	0	-	0	-	0	-	ns
T_{HOE}	$\overline{OE}$ hold time (guarantees counters are reset)	20	-	25	-	100	-	100	-	ns

Notes:
1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.

AC Characteristics Over Operating Condition When Cascading



Symbol	Description	XC1701, XC17128E, XC17256E, XC1704L, XC1702L		XC17128EL, XC17256EL, XC1701L, XC17512L		XC1736E, XC1765E		XC1765EL		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{CDF}	CLK to data float delay(2,3)	-	50	-	50	-	50	-	50	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3)	-	30	-	30	-	30	-	30	ns
T_{OCE}	CE to $\overline{CEO}$ delay(3)	-	35	-	35	-	35	-	35	ns
T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ delay(3)	-	30	-	30	-	30	-	30	ns
T_{CCE}	CE to data delay when cascading	-	45	-	90	-	60	-	110	ns

Notes:
1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. For cascaded PROMs:
   - T_{CYC} min = T_{OCK} + T_{CCE} + FPGA data setup time (T_{DCC}/T_{DSCK}).
     Example: If the XC1701L is cascaded to configure an FPGA T_{DCC} = 5 sec, then the actual T_{CYC} min = 30 ns + 90 ns + 5 ns = 125 ns, or max CLK frequency = 8 MHz.
   - T_{CAC} max = T_{OCK} + T_{CCE}.
     Example: For the XC1701L when cascading, the actual T_{CAC} max = 30 ns + 90 ns = 120 ns.

Ordering Information

XC1701L PC20 C

Device Number

XC1736E
XC1765E
XC1765EL
XC17128E
XC17128EL
XC17256E
XC17256EL
XC17512L
XC1701
XC1701L
XC1704L
XC1702L

Package Type

PD8=8-pin Plastic DIP
SO8=8-pin Plastic Small-Outline Package
VO8=8-pin Plastic Small-Outline Thin Package
SO20=20-pin Plastic Small-Outline Package
PC20=20-pin Plastic Leaded Chip Carrier
VQ44=44-pin Plastic Quad Flat Package
PC44=44-pin Plastic Chip Carrier

Operating Range/Processing

C=Commercial (T_A = 0° to +70°C)
I=Industrial (T_A = –40° to +85°C)

Valid Ordering Combinations

XC1736EPD8C	XC1765EPD8C	XC17128EPD8C	XC17256EPD8C	XC1701PD8C	XC1702LVQ44C
XC1736ESO8C	XC1765ESO8C	XC17128EVO8C	XC17256EVO8C	XC1701PC20C	XC1702LPC44C
XC1736EVO8C	XC1765EVO8C	XC17128EPC20C	XC17256EPC20C	XC1701SO20C	XC1704LVQ44C
XC1736EPC20C	XC1765EPC20C	XC17128EPD8I	XC17256EPD8I	XC1701PD8I	XC1704LPC44C
XC1736EPD8I	XC1765EPD8I	XC17128EVO8I	XC17256EVO8I	XC1701PC20I	XC1702LVQ44I
XC1736ESO8I	XC1765ESO8I	XC17128EPC20I	XC17256EPC20I	XC1701SO20I	XC1702LPC44I
XC1736EVO8I	XC1765EVO8I				XC1704LVQ44I
XC1736EPC20I	XC1765EPC20I				XC1704LPC44I
	XC1765ELPD8C	XC17128ELPD8C	XC17256ELPD8C	XC1701LPD8C	XC17512LPD8C
	XC1765ELSO8C	XC17128ELVO8C	XC17256ELVO8C	XC1701LPC20C	XC17512LPC20C
	XC1765ELVO8C	XC17128ELPC20C	XC17256ELPC20C	XC1701LSO20C	XC17512LSO20C
	XC1765ELPC20C	XC17128ELPD8I	XC17256ELPD8I	XC1701LPD8I	XC17512LPD8I
	XC1765ELPD8I	XC17128ELVO8I	XC17256ELVO8I	XC1701LPC20I	XC17512LPC20I
	XC1765ELSO8I	XC17128ELPC20I	XC17256ELPC20I	XC1701LSO20I	XC17512LSO20I
	XC1765ELVO8I				
	XC1765ELPC20I				

Marking Information

Due to the small size of the commercial serial PROM packages, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows:

1701L J C

Device Number

1736E
1765E
1765X(1)
17128E
17128X(1)
17256E
17256X(1)
1704L
1702L
1701
1701L
17512L

Package Type

P=8-pin Plastic DIP
S(2)=8-pin Plastic Small-Outline Package
V=8-pin Plastic Small-Outline Thin Package
S(3)=20-pin Plastic Small-Outline Package
J=20-pin Plastic Leaded Chip Carrier
VQ44=44-pin Plastic Quad Flat Package
PC44=44-pin Plastic Chip Carrier

Operating Range/Processing

C=Commercial (T_A = 0° to +70°C)
I=Industrial (T_A = –40° to +85°C)

Notes:
1. When marking the device number on the EL parts, an X is used in place of an EL.
2. For XC1700E/EL only.
3. For XC1700L only.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
7/14/98	1.1	Major revisions to include the XC1704L, XC1702L, and the XQ1701L devices, packages and operating conditions. Also revised the timing specifications on page 10.
9/8/98	2.0	Revised the marking information for the VQ44. Updated **DC Characteristics Over Operating Condition**, page 8 and page 9. Added references to the XC4000XLA and XC4000XV families in **Xilinx FPGAs and Compatible PROMs**, page 4 and Figure 2, page 6.
12/18/98	2.1	Added Virtex FPGAs to **Xilinx FPGAs and Compatible PROMs**, page 4. Added the PC44 package for the XC1702L and XC1704L products.
1/27/99	2.2	Changed Military I_{CCS}.
7/8/99	2.3	Changed I_{CCS} standby on XC1702/XC1704 from 50 µA to 300 µA.
3/30/00	3.0	Combined data sheets XC1700E and XC1700L. Added DS027, removed Military Specs. Added Virtex-E and EM references.
07/05/00	3.1	Added 4.7K resistor to Figure 2, updated format.
09/07/04	3.2	• Updated **Xilinx FPGAs and Compatible PROMs**, page 4 and **Absolute Maximum Ratings**, page 8. Added **Pinout Diagrams**, page 3. • Added footnote to table in **AC Characteristics Over Operating Condition When Cascading**, page 11, defining T_{CCE} when cascading, and redrew associated timing diagram.