PRODUCT BRIEF
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WinPath2

WINPATH2™ NEXT GENERATION ACCESS PACKET PROCESSOR

Highlights

- **Next generation of access processors providing 2x the performance and more integration than original WinPath family**
- **Royalty free "production hardened" data path software supporting over 40 protocols is included, plus C language API for rapid integration into high performance telecom systems**
- **RAM based Data Path code store to facilitate evolving standards in wireline, wireless, VoP, and multi-service designs**
- **Custom programming available via rich suite of development tools plus extensive library of source code and example programs**
- **Numerous WAN and LAN interfaces are supported including 24 Fast Ethernet, 4 Gigabit Ethernet, multiple OC3/OC12/OC48 ATM and SPI-3/POS level 2 interfaces**
- **Growing list of available protocols including PWE3, IMA, Header Compression, Security Processing, and a wide variety of interworking scenarios**
- **Wide range of bus interfaces available including PowerPC™ 60x, PCI 2.2**
- **Highly flexible integrated memory controllers support DDR1, DDR2, SDRAM, ZBT SRAM, ASRAM, all with ECC**

WinPath2 - Next Generation Access Processing

Wintegra's latest access processor, WinPath2, offers a complete solution to protocol handling in the wireline and wireless access infrastructure equipment market. WinPath2 extends the successful Wintegra formula for access designs to a higher level of performance. It incorporates an integrated high performance control path processor with a fully programmable RAM based data path processor while leveraging the broad set of supplied protocols developed for WinPath1. These protocols include support for IP, Ethernet, TDM, ATM, Frame Relay, and emerging standards like PWE3 and WT-101. Wintegra supplies these production hardened protocols with the silicon, with no NRE or royalties. WinPath2 performs termination, routing, bridging, switching, protocol conversion and interworking between any input stream to any output stream at wire speeds from 64 Kbps voice channels to 4 Gbps Ethernet connectivity. WinPath2 is designed for easy migration from WinPath1, while providing powerful new capabilities that allows designers to create the next generation of access systems with a

minimum of design risk, short time to market and low cost. WinPath2 provides greater performance than WinPath1 by utilizing 6 data processing elements (WinGines) at 350 MHz each, plus new high-speed memory interfaces. WinPath2 also provides new hardware accelerators, such as an integrated security engine, hierarchical shaping, deep packet classification, intrusion detection, content searching and more. At the same time, Wintegra maintains the commitment to low power consumption and a low system cost that make the WinPath2 the best choice for access class designs.

Control Plane Processing

An integrated, high performance general-purpose MIPS 24K processor provides the control path software processing for high-end access designs. This block is a licensed core, so standard 3rd party tools such as compiler, assemblers and EJTAG devices are fully compatible. The clock for the MIPS core is decoupled from the data path processors to better tune the system-wide control processing.

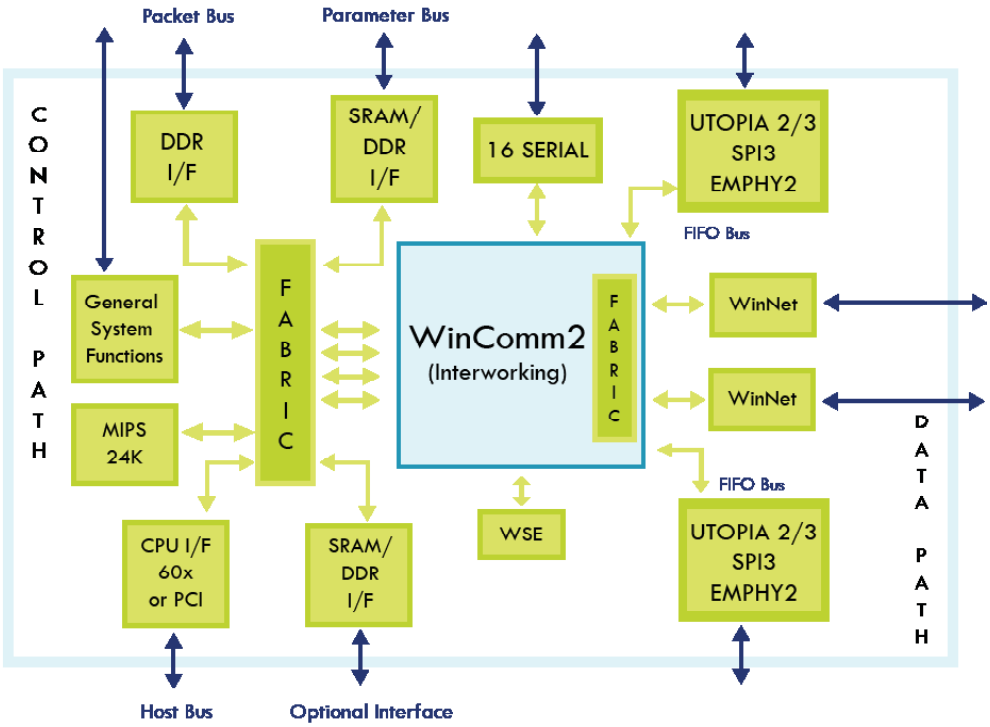
Data Path Processing (WinComm2)

A sophisticated multi-core communication engine with a large program RAM provides superior overall processing power plus scalability and flexibility. Being RAM based, WinComm2 can be software upgraded as protocols evolve and standards change. Original WinPath1 protocols are supported, plus new protocols that take advantage of WinPath2 specific features. The number of processing cores (WinGines) is increased in WinPath2 to six. Unlike traditional network processors or other micro-coded solutions, where protocol software is located in ROM or partitioned into small, segmented micro-blocks, the WinPath2 DPS runs from a large shared memory space, increasing flexibility and performance. This means code doesn't require prior partitioning, coherency, or order management between engines, these are handled internally through special hardware at run time.

Industry Standard Interfaces

Numerous, highly flexible Ethernet options are available. Up to 24 10/100 Ethernet ports or 4 Gigabit ports can be utilized at the same time. Additionally, 16 TDM ports support T1/E1 or T3/E3 connectivity. Two UTOPIA/POS L2/L3 ports are also available. The POS ports support SPI-3 as well. A 64-bit, 66 MHz PCI 2.2 bus is available, plus a 60x compatible PowerPC bus interface. Wintegra offers complete software packages enabling any-port-to-any-port routing, bridging, switching and interworking with these various interfaces.

WinPath 2



High Performance/Cost Effective Memory Support

WinPath2 provides bus interfaces and memory controllers to support popular high performance, low cost memories like DDR1/DDR2, SDRAM, and SRAM. These memory controllers provide transaction optimization, auto alignment support, out of order transaction support, efficient bus utilization, and guaranteed low latency cycles which enables application level quality-of-service. On chip Error Checking and Correction (ECC) algorithms support all internal as well as external memories.

Security Acceleration Hardware

WinPath2 adds powerful security processing that supports up to 1 Gbps data encryption and authentication with a variety of cryptographic engines such as AES, 3xDES, Kasumi and H-MAC (SHA-1 and MD5). The WinPath2 Security Engine (WSE) eliminates the need for inefficient external security devices in the wireless and wireline access systems. Packet forwarding, protocol processing, and security tasks can be executed on each data quantum on the fly (even simultaneously). While a specific data unit traverses from on-chip network interfaces to external memory storage, the innovative WinPath2 thread processing architecture allows multiple hardware elements to process the same data unit. In this way, security tasks are performed as an integrated component of the protocol data processing and data forwarding. With this on-chip security processing, the WinPath2 can provide higher levels of overall system bandwidth while maintaining lower system cost and design complexity.

Feature Summary:

RISC Control Processor (Optionally Disabled)
More than 2x the performance (compared to original WinPath series)
MIPS 24Kc @ 600 MHz
MIPS core and WinComm2 may run at different frequencies
32-bit address, 64-bit data path to caches and external interfaces
8-stage pipeline

Data Path (WinComm2):
More than 2x the performance of original WinPath family (at 200 MHz)
6 WinGines @ 350 MHz
Application level-backwards compatibility with WinPath1
Large DPS program RAM

Bus and Memory Interfaces:
PCI 2.2 interface, 32 and 64-bit, 66 MHz, supports target or initiator mode, programmable burst sizes, arbitration logic supports up to three external initiators
Three optional memory interfaces (Packet, Parameter and Application) supporting up to 200 MHz DDR1 and DDR2 SDRAM/SRAM. Supports industry standard DDR1 and DDR2, and ASRAM, devices.
PPC 60x compatible bus
ECC is supported on all memories, both internal and external

Serial interfaces:
4 Gigabit Ethernet Ports or 24 Fast Ethernet ports supporting MII, RMII, GMII, RGMII, TBI, RTBI, SMII. Varying configurations are possible from 4 GE ports and no 10/100 versions to 24 10/100 and no GE. RMON MIBs are supported as well as jumbo frames.
Two UTOPIA-2/3 or POS interfaces supporting up to 104 MHz operation. UTOPIA ports offer master or slave mode. Each port supports OC-48, or 4 OC-12/STM-4 interfaces, or 4 OC-3/DS-3/E3 interfaces or up to 188 low speed devices such as xDSL framers or DSPs
Sixteen serial TDM interfaces supporting T3, E3, T1, E1, J1, or other serial interfaces up to 50 MHz. Built-in support for ATM Transmission Convergence. Through on-chip Time-Division Multiplex machine, supports fractional ATM, HDLC and Transparent modes

New hardware accelerators
Special Hardware for Hierarchical Shaping. Shaping support by cells, packet or byte count. WinPath2 supports 5 level shaping through mix of hardware and software. Shaping capabilities for WRR, fixed priority, min/max rate limit.
Integrated Security Engine (WSE). Support for Confidentiality Acceleration (DES, 3DES, AES, Kasumi F-8). Also supports Authentication Acceleration (HMAC, AES, Kasumi F-9)
TDI Clock Recovery circuitry for the 16 TDI ports.
Deep Packet Classification, Intrusion detection and Content Searching
Programmable CRC machines

Electrical:

0.13 Micron technology

Low power consumption, 6W or less

3.3V and 2.5/1.8V I/O, 1.2V internal

Market Tuning:

Customization of Serial and Pin Muxing Configurations

WinPath2 can be optimized for different market segments and offers a flexible (programmable) serial configuration pin muxing. Customers choose, and pay for, only the elements they need. This means no unnecessary redundancies and no unused capability. Some examples of the available configurations are listed bellow:

- DSL: 4 GigE + 2 POS-PHY2 192 phys
- PON: 1 UTOPIA level 3 + 16 Fast Ethernet + 6 TDM
- PON: 1 UTOPIA level 3 + 1 UTOPIA Level-2 + 6 TDM
- Multi service Access (MSA): 1 SPI-3 + 12 Fast Ethernet
- Multi service Access (MSA): 1x SPI-3 + 2 GigE
- Wireless transport: 2 GigE + 1 UTOPIA Level-2
- Wireless Access: 2 GigE + TDM

HFC-BGA 1020 pin

Protocols Supported by Standard DPS/WDDI:

Traffic Management for ATM	TM4.1 UBR, CBR, GFR, VBR Hierarchical shaping (up to 5 levels) Policing Single/Dual Leaky Bucket Congestion Control (EPD/PPD) Per VC Queuing
Traffic Management for Packet Interfaces	Hierarchical shaping WFQ Policing Single/Dual Leaky Bucket Congestion Control (WRED/TD) Per Flow Queuing
Quality of Service/ Classes of Service	Multiple Priority Levels on all interfaces Multiple flows per VC Strict or WRR priorities Up to 64K queues Buffer Management Diffserv Three Color Marking Deep packet classification (L2/3/4) Unanchored strings search anywhere in the packet header/payload Intrusion Detection Flexible Statistics Collection and Reporting implemented in software Multi-channel back-pressure over packet backplane interfaces (POS and Ethernet)
Layer 1 Interfaces	UTOPIA – L2/3 POS – L2 SPI-3 10/100/1000 Ethernet T1/E1/J1/SDSL/T3/E3 ADSL2+/VDSL2 (selectable per PHY) Channelized OC12 (8064 DS0) supporting Any Service over Any Port

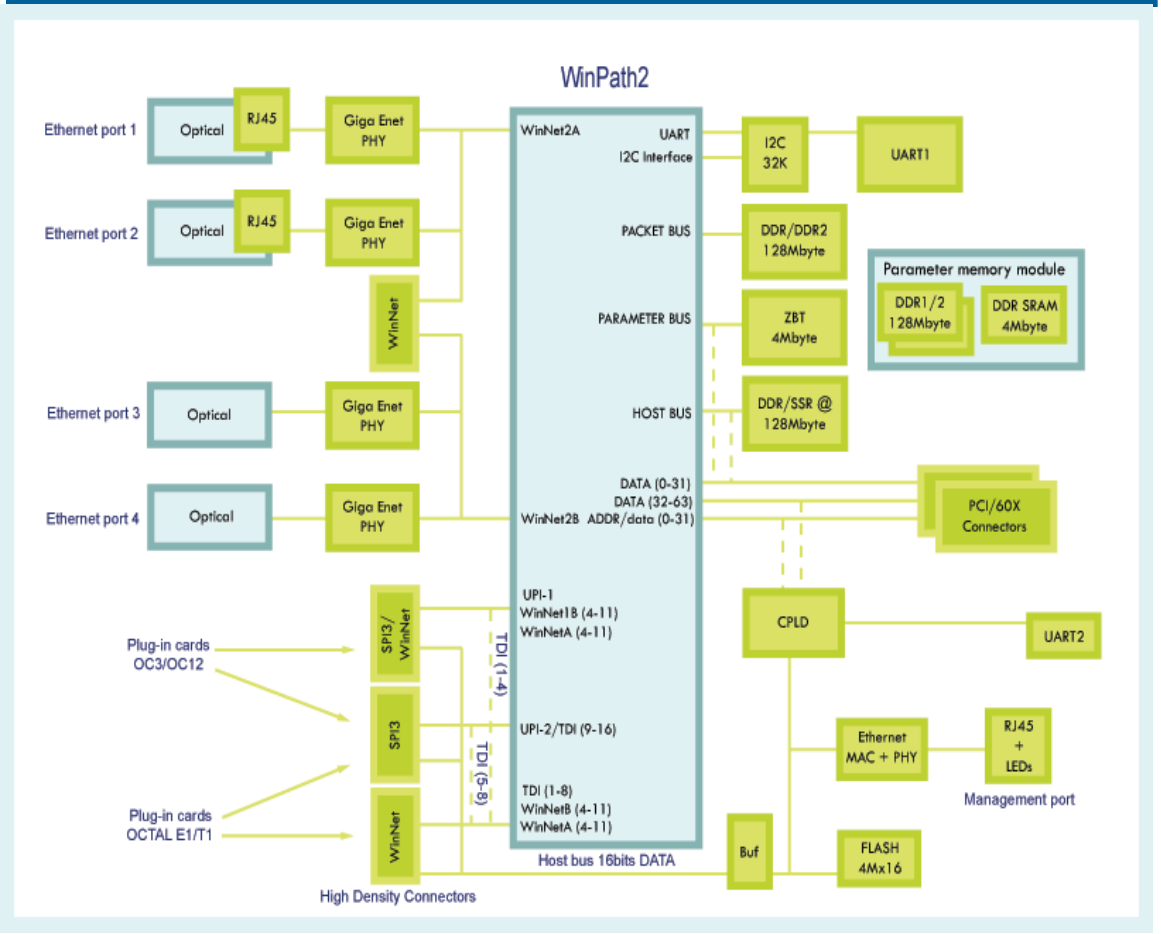
Protocols Continued:

Aggregation	IMA Multi-Link PPP Multi-Class PPP PPP Mux Multi-Link Frame Relay ATM G.Bond (G.998.1) Ethernet G.Bond (G.998.2) Ethernet Link Aggregation (802.3ae)
Encapsulation	RFC1483/2684/1577 PPPoA PPPoE PPPoEoA 802.1ad Q-in-Q 802.1ah MAC-in-MAC GRE GTP L2TP
Layer 2	ATM AAL0/1/2(CPS, SSSAR, SSTED)/5 ATM OAM/F4/F5 Ethernet Ethernet OAM PPP HDLC FR
Layer 2 Switching	Ethernet switch 802.1Q tag switching AAL2 CPS switch ATM cell switch FR switch
Layer 2 Bridging	Supports Bridging between Ethernet, ATM, PPP, FR VLAN aware or Transparent Support for multicast, flooding, address learning and aging ATM VC to 802.1Q Tag Mapping

Protocols Continued:

Layer 2 and above Interworking	CES Structured and Unstructured IPv4 to IPv6 translation HDLC to ATM AAL2 CPS to packet Interworking AAL2 SSSAR to packet interworking AAL0 to packet interworking FR to ATM interworking iTDM PWE3: TDM (SAToP, CESoPSN), ATM, HDLC
Layer 2.5	MPLS

Wintegra Development System2



Wintegra Development System2 (WDS2)

Wintegra offers a WinPath2 Development system similar to the one offered for WinPath1. New serial cards are available for the WDS2 board including:

- 16 10/100 port board
- OC48 with SPI-3/UL3 (32 bit)
- Octal T1/E1
- OC12
- Quad OC3
- UFE3

Board support packages for Linux and WindRiver VxWorks are available. Schematics, BOM, and example code are all available from Wintegra.

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For more information, see www.wintegra.com

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