Datasheet

VSC8025/VSC8026

2.488 Gb/s ATM/SDH/SONET STM-16/STS-48 Mux/Demux and Section Terminator IC Chipset

Features

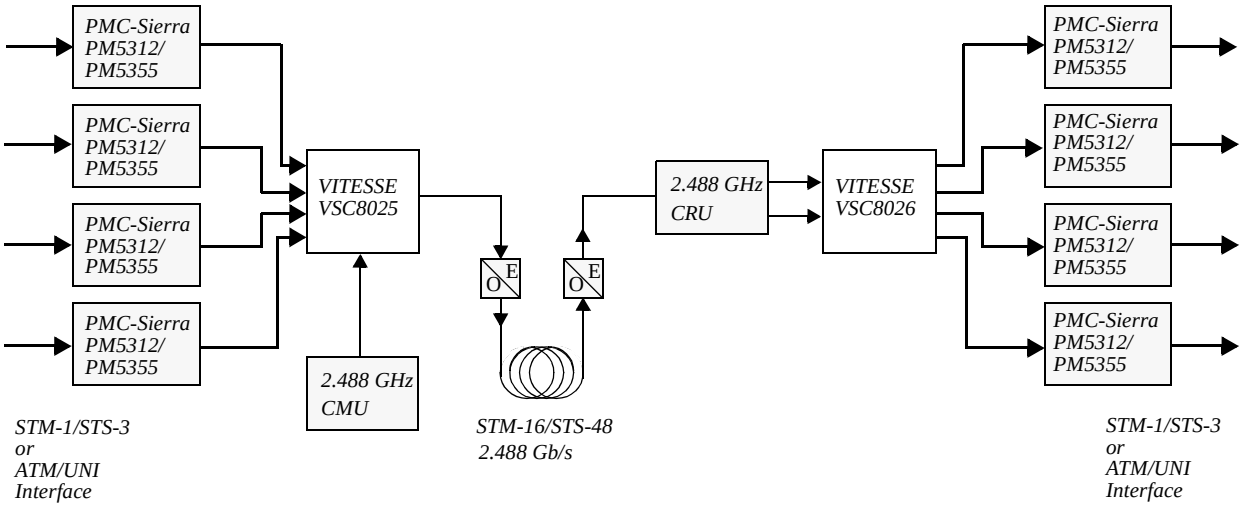
VSC8025 (MUX)

- SDH/SONET compliant multiplexing of four byte-wide STM-4/STS-12 data streams into one serial STM-16/STS-48 data stream
- Frame Synchronous Scrambling (optional)
- B1 Calculation and Insertion (optional)
- J0/Z0 Section-Trace Insertion (optional)
- Supports Contra- & Co-directional Timing
- Supports STS-48c Multiplexing
- Provides Equipment And Facility Loopbacks
- Dual Supply Operation -2, +3.3 Volts
- 192 TBGA Package

VSC8026 (DEMUX)

- SDH/SONET compliant demultiplexing of one serial STM-16/STS-48 data stream into four byte-wide STM-4/STS-12 data streams
- Frame Acquisition
- Frame Synchronous Descrambling (optional)
- B1 Error Reporting
- SEF/LOF Alarm Generation
- Supports STS-48c Demultiplexing
- Provides Equipment And Facility Loopbacks
- Dual Supply Operation -2, +3.3 Volts
- 192 TBGA Package

System Block Diagram



General Description

The VSC8025/VSC8026 chipset is designed to provide a SDH/SONET compliant interface between the PM5312 STTX (STM-1/STS-3 to STM-4/STS-12 mux/demux) or the PM5355 S/UNI-622 User Network Interface device and a SDH/SONET compliant 2.488 Gb/s interface, as depicted in the system block diagram above. This chipset allows one to create an ATM-UNI or STM-1/STS-3 to STM-16/STS-48 link. Both the mux (VSC8025) and the demux (VSC8026) are packaged in a 192 TBGA for optimum high-speed package performance. The VSC8025/VSC8026 chipset provides an integrated solution for ATM physical layers, SDH/SONET transmission systems, digital-video distribution systems, and SDH/SONET test equipment.

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2.488 Gb/s ATM/SDH/SONET STM-16/STS-48
Mux/Demux and Section Terminator IC Chipset

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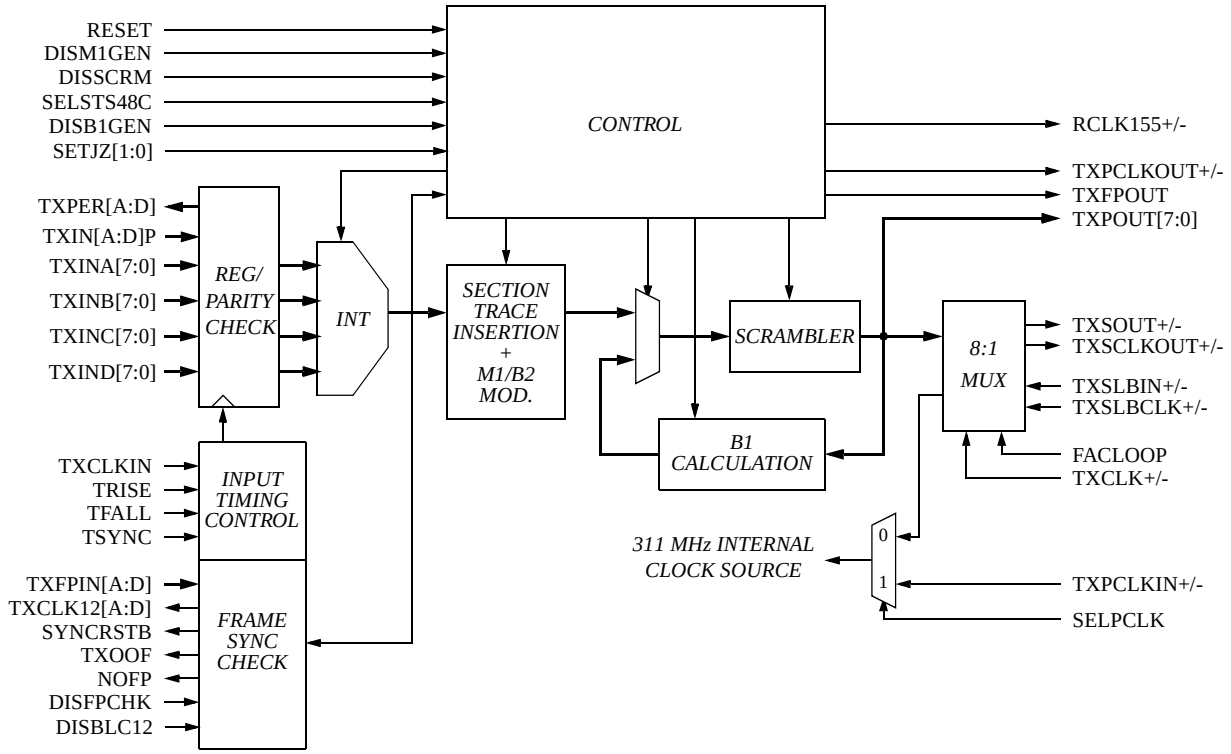
VSC8025 Functional Description

The VSC8025 multiplexer serializes four byte-wide STS-12/STM-4 data streams into a 2.488 Gb/s serial STS-48/STM-16 data stream and generates selected transmission frame section overhead bytes. The VSC8025 performs B1 calculation, scrambling and section-trace insertion. A functional block diagram of the VSC8025 is shown in Figure 1.

The part is clocked by a 2.488 GHz clock, which has to be provided by an external source to TXCLK. The VSC8025 is equipped with a 155.52 MHz differential ECL output clock, RCLK155, to facilitate the creation of an external PLL circuit. Byte-wide data is presented to the TXINA[7:0], TXINB[7:0], TXINC[7:0] and TXIND[7:0] input ports (e.g. originating from four PM5312/PM5355s) and is captured on the rising edge of TXCLKIN (refer to Figure 6). Each of the four PM5312/PM5355s output a frame pulse aligned to the first payload byte of every frame, as shown in the functional timing diagram, Figure 2. These frame pulses are connected to TXFPIN[A:D] and are used for verifying that the four STS-12/STM-4 input data streams are synchronized (refer to Input Synchronization below). TXFPIN[A:D] is captured on the rising edge of TXCLKIN. The four STS-12/STM-4 data streams are byte-interleaved consistent with existing requirements for SONET/SDH intermediate level multiplexing. Section-trace bytes, J0/Z0, and Section Error Performance byte, B1, are inserted, the data stream is scrambled and serialized. The serial STS-48/STM-16 data stream is presented at the differential output, TXSOUT, on the falling edge of TXSCLKOUT+ (refer to Figure 7).

Figure 1: VSC8025 Functional Block Diagram



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Input Synchronization

The four STS-12/STM-4 input data streams must be frame-aligned prior to being fed into the VSC8025. The frame pulses TXFPIN[A:D] (active high) associated with each of the four STS-12/STM-4 data streams are used to initiate and verify the frame-synchronization. These frame pulses must be aligned with the first payload byte of the STS-12/STM-4 frames. The byte-interleave mux will be reset on the occurrence of the first valid frame pulse on TXFPIN[A:D]. A valid frame pulse will only be detected if all four TXFPIN[A:D] inputs are high at the same time. In the event that TXFPIN[A:D] are not exactly aligned to each other, a 'reset sequence' will be generated by the VSC8025 to re-synchronize the four STS-12/STM-4 input frames (refer to Synchronous Reset Timing Diagram, Figure 3). The 'reset sequence' is designed specifically to a setup where the four STS-12/STM-4 inputs are being driven from four PM5312/PM5355s. SYNCRSTB is asserted low for sixteen 77.76 MHz (TXCLK12) clock cycles. TXCLK12 outputs will be held low (blocked) during these sixteen cycles and for an additional sixteen cycles thereafter if DISBLC12 is low, if DISBLC12 is high TXCLK12 outputs are not blocked. TXOOF will be held high for sixteen TXCLK12 cycles after the TXCLK12 clocks start running again to indicate that the CPU needs to reload the registers in the four PM5312/PM5355s. The 'reset sequence' circuitry can be disabled by asserting the asynchronous DISFPCHK input high. Once a valid frame pulse has been detected, the VSC8025 performs additional frame alignment checks with the results indicated on output NOFP. When DISFPCHK is set to logic "0", NOFP goes high to indicate mis-alignment between the VSC8025 internal frame counter and a valid frame pulse (TXFPIN[A:D] = 1). NOFP will go high for minimum of 13.4uS for this mis-alignment condition. When NOFP occurs, frame synchronization can only be established by resetting the VSC8025. The VSC8025 will re-establish frame synchronization on the next valid frame pulse following the reset. Typically, some external controller, operating off a clock which is not derived from the VSC8025, should monitor NOFP and perform the appropriate reset when detected. When DISFPCHK is set to logic "1", NOFP behaves as described above with the exception that NOFP will go high if any of the four frame pulses is missing when expected.

Input Timing Modes

There are two methods for driving TXCLKIN (clock signal associated with the byte-wide STS-12/STM-4 input ports). The first method, referred to as contra-directional, simply drives the input clock TXCLKIN and the PMC devices (PM5312 or PM5355) using the output clock TXCLK12A. In this mode, there is a maximum delay bound between the TXCLK12 output and the TXCLKIN input (see Figure 5). The second method, referred to as co-directional, uses an externally generated 77.76 MHz source to drive TXCLKIN; TXCLK12s can be used. This mode assumes no phase-relation between the TXCLKIN input and the TXCLK12 outputs (contrary to contra-directional timing mode - see Figure 5), but does assume a frequency lock to the 2.5GHz (serial) or 311MHz (parallel) clock.

In co-directional mode, internal clocking is adjusted to the external clock TXCLKIN shortly after a RESET; and, if enabled, shortly after a rising edge on the TSYNC input. Input data may be missed during a clock adjustment, so the frequency of updates should be kept low. See Table 2 to determine pin connections for input data clocking modes (also reference Figure 4 and Figure 5, and application notes)

Equipment Loopback

The VSC8025 is equipped with a parallel output port which can be used for an equipment loopback by connecting it to the parallel STS-48/STM-16 input port on the VSC8026. This port can also be used to feed an STS-192/STM-64 MUX. TXFPOUT contains a frame pulse synchronized with the parallel STS-48/STM-16

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data stream. This frame pulse is aligned with the first payload byte in every STS-48/STM-16 frame. Data on TXPOUT[7:0] and TXFPOUT is clocked out on the rising edge of TXPCLKOUT+ (refer to Figure 9).

When only the parallel STS-48/STM-16 output port is used, e.g. when the VSC8025 is used to feed an STS-192/STM-64 MUX, the VSC8025 does not have to be supplied with a 2.488 GHz clock, since the serial output mux is not used. Instead, a 311.04 MHz clock can be provided on the TXPCLKIN differential ECL input pins. The asynchronous SELPCLK input needs to be held high to select the TXPCLKIN clock source. Refer to Figure 21 for a detailed equipment loopback diagram.

Facility Loopback

To create a facility (or line) loopback, the VSC8025 is equipped with a high-speed clock (TXSLBCLK) and data (TXSLBIN) input. TXSLBIN is captured on the falling edge of TXSLBCLK+ (refer to Figure 8) and clocked out through the TXSOUT port on the falling edge of TXSCLKOUT+ (refer to Figure 7), when the asynchronous FACLOOP input is held high. Refer to Figure 21 for a detailed facility loopback diagram.

STS-48c Mode

To support STS-48c operation, where bytes from the four STS-12/STM-4 inputs are interleaved on at a time (as opposed to four at a time in STS-48 mode), the byte interleaver can be configured for STS-48c multiplexing by holding the asynchronous SELSTS48C input high.

Scrambler

The VSC8025 performs optional scrambling using a frame synchronous scrambler with generating polynomial $1 + x^6 + x^7$ and a sequence length of 127. The scrambler is disabled by asserting input DISSCRM high. DISSCRM is latched-in once every frame by a valid frame pulse.

Error Performance (B1)

The bit interleaved parity byte B1 is calculated over the entire scrambled STS-48/STM-16 frame and inserted into the B1 location of the next frame before scrambling. The B1 generation can be disabled by setting DISB1GEN input high. DISB1GEN is latched-in once every frame by a valid frame pulse.

Section-Trace Insertion (J0/Z0)

The section-trace bytes (J0/Z0) can optionally be filled by setting the SETJZ[1:0] as indicated in Table 1. When SETJZ[1:0] is held at ‘00’, the J0/Z0 bytes will be passed on transparently. For SETJZ[1:0] at ‘01’ an increasing binary value of 01\hex to 30\hex fill the J0/Z0 bytes. Since the first section-trace byte J0 could carry a section-trace message it can be passed on transparently while the Z0 bytes are set to an increasing binary number from 02\hex to 30\hex by setting SETJZ[1:0] to ‘10’. The last mode SETJZ[1:0] = ‘11’ allows for a transparent J0 byte and CC\hex filled Z0 bytes.

M1/B2 Modification

When multiplexing four STS-12/STM-4 SONET/SDH frames into one STS-48/STM-16 frame, the M1 byte of the outgoing STS-48/STM-16 frame must be calculated from the four M1 bytes contained in the STS-12/STM-4 frames. The VSC8025 extracts the M1 bytes from the four STS-12/STM-4 input frames, adds them together (and truncates to 255, if the sum is larger), and inserts the result in the M1 byte of the STS-48/STM-16

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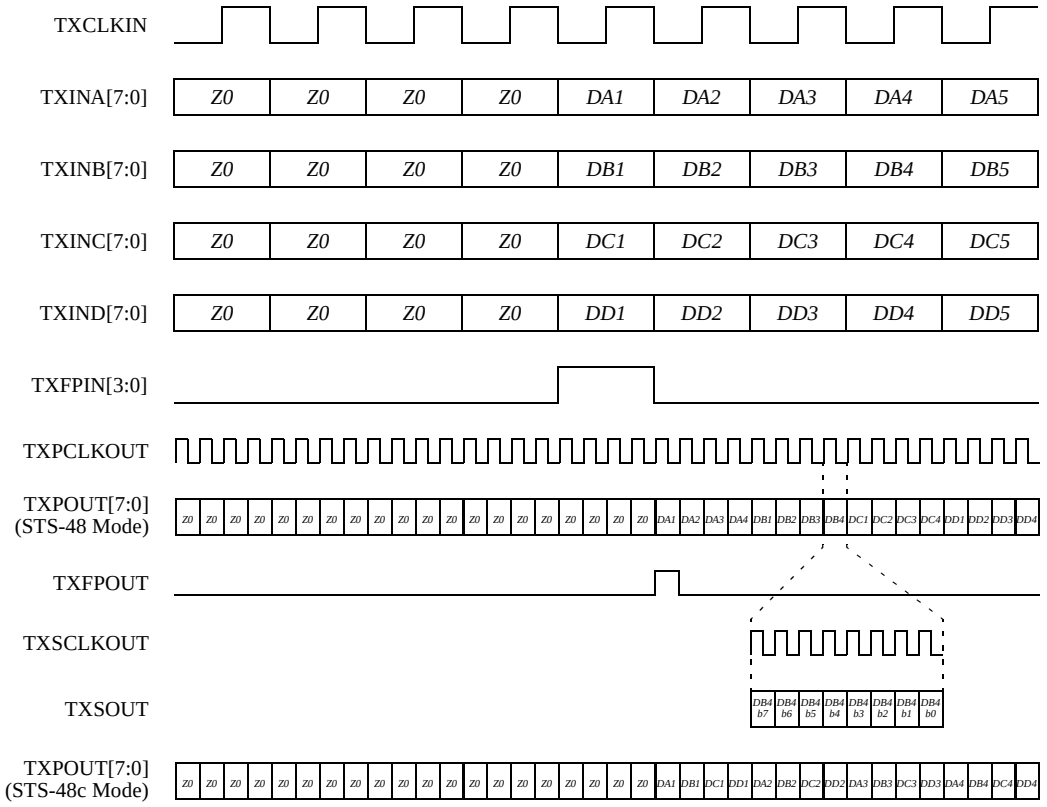
frame. The M1 bytes of the STS-12/STM-4 frames are simultaneously nulled (00\hex is inserted). The errors introduced into the B2 bytes by this M1 modification are also corrected.

The M1/B2 circuitry can be disabled by holding the asynchronous input DISM1GEN high.

Parity

An even parity input is provided for each byte wide data bus and respective frame pulse on TXIN[A:D]P. The parity inputs are captured on the rising edge of TXCLKIN and compared with parity calculated internally. Any resulting errors are clocked out by TXCLKIN on TXPER[A:D]. Parity errors are reported one cycle delayed from input data. For no parity errors to result, the parity input for the bus must be logic 1 when an odd number of bits in the byte wide data and frame pulse are logic 1; otherwise, it must be logic 0.

Figure 2: VSC8025 Functional Timing Diagram



Note:

(1) The correct latency between TXINA-D, TXPOUT and TXSOUT is NOT shown.

(2) TXPOUT is equivalent to TXSOUT (byte wide). TXFPOUT is not applicable to serial output TXSOUT.

(3) MSB leads on TXSOUT; MSB is bit 7 on the TXINA-D inputs and TXPOUT outputs.

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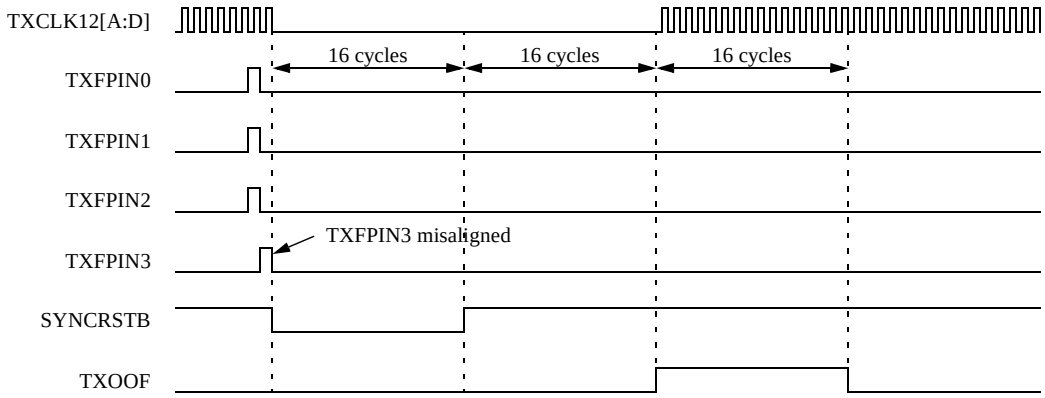
Figure 3: VSC8025 Synchronous Reset Timing Diagram



Note: DISFPCHK = DISBLC12 = logic '0'.

Table 1: VSC8025 Section-Trace Insertion Select Settings

SETJZ[1]	*SETJZ[0]*	*Function*
0	0	Transparent
0	1	01\hex-30\hex
1	0	J0 Transparent, Z0:02-30\hex
1	1	J0 Transparent, Z0:CC\hex

Table 2: VSC8025 Input Timing Mode Select Settings

Mode	*TRISE*	*TFALL*	*TSYNC*	*TXCLKIN*
Contra-Directional	0	0	0	TXCLK12
Co-Directional Adjust clock only after RESET	1	1	0	External 77.76 MHz signal
Co-Directional Adjust clock after RESET and after rising edge on TSYNC	1	0	External Signal	External 77.76 MHz signal

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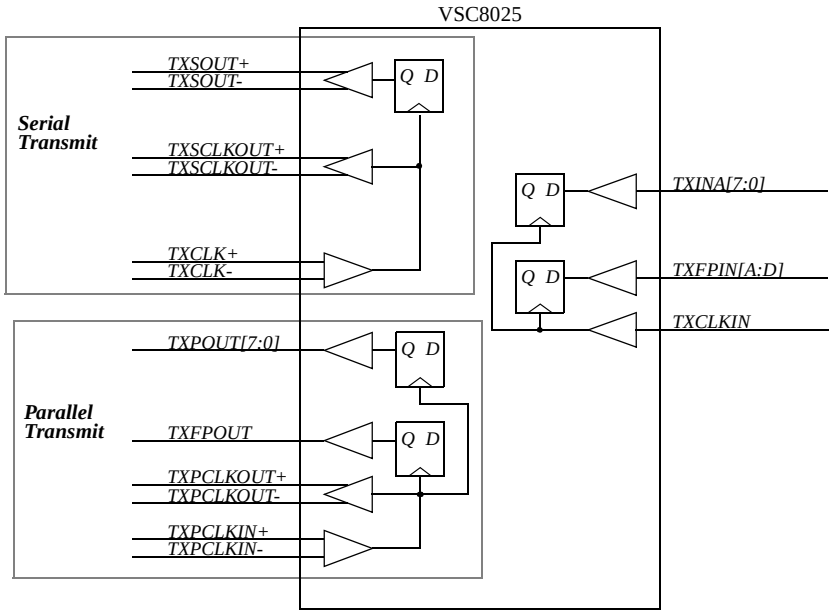
VSC8025 AC Timing Characteristics

Figure 4: VSC8025 Clock and Data Interface (Serial Transmit & Parallel Transmit Mode)



Note: 1). Parallel transmit mode bypasses the 8:1 MUX, and serial transmit mode uses the 8:1 MUX.

2). TXINB [7:0], TXINC [7:0], and TXIND [7:0] inputs have been omitted for simplicity.

2). In serial transmit mode, SELPCLK = logic "0".

3). In parallel transmit mode, SELPCLK = logic "1".

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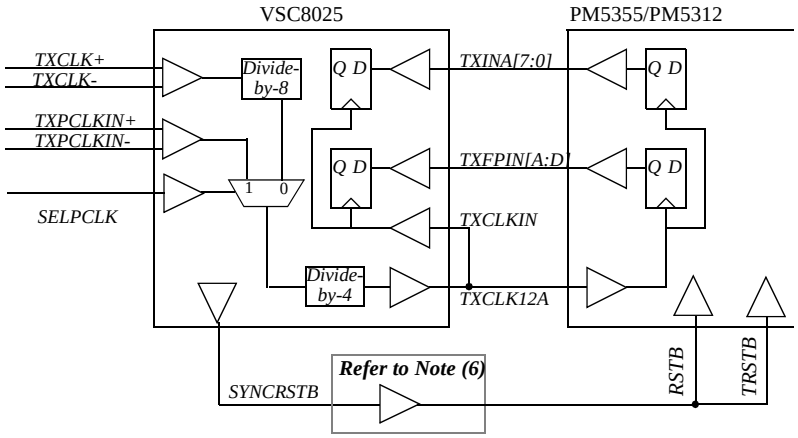
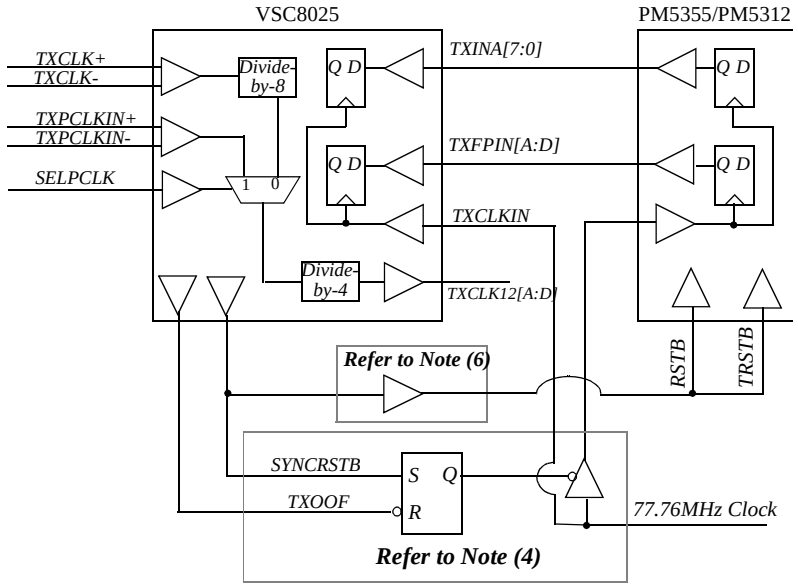
Figure 5: VSC8025 Clock and Data Interface (Contra-directional & Co-directional Mode)



(A). Contra-directional Mode Interface



(B). Co-directional Mode Interface

Note: 1. TXINB [7:0], TXINC [7:0], and TXIND [7:0] inputs have been omitted for simplicity.
2. TXCLK12B, TXCLK12C, and TXCLK12D output have been omitted for simplicity.
3. In contra-directional mode, TRISE=TFALL=logic "0".
4. In co-directional mode, TRISE=logic "1"; TFALL=logic "1" when not using TSYNC, logic "0" if using TSYNC.
5. In co-directional mode, the 77.76MHz input clock to PM5355/PM5212 must be blocked out for at least 32 cycles when SYNCRSTB transitions low (logic "0") due to misalignment of TXFPIN[A:D] as shown in Figure 3.
6. SYNCRSTB, a TTL output with a minimum V_{OH} of 2.4V, needs to be buffered up to drive the reset pins of the PMC parts. RSTB and TRSTB on the PM5355/PM5312 have a minimum V_{IH} of 3.5V.

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Table 3: VSC8025 Serial Clock Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{TXCLK}	High speed input clock period	-	401.9	-	ps
D_{TXCLK}	High speed input clock duty cycle	45	50	55	%

Table 4: VSC8025 Parallel Data Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{TXCLK12}$	Divide-by-32 output clock period	-	12.86	-	ns
$D_{TXCLK12}$	Divide-by-32 output clock duty cycle	45	50	55	%
$T_{TXCLKIN}$	Parallel input data load clock period	-	12.86	-	ns
$D_{TXCLKIN}$	Parallel input data load clock duty cycle	40	50	60	%
T_{JITTER}	TXCLKIN jitter			2	ns
T_{TXPSU}	TXIN[A:D][7:0], TXFPIN[A:D], and TXIN[A:D]P data setup time with respect to rising edge of TXCLKIN	0.35	-	-	ns
T_{ERR}	Propagation delay from rising edge of TXCLKIN to TXPER[A:D]	1.7	-	6.8	ns
T_{TXPH}	TXIN[A:D][7:0], TXFPIN[A:D], and TXIN[A:D]P data hold time with respect to rising edge of TXCLKIN	1.1	-	-	ns
T_{CSKEW}	TXCLK12[A:D] clock skew	-	-	0.67	ns
T_{PROP}	Maximum allowable propagation delay for connecting TX12CLKA to TXCLKIN in Contra-Directional Mode (TRISE=TFALL=logic '0', $T_{TXCLK12}$ = typ)	-	-	6	ns

Figure 6: VSC8025 Parallel Data Input Timing Diagram

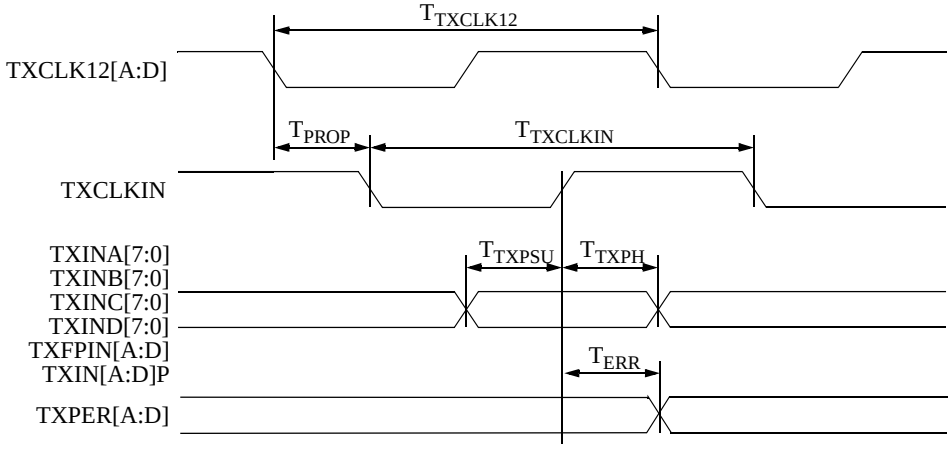

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Table 5: VSC8025 Serial Data Output Timing

Parameter	*Description*	*Min*	*Type*	*Max*	*Units*
$T_{TXSCLKOUT}$	Serial Transmit clock period	-	401.9	-	ps
T_{SSKEW}	Delay from falling edge of TXSCLKOUT+ and valid data on TXSOUT	20	-	140	ps

Figure 7: VSC8025 Serial Data Output Timing Diagram

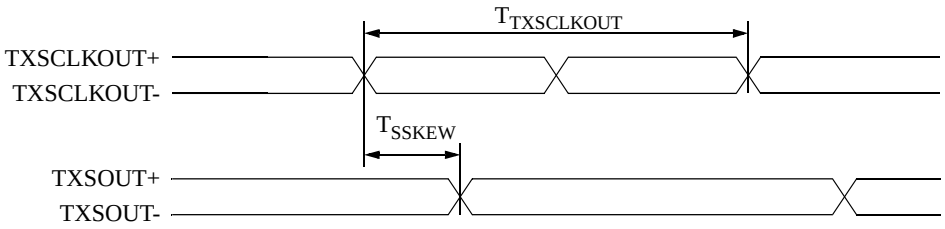

Table 6: VSC8025 Serial Data Input Timing (Facility Loopback)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{TXSLBCLK}$	Serial loopback clock period	-	401.9	-	ps
T_{TXLSU}	Serial loopback input data TXSLBIN setup time with respect to falling edge of TXSLBCLK+	120	-	-	ps
T_{TXLSH}	Serial loopback input data TXSLBIN hold time with respect to falling edge of TXSLBCLK+	60	-	-	ps

Figure 8: VSC8025 Serial Data Input Timing Diagram (Facility Loopback)

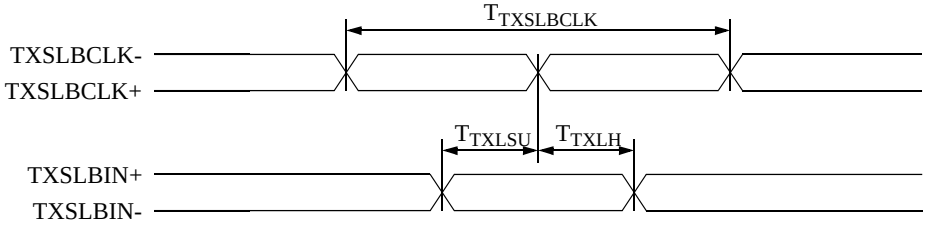

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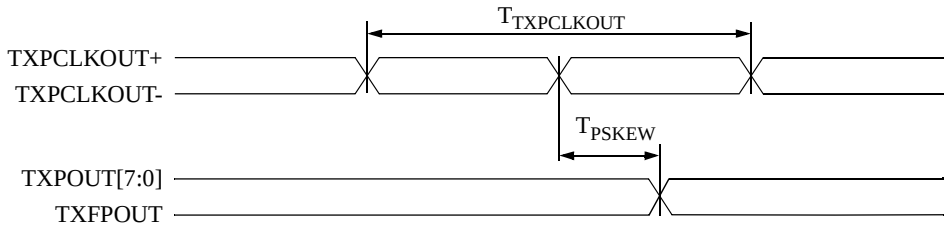
Table 7: VSC8025 Parallel Data Output Timing (Equipment Loopback)

Parameter	*Description*	*Min*	*Type*	*Max*	*Units*
$T_{TXPCLKOUT}$	Parallel transmit clock period	-	3.215	-	ns
T_{PSKEW}	Delay from rising edge of TXPCLKOUT+ to valid data on TXPOUT [7:0] and on TXFPOUT	0.1	-	1.3	ns

Figure 9: VSC8025 Parallel Data Output Timing Diagram (Equipment Loopback)



Note: Duty cycle for TXPCLKOUT is 50% ± 10% when configured for serial output mode (SELPCLK=Ø)
Duty cycle for TXPCLKOUT depends on TXPCKLIN duty cycle when configured for parallel output only (SELPCLK=1)

VSC8025 Power Dissipation

Table 8: VSC8025 Power Supply Currents (Outputs Open)

Parameter	*Description*	*(Max)*	*Units*
I_{TT}	Power supply current from V_{TT}	2.12	A
I_{TTL}	Power supply current from V_{TTL}	103	mA
I_{DD}	Power supply current from V_{DD}	0.48	A
P_D	Power dissipation	7.44	W

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VSC8025 Package Pin Description

Table 9: Pin Identification Table

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VSCTE	A01	I	-2.0	Test Enable (tie to -2V)
N/C	A02			No Connection (tie to 0V or leave open)
VTT	A03	PWR	-2V	-2.0V power supply
TXPERD	A04	O	TTL	Parallel input bus D parity error
TXPERB	A05	O	TTL	Parallel input bus B parity error
TXPERA	A06	O	TTL	Parallel input bus A parity error
TXINDP	A07	I	TTL	Parallel input bus/frame pulse D parity
TXINCP	A08	I	TTL	Parallel input bus/frame pulse C parity
TXCLK12D	A09	O	TTL	Transmit clock divided by 32
TXCLK12C	A10	O	TTL	Transmit clock divided by 32
TXCLK12B	A11	O	TTL	Transmit clock divided by 32
NOFP	A12	O	TTL	No frame pulse detected (active high)
SYNCRSTB	A13	O	TTL	Synchronous reset when not byte aligned (active low)
VCC	A14	PWR	GND	Ground
TXIND5	A15	I	TTL	Parallel input bus data D
TXINC7	A16	I	TTL	Parallel input bus data C
SETJZ1	B01	I	TTL	Section trace byte control
N/C	B02			No Connection (tie to 0V or leave open)
N/C	B03			No Connection (tie to 0V or leave open)
DISM1GEN	B04	I	TTL	Disable M1/B2 circuitry (active high)
DISBLC12	B05	I	TTL	Disable blocking of TXCLK12 (active high)
TXPERC	B06	O	TTL	Parallel input bus C parity error
VCC	B07	PWR	GND	Ground
TXINBP	B08	I	TTL	Parallel input bus/frame pulse B parity
TXINAP	B09	I	TTL	Parallel input bus/frame pulse A parity
VCC	B10	PWR	GND	Ground
TXOOF	B11	O	TTL	Transmit out of frame (active high)
TXIND7	B12	I	TTL	Parallel input bus data D
TXIND6	B13	I	TTL	Parallel input bus data D
TXIND4	B14	I	TTL	Parallel input bus data D
TXFPIND	B15	I	TTL	Transmit frame pulse in (active high)
TXINC5	B16	I	TTL	Parallel input bus data C
VCC	C01	PWR	GND	Ground
SETJZ0	C02	I	TTL	Section trace byte control
N/C	C03			No Connection (tie to 0V or leave open)

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Table 9: Pin Identification Table

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
N/C	C04			No Connection (tie to 0V or leave open)
VCC	C05	PWR	GND	Ground
VTT	C06	PWR	-2V	-2.0V power supply
VTTL	C07	PWR	+3.3V	+3.3V power supply
VTT	C08	PWR	-2V	-2.0V power supply
VTT	C09	PWR	-2V	-2.0V power supply
VTTL	C10	PWR	+3.3V	+3.3 V power supply
VTT	C11	PWR	-2V	-2.0V power supply
VCC	C12	PWR	GND	Ground
TXIND3	C13	I	TTL	Parallel input bus data D
TXIND1	C14	I	TTL	Parallel input bus data D
TXINC6	C15	I	TTL	Parallel input bus data C
VCC	C16	PWR	GND	Ground
DISB1GEN	D01	I	TTL	Disable B1 generation (active high)
N/C	D02			No Connection (tie to 0V or leave open)
VGND	D03	PWR	GND	Ground
N/C	D04			No Connection (tie to 0V or leave open)
N/C	D05			No Connection (tie to 0V or leave open)
VCC	D06	PWR	GND	Ground
VCC	D07	PWR	GND	Ground
VCC	D08	PWR	GND	Ground
VCC	D09	PWR	GND	Ground
VCC	D10	PWR	GND	Ground
VCC	D11	PWR	GND	Ground
TXIND2	D12	I	TTL	Parallel input bus data D
TXIND0	D13	I	TTL	Parallel input bus data D
VCC	D14	PWR	GND	Ground
TXINC4	D15	I	TTL	Parallel input bus data C
TXINC3	D16	I	TTL	Parallel input bus data C
TXPCLKIN-	E01	I	ECL	Transmit parallel clock in
N/C	E02			No Connection (tie to 0V or leave open)
VCC	E03	PWR	GND	Ground
VTTL	E04	PWR	+3.3V	+3.3V power supply
VTTL	E13	PWR	+3.3V	+3.3V power supply
VCC	E14	PWR	GND	Ground
TXINC1	E15	I	TTL	Parallel input bus data C
TXFPINC	E16	I	TTL	Transmit frame pulse in (active high)
N/C	F01			No Connection (tie to 0V or leave open)

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Table 9: Pin Identification Table

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
TXPCLKIN+	F02	I	ECL	Transmit parallel clock in
DISSCRM	F03	I	TTL	Disable scrambler (active high)
VTT	F04	PWR	-2V	-2.0V power supply
VTT	F13	PWR	-2V	-2.0V power supply
TXINC2	F14	I	TTL	Parallel input bus data C
TXINC0	F15	I	TTL	Parallel input bus data C
TEST 24	F16	O	TTL	Test pin (leave open)
TXCLKREF	G01			Transmit clock termination. If AC coupling, connect to GND with a decoupling capacitor. If DC coupling, connect to Vtt directly.
VCC	G02	PWR	GND	Ground
VTTL	G03	PWR	+3.3V	+3.3V power supply
VCC	G04	PWR	GND	Ground
VCC	G13	PWR	GND	Ground
VTTL	G14	PWR	+3.3V	+3.3V power supply
VCC	G15	PWR	GND	Ground
TXCLK12A	G16	O	TTL	Transmit clock divided by 32
TXCLK-	H01	I	HSECL	Transmit clock from CMU
TXCLK+	H02	I	HSECL	Transmit clock from CMU
VGND	H03	PWR	GND	Ground
VTT	H04	PWR	-2V	-2.0V power supply
VTT	H13	PWR	-2V	-2.0V power supply
VCC	H14	PWR	GND	Ground
TFALL	H15	I	TTL	Contra/Co-directional programming pin
TXCLKIN	H16	I	TTL	Parallel input data load clock
TXSOUT+	J01	O	HSECL	High-speed serial data out
TXSOUT-	J02	O	HSECL	High-speed serial data out
VCC	J03	PWR	GND	Ground
VTT	J04	PWR	-2V	-2.0V power supply
VTT	J13	PWR	-2V	-2.0V power supply
VCC	J14	PWR	GND	Ground
TXINB7	J15	I	TTL	Parallel input bus data B
TRISE	J16	I	TTL	Contra/Co-directional programming pin
TXSCLKOUT+	K01	O	HSECL	High-speed serial clock out
VCC	K02	PWR	GND	Ground
VTTL	K03	PWR	+3.3V	+3.3V power supply
VCC	K04	PWR	GND	Ground
VCC	K13	PWR	GND	Ground

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Table 9: Pin Identification Table

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VTTL	K14	PWR	+3.3V	3.3V power supply
VCC	K15	PWR	GND	Ground
TXINB6	K16	I	TTL	Parallel input bus data B
TXSCLKOUT-	L01	O	HSECL	High-speed serial clock out
N/C	L02			No connection (leave open)
TXSLBIN-	L03	I	HSECL	Serial loop back input
VTT	L04	PWR	-2V	-2.0V power supply
VTT	L13	PWR	-2V	-2.0V power supply
TXINB1	L14	I	TTL	Parallel input bus data B
TXINB3	L15	I	TTL	Parallel input bus data B
TXINB5	L16	I	TTL	Parallel input bus data B
N/C	M01			No connection (leave open)
TXSLBIN+	M02	I	HSECL	Serial loop back input
VCC	M03	PWR	GND	Ground
VTTL	M04	PWR	+3.3V	+3.3V power supply
VTTL	M13	PWR	+3.3V	+3.3V power supply
VCC	M14	PWR	GND	Ground
TXINB2	M15	I	TTL	Parallel input bus data B
TXINB4	M16	I	TTL	Parallel input bus data B
TXSLBINREF	N01			Serial loopback data termination. If AC coupling, connect to GND with a decoupling capacitor. If DC coupling, connect to Vtt directly.
N/C	N02			No connection (leave open)
VCC	N03	PWR	GND	Ground
TEST 23	N04	I	TTL	Test pin (tie to 0V)
SELSTS48C	N05	I	TTL	STS-48c mode (active high)
VCC	N06	PWR	GND	Ground
VDD	N07	PWR	+3.3V	+3.3V power supply
VCC	N08	PWR	GND	Ground
VCC	N09	PWR	GND	Ground
VCC	N10	PWR	GND	Ground
VCC	N11	PWR	GND	Ground
TXINA2	N12	I	TTL	Parallel input bus data A
TXINA4	N13	I	TTL	Parallel input bus data A
VCC	N14	PWR	GND	Ground
TXFPINB	N15	I	TTL	Transmit frame pulse in (active high)
TXINB0	N16	I	TTL	Parallel input bus data B
VCC	P01	PWR	GND	Ground

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Table 9: Pin Identification Table

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
RCLK155-	P02	O	ECL	Divide by 16 clock output for external CMU
FACLOOP	P03	I	TTL	Facility loop back enable (active high)
DISFPCHK	P04	I	TTL	Disable frame pulse check (active high)
VCC	P05	PWR	GND	Ground
VTT	P06	PWR	-2V	-2.0V power supply
VDD	P07	PWR	+3.3V	+3.3V power supply
VTT	P08	PWR	-2V	-2.0V power supply
VTT	P09	PWR	-2V	-2.0V power supply
VTTL	P10	PWR	+3.3V	+3.3V power supply
VTT	P11	PWR	-2V	-2.0V power supply
VCC	P12	PWR	GND	Ground
TXINA1	P13	I	TTL	Parallel input bus data A
TXINA3	P14	I	TTL	Parallel input bus data A
TESTAC7	P15	O	ECL	Test pin (leave open)
VCC	P16	PWR	GND	Ground
RCLK155+	R01	O	ECL	Divide by 16 clock output for external PLL
TEST 22	R02	I	TTL	Test pin (tie to 0V)
RESET	R03	I	TTL	Reset (active high)
TESTAC5	R04	I	TTL	Test pin (tie to 0V)
TXPCLKOUT+	R05	O	ECL	Parallel transmit clock out
TXSLBCKREF	R06			Serial loopback clock termination. If AC coupling, connect to GND with a decoupling capacitor. If DC coupling, connect to Vtt directly.
VCC	R07	PWR	GND	Ground
TXFPOUT	R08	O	ECL	Parallel transmit frame pulse out
TXPOUT0	R09	O	ECL	Parallel transmit data out
VCC	R10	PWR	GND	Ground
TXPOUT5	R11	O	ECL	Parallel transmit data out
TXPOUT7	R12	O	ECL	Parallel transmit data out
TESTAC6	R13	I	TTL	Test pin (tie to 0V)
TXINA0	R14	I	TTL	Parallel input bus data A
TXINA5	R15	I	TTL	Parallel input bus data A
TXINA7	R16	I	TTL	Parallel input bus data A
TESTAC4	T01	I	TTL	Test pin (tie to 0V)
SELPCLK	T02	I	TTL	Select parallel clock (active high)
VCC	T03	PWR	GND	Ground
TXPCLKOUT-	T04	O	ECL	Parallel transmit clock out
TSYNC	T05	I	TTL	

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Table 9: Pin Identification Table

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
TXSLBCLK+	T06	I	HSECL	Serial loopback clock
TXSLBCLK-	T07	I	HSECL	Serial loopback clock
N/C	T08			No connection (leave open)
TXPOUT1	T09	O	ECL	Parallel transmit data out
TXPOUT2	T10	O	ECL	Parallel transmit data out
TXPOUT3	T11	O	ECL	Parallel transmit data out
TXPOUT4	T12	O	ECL	Parallel transmit data out
TXPOUT6	T13	O	ECL	Parallel transmit data out
VTT	T14	PWR	-2V	-2.0V power supply
TXFPINA	T15	I	TTL	Transmit frame pulse in (active high)
TXINA6	T16	I	TTL	Parallel input bus data A

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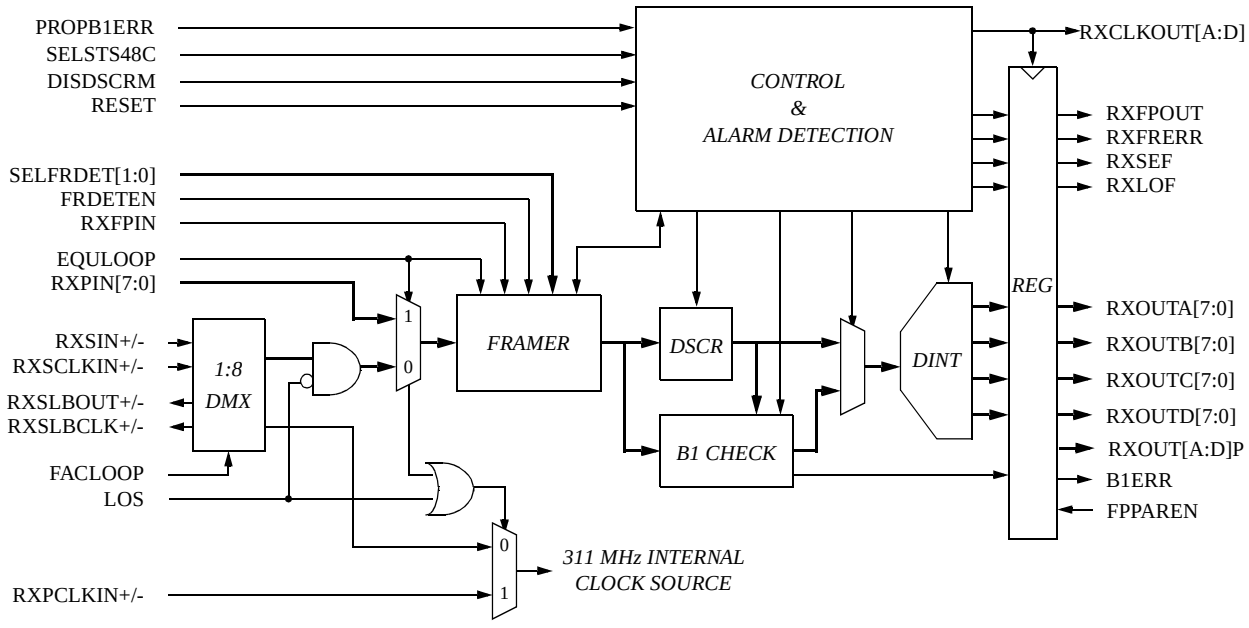
VSC8026 Functional Description

The VSC8026 demultiplexer deserializes a 2.488 Gb/s serial SONET/SDH data stream into four byte-wide STS-12/STM-4 data streams and terminates the transmission frame section overhead. The VSC8026 performs frame boundary detection and synchronization, optional descrambling, and provides section level alarm and performance monitoring. A functional block diagram of the VSC8026 is shown in Figure 10.

Serial STS-48/STM-16 data is presented at the differential RXSIN input together with an associated differential clock RXSCLKIN, originating from the Clock and Data Recovery Unit (CRU). Data is captured on the rising edge of RXSCLKIN+ (refer to Figure 17). Following the 1:8 deserialization, the frame boundary is detected and the data stream is byte aligned before descrambling. The descrambled data stream is then byte de-interleaved into four 8-bit parallel STS-12/STM-4 data streams at 77.76 MHz (to four PM5312s or four PM5355s), consistent with the existing requirements for SONET/SDH intermediate level de-multiplexing. The STS-12/STM-4 data streams are presented on the RXOUTA[7:0], RXOUTB[7:0], RXOUTC[7:0] and RXOUTD[7:0] output pins at the falling edge of RXCLKOUT[A:D] (refer to Figure 19).

Figure 10: VSC8026 Functional Block Diagram



Equipment Loopback

The VSC8026 is equipped with a parallel input port, which for equipment loopback purposes interfaces to the VSC8025 byte-wide STS-48/STM-16 output port. This port can also be used for interfacing to an STS-192/STM-64 Demux circuit. When EQULOOP is high, the 1:8 Demux circuit is bypassed with data from the paral-

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lel input port RXPIN[7:0]. In this mode of operation, the internal clock source is RXPCLKIN, rather than the divide-by-8 clock generated by the 1:8 Demux. The parallel input is also equipped with a frame pulse input RXFPIN, which can be used for synchronizing the internal frame counter when the frame detection circuit is disabled, which might be desirable if the VSC8026 is used in a STS-192/STM-64 setup. Data on RXPIN[7:0] and RXFPIN are captured on the falling edge of RXPCLKIN+ (refer to Figure 18).

Facility Loopback

To create a facility (or line) loopback the registered RXSIN data and the RXSCLKIN are brought out of the chip (RXSLBOUT and RXSLBCLK). These two signals should be connected to the TXSLBIN and TXSLBCLK inputs on the VSC8025 to create a facility loopback. RXSLBOUT and RXSLBCLK outputs are added to minimize the loading on the high speed clock and data lines coming from the RX optics module. To minimize jitter on RXSIN and RXSCLKIN inputs during normal operation, the RXSLBOUT and RXSLBCLK outputs can be disabled by holding the asynchronous FACLOOP input low. Please refer to Figure 21 for a detailed facility loopback circuit diagram.

STS-48c Mode

To support STS-48c operation, where bytes from the four STS-12/STM-4 inputs are interleaved on at a time (as opposed to four at a time in STS-48 mode), the byte interleaver can be configured for STS-48c multiplexing by holding the asynchronous SELSTS48C input high.

Descrambler

The VSC8026 performs optional descrambling using a frame synchronous descrambler with generating polynomial $1 + x^6 + x^7$and a sequence length of 127. The descrambler is disabled by asserting DISDSCRM high. DISDSCRM is latched-in once every frame.

Error Performance (B1)

The section bit-interleaved parity (BIP-8) error detection code B1 will be calculated for every frame before descrambling, and compared to its extracted value after descrambling in the following frame. The B1 errors will be presented on the B1ERR output as 25.72 ns wide pulses (up to 8 per frame). The first pulse will be aligned with the B1 byte of the current frame (refer to Figure 14). Besides calculating the BIP-8 over the entire STS-48/STM-16 frame, the VSC8026 also calculates a BIP-8 over the first STS-12/STM-4 frame interleaved into the STS-48/STM-16 frame. This calculated $B1_{STS\text{-}12\#1}$ is XORed with the error-mask derived from XORing the extracted $B1_{STS\text{-}48}$ with the calculated $B1_{STS\text{-}48}$ over the entire STS-48/STM-16 frame. The result is inserted into the B1 byte position of the first outgoing STS-12 data stream (on RXOUTA[7:0]), when the asynchronous PROPB1ERR is held high. This will make the B1 error count on the B1ERR output identical to the B1 error count in the first STS-12/STM-4 channel, which can be easily monitored through the microprocessor interface of the PM5355/PM5312s.

Loss of Signal

A Loss Of Signal (LOS) input is provided to prevent random data from propagating downstream during a LOS condition. Random data will be clocked into the VSC8026 in the absence of alternating input data, if ac-coupling is applied between the optics module and the RXSIN input. Also, during a LOS condition, the internal clock source is switched over to the parallel input clock RXPCLKIN, since the high speed clock (RXSCLKIN)

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might be absent during LOS (depending on the CRU used). Switching over to RXPCLKIN during LOS prevents the VSC8026 from 'freezing' in the absence of a serial input clock.

Framer

The frame acquisition algorithm determines the in-frame/out-of-frame status of the receiver. Out-of-frame is defined as a state where the frame boundaries of the received SONET/SDH signal are unknown, i.e. after system reset or if for some reason the receiver looses synchronization, e.g. due to 'bit slips'. In-frame is defined as a state where the frame boundaries are known.

The frame boundary detection/verification is based on either 12, 24 or 48 bits of the A1/A2 overhead as shown in Figure 11, based on the SELFRDET[1:0] settings shown in Table 10. Frame acquisition is initiated when FRDETEN is held high. This control is level sensitive and the VSC8026 will continually perform frame acquisition as long as FRDETEN is held high. A functional block diagram of the frame acquisition circuit is shown in Figure 12.

While in-frame (FRDETEN low), the receiver monitors the frame synchronization by checking the framing pattern in each frame. If one or more bit errors are detected in the framing pattern, FRERR will be asserted for 25.72 ns (refer to Figure 13). If framing pattern errors are detected for four consecutive frames, a Severely Errored Frame (SEF) alarm will be declared (RXSEF). The SEF alarm is terminated when two consecutive frames with error free framing patterns have been detected.

A frame detect based on 24 bits will result in a SEF (Severely Errored Frame) alarm at an average of no more than once every 6 minutes assuming a BER of 10^{-3} as specified by the SONET Bellcore spec. A frame detect based on 48 or 12 bits will result in a mean time between SEF detects of 0.43 and 103 minutes, respectively. The frame detection circuit can be disabled by holding both asynchronous SELFRDET[1:0] inputs high. To achieve SONET/SDH specifications for framing, the user needs to connect the RXSEF output to the FRDETEN input.

Loss of Frame

A Loss Of Frame (LOF) alarm is declared (RXLOF) when a Severely Errored Frame (SEF) condition persists for 3 ms. The LOF state detection is based on an integrating timer. To provide for the case of intermittent SEF's, the integrating timer is not reset until an in-frame condition (SEF low) persists continuously for 3 ms. Once in a LOF state, this state is terminated when the in-frame condition persists continuously for 3 ms.

Parity

Even parity is provided for each byte wide data bus on outputs RXOUT[A:D]P; the parity calculation includes the frame pulse if FPPAREN is logic 1. The even parity output for a bus is a logic 1 when an odd number of bits in the byte wide data and frame pulse (if FPPAREN is logic 1) are logic 1; otherwise, it is logic 0.

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Figure 11: VSC8026 Frame Detection Patterns

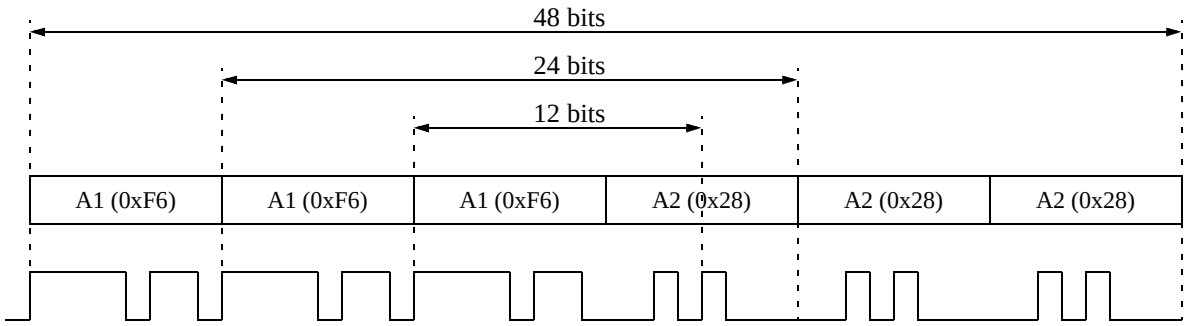

Table 10: VSC8026 Frame Detection Select Settings

Function	*SELFRDET1*	*SELFRDET0*
24 bits	1	0
48 bits	0	1
12 bits	0	0
Frame detection disabled	1	1

Figure 12: VSC8026 Functional Block Diagram of Frame Acquisition Circuit

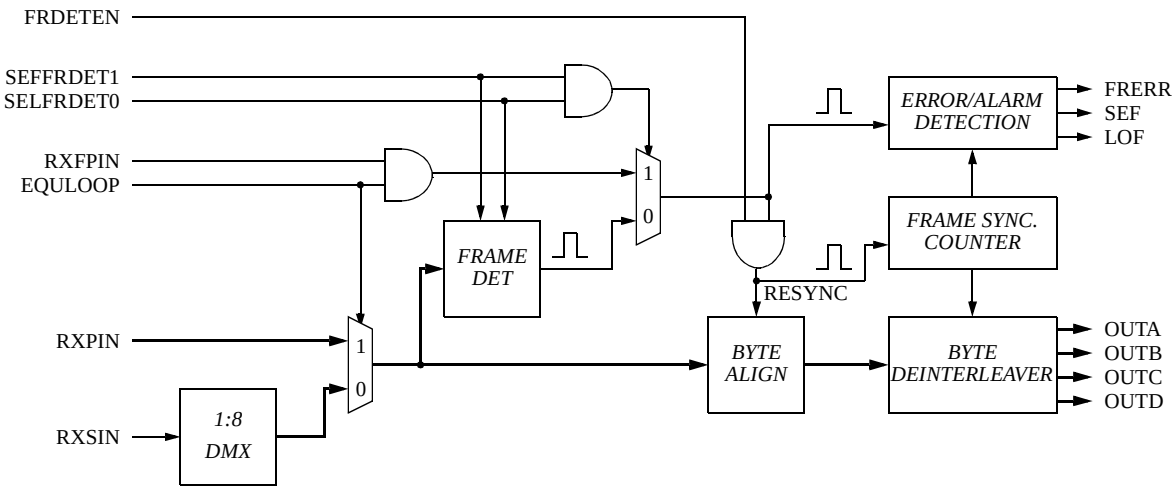

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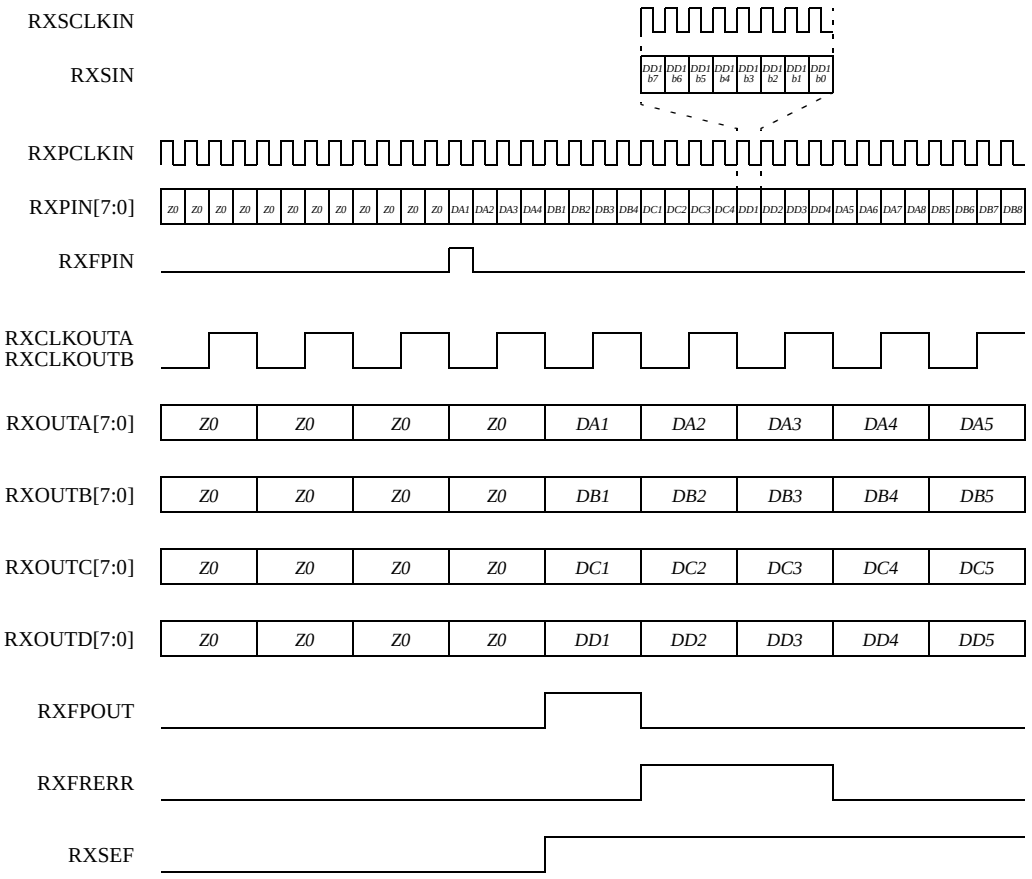
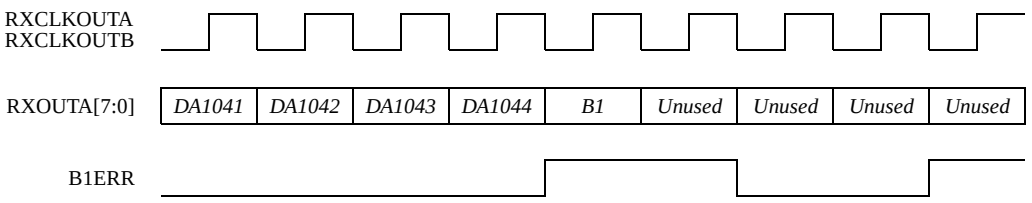
Figure 13: VSC8026 Functional Timing Diagram (STS-48 Mode)



Note:
(1) The correct latency between RXPIN, RXSIN and RXOUTA-D is NOT shown.
(2) RXPIN is equivalent to RXSIN (byte wide) in normal operation (EQULOOP low). RXFPIN is not applicable in normal operation.

Figure 14: VSC8026 Functional Timing (B1ERR output)



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VSC8026 AC Timing Characteristics

Figure 15: VSC8026 Clock and Data Interface Block Diagram (Serial Receive Mode)

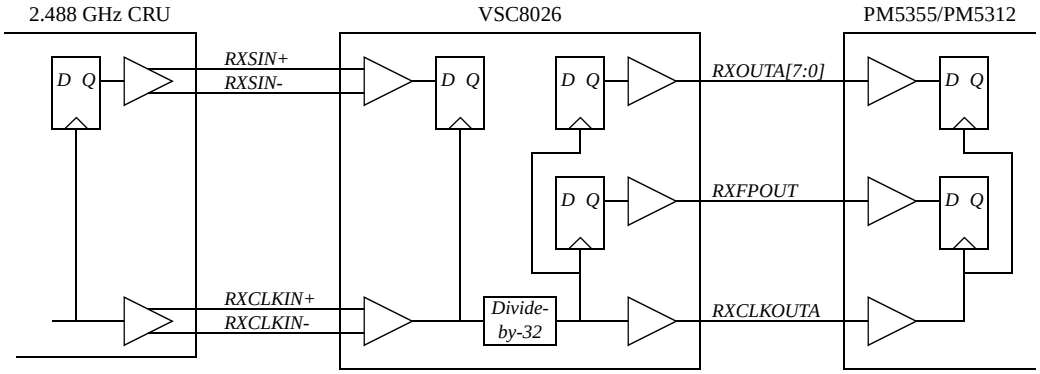

Figure 16: VSC8026 Clock and Data Interface Block Diagram (Parallel Receive Mode)

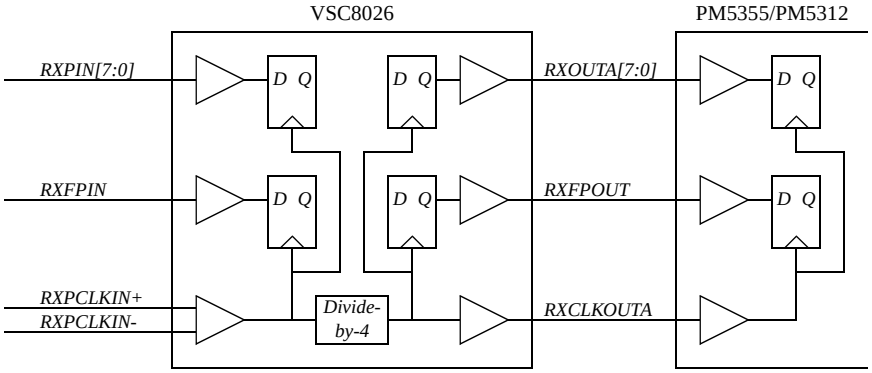

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Table 11: VSC8026 Serial Data Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXSCLKIN}$	Serial Receive clock period	-	401.9	-	ps
T_{RXSSU}	Serial Receive input data RXSIN setup time with respect to rising edge of RXSCLKIN+	120	-	-	ps
T_{RXSH}	Serial Receive input data RXSIN hold time with respect to rising edge of RXSCLKIN+	60	-	-	ps

Figure 17: VSC8026 Serial Data Input Timing Diagram

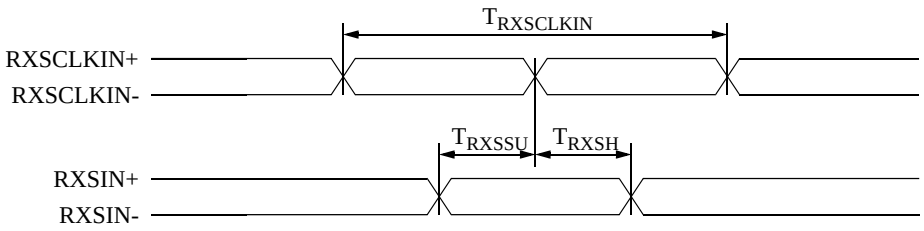

Table 12: VSC8026 Parallel Data Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXPCLKIN}$	Parallel Receive clock period	-	3.215	-	ns
T_{RXPSU}	Parallel Receive input data RXPIN[7:0]/RXFPIN setup time with respect to falling edge of RXPCLKIN+	0.0	-	-	ns
T_{RXPH}	Parallel Receive input data RXPIN[7:0]/RXFPIN hold time with respect to falling edge of RXPCLKIN+	0.8	-	-	ns

Figure 18: VSC8026 Parallel Data Input Timing Diagram (Equipment Loopback)

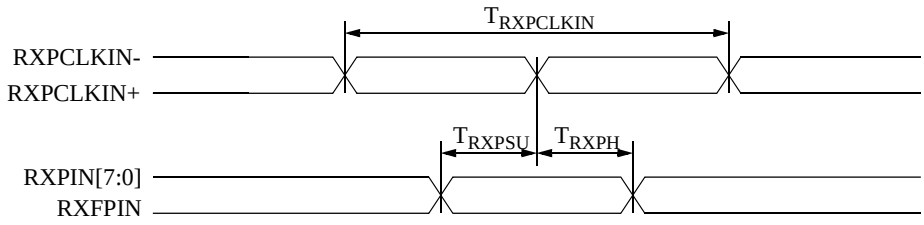

Table 13: VSC8026 Parallel Data Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXCLKOUT}$	Receive data output clock period	-	12.86	-	ns

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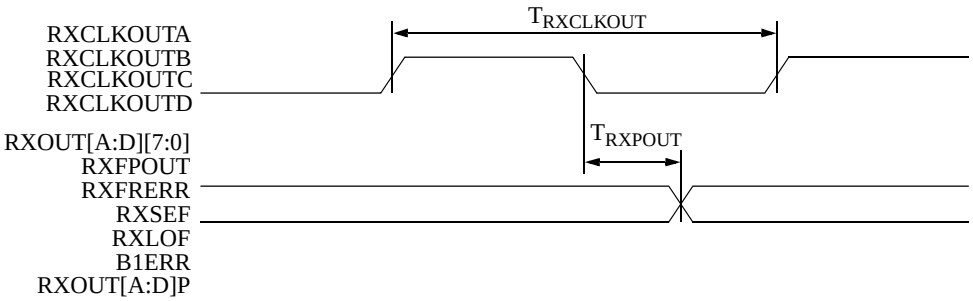
Parameter	Description	Min	Typ	Max	Units
T_{RXPOUT}	Delay from falling edge of RXCLKOUT[A:D] to valid data on RXOUTA[7:0], RXOUTB [7:0], RXOUTC [7:0], RXOUTD[7:0], RXFPOUT, RXFRERR, RXSEF, RXLOF, B1ERR, and RXOUT[A:D]P	-2.7	-	+0.7	ns
T_{CSKEW}	RXCLKOUT[A:D] rising edge clock skew	-	-	0.65	ns

Figure 19: VSC8026 Parallel Data Output Timing Diagram

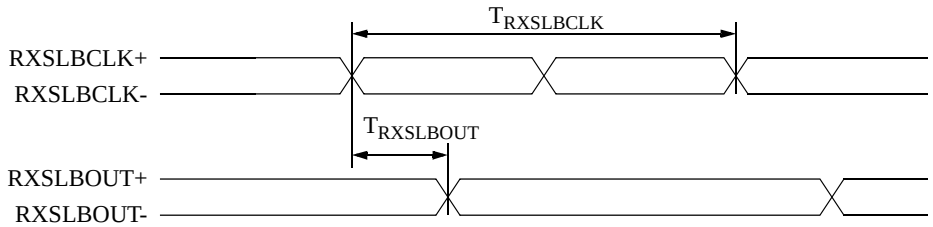


Note: (1) The T_{RXPOUT} timing parameter is relative to both RXCLKOUTA and RXCLKOUTB.
(2) Duty cycle for RXCLKOUT[A:D] is 50% ± 10% when configured for serial input mode (EQULOOP=Ø)

Table 14: VSC8026 Serial Data Output Timing (Facility Loopback)

Parameter	Description	Min	Typ	Max	Units
$T_{RXSLBCLK}$	Serial loopback clock period	-	401.9	-	ps
$T_{RXSLBOUT}$	Delay from falling edge of RXSLBOUT+ to data transition edge of RXSLBOUT	-10	-	170	ps

Figure 20: VSC8026 Serial Data Output Timing Diagram (Facility Loopback)



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VSC8026 Power Dissipation

Table 15: VSC8026 Power Supply Currents (Outputs Open)

Parameter	*Description*	*(Max)*	*Units*
I_{TT}	Power supply current from V_{TT}	2.37	A
I_{TTL}	Power supply current from V_{TTL}	75	mA
I_{DD}	Power supply current from V_{DD}	266	mA
P_D	Power dissipation	6.7	W

VSC8026 Package Pin Description

Table 16: Pin Identification Table

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VSCTE	A01	I	-2V	Test enable (tie to -2V)
N/C	A02			No connection (leave open)
VTT	A03	PWR	-2V	-2.0V power supply
RXPCLKIN+	A04	I	ECL	Receive parallel clock in
N/C	A05			No connection (leave open) No connection (leave open)
RXSLBCLK+	A06	O	HSECL	Serial loop back clock out
RXSLBCLK-	A07	O	HSECL	Serial loop back clock out
RXFPIN	A08	I	ECL	Receive parallel frame pulse in
RXPIN1	A09	I	ECL	Receive parallel data in
RXPIN2	A10	I	ECL	Receive parallel data in
RXPIN3	A11	I	ECL	Receive parallel data in
RXPIN5	A12	I	ECL	Receive parallel data in
RXPIN7	A13	I	ECL	Receive parallel data in
VCC	A14	PWR	GND	Ground
N/C	A15			No connection (leave open)
N/C	A16			No connection (leave open)
N/C	B01			No connection (leave open)
LOS	B02	I	TTL	Loss of signal (active high)
N/C	B03			No connection (leave open)
N/C	B04			No connection (leave open)
RXPCLKIN-	B05	I	ECL	Receive parallel clock in
N/C	B06			No connection (leave open)
VCC	B07	PWR	GND	Ground
N/C	B08			No connection (leave open)
RXPIN0	B09	I	ECL	Receive parallel data in

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Table 16: Pin Identification Table

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VCC	B10	PWR	GND	Ground
RXPIN4	B11	I	ECL	Receive parallel data in
RXPIN6	B12	I	ECL	Receive parallel data in
NC	B13			No connection (leave open)
NC	B14			No connection (leave open)
NC	B15			No connection (leave open)
RXOUTCP	B16	O	TTL	Parallel output bus C parity
VCC	C01	PWR	GND	Ground
N/C	C02			No connection (leave open)
N/C	C03			No connection (leave open)
N/C	C04			No connection (leave open)
VCC	C05	PWR	GND	Ground
VTT	C06	PWR	-2V	-2.0V power supply
VTTL	C07	PWR	+3.3V	+3.3V power supply
VTT	C08	PWR	-2V	-2.0V power supply
VTT	C09	PWR	-2V	-2.0V power supply
VTTL	C10	PWR	+3.3V	+3.3V power supply
VTT	C11	PWR	-2V	-2.0V power supply
VCC	C12	PWR	GND	Ground
N/C	C13			No connection (leave open)
N/C	C14			No connection (leave open)
RXOUTDP	C15	O	TTL	Parallel output bus D parity
VCC	C16	PWR	GND	Ground
N/C	D01			No connection (leave open)
N/C	D02			No connection (leave open)
VCC	D03	PWR	GND	Ground
SELFRDET0	D04	I	TTL	Frame detect mode select
N/C	D05			No connection (leave open)
VCC	D06	PWR	GND	Ground
VDD	D07	PWR	+3.3V	+3.3V power supply
VCC	D08	PWR	GND	Ground
VCC	D09	PWR	GND	Ground
VCC	D10	PWR	GND	Ground
VCC	D11	PWR	GND	Ground
N/C	D12			No connection (leave open)
N/C	D13			No connection (leave open)
VCC	D14	PWR	GND	Ground
RXCLKOUTD	D15	O	TTL	Receive parallel data clockout D

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Table 16: Pin Identification Table

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
RXCLKOUTC	D16	O	TTL	Receive parallel data clockout C
N/C	E01			No connection (leave open)
RXSLBOUT+	E02	O	HSECL	Serial loop back data out
VCC	E03	PWR	GND	Ground
VTTL	E04	PWR	+3.3V	+3.3V power supply
VTTL	E13	PWR	+3.3V	+3.3V power supply
VCC	E14	PWR	GND	Ground
RXOUTD7	E15	O	TTL	Parallel output bus data D
RXOUTD6	E16	O	TTL	Parallel output bus data D
RXCLKREF	F01			Serial receive clock termination. If AC coupling, connect to GND with a decoupling capacitor. If DC coupling, connect to Vtt directly.
N/C	F02			No connection (leave open)
RXSLBOUT-	F03	O	HSECL	Serial loop back data out
VTT	F04	PWR	-2V	-2.0V power supply
VTT	F13	PWR	-2V	-2.0V power supply
RXOUTD3	F14	O	TTL	Parallel output bus data D
RXOUTD5	F15	O	TTL	Parallel output bus data D
RXOUTD4	F16	O	TTL	Parallel output bus data D
RXSREF	G01			Serial receive data termination. If AC coupling, connect to GND with a decoupling capacitor. If DC coupling, connect to Vtt directly.
VCC	G02	PWR	GND	Ground
VTTL	G03	PWR	+3.3V	+3.3V power supply
VCC	G04	PWR	GND	Ground
VCC	G13	PWR	GND	Ground
VTTL	G14	PWR	+3.3V	+3.3V power supply
VCC	G15	PWR	GND	Ground
RXOUTD2	G16	O	TTL	Parallel output bus data D
RXSCLKIN-	H01	I	HSECL	Serial receive clock
RXSCLKIN+	H02	I	HSECL	Serial receive clock
VCC	H03	PWR	GND	Ground
VTT	H04	PWR	-2V	-2.0V power supply
VTT	H13	PWR	-2V	-2.0V power supply
VCC	H14	PWR	GND	Ground
RXOUTD1	H15	O	TTL	Parallel output bus data D
RXOUTD0	H16	O	TTL	Parallel output bus data D
RXSIN+	J01	I	HSECL	Serial receive data
RXSIN-	J02	I	HSECL	Serial receive data

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Table 16: Pin Identification Table

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VCC	J03	PWR	GND	Ground
VTT	J04	PWR	-2V	-2.0V power supply
VTT	J13	PWR	-2V	-2.0V power supply
VCC	J14	PWR	GND	Ground
RXOUTC6	J15	O	TTL	Parallel output bus data C
RXOUTC7	J16	O	TTL	Parallel output bus data C
RXOUTAP	K01	O	TTL	Parallel output bus A parity
VCC	K02	PWR	GND	Ground
VTTL	K03	PWR	+3.3V	+3.3V power supply
VCC	K04	PWR	GND	Ground
VCC	K13	PWR	GND	Ground
VTTL	K14	PWR	+3.3V	+3.3V power supply
VCC	K15	PWR	GND	Ground
RXOUTC5	K16	O	TTL	Parallel output bus data C
RXLOF	L01	O	TTL	Loss of frame (active high)
FRERR	L02	O	TTL	Frame error (active high)
RXOUTBP	L03	O	TTL	Parallel output bus B parity
VTT	L04	PWR	-2V	-2.0V power supply
VTT	L13	PWR	-2V	-2.0V power supply
RXOUTC2	L14	O	TTL	Parallel output bus data C
RXOUTC4	L15	O	TTL	Parallel output bus data C
RXOUTC3	L16	O	TTL	Parallel output bus data C
B1ERR	M01	O	TTL	Parity byte B1 error (active high)
RXSEF	M02	O	TTL	Severely errored frame (active high)
VCC	M03	PWR	GND	Ground
VTTL	M04	PWR	+3.3V	+3.3V power supply
VTTL	M13	PWR	+3.3V	+3.3V power supply
VCC	M14	PWR	GND	Ground
RXOUTC0	M15	O	TTL	Parallel output bus data C
RXOUTC1	M16	O	TTL	Parallel output bus data C
SELFRDET1	N01	I	TTL	Frame detect mode select
FRDETEN	N02	I	TTL	Frame detect enable (active high)
VCC	N03	PWR	GND	Ground
N/C	N04			No connection (leave open)
N/C	N05			No connection (leave open)
VCC	N06	PWR	GND	Ground
VCC	N07	PWR	GND	Ground
VCC	N08	PWR	GND	Ground

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Table 16: Pin Identification Table

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VCC	N09	PWR	GND	Ground
VCC	N10	PWR	GND	Ground
VCC	N11	PWR	GND	Ground
N/C	N12			No connection (leave open)
N/C	N13			No connection
VCC	N14	PWR	GND	Ground
RXCLKOUTB	N15	O	TTL	Receive parallel data clock out B
RXCLKOUTA	N16	O	TTL	Receive parallel data clock out A
VCC	P01	PWR	GND	Ground
EQULOOP	P02	I	TTL	Equipment loop back enable (active high)
FACLOOP	P03	I	TTL	Facility loop back enable (active high)
N/C	P04			No connection (leave open)
VCC	P05	PWR	GND	Ground
VTT	P06	PWR	-2V	-2.0V power supply
VTTL	P07	PWR	+3.3V	+3.3V power supply
VTT	P08	PWR	-2V	-2.0V power supply
VTT	P09	PWR	-2V	-2.0V power supply
VTTL	P10	PWR	+3.3V	+3.3V power supply
VTT	P11	PWR	-2V	-2.0V power supply
VCC	P12	PWR	GND	Ground
N/C	P13			No connection (leave open)
N/C	P14			No connection (leave open)
VSCOPNC	P15	O	ECL	Test output (leave open)
VCC	P16	PWR	GND	Ground
PROPB1ERR	R01	I	TTL	Propagate B1 error (active high)
N/C	R02			No connection (leave open)
SYSRST	R03	I	TTL	System reset (active high)
SF	R04	I	TTL	Test input (tie to 0V)
RXOUTA2	R05	O	TTL	Parallel output bus data A
RXOUTA4	R06	O	TTL	Parallel output bus data A
VCC	R07	PWR	GND	Ground
RXOUTA6	R08	O	TTL	Parallel output bus data A
RXOUTB1	R09	O	TTL	Parallel output bus data B
VCC	R10	PWR	GND	Ground
RXOUTB3	R11	O	TTL	Parallel output bus data B
RXOUTB5	R12	O	TTL	Parallel output bus data B
N/C	R13			No connection (leave open)
N/C	R14			No connection (leave open)

Table 16: Pin Identification Table

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
FPPAREN	R15	I	TTL	Frame pulse included in parity enable
RXFPOUT	R16	O	TTL	Receive frame pulse out
DISDSCRM	T01	I	TTL	Disable descramble mode (active high)
SELSTS48C	T02	I	TTL	STS-48c mode (active high)
VCC	T03	PWR	GND	Ground
RXOUTA0	T04	O	TTL	Parallel output bus data A
RXOUTA1	T05	O	TTL	Parallel output bus data A
RXOUTA3	T06	O	TTL	Parallel output bus data A
RXOUTA5	T07	O	TTL	Parallel output bus data A
RXOUTA7	T08	O	TTL	Parallel output bus data A
RXOUTB0	T09	O	TTL	Parallel output bus data B
RXOUTB2	T10	O	TTL	Parallel output bus data B
RXOUTB4	T11	O	TTL	Parallel output bus data B
RXOUTB6	T12	O	TTL	Parallel output bus data B
RXOUTB7	T13	O	TTL	Parallel output bus data B
VTT	T14	PWR	-2V	-2.0V power supply
N/C	T15			No connection (leave open)
VSCIPNC	T16	I	ECL	Test input (tie to -2V)

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Absolute Maximum Ratings (VSC8025/VSC8026)

Power Supply Voltage (V_{TT}) Potential to GND ..... -2.5 V to +0.5 V
Power Supply Voltage (V_{TTL}) Potential to GND ..... -0.5 V to +4.3 V
TTL Input Voltage Applied ..... -0.5 V to + 5.5V
ECL Input Voltage Applied ..... +0.5 V to V_{TT} -0.5 V
Output Current (I_{OUT}) ..... 50 mA
Case Temperature Under Bias (T_C) ..... -55° to + 125°C
Storage Temperature (T_{STG}) ..... -65° to + 150°C

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions (VSC8025/VSC8026)

Power Supply Voltage (V_{TT}) ..... -2.0 V ±5 %
Power Supply Voltage (V_{DD}) ..... +3.3 V ±5 %
Power Supply Voltage (V_{TTL}) ..... +3.3 V ±5 %
Commercial Operating Temperature Range* (T) ..... 0° to 85°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

ESD Ratings (VSC8025/VSC8026)

Proper ESD procedures should be used when handling this product. The VSC8025 and VSC8026 are rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

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DC Characteristics (VSC8025/VSC8026)

Table 17: Standard ECL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-	-700	mV	50 ohm to V_{TT}
V_{OL}	Output LOW voltage	-2000	-	-1620	mV	50 ohm to V_{TT}
V_{IH}	Input HIGH voltage	-1165	-	-700	mV	—
V_{IL}	Input LOW voltage	-2000	-	-1475	mV	—
I_{IH}	Input HIGH current	-	-	200	uA	$V_{IN}=V_{IH}$ (max)
I_{IL}	Input LOW current	-50	-	-	uA	$V_{IN}=V_{IL}$ (min)
V_{DIFF}	Input Voltage Differential	200	-	-	mV	—
V_{CM}	Common Mode Voltage	-1.5	-	-0.5	V	—

Note: Differential ECL output pins must be terminated identically.

Table 18: High-Speed Differential ECL Inputs and Outputs (HSECL)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OD}	Output differential voltage	0.45	-	1.0	V	—
V_{OCM}	Output common-mode voltage	-1.35	-	-0.95	V	—
R_O	Output Impedance	3	-	7	ohms	Guaranteed, not tested.
V_{ID}	Input differential voltage	0.45	-		V	—
V_{ICM}	Input common-mode voltage	-1.6	-	-0.5	V	—
V_{IT}	Input threshold matching	-25	-	25	mV	—

Note: HSECL inputs are NOT terminated on chip (high impedance inputs).

Table 19: TTL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	-	-	V	I_{OH}=-2.4 mA
V_{OL}	Output LOW voltage	0	-	0.4	V	I_{OL}=16 mA
V_{IH}	Input HIGH voltage	2.0	-	5.5	V	—
V_{IL}	Input LOW voltage	0	-	0.8	V	—
I_{IH}	Input HIGH current	-	-	50	uA	$V_{IN}=V_{DD}$ (max)
I_{IL}	Input LOW current	-1000	-	-	uA	$V_{IN}=V_{IL}$ (min)

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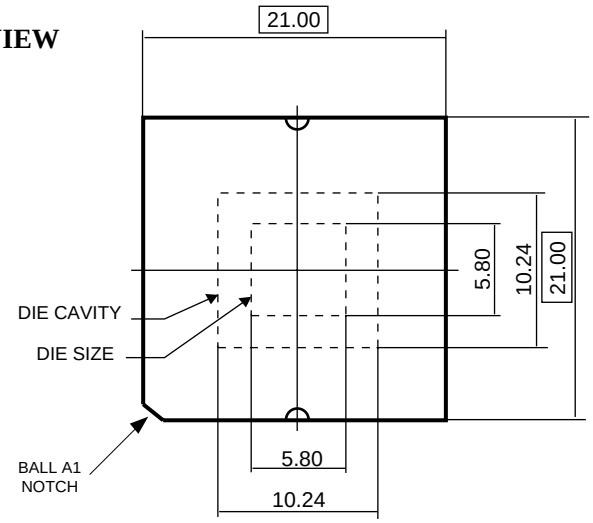
Package Information

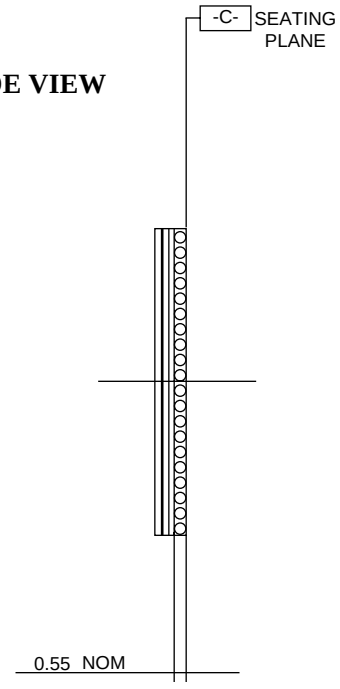
192 TBGATBGA Package Dimensions

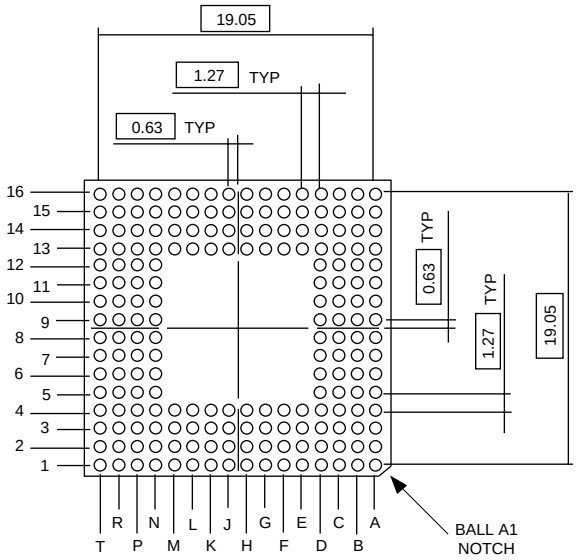
TOP VIEW



BOTTOM VIEW

SIDE VIEW





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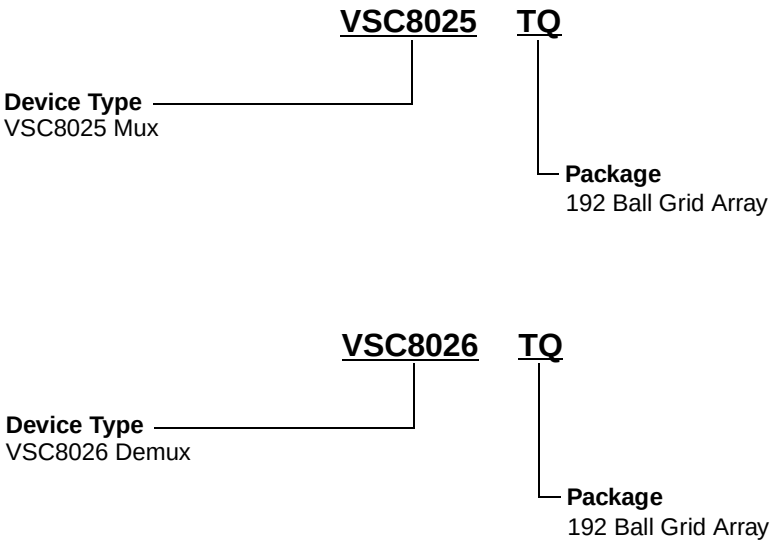
Ordering Information

The order number for this product is formed by a combination of the device number, and package type.



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Application Notes

The byte clocks (TXCLK12[A:D] and TXCLKIN) on the VSC8025 have been brought off-chip to allow as much flexibility in system-level clocking schemes as possible. Refer to Figure 4 & Figure 5 for connection examples.

Interconnecting the VSC8025 Byte Clocks (TXCLK12[A:D] and TXCLKIN)

Contra-Directional Timing Mode

In this mode, the byte clock (TXCLK12A) clocks both the VSC8025 and data interface devices. It is important to pay close attention to the routing of this signal. The PMC devices are CMOS parts which can have very wide spreads in timing (2ns-11ns clock in to parallel data out for the PM5355) which utilizes most of the 12.86 ns period (at 77.76 MHz), leaving little for the trace delays and set-up times required to interconnect the devices. The recommended configuration of PMC devices is to route TXCLK12A to all four devices in a star like pattern; keep route lengths short, and tap TXCLKIN from a point which will match the net length to that of data interface device connections. TXCLK12[B:D] can be used to simplify clock distribution and improve signal integrity; however, it is important to verify setup and hold values for each data interface using the route lengths, clock skew, and any other system variables.

Co-Directional Timing Mode

In the co-directional mode an internal data synchronizing circuit is used to optimize the phase relationship between a supplied TXCLKIN and internal clocks. The TXCLKIN signal needs to meet setup and hold timing relative to the data stream and frame pulses, duty cycle, and 2.5GHz (or 311MHz) frequency lock.

Equipment and Facility Loopbacks

In order to create an Equipment Loopback, the EQULOOP VSC8026 input is held high. The byte-wide STM-16/STS-48 data on the VSC8025 TXPOUT [7:0] outputs is clocked into the VSC8026 RXPIN [7:0] inputs with the TXPCLKOUT clock. A frame pulse aligned with the first payload byte on the TXPOUT [7:0] databus is provided to assure proper alignment. Both the Facility and the Equipment Loopbacks can be enabled simultaneously. It is possible to disable (hold at a logic low) the serial high-speed outputs on the VSC8026 by holding the asynchronous FACLOOP input low.

The diagram below (Figure 21) shows how an Equipment and a Facility Loopback are created. When in Facility Loopback mode (FACLOOP is held high) the serial 2.488 Gb/s data and clock from the receive optics module is first clocked into the VSC8026 and then fed back into the VSC8025 through TXSLBIN and TXSLBCLK. The FACLOOP input (held high) selects the data from the VSC8026 instead of the data from the 8:1 Mux. The result is a line loopback from the receive optics module back out to the transmit optics module.

On-Chip Terminations

The VSC8025 and VSC8026 provide on chip terminations for the HSECL inputs as shown in Figure 22. When using AC coupled input signals a 0.1µF capacitor is recommended on the REF points.

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Power Supply Sequencing

The +3.3V supply should not be allowed to remain in the absence of the -2.0V supply. If the -2.0V supply should fault during the system operation, provisions should be made to sense this condition and turn off the -3.3V supply within 1 second.

Power Supply Decoupling

This is a summary of the recommended bypass and decoupling components. The listed components should be used for each VSC8025 and VSC8026 part. Component placement under the TBGA means on the back side of the circuit board centered under the device.

V_{TT} (-2V)

This supply is quiet, the entire core operates off current steering logic, with the exception of the ECL I/O macros. However, the vast majority of it's switching current comes from the external 50Ω pull down resistors through the output FET to ground.

- Quantity (2) - 0.001µF low inductance (0603/0403 pkg) ceramic SMT X7R capacitors, placed under TBGA as close to the V_{TT} balls as possible.
- Quantity (6) - 0.01µF HF low inductance (0603/0403 pkg) ceramic SMT X7R capacitor. Two of the six should be placed under the TBGA.
- Quantity (6) - 0.1µF HF low inductance (0603 pkg) ceramic SMT X7R capacitor. Two of the six should be placed under the TBGA.

LF Decoupling: 47µF tantalum low inductance SMT caps are sprinkled over the boards main -2V plane.

V_{TTL} (+3.3V)

This is a particularly important power supply because it contains the only switching currents due mostly to the TTL and some to the ECL I/Os. All core cells use current steering logic. The High speed core logic called SCFL (Series Coupled FET Logic), similar to ECL, operates off the -2V VTT to the +3.3V VDD supply. The same is true for the low speed logic called DCFL (Direct Coupled FET Logic) which operates from -2V to 0V. Because the SCFL uses +3.3V its supplied through dedicated VDD Pins which should be filtered through a C-L-C filter. There is usually only one digital +3.3V supply, so all other +3.3V supplies of concern must be filtered to keep the noise from the +3.3V digital switching power supply out.

- Quantity (3) - 0.01µF HF low inductance (0603/0403 pkg) ceramic SMT X7R capacitor. Place two under the TBGA.
- Quantity (8) - 0.1µF HF low inductance (0603 pkg) ceramic SMT X7R capacitor. Place two under the TBGA.
- Quantity (3) - 1.0µF HF low inductance (0603 pkg) ceramic SMT X7R capacitor.

LF Decoupling: 47µF tantalum low inductance SMT are sprinkled over the board main +3.3V plane and placed close to the C-L-C pie filter.

V_{DD} (+3.3V)

As explained above this is the top rail to the SCFL core logic and must be filtered through a C-L-C pie filter.

- Quantity (1) - 0.01µF low inductance (0603 pkg) ceramic SMT X7R capacitor. Placed under the TBGA as close to the V_{DD} pins as possible.
- Quantity (1) - 0.1µF HF low inductance (0603 pkg) ceramic SMT X7R capacitor. Placed under the TBGA as close to the V_{DD} pins as possible.

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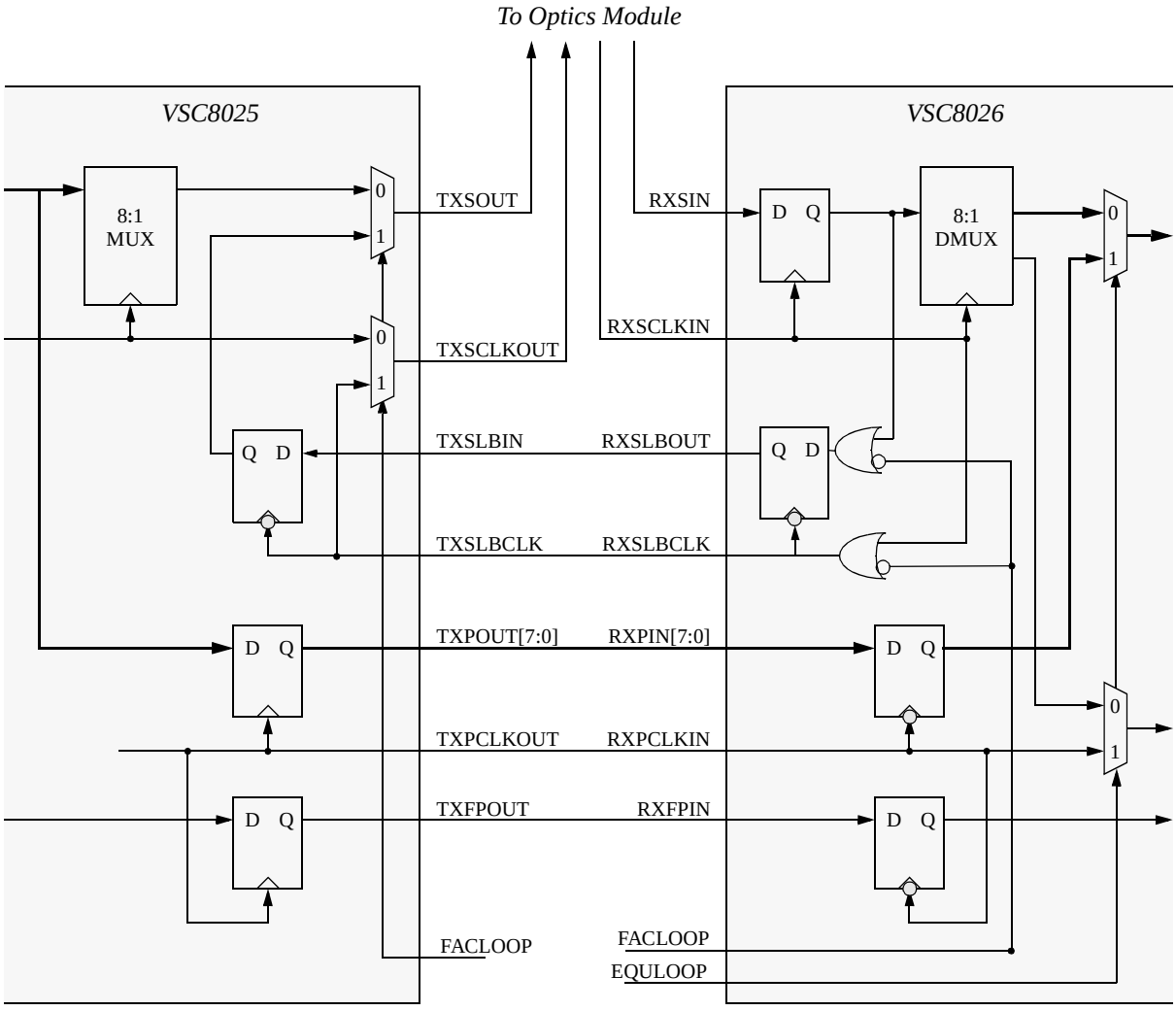
The V_{DD} pin(s) will be isolated from and connect to the main +3.3V plane through a 10µH C-L-C filter. Each board is different. The frequencies of the noise differs, so in the end one should lay the board out with as many extra lands for extra decoupling capacitors, as well as, accommodating either a ferrite bead or an inductor. During the prototype evaluation phase, a spectrum analyzer is used to determine if the noise has been filtered to acceptable levels.

Figure 21: Loopback Functional Block Diagram



Note: All signals are drawn as single ended

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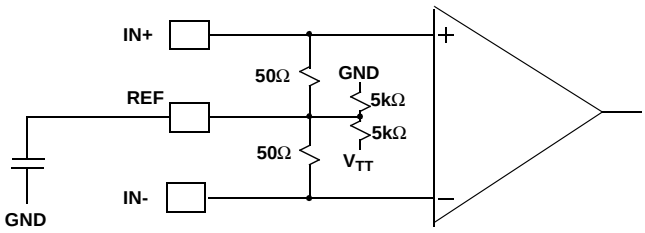
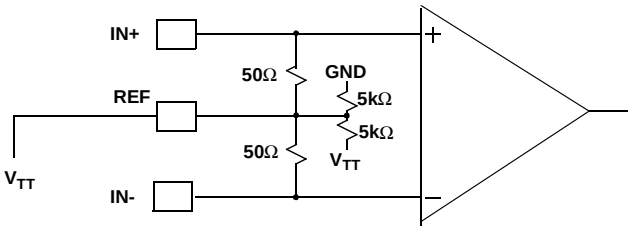
Figure 22: HSECL Input Termination



(A). If the high speed inputs are AC coupled, the REF pin needs to be connected to GND with a decoupling capacitor.



(B). If the high speed inputs are DC coupled, the REF pin needs to be connected to V_{TT} directly.

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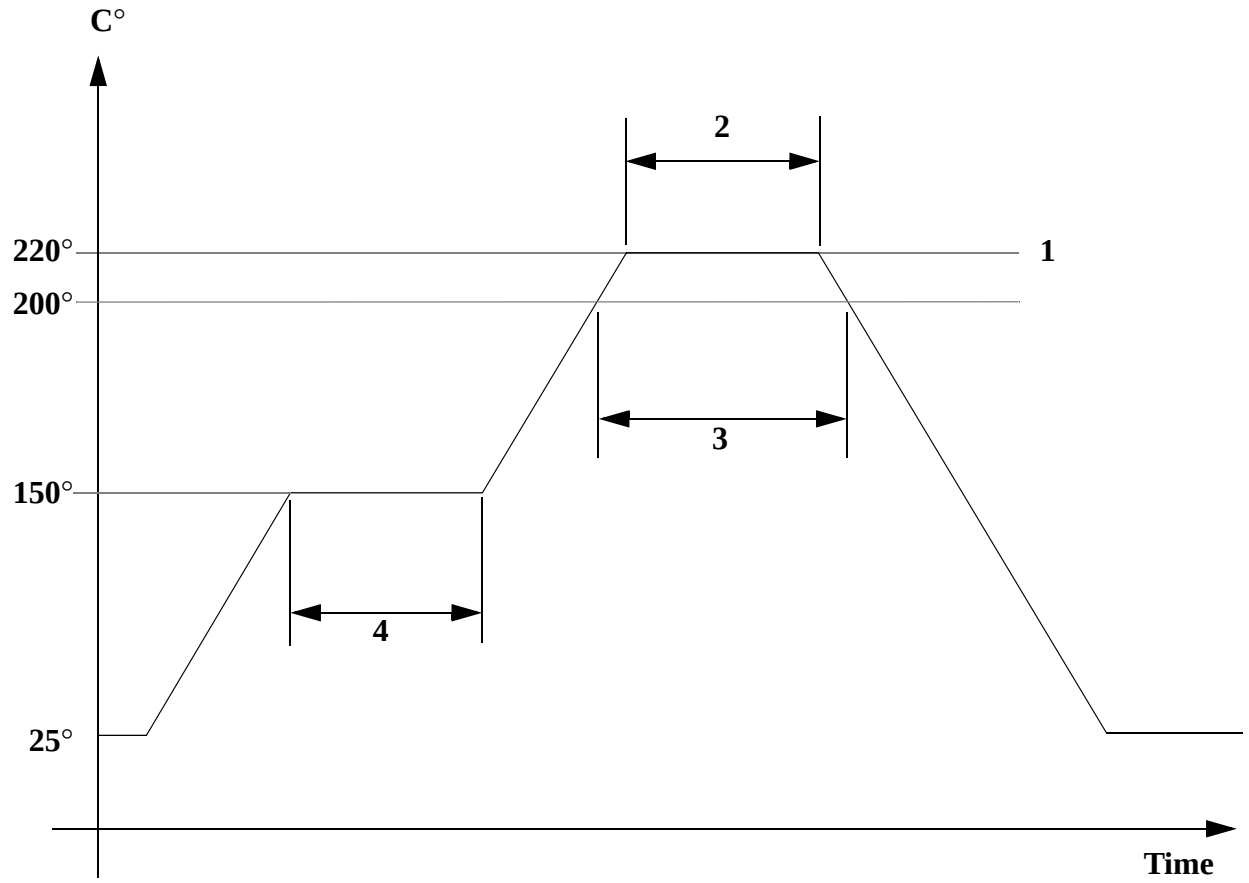
IR Reflow Profile for Assembly of ASAT 192 TBGA

Figure 23: IR Reflow Profile for Assembly of ASAT 192 TBGA



Notes: 1) Peak temperature = 220°C
2) Peak time = 70 - 80 seconds
3) Time over 200°C = 110 - 120 seconds
4) Preheat time = ≥ 40 seconds (TYP)

All slopes are 1°C/sec for ramp up and ramp down
Industry standard eutectic solder balls: 62% tin, 36% lead, 2% silver

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

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