VITESSE

VSC7108 Datasheet

6.5 Gbps Octal Signal Conditioner

Features

- 6.5 Gigabit per second (Gbps) Non-Return-to-Zero (NRZ) data bandwidth
- User-programmable input signal equalization
- User-programmable output pre-emphasis
- 2.5 V or 3.3 V CMOS/TTL control inputs
- Differential Common-Mode Logic (CML) data output driver
- On-chip input and output terminations
- Single 2.5 V power supply, 3.3 V optional control pins
- 1.8 W typical power
- High-performance 69-pin CBGA package

Applications

- Wideband signal clean-up device
- Line driver or receiver
- Backplane driver or receiver
- Cable driver or receiver

General Description

The VSC7108 is an octal signal conditioner designed for use in broadband data stream applications. It features an asynchronous design that allows the user to use it in applications calling for the simultaneous transmission of different data rates (up to 6.5 Gbps) on different signal channels. A high degree of signal integrity is provided because of the device's use of fully differential signal paths.

Each of the inputs on the VSC7108 connects directly to one of its corresponding outputs. All signal paths are unregistered and fully asynchronous; there are no restrictions on the phase, frequency, or signal pattern of any input.

Data inputs are terminated on-die using 100 ohm resistors between true and complement with a common connection to an internal bias source for AC-coupling. Each high-speed output also incorporates on-die terminations to provide maximum signal integrity.

The device also features Vitesse's innovative programmable Input Signal Equalization (ISE). This allows the user to compensate for varying trace lengths on the printed circuit board by enabling a discrete implementing any of three, discrete levels of conditioning. Similar compensation is available for outputs using a user-set pre-emphasis of the output. Pre-emphasis adds a fixed overshoot or undershoot to the output waveform.

Block Diagram

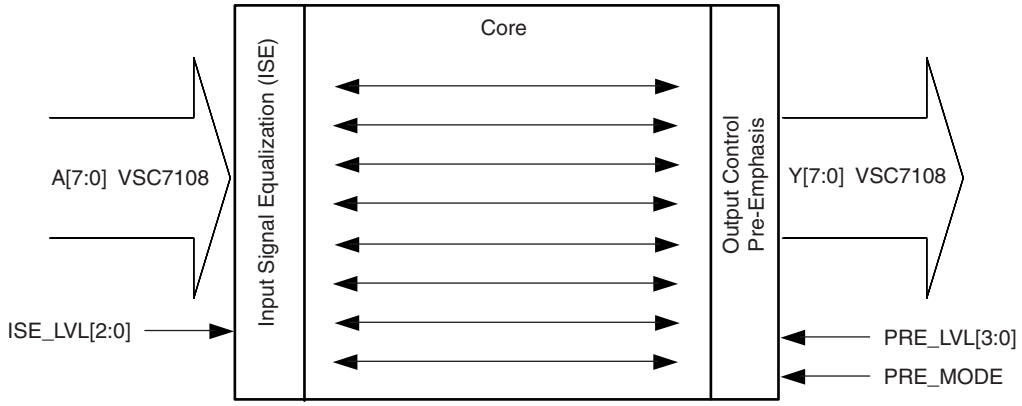


Figure 1. Block Diagram

Application Example

The following diagram depicts the VSC7108 used as a serial repeater and multiple rate, multiple protocol signal conditioner with signal clean-up functionality.

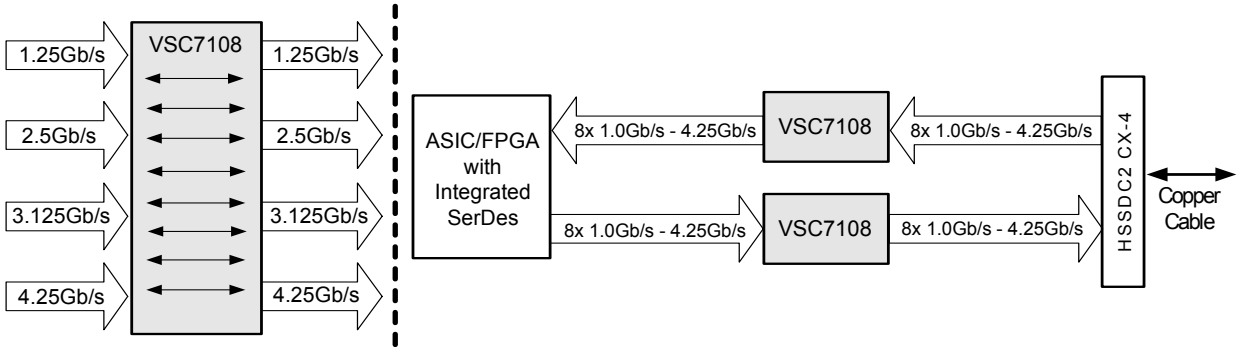


Figure 2. Typical Application

Functional Description

Input Signal Equalization

Adjusting the ISE setting for the VSC7108 changes the input response of the device's input buffers. The feature is designed to compensate for the input signal's having traversed through varying lengths of printed circuit board traces or between other devices in the application.

The level of equalization is set globally in the VSC7108, affecting all of the inputs to the device. Generally, lower equalization is used when the traces for incoming signals are relatively short; higher equalization is used for longer traces. The "correct" setting depends upon several environmental factors, and typically requires experimentation with each of the different levels to determine the optimum for the particular application.

Use the ISE_LVL# pins to choose which of the four, predetermined levels of equalization are implemented. Table 1 lists the settings available. Refer to the package drawings (Figure 5 and Figure 6) and the pin tables starting on page 4, for the location of the pins used to control this feature in the VSC7108.

Table 1. Input Equalization Control for Pins ISE_LVL0, ISE_LVL1, and ISE_LVL2

Bit	Equalization
2-0	000 = No equalization 001 = Minimum equalization 011 = Medium equalization 111 = Maximum equalization

Output Pre-Emphasis

Pre-emphasis at the output driver adds a fixed overshoot or undershoot to the output waveform. As in the case of ISE, output pre-emphasis compensates for different trace lengths and board characteristics.

In the VSC7108, the user can program the device for any of 16, predetermined time constants for the signal amplitude boost. The PRE_LVL# pins are used to configure the constants. Table 2 lists the settings and the corresponding pre-emphasis levels available.

Table 2. Output Pre-Emphasis Control for Pins PRE_LVL0, PRE_LVL1, PRE_LVL2, and PRE_LVL3

Bit	Description
3 - 0	Range 0 to 15 0000 = ~450ps to 1111 = ~700ps

Electrical Specifications

Unless stated otherwise, all specifications are assumed to over recommended operating conditions.

AC Characteristics

Table 3. High-Speed Data Inputs (A, $\overline{A}$)(1)

Symbol	Parameter	Typical	Maximum	Unit	Condition
DR_A	Serial NRZ input data rate		6.5	Gbps	Minimum data rate will be limited by the AC-coupling capacitor value (if AC-coupled).
t_{PD-AY}	Propagation delay from input to output	500		ps	
t_{SKEW}	Output channel-to-channel delay skew	20	60	ps	From any input to any output
t_{R-A}, t_{F-A}	Serial data input rise and fall times		200	ps	20% to 80%.

1. Inputs are guaranteed by characterization.

Table 4. High-Speed Data Outputs (Y, $\overline{Y}$)(1)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
DR_Y	Serial NRZ output data rate			6.5	Gbps	Minimum data rate will be limited by the AC-coupling capacitor value (if AC-coupled).
t_{Jp-p}	Serial output data added delay jitter, peak-to-peak(2)			20	ps	
t_{R-Y}, t_{F-Y}	Serial output data rise and fall times		50	80	ps	20% to 80%. With 50 Ω to V_{CC}.
DC_Y	Serial data output duty cycle	40	50	60	%	Only relevant with 101010 input data patterns.

1. Outputs are guaranteed by characterization.

2. Broadband (unfiltered) deterministic jitter added to input: $2^{23} – 1$ PRBS data pattern.

DC Characteristics

Table 5. High-Speed Data Inputs (A, $\overline{A}$) — Differential CML

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{A-DE}	Voltage input swing (differential drive)	100		2400	mVp-p	Differential peak-to-peak.
V_{ICM}	Input common-mode voltage	1.0	2	$V_{CC} – 0.3$	V	
R_{IN-A}	Input resistance	80	100	120	Ω	Between true and complement inputs.

Table 6. High-Speed Data Outputs (Y, $\overline{Y}$) — Differential CML

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{OUT-LD}	Serial data output voltage swing, Nominal Drive mode	505		850	mVp-p	Peak-to-peak differential amplitude between true and complement outputs terminated 50 Ω to V_{CC}.
V_{OUT-HD}	Serial data output voltage swing, Pre-emphasis mode	1000		1700	mVp-p	Peak-to-peak differential amplitude between true and complement outputs terminated 50 Ω to V_{CC}.
R_{OUT-Y}	Back-terminated output resistance	40	50	60	Ω	See Figure 3, page 7.

Table 7. LVTTL/CMOS Input Signals

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{IH}	Input HIGH voltage	1.7	V_{DDO} + 1.0	V	V_{DDO} = 2.5 V or 3.3 V.
V_{IL}	Input LOW voltage	0	0.8	V	V_{DDO} = 2.5 V or 3.3 V.
I_{IH}	Input HIGH current		100	µA	
I_{IL}	Input LOW current	–100		µA	

Table 8. Power Supply Requirements

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{CC}	Power supply voltage	2.375	2.5	2.625	V	±5% tolerance.
V_{DDO}	Power supply voltage (Pre-emphasis and ISE control optional 2.5 V or 3.3 V)	2.375	2.5 or 3.3	3.465	V	±5% tolerance.
P_{D-LD}	Total power dissipation, Nominal Drive mode			2.1	W	
P_{D-HD}	Total power dissipation, Pre-emphasis mode			2.65	W	

Operating Conditions

Table 9. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{CC}	Power supply voltage	2.375	2.5	2.625	V	
V_{DDO}	Power supply voltage		2.5 or 3.3		V	Optional, depending on control signals.
T	Operating temperature range(1)	0		+110	°C	

1. Lower limit of specification is ambient temperature and upper limit is die backside temperature.

Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{CC}	Power supply voltage, potential to GND	–0.5	+3.5	V
	DC input voltage applied (TTL)	–0.5	V_{CC} +1.0	V
	DC input voltage applied (CML)	–0.5	V_{CC} +0.5	V
I_{OUT}	Output current	–50	+50	mA
T_C	Case temperature under bias	–30	+125	°C
T_S	Storage temperature	–40	+125	°C
V_{ESD}	Electrostatic discharge (human body model)	–500	+500	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

I/O Equivalent Circuits

Input Termination

Termination resistor pairs are isolated between each input to minimize crosstalk. The termination will self-bias to +2.0 V (nominal) for AC-coupled applications.

All input data must be differential and nominally biased to +2.0 V, relative to V_{EE}, or AC-coupled. Internal terminations are provided with nominally 50 Ω resistors from the true and complement inputs to a common bias point.

Output Termination

The high-speed outputs of the VSC7108 are current sinks, internally back-terminated by 50 Ω pull-up resistors to the positive supply rail. Typical DC terminations are 50Ω pull-up resistors to the positive supply rail, 50 Ω terminations to +2.0 V, and 100 Ω terminations from true to complement.

Data outputs are provided through differential current switches with on-chip 50 Ω back-termination. Two drive modes are provided to facilitate power and/or noise margin optimization.

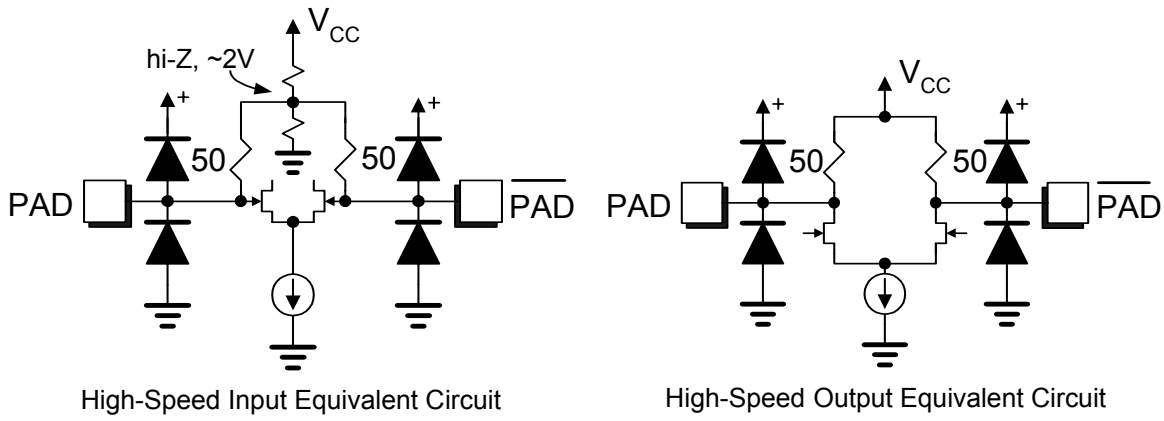


Figure 3. Input and Output Equivalent Circuits

Package Information

The VSC7108 device is available in several packages. VSC7108VP and VSC7108VP-01 is a 69-pin ceramic ball grid array (CBGA) with an 8 mm × 8 mm body size and a 0.8 mm pin pitch. VSC7108SX and VSC7108SX-01 is a 69-pin CBGA with a 10 mm × 10 mm body size and a 1.0 mm pin pitch. VSC7108 is also available in lead(Pb)-free packages designated as VSC7108XVP, VSC7108XVP-01, VSC7108XSX, and VSC7108XSX-01.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides package information including the pin diagram and pin descriptions, package drawings, thermal specifications, and moisture sensitivity information.

Pin Diagram

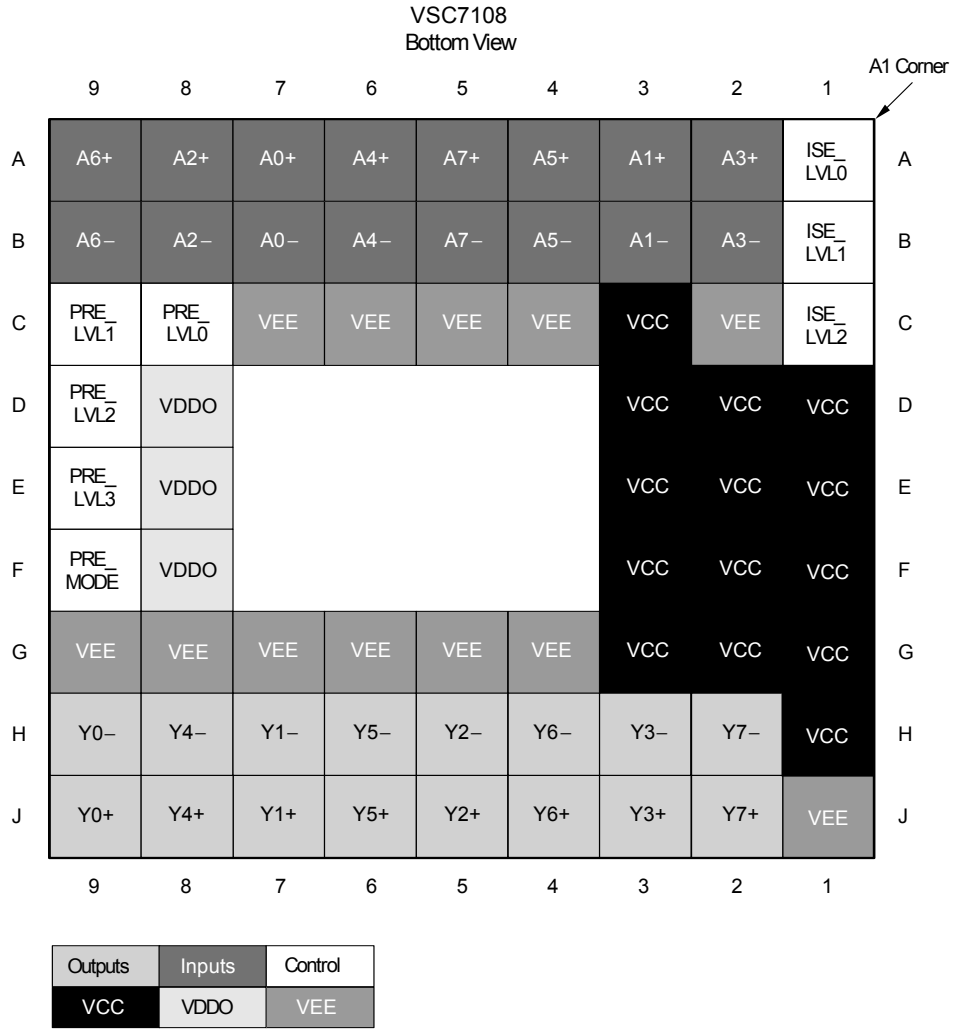


Figure 4. Pin Diagram for the 69-Pin CBGA

Pinout Information

Table 11. Data Input Pins

Signal	Pin Number	Level	Description
A0–	B7	CML	Data input channel 0, complement.
A0+	A7	CML	Data input channel 0, true.
A1–	B3	CML	Data input channel 1, complement.
A1+	A3	CML	Data input channel 1, true.
A2–	B8	CML	Data input channel 2, complement.
A2+	A8	CML	Data input channel 2, true.
A3–	B2	CML	Data input channel 3, complement.
A3+	A2	CML	Data input channel 3, true.
A4–	B6	CML	Data input channel 4, complement.
A4+	A6	CML	Data input channel 4, true.
A5–	B4	CML	Data input channel 5, complement.
A5+	A4	CML	Data input channel 5, true.
A6–	B9	CML	Data input channel 6, complement.
A6+	A9	CML	Data input channel 6, true.
A7–	B5	CML	Data input channel 7, complement.
A7+	A5	CML	Data input channel 7, true.
PRE_LVL0	C8	LVTTL	Pre-emphasis time constant (LSB).
PRE_LVL1	C9	LVTTL	Pre-emphasis time constant.
PRE_LVL2	D9	LVTTL	Pre-emphasis time constant.
PRE_LVL3	E9	LVTTL	Pre-emphasis time constant (MSB).
PRE_MODE	F9	LVTTL	Pre-emphasis mode control, 1= on, 0 = off.
ISE_LVL0	A1	LVTTL	Input Signal Equalization level (LSB).
ISE_LVL1	B1	LVTTL	Input Signal Equalization level.
ISE_LVL2	C1	LVTTL	Input Signal Equalization level (MSB).

Table 12. Data Output Pins

Signal	Pin Number	Level	Description
Y0–	H9	CML	Data output channel 0, complement.
Y0+	J9	CML	Data output channel 0, true.
Y1–	H7	CML	Data output channel 1, complement.
Y1+	J7	CML	Data output channel 1, true.
Y2–	H5	CML	Data output channel 2, complement.
Y2+	J5	CML	Data output channel 2, true.
Y3–	H3	CML	Data output channel 3, complement.
Y3+	J3	CML	Data output channel 3, true.
Y4–	H8	CML	Data output channel 4, complement.
Y4+	J8	CML	Data output channel 4, true.
Y5–	H6	CML	Data output channel 5, complement.

Table 12. Data Output Pins *(continued)*

Signal	Pin Number	Level	Description
Y5+	J6	CML	Data output channel 5, true.
Y6–	H4	CML	Data output channel 6, complement.
Y6+	J4	CML	Data output channel 6, true.
Y7–	H2	CML	Data output channel 7, complement.
Y7+	J2	CML	Data output channel 7, true.

Table 14. Control Pins

Signal	Pin Number	I/O	Level	Description
PRE_LVL0	C8	I	LVTL	Pre-emphasis time constant (LSB).
PRE_LVL1	C9	I	LVTTL	Pre-emphasis time constant.
PRE_LVL2	D9	I	LVTTL	Pre-emphasis time constant.
PRE_LVL3	E9	I	LVTTL	Pre-emphasis time constant (MSB).
PRE_MODE	F9	I	LVTTL	Pre-emphasis mode control; 1 = ON, 0 = OFF.
ISE_LVL0	A1	I	LVTTL	Input signal equalization level (LSB).
ISE_LVL1	B1	I	LVTTL	Input signal equalization level.
ISE_LVL	C1	I	LVTTL	Input signal equalization level (LSB).

Table 15. Power Supply Pins

Signal	Pin Number	Description
VCC	C3, D1, D2, D3, E1, E2, E3, F1, F2, F3, G1, G2, G3, H1	Positive power supply, +2.5 V.
VDDO	D8, E8, F8	Positive power supply for control port, V_{CC} or 3.3 V.
VEE	C2, C4, C5, C6, C7, G4, G5, G6, G7, G8, G9, J1	Ground.

Package Drawings

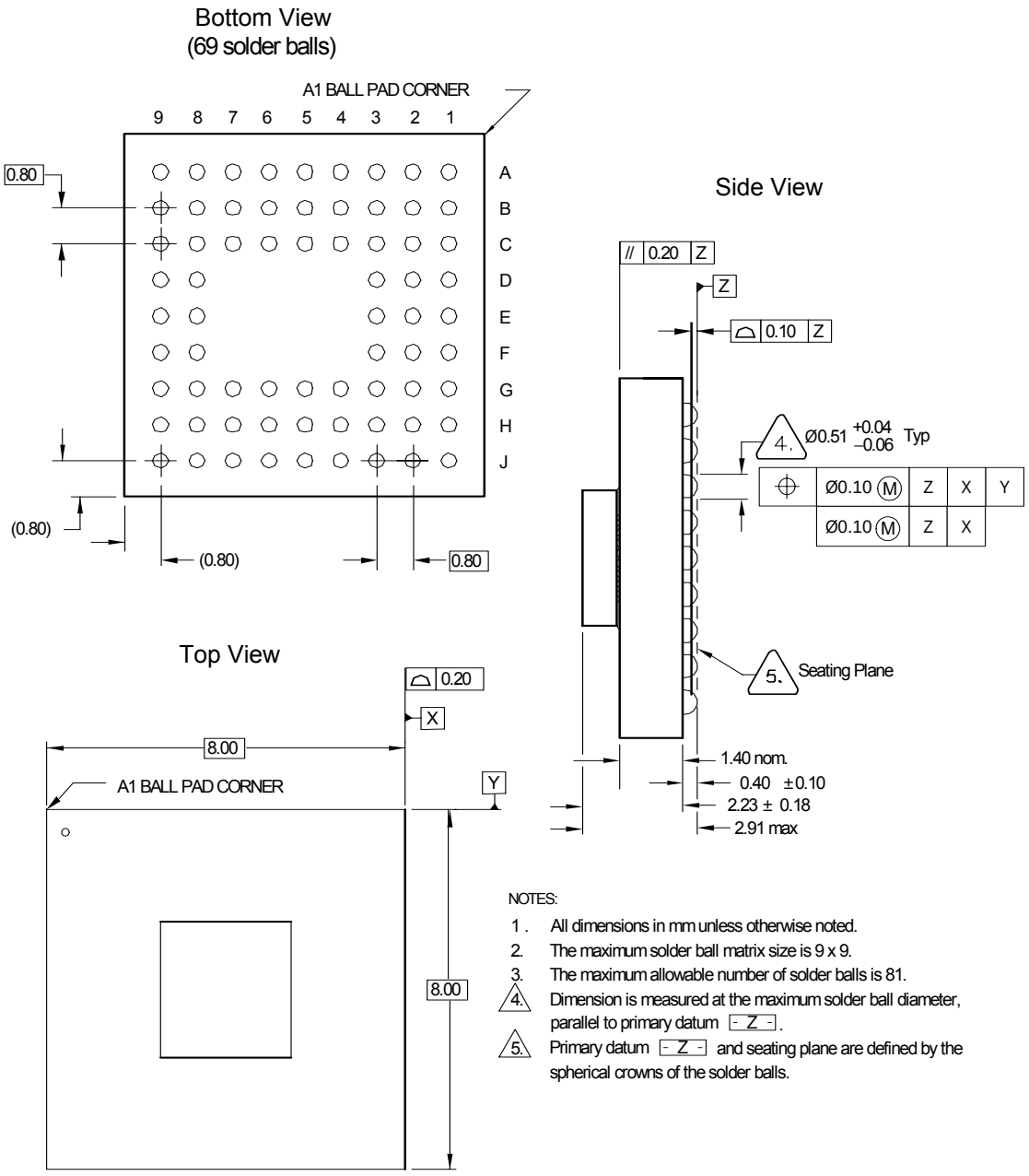
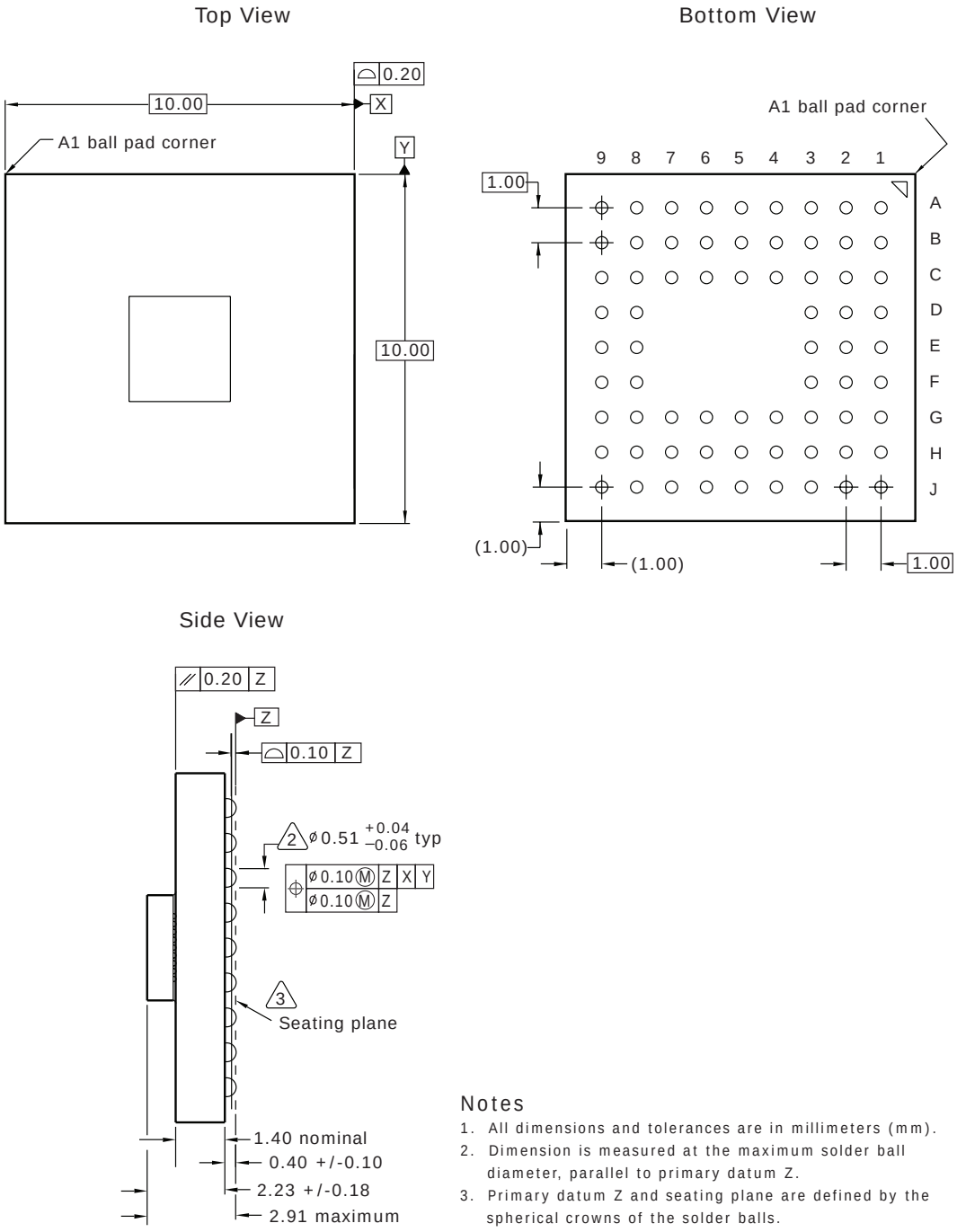


Figure 5. Package Drawing for the 69-Pin CBGA (VP and XVP)



Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls.

Figure 6. Package Drawing for the 69-Pin CBGA (SX and XSX)

Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 16. Thermal Resistances

Part Number	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC7108VP VSC7108VP-01	0.5	32	29	27
VSC7108XVP VSC7108XVP-01	0.5	32	29	27
VSC7108SX VSC7108SX-01	0.5	32	29	27
VSC7108XSX VSC7108XSX-01	0.5	32	29	27

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

Ordering Information

This section contains the ordering information for the VSC7108 and VSC7108-01, which are electrically identical devices. VSC7108-01 represents a manufacturing update.

The VSC7108 device is available in several packages. VSC7108VP and VSC7108VP-01 is a 69-pin ceramic ball grid array (CBGA) with an 8 mm × 8 mm body size and a 0.8 mm pin pitch. VSC7108SX and VSC7108SX-01 is a 69-pin CBGA with a 10 mm × 10 mm body size and a 1.0 mm pin pitch. VSC7108 is also available in lead(Pb)-free packages designated as VSC7108XVP, VSC7108XVP-01, VSC7108XSX, and VSC7108XSX-01.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

Because of the small package size, the devices are designated by a four-letter code located on the first line of the marking on the package. The following table shows the ordering information, including this four-letter device code.

VSC7108 6.5 Gbps Octal Signal Conditioner

Part Number	Device Code	Description
VSC7108VP	AYCF	69-pin CBGA, 8 mm x 8 mm body size, 0.8 mm pin pitch
VSC7108VP-01	CQDF	69-pin CBGA, 8 mm x 8 mm body size, 0.8 mm pin pitch
VSC7108XVP	BSCF	Lead(Pb)-free 69-pin CBGA, 8 mm x 8 mm body size, 0.8 mm pin pitch
VSC7108XVP-01	CRDF	Lead(Pb)-free 69-pin CBGA, 8 mm x 8 mm body size, 0.8 mm pin pitch
VSC7108SX	BJCF	69-pin CBGA, 10 mm x 10 mm body size, 1.0 mm pin pitch
VSC7108SX-01	CYDF	69-pin CBGA, 10 mm x 10 mm body size, 1.0 mm pin pitch
VSC7108XSX	BVCF	Lead(Pb)-free 69-pin CBGA, 10 mm x 10 mm body size, 1.0 mm pin pitch
VSC7108XSX-01	CZDF	Lead(Pb)-free 69-pin CBGA, 10 mm x 10 mm body size, 1.0 mm pin pitch

CORPORATE HEADQUARTERS
Vitesse Semiconductor Corporation
741 Calle Plano
Camarillo, CA 93012
Tel: 1-800-VITESSE • FAX:1-(805) 987-5896

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