# Dual N-Channel 30-V (D-S) MOSFET with Schottky Diode

## PRODUCT SUMMARY

| | $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) | $I_D$ (A) |
|---|---|---|---|
| Channel-1 | 30 | 0.022 at $V_{GS}$ = 10 V | 6.3 |
| | | 0.030 at $V_{GS}$ = 4.5 V | 5.4 |
| Channel-2 | | 0.013 at $V_{GS}$ = 10 V | 10 |
| | | 0.0185 at $V_{GS}$ = 4.5 V | 8.6 |

## SCHOTTKY PRODUCT SUMMARY

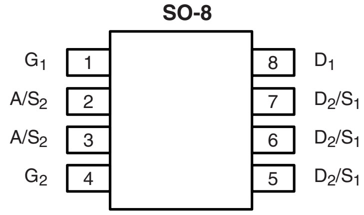
| $V_{DS}$ (V) | $V_{SD}$ (V) Diode Forward Voltage | $I_F$ (A) |
|---|---|---|
| 30 | 0.50 V at 1.0 A | 2.0 |

## FEATURES

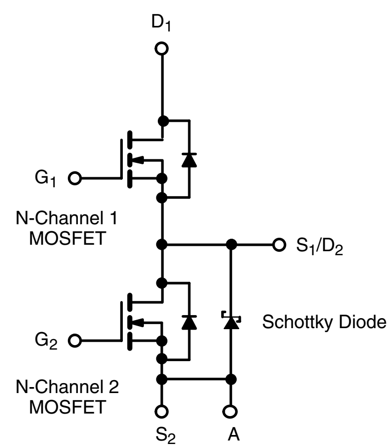
- **Halogen-free According to IEC 61249-2-21 Definition**
- LITTLE FOOT® *Plus* Power MOSFET
- 100 % $R_g$ Tested
- Compliant to RoHS Directive 2002/95/EC

RoHS COMPLIANT
HALOGEN FREE Available

SO-8




Top View




**Ordering Information:** Si4816DY-T1-E3 (Lead (Pb)-free)
Si4816DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

## ABSOLUTE MAXIMUM RATINGS $T_A$ = 25 °C, unless otherwise noted

| Parameter | | Symbol | Channel-1 10 s | Channel-1 Steady State | Channel-2 10 s | Channel-2 Steady State | Unit |
|---|---|---|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 30 | | | | V |
| Gate-Source Voltage | | $V_{GS}$ | 20 | | | | V |
| Continuous Drain Current ($T_J$ = 150 °C)[a] | $T_A$ = 25 °C | $I_D$ | 6.3 | 5.3 | 10 | 7.7 | A |
| | $T_A$ = 70 °C | | 5.4 | 4.2 | 8.2 | 6.2 | |
| Pulsed Drain Current | | $I_{DM}$ | 30 | | 40 | | |
| Continuous Source Current (Diode Conduction)[a] | | $I_S$ | 1.3 | 0.9 | 2.2 | 1.15 | |
| Avalanche Current[b] | L = 0.1 mH | $I_{AS}$ | 12 | | 25 | | |
| Single Pulse Avalanche Energy[b] | | $E_{AS}$ | 7.2 | | 31.25 | | mJ |
| Maximum Power Dissipation[a] | $T_A$ = 25 °C | $P_D$ | 1.4 | 1.0 | 2.4 | 1.25 | W |
| | $T_A$ = 70 °C | | 0.9 | 0.64 | 1.5 | 0.8 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | - 55 to 150 | | | | °C |

## THERMAL RESISTANCE RATINGS

| Parameter | | Symbol | Channel-1 Typ. | Channel-1 Max. | Channel-2 Typ. | Channel-2 Max. | Schottky Typ. | Schottky Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Maximum Junction-to-Ambient[a] | t ≤ 10 s | $R_{thJA}$ | 72 | 90 | 43 | 53 | 48 | 60 | °C/W |
| | Steady State | | 100 | 125 | 82 | 100 | 80 | 100 | |
| Maximum Junction-to-Foot (Drain) | Steady State | $R_{thJC}$ | 51 | 63 | 25 | 30 | 28 | 35 | |

Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. Starting date code W46BAA.

| MOSFET SPECIFICATIONS $T_J$ = 25 °C, unless otherwise noted | | | | | | | |
|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Test Conditions | | Min. | Typ.[a] | Max. | Unit |
| **Static** | | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = 250 µA | Ch-1 | 0.8 | | 2 | V |
| | | | Ch-2 | 1.0 | | 3 | |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = 20 V | Ch-1 | | | 100 | nA |
| | | | Ch-2 | | | 100 | |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V | Ch-1 | | | 1 | µA |
| | | | Ch-2 | | | 100 | |
| | | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V, $T_J$ = 85 °C | Ch-1 | | | 15 | |
| | | | Ch-2 | | | 2000 | |
| On-State Drain Current[b] | $I_{D(on)}$ | $V_{DS}$ = 5 V, $V_{GS}$ = 10 V | Ch-1 | 20 | | | A |
| | | | Ch-2 | 30 | | | |
| Drain-Source On-State Resistance[b] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 6.3 A | Ch-1 | | 0.018 | 0.022 | Ω |
| | | $V_{GS}$ = 10 V, $I_D$ = 10 A | Ch-2 | | 0.0105 | 0.013 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 5.4 A | Ch-1 | | 0.024 | 0.030 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 8.6 A | Ch-2 | | 0.015 | 0.0185 | |
| Forward Transconductance[b] | $g_{fs}$ | $V_{DS}$ = 15 V, $I_D$ = 6.3 A | Ch-1 | | 17 | | S |
| | | $V_{DS}$ = 15 V, $I_D$ = 10 A | Ch-2 | | 28 | | |
| Diode Forward Voltage[b] | $V_{SD}$ | $I_S$ = 1.3 A V, $V_{GS}$ = 0 V | Ch-1 | | 0.7 | 1.1 | V |
| | | $I_S$ = 1 A V, $V_{GS}$ = 0 V | Ch-2 | | 0.47 | 0.5 | |
| **Dynamic[a]** | | | | | | | |
| Total Gate Charge | $Q_g$ | Channel-1<br>$V_{DS}$ = 15 V, $V_{GS}$ = 5 V, $I_D$ = 6.3 A<br><br>Channel-2<br>$V_{DS}$ = 15 V, $V_{GS}$ = 5 V, $I_D$ = - 10 A | Ch-1 | | 8.0 | 12 | nC |
| | | | Ch-2 | | 15 | 23 | |
| Gate-Source Charge | $Q_{gs}$ | | Ch-1 | | 1.75 | | |
| | | | Ch-2 | | 5.3 | | |
| Gate-Drain Charge | $Q_{gd}$ | | Ch-1 | | 3.2 | | |
| | | | Ch-2 | | 4.6 | | |
| Gate Resistance | $R_g$ | | Ch-1 | 1.5 | | 6.1 | Ω |
| | | | Ch-2 | 0.5 | | 2.6 | |
| Turn-On Delay Time | $t_{d(on)}$ | Channel-1<br>$V_{DD}$ = 15 V, $R_L$ = 15 Ω<br>$I_D \cong$ 1 A, $V_{GEN}$ = 10 V, $R_g$ = 6 Ω<br><br>Channel-2<br>$V_{DD}$ = 15 V, $R_L$ = 15 Ω<br>$I_D \cong$ 1 A, $V_{GEN}$ = 10 V, $R_g$ = 6 Ω | Ch-1 | | 10 | 20 | ns |
| | | | Ch-2 | | 15 | 30 | |
| Rise Time | $t_r$ | | Ch-1 | | 5 | 10 | |
| | | | Ch-2 | | 5 | 10 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | Ch-1 | | 26 | 50 | |
| | | | Ch-2 | | 44 | 80 | |
| Fall Time | $t_f$ | | Ch-1 | | 8 | 16 | |
| | | | Ch-2 | | 12 | 24 | |
| Source-Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = 1.3 A, dI/dt = 100 A/µs | Ch-1 | | 30 | 60 | |
| | | $I_F$ = 2.2 A, dI/dt = 100 µA/µs | Ch-2 | | 32 | 70 | |

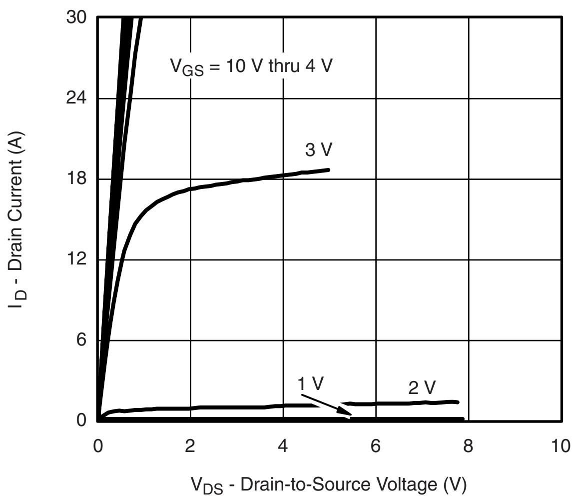
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

| SCHOTTKY SPECIFICATIONS $T_J$ = 25 °C, unless otherwise noted | | | | | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
| Forward Voltage Drop | $V_F$ | $I_F$ = 1.0 A | | 0.47 | 0.50 | V |
| | | $I_F$ = 1.0 A, $T_J$ = 125 °C | | 0.36 | 0.42 | |
| Maximum Reverse Leakage Current | $I_{rm}$ | $V_R$ = 30 V | | 0.004 | 0.100 | mA |
| | | $V_R$ = 30 V, $T_J$ = 100 °C | | 0.7 | 10 | |
| | | $V_R$ = - 30 V, $T_J$ = 125 °C | | 3.0 | 20 | |
| Junction Capacitance | $C_T$ | $V_R$ = 10 V | | 50 | | pF |

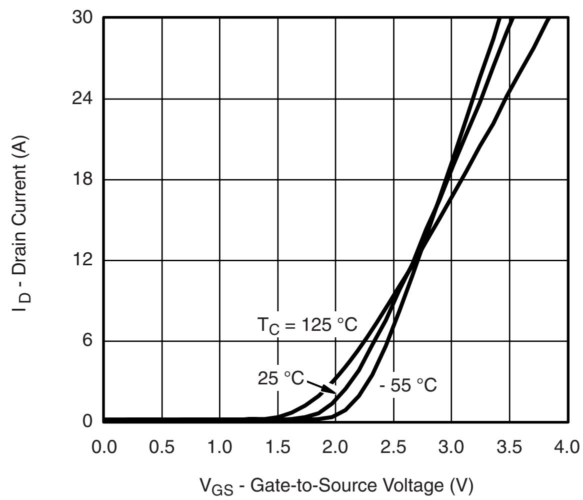
*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*


Document Number: 71121
S09-0868-Rev. G, 18-May-09

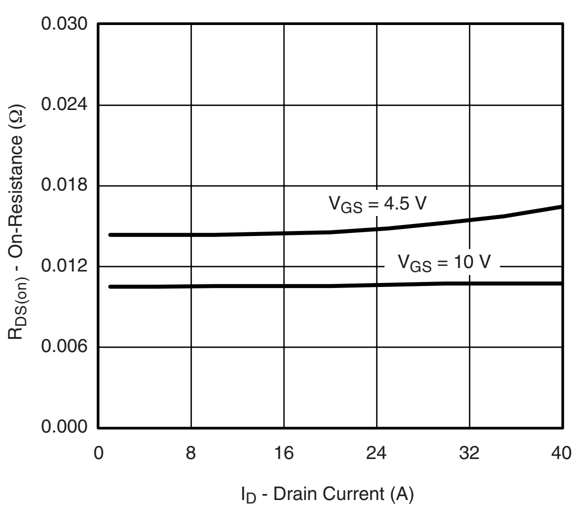
**CHANNEL-1 TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



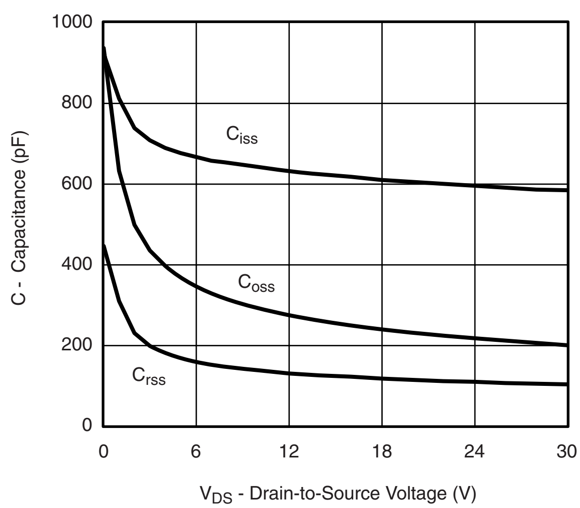

**Output Characteristics**



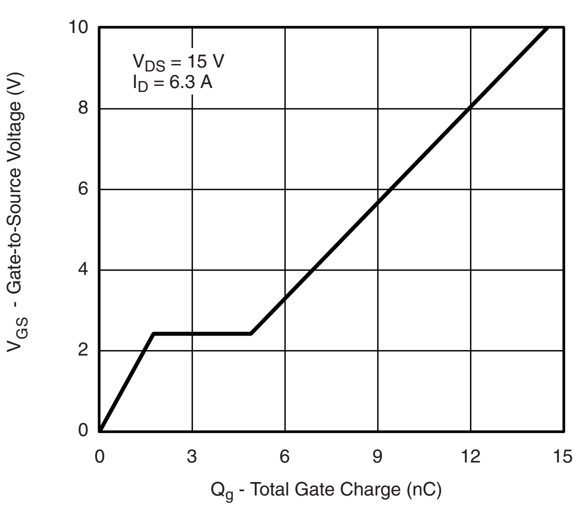

**Transfer Characteristics**



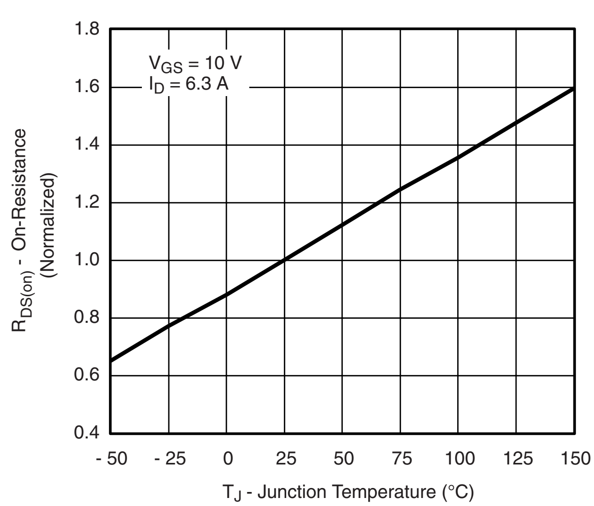

**On-Resistance vs. Drain Current**




**Capacitance**

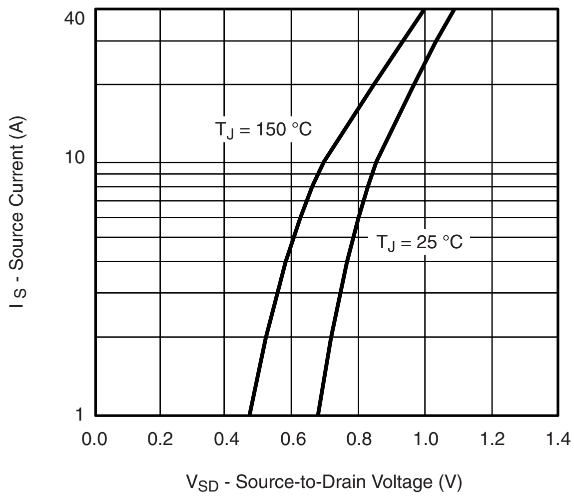



**Gate Charge**

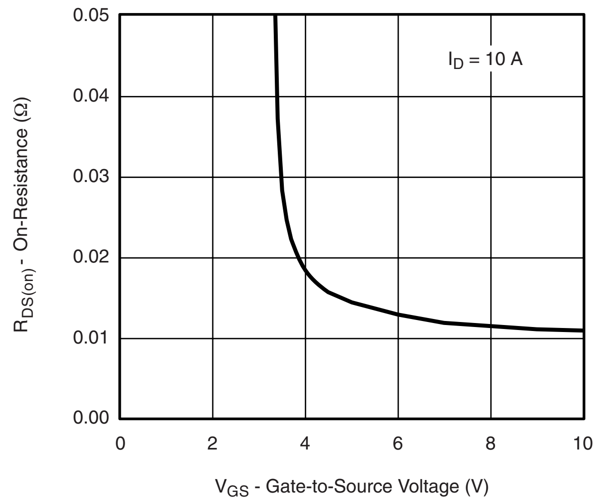



**On-Resistance vs. Junction Temperature**

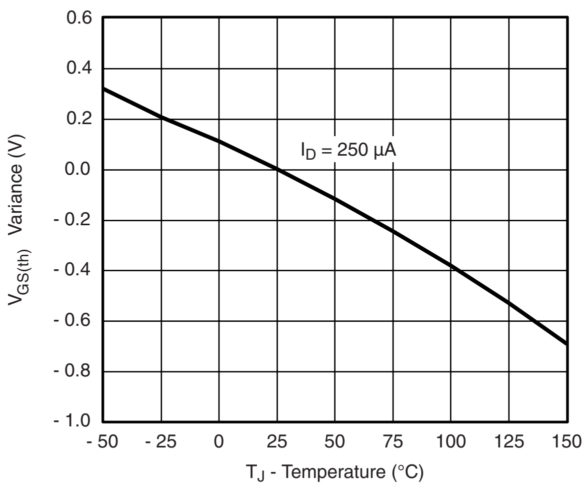
**CHANNEL-1 TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



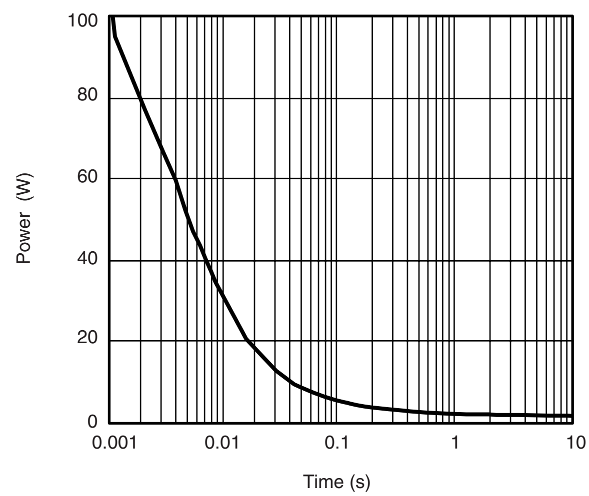

**Source-Drain Diode Forward Voltage**



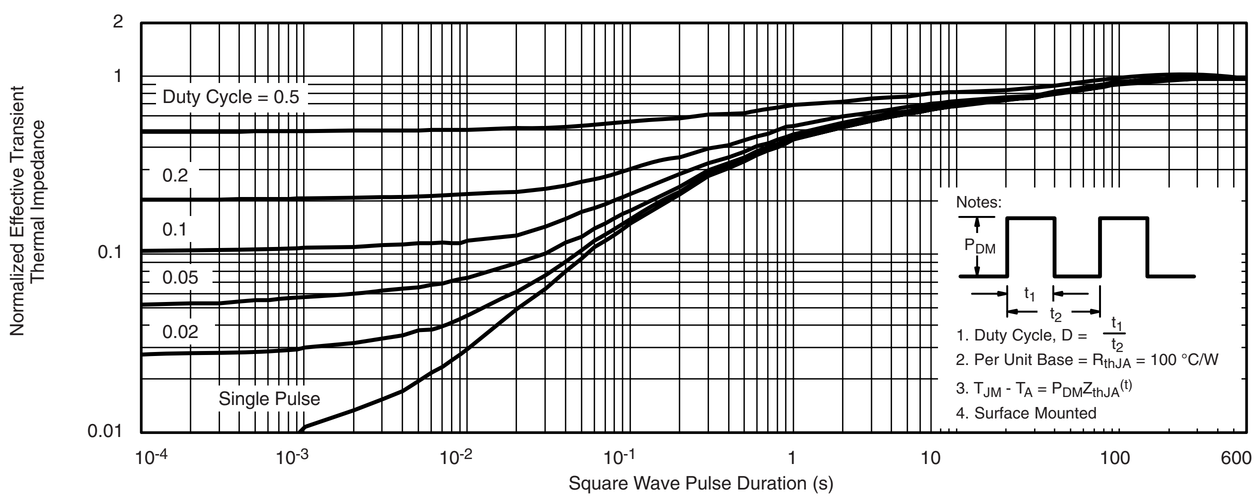

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**

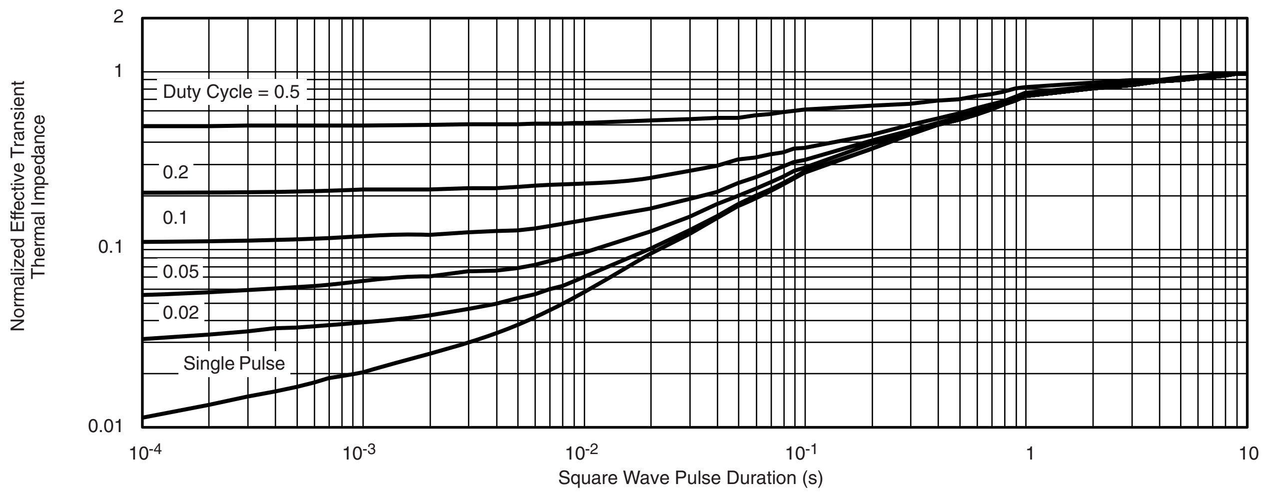



**Single Pulse Power, Junction-to-Ambient**



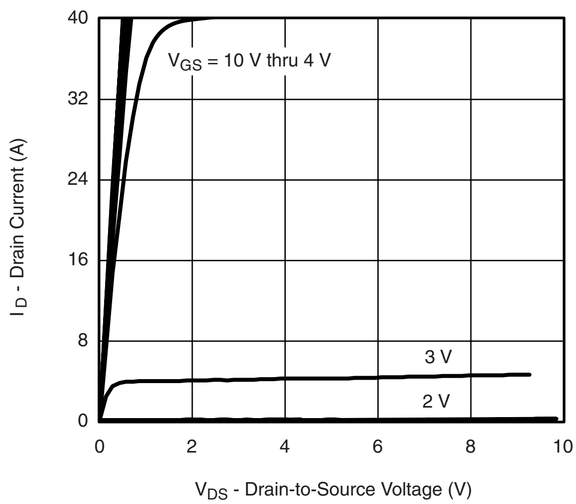

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

## CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

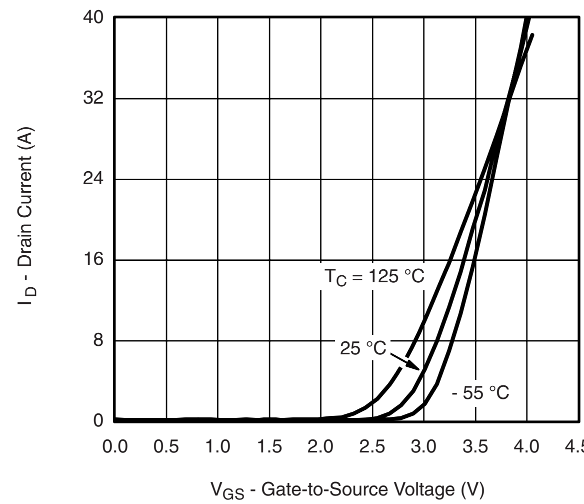



**Normalized Thermal Transient Impedance, Junction-to-Foot**

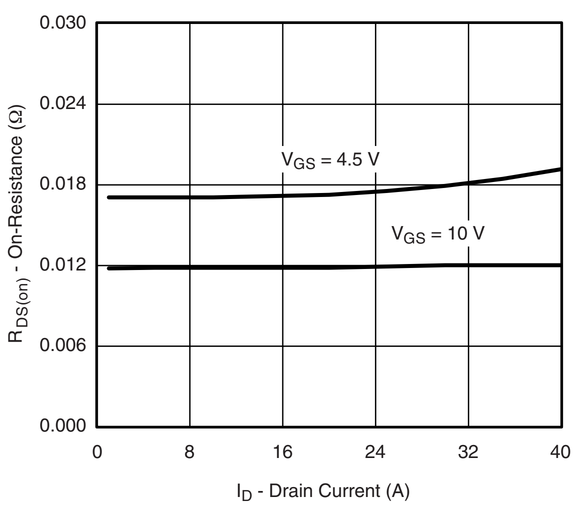
## CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



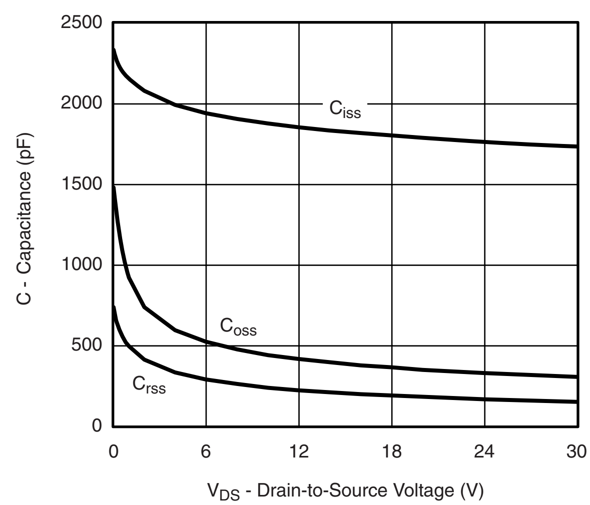

**Output Characteristics**




**Transfer Characteristics**

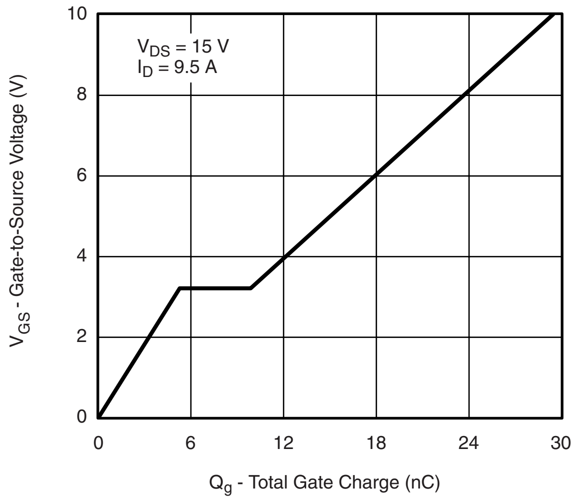



**On-Resistance vs. Drain Current**

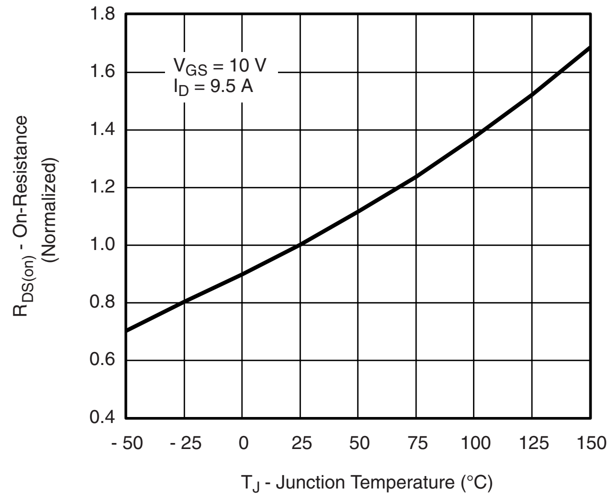



**Capacitance**

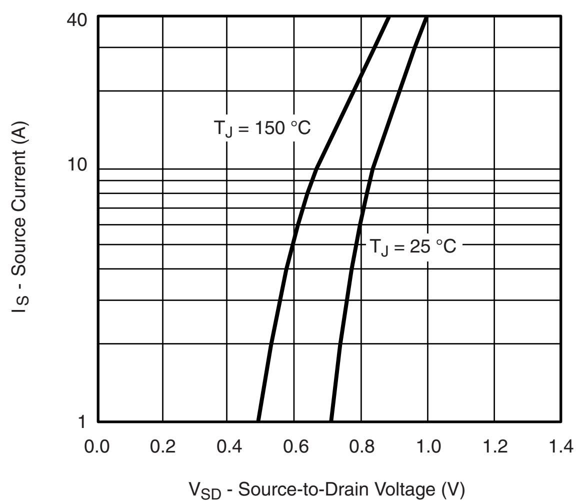
**CHANNEL-2 TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



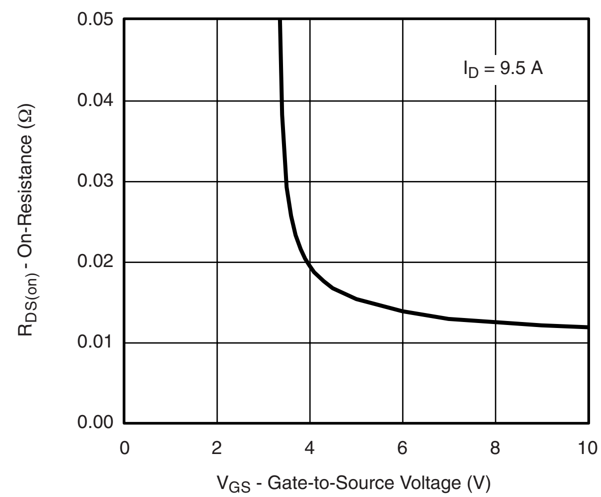

**Gate Charge**



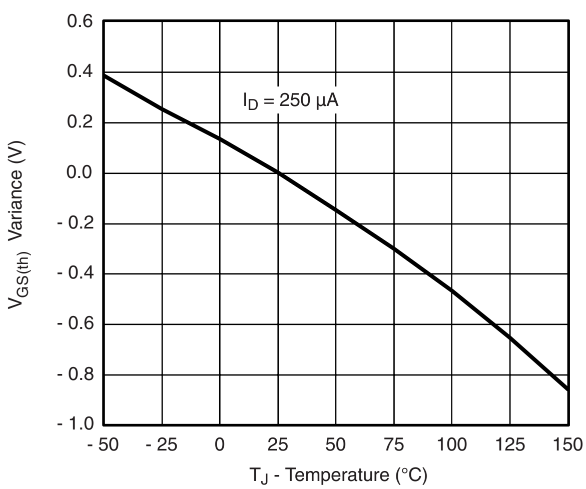

**On-Resistance vs. Junction Temperature**



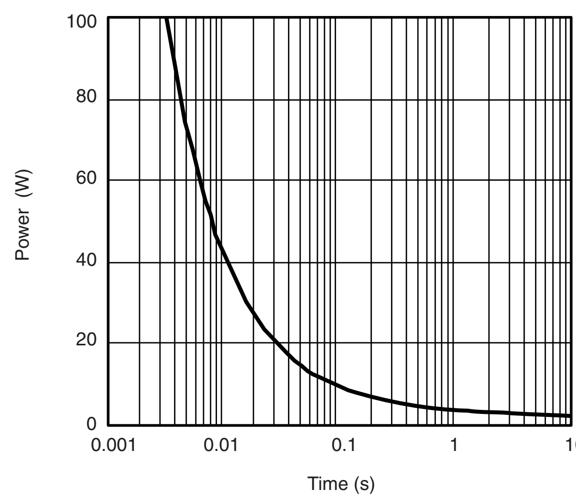

**Source-Drain Diode Forward Voltage**




**On-Resistance vs. Gate-to-Source Voltage**

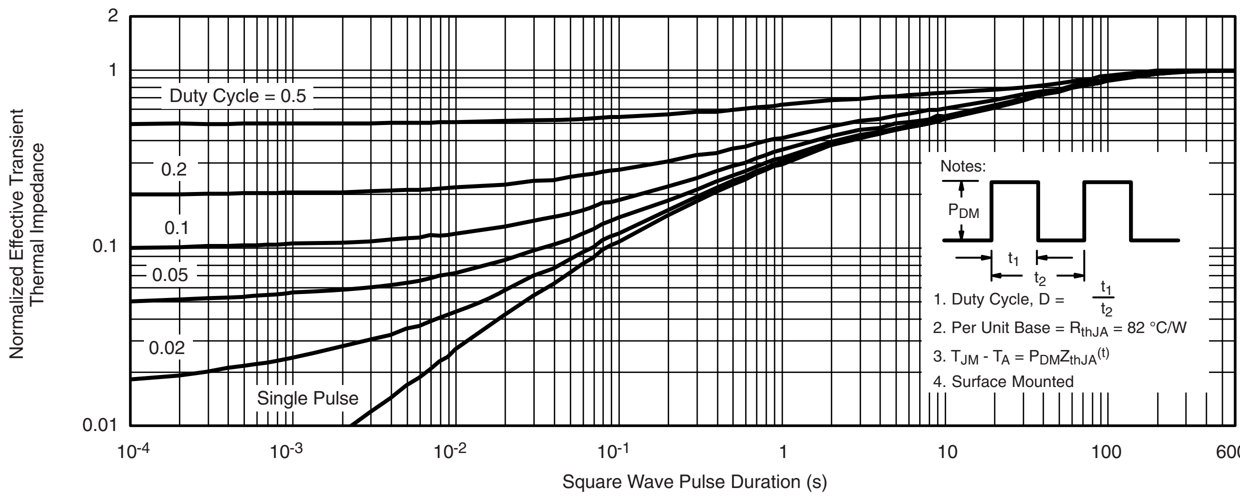



**Threshold Voltage**

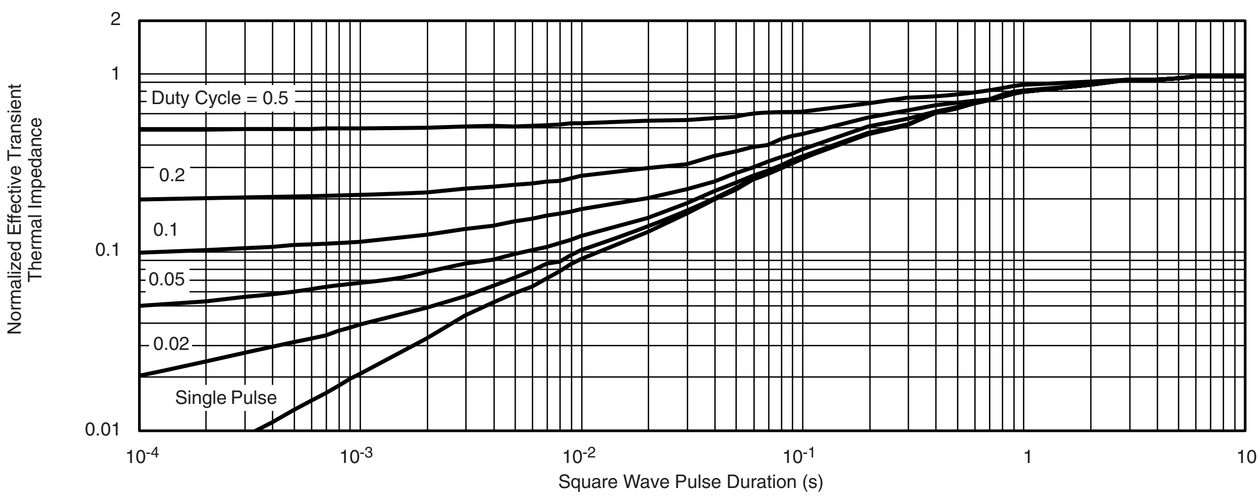



**Single Pulse Power, Junction-to-Ambient**

**CHANNEL-2 TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

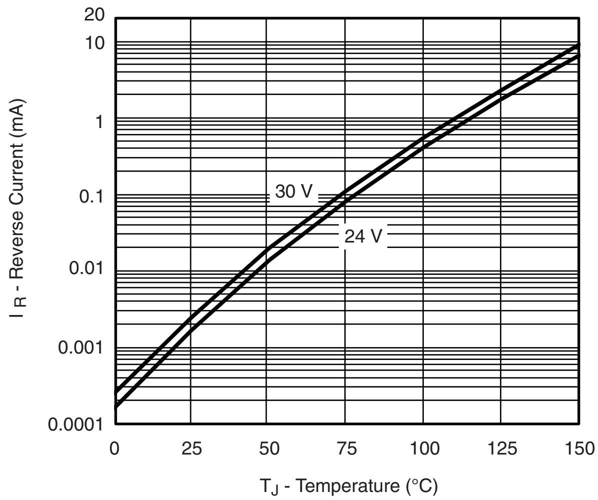



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

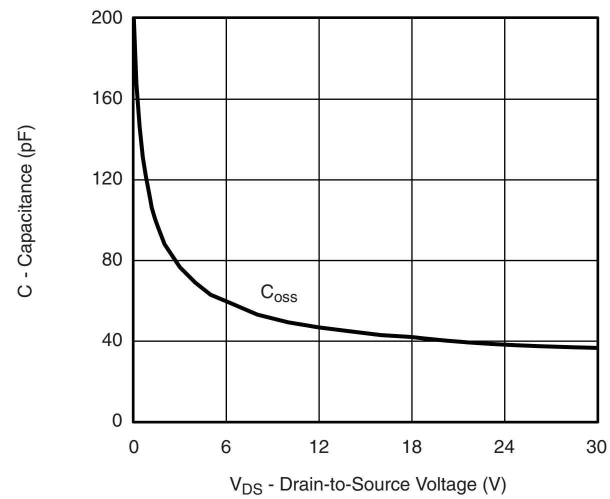



**Normalized Thermal Transient Impedance, Junction-to-Foot**

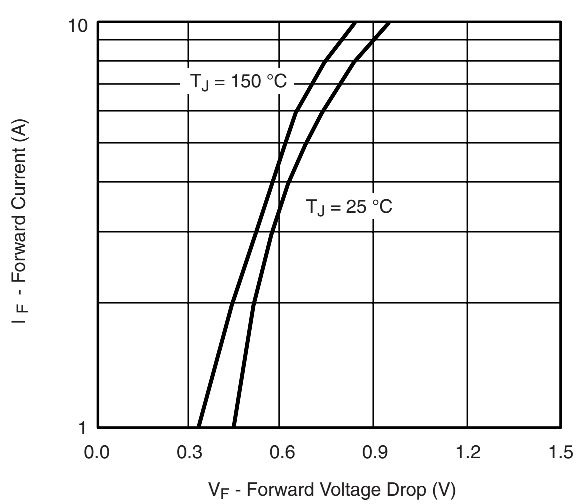
**SCHOTTKY TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted




**Reverse Current vs. Junction Temperature**




**Capacitance**

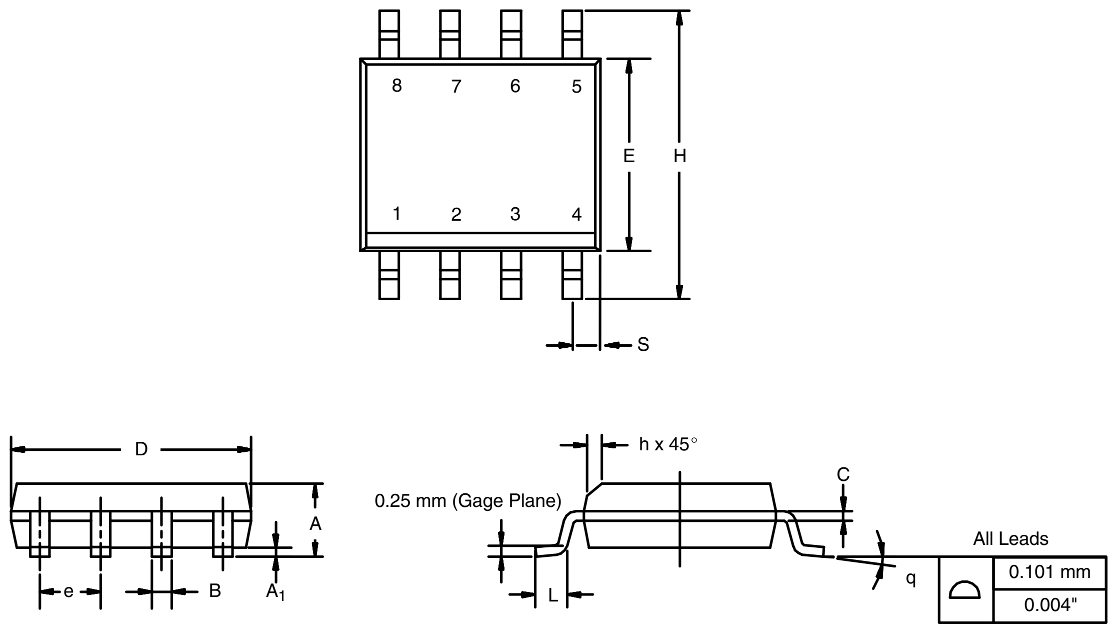



**Forward Voltage Drop**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71121.*

## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012




| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| $A_1$ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.35 | 0.51 | 0.014 | 0.020 |
| C | 0.19 | 0.25 | 0.0075 | 0.010 |
| D | 4.80 | 5.00 | 0.189 | 0.196 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.020 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| q | 0° | 8° | 0° | 8° |
| S | 0.44 | 0.64 | 0.018 | 0.026 |
| ECN: C-06527-Rev. I, 11-Sep-06<br>DWG: 5498 | | | | |

# Mounting LITTLE FOOT®, SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/ppg?72286), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

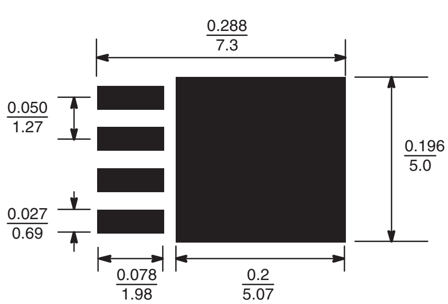



Figure 1. Single MOSFET SO-8 Pad Pattern With Copper Spreading

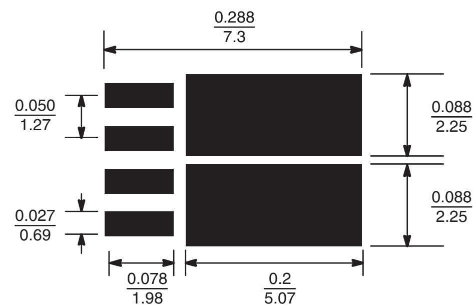


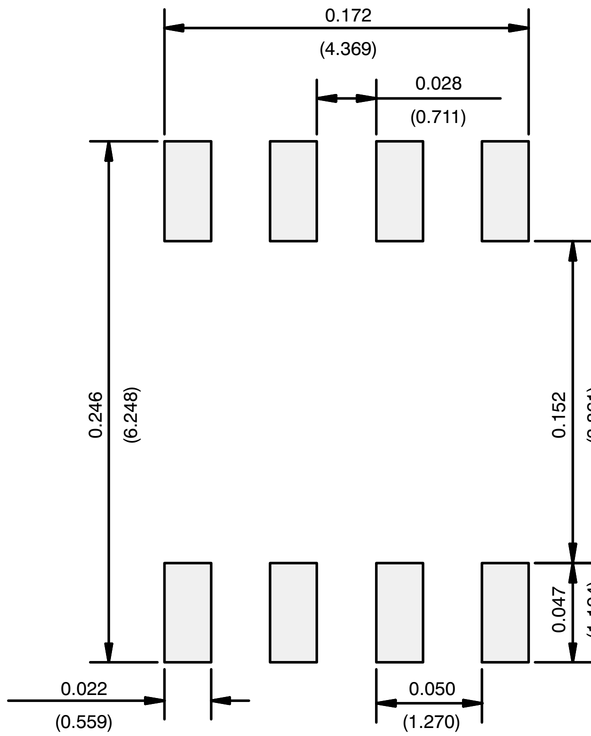

Figure 2. Dual MOSFET SO-8 Pad Pattern With Copper Spreading

The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

**RECOMMENDED MINIMUM PADS FOR SO-8**




Recommended Minimum Pads
Dimensions in Inches/(mm)

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# Material Category Policy

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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

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