

T-4623-14

131,072 WORDS x 8 BIT STATIC RAM

DESCRIPTION

The TC551001PL/FL is 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated a single 5 V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5 mA / MHz (Typ.) and minimum cycle time of 85 / 100 ns. When $\overline{CE1}$ is a logical high, or $\overline{CE2}$ is low, the device is placed in low power standby mode in which standby current is 2 μ A typically. The TC551001PL/FL has three control inputs. Chip enable inputs ($\overline{CE1}, \overline{CE2}$) allow for device selection and data retention control, and an output enable input (\overline{OE}) provides fast memory access. Thus the TC551001PL/FL is suitable for use in various microprocessor application system where high speed, low power, and battery back up are required.

The TC551001PL/FL is offered in both a dual-in-line 32 pin standard plastic package and small-out line plastic flat package.

FEATURES

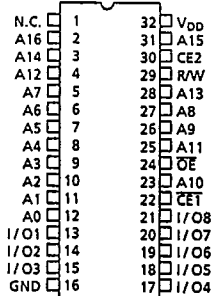
- Low Power Dissipation : 27.5 mW / MHz (Typ.)
- Standby Current : 100 μ A (Max.)
- 5 V Single Power Supply
- Power Down Feature : $\overline{CE1}, \overline{CE2}$
- Data retention Supply Voltage : 2.0 ~ 5.5 V
- Directly TTL Compatible : All Inputs and Outputs

• Access Time

| | TC551001 PL/FL-85 | TC551001 PL/FL-10 |
|-------------------------------------|-------------------|-------------------|
| Access Time (max.) | 85 ns | 100 ns |
| $\overline{CE1}$ Access Time (max.) | 85 ns | 100 ns |
| $\overline{CE2}$ Access Time (max.) | 85 ns | 100 ns |
| \overline{OE} Access Time (max.) | 45 ns | 50 ns |

- Package : TC551001PL : DIP32-P-600
- TC551001FL : SOP32-P-525

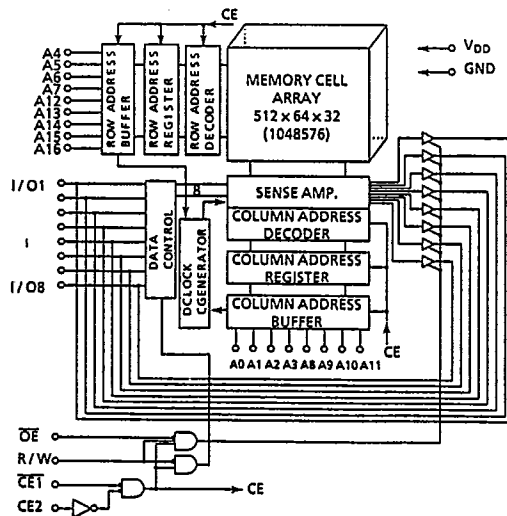
PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|----------------------------------|--------------------------|
| A0-A16 | Address Inputs |
| R/W | Read/Write Control Input |
| \overline{OE} | Output Enable Input |
| $\overline{CE1}, \overline{CE2}$ | Chip Enable Input |
| I/O1-I/O8 | Data Input/Output |
| V _{DD} | Power (+ 5 V) |
| GND | Ground |
| N.C. | No Connection |

BLOCK DIAGRAM



TC551001PL-85/PL-10
 TC551001FL-85/FL-10

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OPERATION MODE

| OPERATION MODE | $\overline{CE1}$ | CE2 | \overline{OE} | RAW | I/O1 ~ I/O8 | POWER |
|-----------------|------------------|-----|-----------------|-----|------------------|-----------------|
| Read | L | H | L | H | D _{OUT} | I _{DD} |
| Write | L | H | * | L | D _{IN} | I _{DD} |
| Output Deselect | L | H | H | H | High-Z | I _{DD} |
| Standby | H | * | * | * | High-Z | I _{DD} |
| | * | L | * | * | High-Z | I _{DD} |

* : H or L

ABSOLUTE MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|---------------------|--------------------------|------------------------------|----------|
| V _{DD} | Power Supply Voltage | -0.3 ~ 7.0 | V |
| V _{IN} | Input Voltage | -0.3* ~ 7.0 | V |
| V _{IO} | Input and Output Voltage | -0.5 - V _{DD} + 0.5 | V |
| P _D | Power Dissipation | 1.0/0.6** | W |
| T _{solder} | Soldering Temperature | 260 · 10 | °C · sec |
| T _{strg.} | Storage Temperature | -55 ~ 150 | °C |
| T _{opr.} | Operating Temperature | 0 ~ 70 | °C |

* : -3.0V at pulse width 50 ns MAX. ** : SOP

D.C. RECOMMENDED OPERATING CONDITIONS.

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|-------------------------------|------|------|-----------------------|------|
| V _{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.2 | - | V _{DD} + 0.3 | |
| V _{IL} | Input Low Voltage | -0.3 | - | 0.8 | |
| V _{DH} | Data Retention Supply Voltage | 2.0 | - | 5.5 | |

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D.C. and OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|------------------------|---|------|------|-----------|---------------|
| I_{IL} | Input Leakage Current | $V_{IN} = 0 \sim V_{DD}$ | - | - | ± 1.0 | μA |
| I_{OH} | Output High Current | $V_{OH} = 2.4\text{V}$ | -1.0 | - | - | mA |
| I_{OL} | Output Low Current | $V_{OL} = 0.4\text{V}$ | 4.0 | - | - | mA |
| I_{CO} | Output Leakage Current | $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$ | - | - | ± 1.0 | μA |
| I_{DDO1} | Operating Current | $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ and $R/W = V_{IH}$, $I_{OUT} = 0\text{mA}$ Other Inputs = V_{IH}/V_{IL} $t_{\text{cycle}} = \text{Min. cycle}$ | - | - | 80 | mA |
| I_{DDO2} | | $\overline{CE1} = 0.2\text{V}$ and $CE2 = V_{DD} - 0.2\text{V}$ $R/W = V_{DD} - 0.2\text{V}$, $I_{OUT} = 0\text{mA}$ Other Inputs = $V_{DD} - 0.2\text{V}/0.2\text{V}$ $t_{\text{cycle}} = \text{Min. cycle}$ | - | - | 70 | mA |
| I_{DD51} | Standby Current | $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ | - | - | 3 | mA |
| $I_{DD52}^{(1)}$ | | $\overline{CE1} = V_{DD} - 0.2\text{V}$ or $CE2 = 0.2\text{V}$ $V_{DD} = 2.0\text{V} \sim 5.5\text{V}$, $T_a = 0 \sim 70^\circ\text{C}$ | - | 2 | 100 | μA |

Note : (1) In standby mode with $\overline{CE1} \geq V_{DD} - 0.2\text{V}$, these specification limits are guaranteed under the condition of $CE2 \geq V_{DD} - 0.2\text{V}$ or $CE2 \leq 0.2\text{V}$.

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

| SYMBOL | PARAMETER | TEST CONDITION | MAX. | UNIT |
|-----------|--------------------|------------------------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = \text{GND}$ | 10 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = \text{GND}$ | 10 | |

Note : This parameter periodically sampled is not 100 % tested.

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A.C. CHARACTERISTICS (Ta = 0 ~ 70 °C, VDD = 5 V ± 10 %)

Read Cycle

| SYMBOL | PARAMETER | TC551001PL-85 TC551001FL-85 | | TC551001PL-10 TC551001FL-10 | | UNIT |
|------------------|--|--------------------------------|------|--------------------------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 85 | - | 100 | - | ns |
| t _{ACC} | Address Access Time | - | 85 | - | 100 | |
| t _{CO1} | CE1 Access Time | - | 85 | - | 100 | |
| t _{CO2} | CE2 Access Time | - | 85 | - | 100 | |
| t _{OE} | Output Enable to Output in Valid | - | 45 | - | 50 | |
| t _{COE} | Chip Enable (CE1, CE2) to Output in Low-Z | 10 | - | 10 | - | |
| t _{OOE} | Output Enable to Output in Low-Z | 0 | - | 0 | - | |
| t _{OD} | Chip Enable (CE1, CE2) to Output in High-Z | - | 30 | - | 35 | |
| t _{OOD} | Output Enable to Output in High-Z | - | 30 | - | 35 | |
| t _{OH} | Output Data Hold Time | 10 | - | 10 | - | |

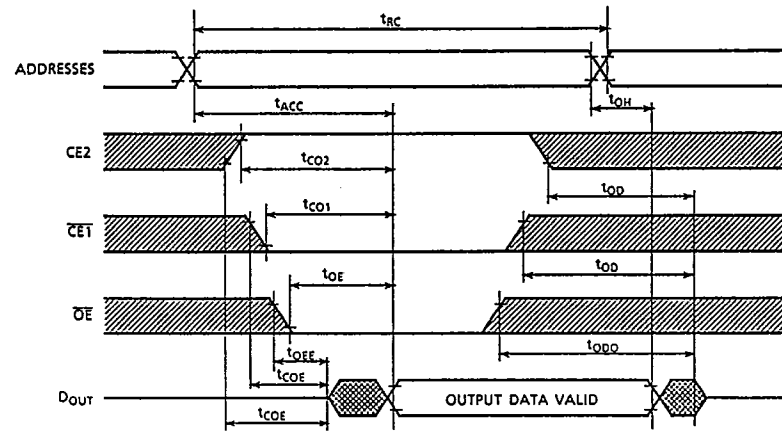
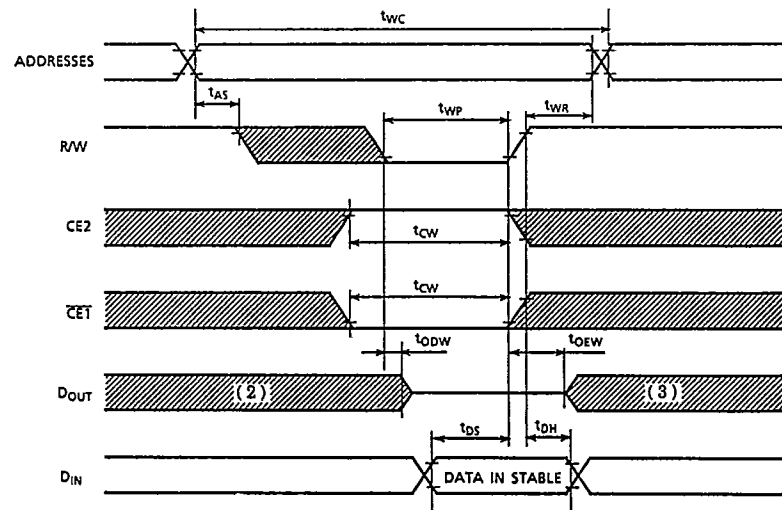
Write Cycle

| SYMBOL | PARAMETER | TC551001PL-85 TC551001FL-85 | | TC551001PL-10 TC551001FL-10 | | UNIT |
|------------------|--------------------------------|--------------------------------|------|--------------------------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 85 | - | 100 | - | ns |
| t _{WP} | Write Pulse Width | 60 | - | 60 | - | |
| t _{CW} | Chip Selection to End of Write | 75 | - | 80 | - | |
| t _{AS} | Address Setup Time | 0 | - | 0 | - | |
| t _{WR} | Write Recovery Time | 0 | - | 0 | - | |
| t _{ODW} | R/W to Output in High-Z | - | 30 | - | 35 | |
| t _{OEW} | R/W to Output in Low-Z | 0 | - | 0 | - | |
| t _{DS} | Data Set up Time | 35 | - | 40 | - | |
| t _{DH} | Data Hold Time | 0 | - | 0 | - | |

A.C. TEST CONDITIONS

Output Load : 100 pF + 1 TTL Gate
 Input Pulse Level : 0.6 V, 2.4 V
 Timing Measurement V_{IN} : 0.8 V, 2.2 V
 Reference Level V_{OUT} : 0.8 V, 2.2 V
 t_r, t_f : 5 ns

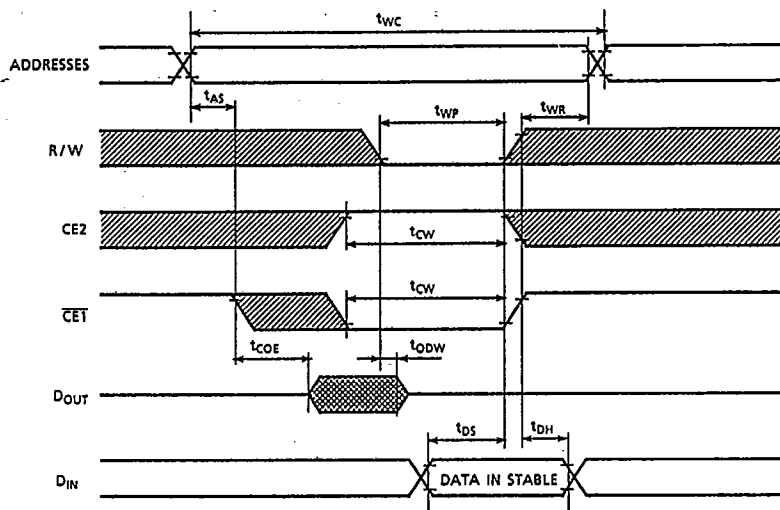
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TIMING WAVEFORMSRead Cycle (1)Write Cycle 1 (4) (R/W Controlled Write)

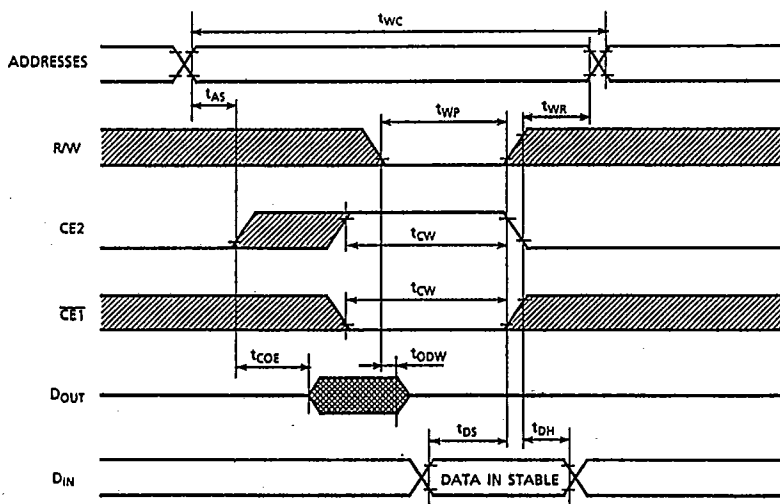
TC551001PL-85/PL-10
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WRITE CYCLE 2 (4) (CE1 Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



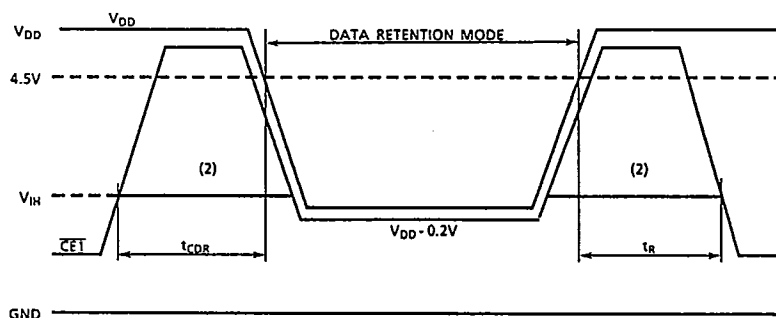
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- Note : (1) R/W is High for Read Cycle.
- (2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
- (3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.
- (4) Assuming that \overline{OE} is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

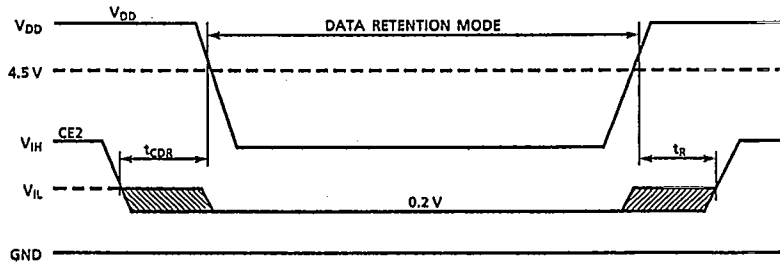
| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|------------------|---|-------------------------|------|------|------|
| V _{OH} | Data Retention Supply Voltage | 2.0 | - | 5.5 | V |
| I _{DD2} | Standby Current | V _{DD} = 3.0 V | - | 50 | μA |
| | | V _{DD} = 5.5 V | - | 100 | |
| t _{CDR} | Chip Deselection to Data Retention Mode | 0 | - | - | nS |
| t _r | Recovery Time | 5 | - | - | mS |

$\overline{CE1}$ Controlled Data Retention Mode (1)



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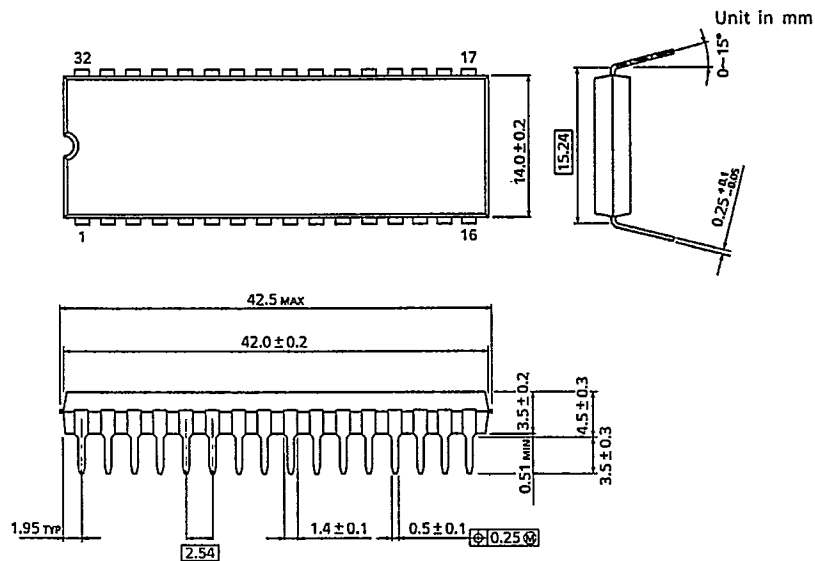
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CE2 Controlled Data Retention Mode (3)

- Note : (1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE2 \leq 0.2V$ or $CE2 \geq V_{DD} - 0.2V$.
- (2) If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDSI} current flows.
- (3) In $CE2$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE2 \leq 0.2V$.

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OUTLINE DRAWING (DIP32 - P - 600)

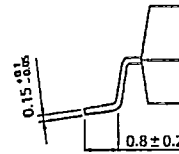
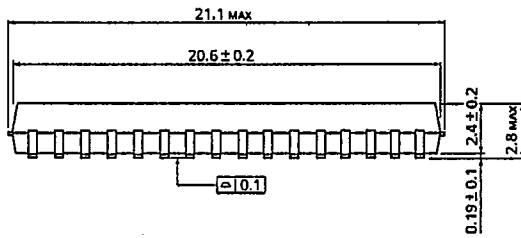
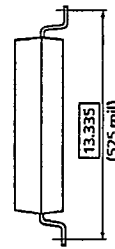
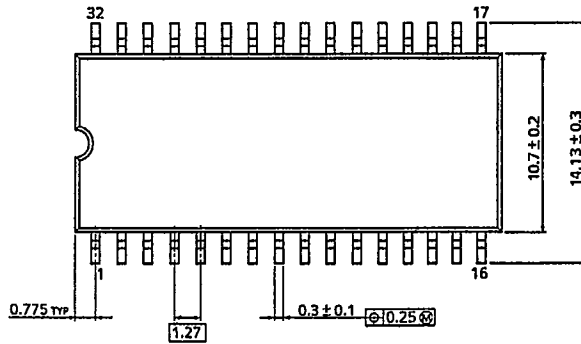


Weight : 4.53g (Typ.)

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OUTLINE DRAWING (SOP32 - P - 525)

Unit in mm



Weight : 1.10g (Typ.)