

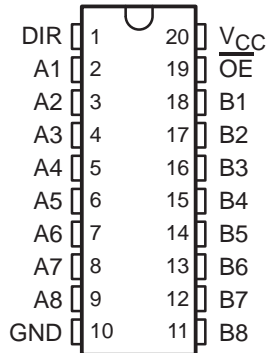
SN74LVT245B

3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

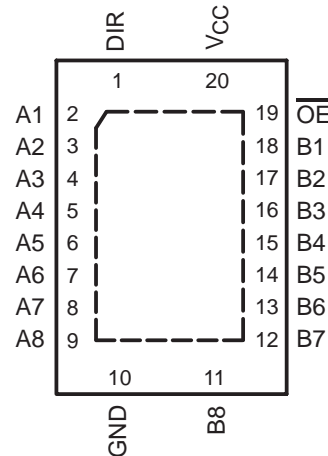
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- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

This octal bus transceiver is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN74LVT245B is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-----------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGY | Tape and reel | SN74LVT245BRGYR | LX245B |
| | SOIC – DW | Tube | SN74LVT245BDW | LVT245B |
| | | Tape and reel | SN74LVT245BDWR | |
| | SOP – NS | Tape and reel | SN74LVT245BNSR | LVT245B |
| | SSOP – DB | Tape and reel | SN74LVT245BDBR | LX245B |
| | TSSOP – PW | Tube | SN74LVT245BPW | LX245B |
| | | Tape and reel | SN74LVT245BPWR | |
| | VFBGA – GQN | Tape and reel | SN74LVT245BGQNR | LX245B |
| | VFBGA – ZQN (Pb-free) | | SN74LVT245BZQNR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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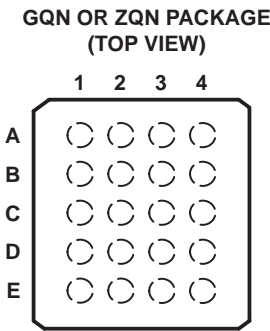
SN74LVT245B 3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES004H – JANUARY 1995 – REVISED SEPTEMBER 2003

description/ordering information (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.



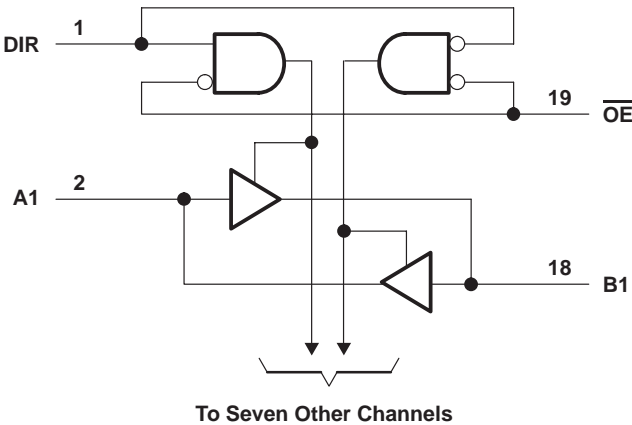
terminal assignments

| | 1 | 2 | 3 | 4 |
|---|-----|-----|----------|-----------------|
| A | A1 | DIR | V_{CC} | \overline{OE} |
| B | A3 | B2 | A2 | B1 |
| C | A5 | A4 | B4 | B3 |
| D | A7 | B6 | A6 | B5 |
| E | GND | A8 | B8 | B7 |

FUNCTION TABLE

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, NS, PW, and RGY packages.

SN74LVT245B

3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES004H – JANUARY 1995 – REVISED SEPTEMBER 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high state, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_O | 128 mA |
| Current into any output in the high state, I_O (see Note 2) | 64 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): DB package | 70°C/W |
| (see Note 3): DW package | 58°C/W |
| (see Note 3): GQN/ZQN package | 78°C/W |
| (see Note 3): NS package | 60°C/W |
| (see Note 3): PW package | 83°C/W |
| (see Note 4): RGY package | 37°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

| | | MIN | MAX | UNIT |
|--------------------------|------------------------------------|-----------------|-----|---------|
| V_{CC} | Supply voltage | 2.7 | 3.6 | V |
| V_{IH} | High-level input voltage | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | V |
| V_I | Input voltage | | 5.5 | V |
| I_{OH} | High-level output current | | –32 | mA |
| I_{OL} | Low-level output current | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 200 | | μs/V |
| T_A | Operating free-air temperature | –40 | 85 | °C |

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74LVT245B

3.3-V ABT OCTAL BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCES004H – JANUARY 1995 – REVISED SEPTEMBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-------------------|--|---|--|--------------|------|-----------|---------------|
| V_{IK} | | $V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$ | | | | -1.2 | V |
| V_{OH} | | $V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$ | | $V_{CC}-0.2$ | | | V |
| | | $V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$ | | 2.4 | | | |
| | | $V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$ | | 2 | | | |
| V_{OL} | $V_{CC} = 2.7\text{ V}$ | $I_{OL} = 100\text{ }\mu\text{A}$ | | | | 0.2 | V |
| | | $I_{OL} = 24\text{ mA}$ | | | | 0.5 | |
| | | $I_{OL} = 16\text{ mA}$ | | | | 0.4 | |
| | $V_{CC} = 3\text{ V}$ | $I_{OL} = 32\text{ mA}$ | | | | 0.5 | |
| | | $I_{OL} = 64\text{ mA}$ | | | | 0.55 | |
| I_I | Control inputs | $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$ | | | | ± 1 | μA |
| | | $V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$ | | | | 10 | |
| | A or B ports‡ | $V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$ | | | | 20 | |
| | | $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ | | | | 1 | |
| | | $V_{CC} = 3.6\text{ V}$, $V_I = 0$ | | | | -5 | |
| I_{off} | | $V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$ | | | | ± 100 | μA |
| I_{OZH} | | $V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$ | | | | 5 | μA |
| I_{OZL} | | $V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$ | | | | -5 | μA |
| I_{OZPU} | | $V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$ | | | | ± 100 | μA |
| I_{OZPD} | | $V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$ | | | | ± 100 | μA |
| I_{CC} | $V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$ | Outputs high | | | | 0.19 | mA |
| | | Outputs low | | | | 5 | |
| | | Outputs disabled | | | | 0.19 | |
| $\Delta I_{CC}\S$ | | $V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$ | | | | 0.2 | mA |
| C_i | | $V_I = 3\text{ V or } 0$ | | | | 4 | pF |
| C_{io} | | $V_O = 3\text{ V or } 0$ | | | | 9 | pF |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused terminals are at $V_{CC}\text{ or GND}$.

§ This is the increase in supply current for each input that is at the specified TTL-voltage level, rather than $V_{CC}\text{ or GND}$.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | | $V_{CC} = 2.7\text{ V}$ | | UNIT |
|-----------|-----------------|-------------|--|------|-----|-------------------------|-----|------|
| | | | MIN | TYP† | MAX | MIN | MAX | |
| t_{PLH} | A or B | B or A | 1.2 | 2.3 | 3.5 | 4 | | ns |
| t_{PHL} | | | 1.2 | 2.1 | 3.5 | 4 | | |
| t_{PZH} | \overline{OE} | A or B | 1.3 | 3.2 | 5.5 | 7.1 | | ns |
| t_{PZL} | | | 1.7 | 3.4 | 5.5 | 6.5 | | |
| t_{PHZ} | \overline{OE} | A or B | 2.2 | 3.5 | 5.9 | 6.5 | | ns |
| t_{PLZ} | | | 2.2 | 3.4 | 5 | 5.1 | | |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.



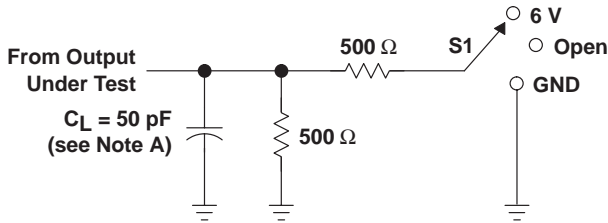
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SN74LVT245B

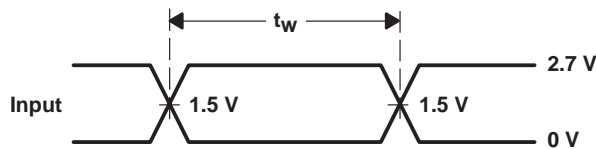
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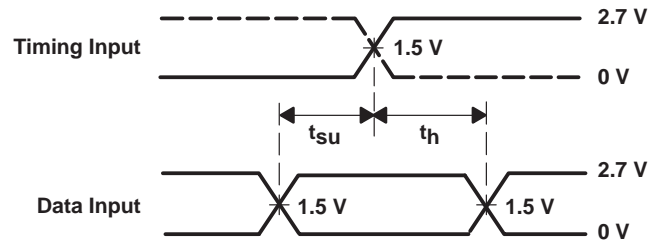
PARAMETER MEASUREMENT INFORMATION



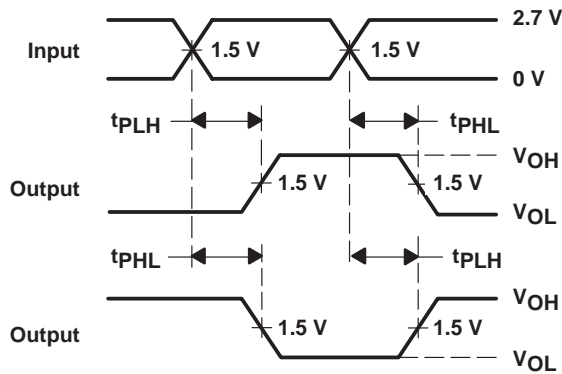
LOAD CIRCUIT



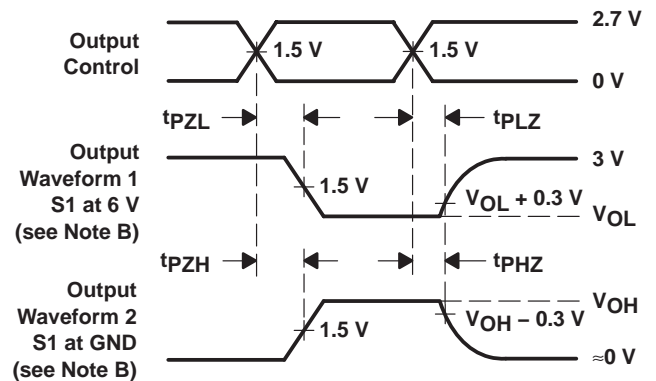
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--|
| SN74LVT245BDBLE | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI |
| SN74LVT245BDBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT245BDBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT245BDW | ACTIVE | SOIC | DW | 20 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LVT245BDWE4 | ACTIVE | SOIC | DW | 20 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LVT245BDWR | ACTIVE | SOIC | DW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LVT245BDWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LVT245BGQNR | ACTIVE | VFBGA | GQN | 20 | 1000 | TBD | SNPB | Level-1-240C-UNLIM |
| SN74LVT245BNSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT245BNSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT245BPW | ACTIVE | TSSOP | PW | 20 | 70 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74LVT245BPWE4 | ACTIVE | TSSOP | PW | 20 | 70 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74LVT245BPWLE | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI |
| SN74LVT245BPWR | ACTIVE | TSSOP | PW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74LVT245BPWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT245BRGYR | ACTIVE | QFN | RGY | 20 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| SN74LVT245BRGYRG4 | ACTIVE | QFN | RGY | 20 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| SN74LVT245BZQNR | ACTIVE | VFBGA | ZQN | 20 | 1000 | Pb-Free (RoHS) | SNAGCU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder

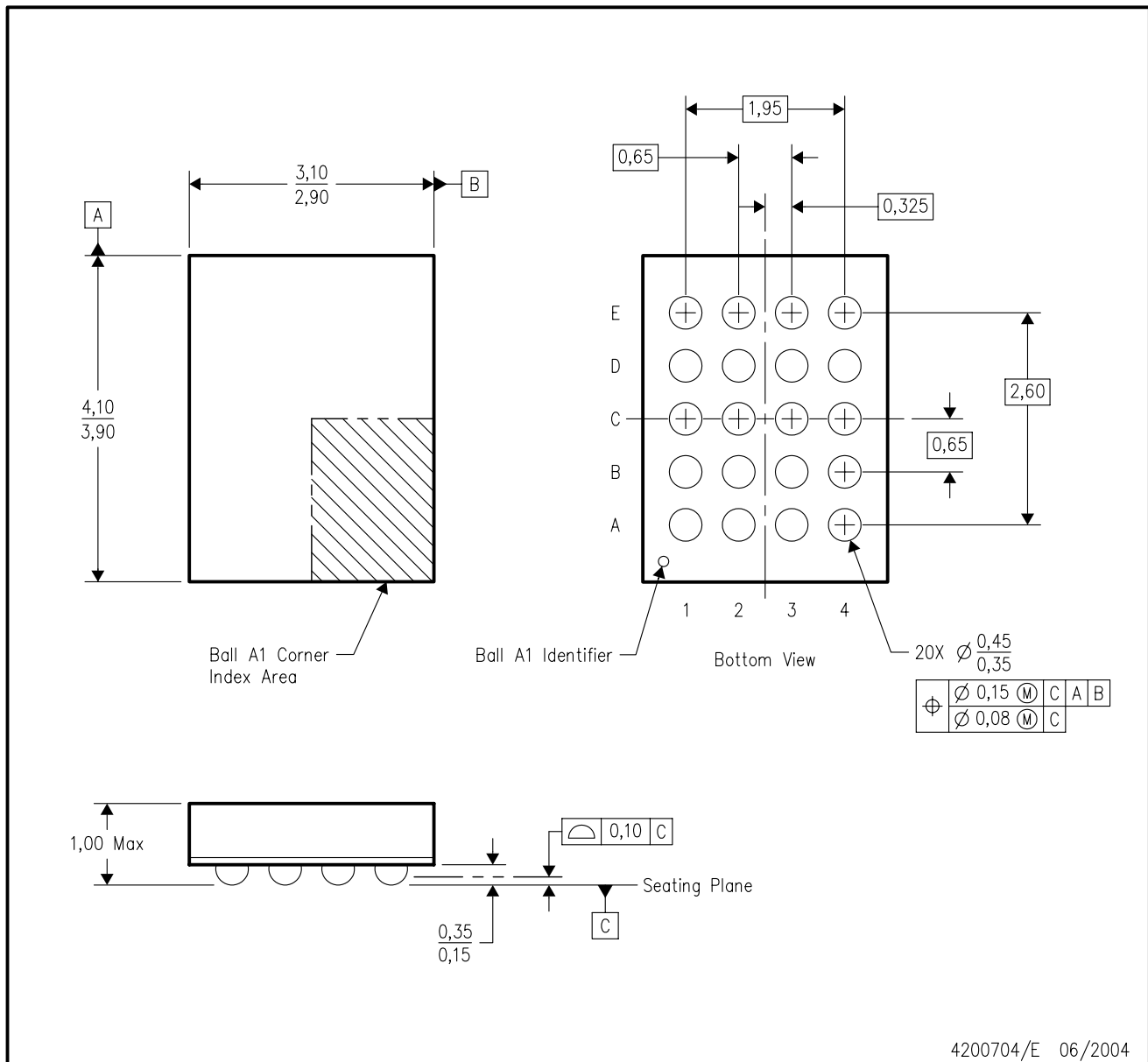
temperature.

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GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY

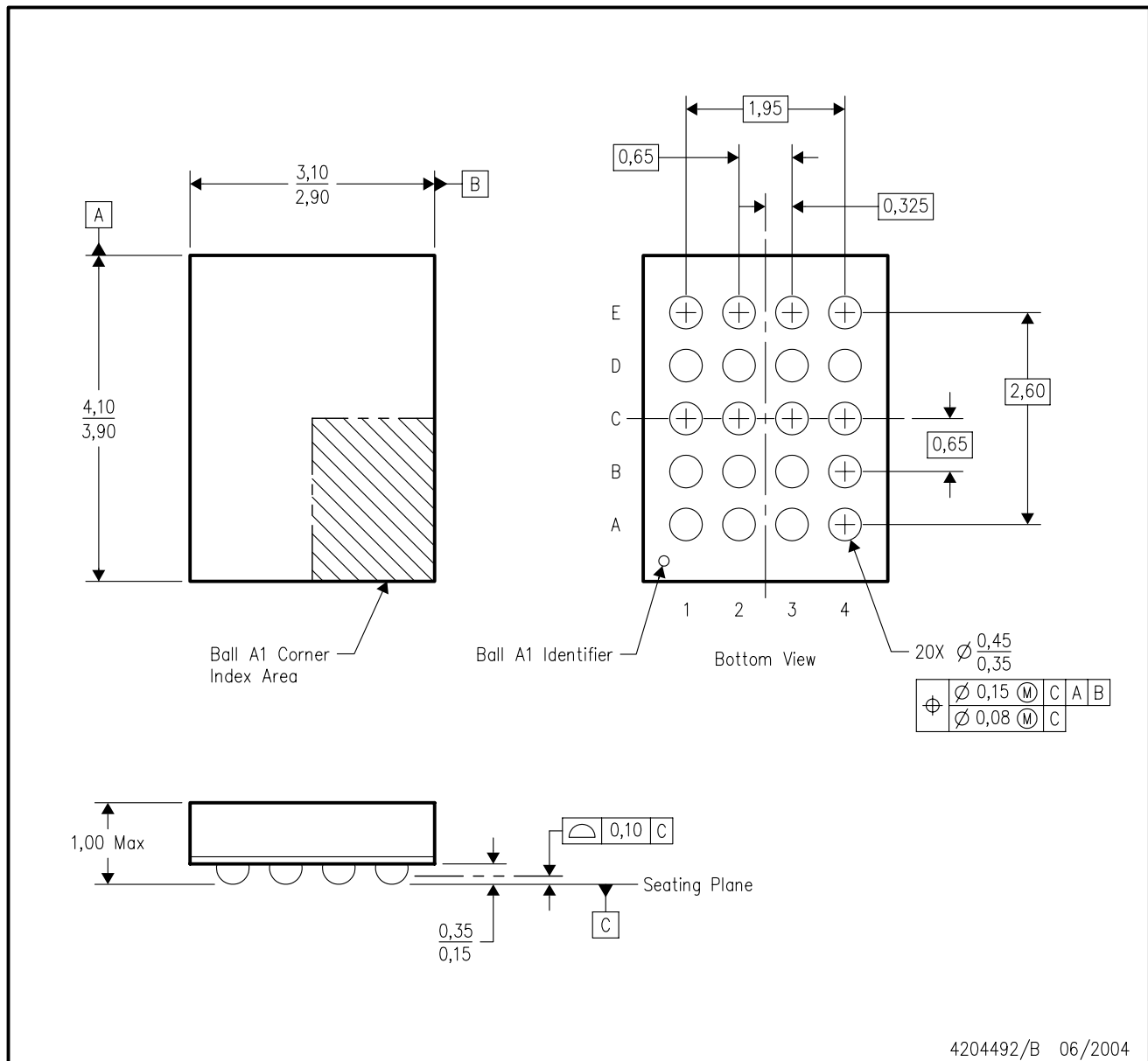


4200704/E 06/2004

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BC.
 - D. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BC.
 - D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE

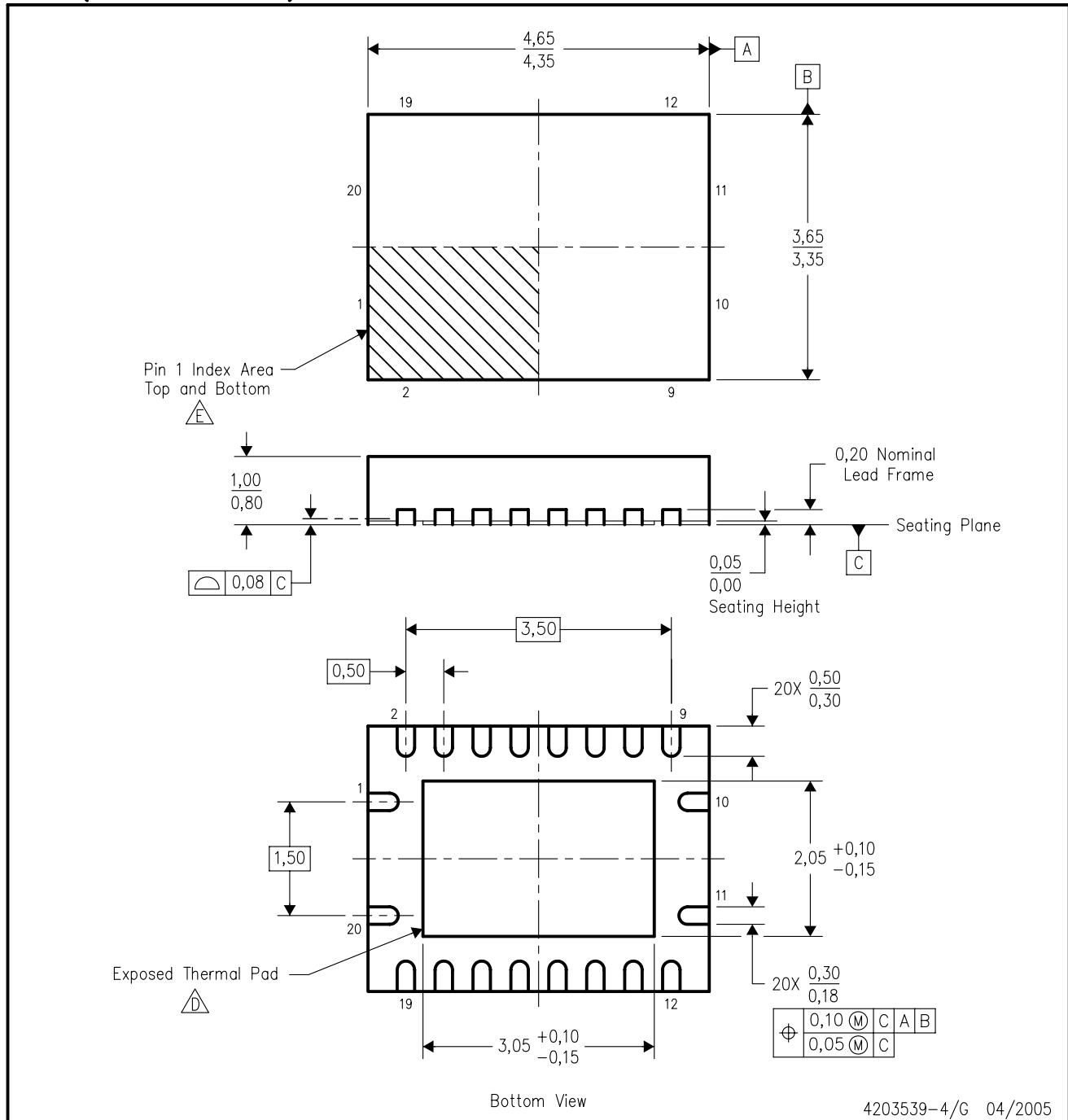


4040000-4/F 06/2004

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



4203539-4/G 04/2005

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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