

SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

SDLS006

D2634, JANUARY 1981 (REVISED MARCH 1988)

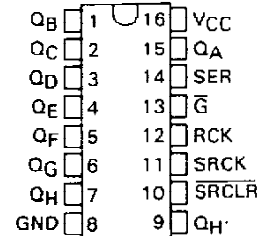
- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Choice of 3-State ('LS595) or Open-Collector ('LS596) Parallel Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20 MHz

description

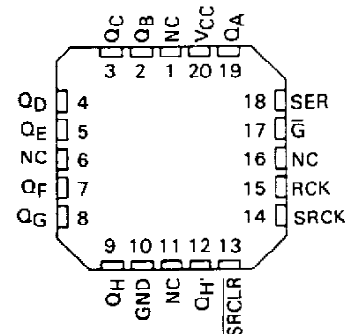
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('LS595) or open-collector ('LS596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

SN54LS595, SN54LS596 . . . J OR W PACKAGE
SN74LS595, SN74LS596 . . . N PACKAGE
(TOP VIEW)



SN54LS595, SN54LS596 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

schematics of inputs and outputs



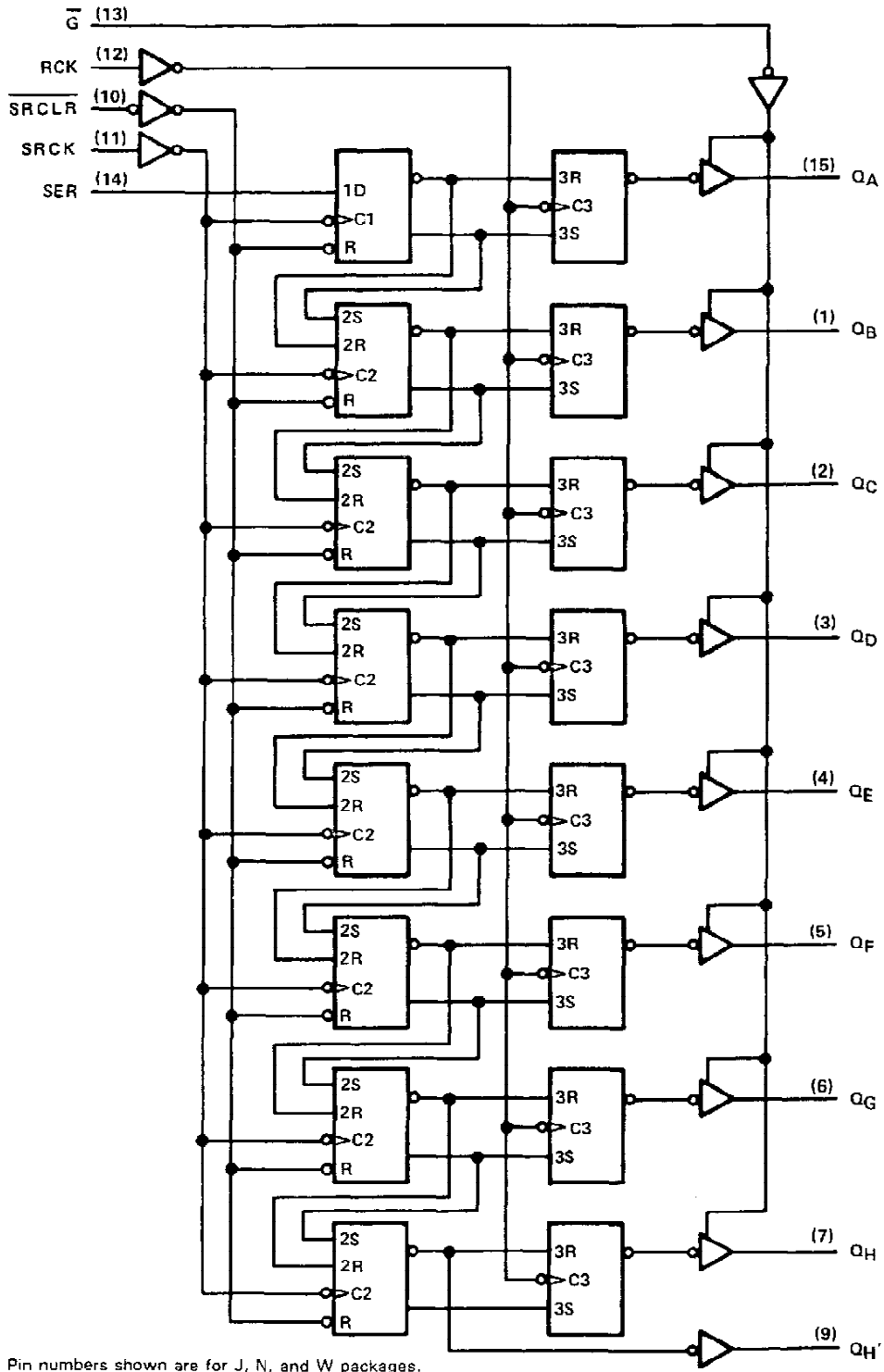
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logic diagram (positive logic)



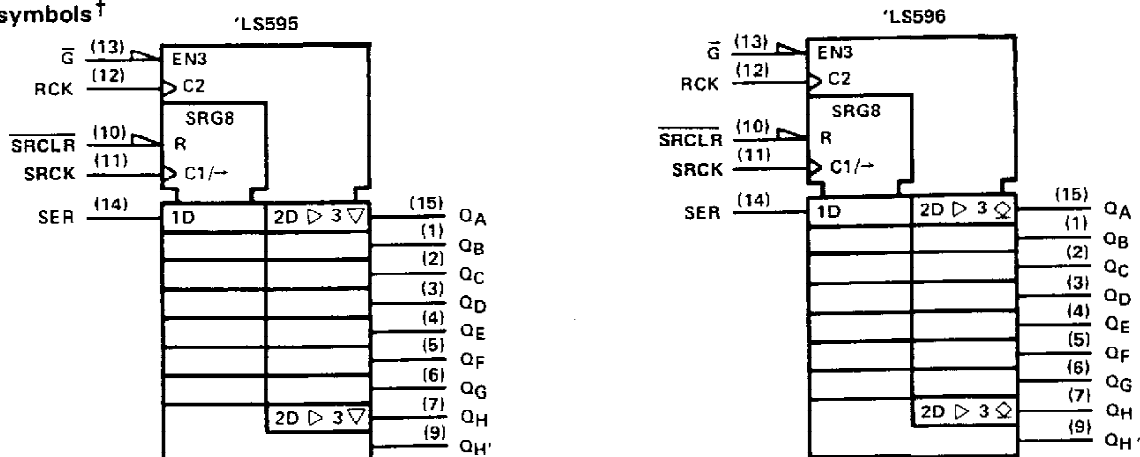
Pin numbers shown are for J, N, and W packages.



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logic symbols †



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS595, SN54LS596	-55°C to 125°C
SN74LS595, SN74LS596	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT		
	MIN	NOM	MAX	MIN	NOM	MAX			
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V		
V_{IH} High-level input voltage	2			2			V		
V_{IL} Low-level input voltage			0.7			0.8	V		
V_{OH} High-level output voltage			5.5			5.5	V		
I_{OH} High-level output current	Q_A thru Q_H , 'LS596 only					-1	mA		
	Q_H'					-1			
I_{OL} Low-level output current	Q_A thru Q_H , 'LS595 only					-2.6	mA		
	Q_H'					-2.6			
f_{SRCK} Shift clock frequency			0	20		0	20	MHz	
$t_w(SRCK)$ Duration of shift clock pulse			25			25		ns	
$t_w(RCK)$ Duration of register clock pulse			20			20		ns	
$t_w(SRCLR)$ Duration of shift clear pulse, low level			20			20		ns	
t_{su} Setup time	SRCLR inactive before SRCK †		20			20		ns	
	SER before SRCK †		20			20			
	SRCK † before RCK † (see Note 2)		40			40			
	SRCLR low before RCK †		40			40			
t_h Hold time	SER after SRCK †		0			0		ns	
T_A Operating free-air temperature			-55		125	0		70	°C

NOTE 2: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together, in which case the storage register state will be one clock pulse behind the shift register.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS*		SN74LS*		UNIT		
		MIN	TYP ‡	MAX	MIN		TYP ‡	MAX
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5		-1.5	V	
V _{OH}	'LS595 Q Q _H '	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = -1 mA	2.4	3.2			
			I _{OH} = -2.6 mA			2.4	3.1	
			I _{OH} = -1 mA	2.4	3.2	2.4	3.2	
I _{OH}	'LS596 Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, V _{OH} = 5.5 V					0.1	mA
V _{OL}	Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	
			I _{OL} = 24 mA			0.35	0.5	
			I _{OL} = 8 mA	0.25	0.4	0.25	0.4	
			I _{OL} = 16 mA			0.35	0.5	
I _{OZH}	'LS595 Q	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _{OH} = 2.7 V			20	20	μA	
I _{OZL}	'LS595 Q	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _{OH} = 0.4 V			-20	-20	μA	
I _I		V _{CC} = MAX, V _I = 7 V			0.1	0.1	mA	
I _{IH}		V _{CC} = MAX, V _I = 2.7 V			20	20	μA	
I _{IL}	SER	V _{CC} = MAX, V _I = 0.4 V			-0.4	-0.4		
	All others				-0.2	-0.2		
I _{OS} §	'LS595 Q	V _{CC} = MAX, V _O = 0 V			-30	-130	-30	-130
	Q _H '				-20	-100	-20	-100
I _{CCH}	'LS595	V _{CC} = MAX, All possible inputs grounded, All outputs open			33	50	33	50
	'LS596				30	45	30	45
I _{CCL}	'LS595	All possible inputs grounded, All outputs open			42	65	42	65
	'LS596				36	55	36	55
I _{CCZ}	'LS595			44	65	44	65	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS595			'LS596			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	SRCK ↑	Q_H'	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	12	18		14	21	ns	
t_{PHL}				17	25		20	30	ns	
t_{PLH}	RCK ↑	Q_A thru Q_H	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$	12	18		28	42	ns	
t_{PHL}				24	35		24	35	ns	
t_{PZH}	\overline{G} ↓	Q_A thru Q_H		20	30				ns	
t_{PZL}				25	38				ns	
t_{PHZ}	\overline{G} ↑	Q_A thru Q_H	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$	20	30				ns	
t_{PLZ}				25	38				ns	
t_{PLH}	\overline{G} ↑	Q_A thru Q_H	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$				40	60	ns	
t_{PHL}	\overline{G} ↓	Q_A thru Q_H					25	38	ns	
t_{PHL}	SRCLR ↓	Q_H'	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	24	35		24	35	ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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