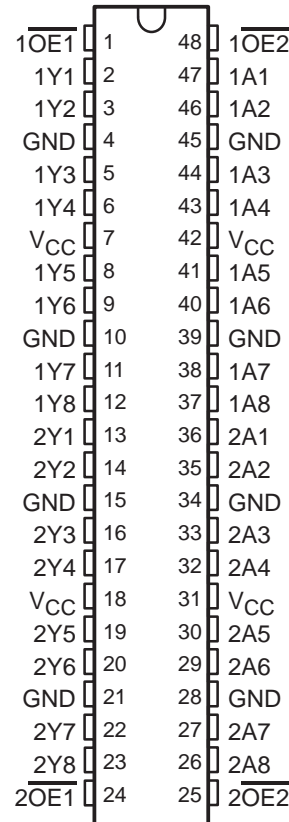


SN54ABT16540, SN74ABT16540A 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16540 . . . WD PACKAGE
SN74ABT16540A . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The SN54ABT16540 and SN74ABT16540A are inverting 16-bit buffers/drivers composed of two 8-bit sections with separate output-enable gates. These buffers and bus drivers provide a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16540 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16540A is characterized for operation from -40°C to 85°C .



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SN54ABT16540, SN74ABT16540A
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

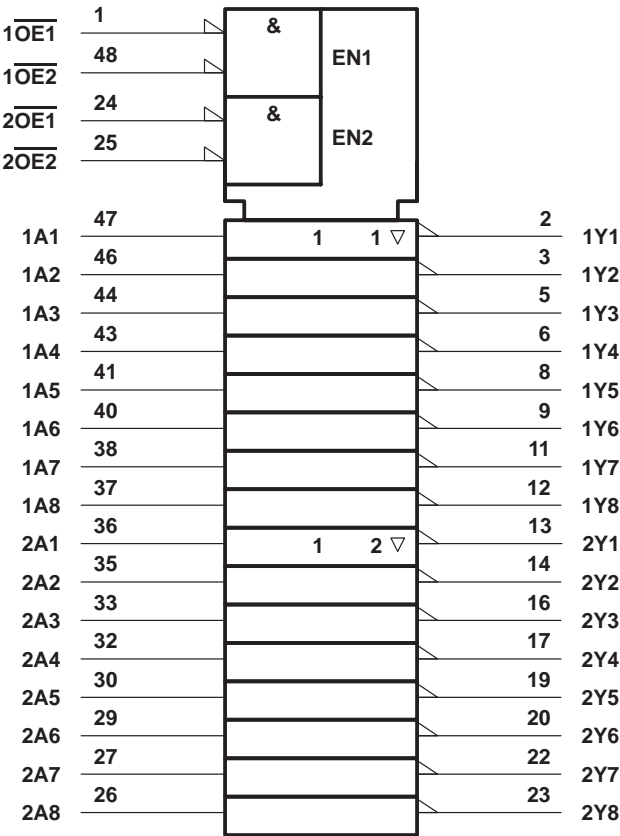
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FUNCTION TABLE

(each 8-bit section)

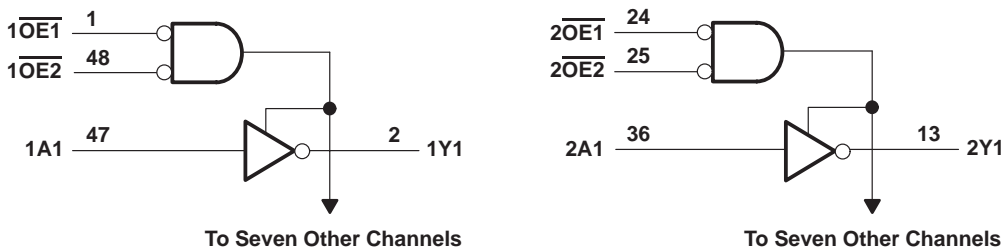
INPUTS			OUTPUT Y
OE1	OE2	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			SN54ABT16540		SN74ABT16540A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = -3 mA	2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = -3 mA	3			3		3		
		V _{CC} = 4.5 V, I _{OH} = -24 mA	2			2				
		V _{CC} = 4.5 V, I _{OH} = -32 mA	2*					2		
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 48 mA			0.55		0.55			V
		V _{CC} = 4.5 V, I _{OL} = 64 mA			0.55*				0.55	
V _{hys}				100						mV
I _I		V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V			10		50		10	μA
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.5 V			-10		-50		-10	μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V, Outputs high			50		50		50	μA
I _{O‡}		V _{CC} = 5.5 V, V _O = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs high			3		2		3	mA
		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs low			34		32		34	
		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs disabled			3		2		3	
ΔI _{CC} §	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND, Outputs enabled			1		1		1	mA
		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND, Outputs disabled			0.05		0.05		0.05	
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	
C _i		V _I = 2.5 V or 0.5 V			3.5					pF
C _O		V _O = 2.5 V or 0.5 V			7.5					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

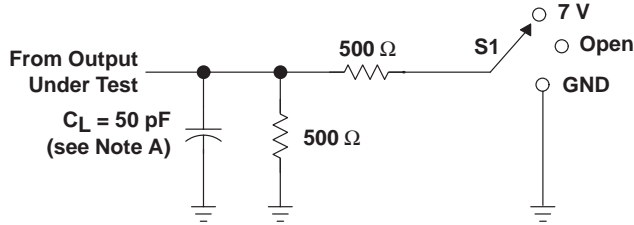
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

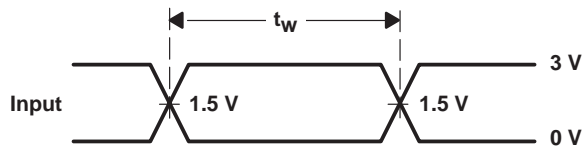
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABT16540		SN74ABT16540A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1	2.3	3.3	1	4.2	1	4.1	ns
t _{PHL}			1.1	2.5	4.1	1.1	4.4	1.1	4.3	
t _{PZH}	$\overline{\text{OE}}$	Y	1.1	3.1	4.2	1.1	5.2	1.1	5.1	ns
t _{PZL}			1.6	3.7	4.8	1.6	6	1.6	5.9	
t _{PHZ}	$\overline{\text{OE}}$	Y	1.6	4	5	1.6	5.4	1.6	5.7	ns
t _{PLZ}			1.4	3.2	4.4	1.4	4.7	1.4	4.7	

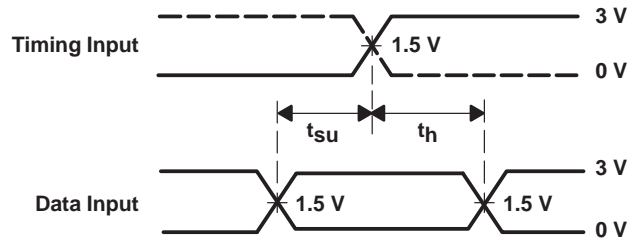
PARAMETER MEASUREMENT INFORMATION



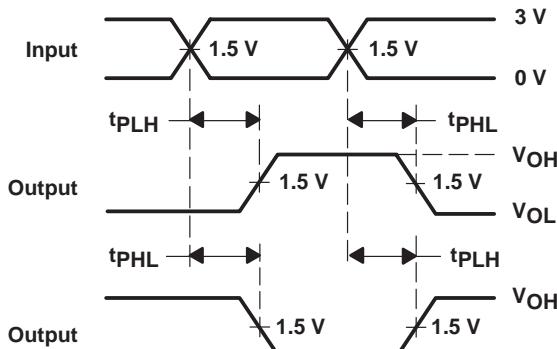
LOAD CIRCUIT



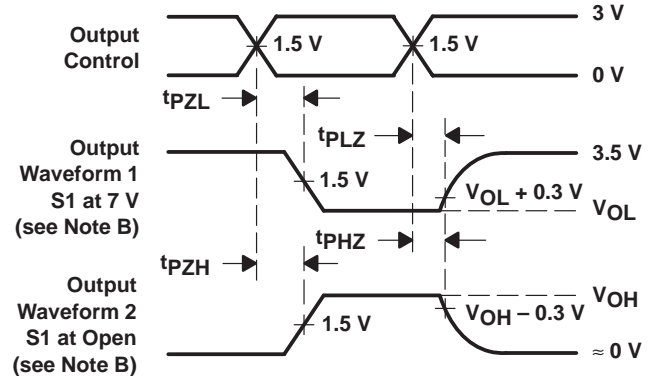
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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