

#### FEATURES

- Good CMRR: typ. 50dB at 60Hz
- Low cost, self contained
- Excellent audio performance
  - Wide bandwidth: typ. >8.6 MHz
  - High slew rate: typ. 12 V/ $\mu$ s
  - Low distortion: typ. 0.0006 % THD
  - Low noise: typ. -103 dBu (re: input)
- Low current: typ. 2 mA
- Several gains: 0 dB,  $\pm 3$  dB, &  $\pm 6$  dB
- Industry-standard pinout

#### APPLICATIONS

- Balanced Audio Line Receivers
- Instrumentation Amplifiers
- Differential Amplifiers
- Precision Summers
- Current Shunt Monitors

#### Description

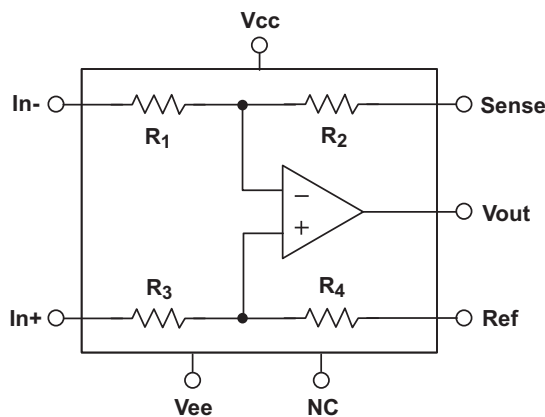
The THAT 1250-series of precision differential amplifiers was designed primarily for use as balanced line receivers for audio applications. Gains of 0 dB,  $\pm 3$  dB, and  $\pm 6$  dB are available to suit various applications requirements.

These devices include on-board precision thin-film resistors which offer good matching and excellent tracking due to their monolithic construction. Manufactured in THAT Corporation's proprietary complementary dielectric isolation (DI) process, the THAT 1250-series provides the sonic benefits of discrete designs with the simplicity, reliability,

matching and small size of an integrated solution.

All three versions of the part typically exhibit 50 dB of common-mode rejection. With 12 V/ $\mu$ s slew rate, >8.6 MHz bandwidth, and 0.0006% THD, these devices are sonically transparent. Moreover, current consumption is typically a low 2 mA. Both surface-mount and DIP packages are available.

The THAT 1256 is pin-compatible with the TI INA137 and Analog Devices SSM2143, while the THAT 1250 is pin-compatible with the TI INA134 and Analog Devices SSM2141.



Part no.	Gain	R <sub>1</sub> , R <sub>3</sub>	R <sub>2</sub> , R <sub>4</sub>
THAT1250	0 dB	9 k $\Omega$	9 k $\Omega$
THAT1253	-3 dB	10.5 k $\Omega$	7.5 k $\Omega$
THAT1256	-6 dB	12 k $\Omega$	6 k $\Omega$

Figure 1. THAT1250-series equivalent circuit diagram

Pin Name	DIP Pin	SO Pin
Ref	1	1
In-	2	2
In+	3	3
Vee	4	4
Sense	5	5
Vout	6	6
Vcc	7	7
NC	8	8

Table 1. 1250 Series pin assignments

Gain	Plastic DIP	Plastic SO
0 dB	1250P08-U	1250S08-U
$\pm 3$ dB	1253P08-U	1253S08-U
$\pm 6$ dB	1256P08-U	1256S08-U

Table 2. Ordering information

**SPECIFICATIONS<sup>1</sup>**

<b>Absolute Maximum Ratings</b>			
Positive Supply Voltage ( $V_{CC}$ )	+20 V	Power Dissipation ( $P_D$ ) ( $T_A = 85^\circ\text{C}$ )	400 mW (DIP)
Negative Supply Voltage ( $V_{EE}$ )	-20 V	Power Dissipation ( $P_D$ ) ( $T_A = 85^\circ\text{C}$ )	260 mW (SO)
Storage Temperature Range ( $T_{ST}$ )	-40 to +125°C	Operating Temperature Range ( $T_{OP}$ )	0 to 85°C
Output Short-Circuit Duration ( $t_{SH}$ )	Continuous	Junction Temperature ( $T_J$ )	125°C
Input Voltages ( $In+$ , $In-$ )	$\pm 50$ V	Lead Temperature (Soldering 10 seconds)	300 °C

<b>Electrical Characteristics<sup>2</sup></b>						
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current	$I_{CC}$	No signal	—	2.0	2.8	mA
Supply Voltage	$V_{CC}$ $V_{EE}$		+3 -3		+18 -18	V V
Input Voltage Range	$V_{IN-DIFF}$  $V_{IN-CM}$	Differential (equal and opposite swing) THAT 1250 (0 dB gain) THAT 1253 (-3 dB gain) THAT 1256 (-6 dB gain) Common mode THAT 1250 (0 dB gain) THAT 1253 (-3 dB gain) THAT 1256 (-6 dB gain)	— — — — — — —	21.5 24.4 27.5 27.5 29.1 31.5	— — — — — —	dBu <sup>3</sup> dBu dBu dBu dBu dBu
Input Impedance <sup>4</sup>	$Z_{IN-CM}$ $Z_{IN-DIFF}$	Common mode (all versions) Differential THAT 1250 (0 dB gain) THAT 1253 (-3 dB gain) THAT 1256 (-6 dB gain)	— — — — —	9 18 21 24	— — — —	k $\Omega$ k $\Omega$ k $\Omega$ k $\Omega$ k $\Omega$
Common Mode Rejection Ratio	CMRR	Matched source impedances; $V_{CM} = \pm 10$ V DC 60 Hz 20 kHz	40 40 40	50 50 50	— — —	dB dB dB
Power Supply Rejection Ratio <sup>5</sup>	PSR	at 60 Hz, with $V_{CC} = -V_{EE}$ THAT 1250 (0 dB gain) THAT 1253 (-3 dB gain) THAT 1256 (-6 dB gain)	— — —	90 90 90	— — —	dB dB dB
Total Harmonic Distortion	THD	$V_{IN-DIFF} = 10$ V; BW = 20 kHz; $f = 1$ kHz, $R_L = 2$ k $\Omega$	—	0.0006	—	%
Small Signal Bandwidth	$BW_{-3dB}$	$R_L = 2$ k $\Omega$ ; $C_L = 10$ pf THAT 1250 (0 dB gain) THAT 1253 (-3 dB gain) THAT 1256 (-6 dB gain) $R_L = 2$ k $\Omega$ ; $C_L = 300$ pf THAT 1250 (0 dB gain) THAT 1253 (-3 dB gain) THAT 1256 (-6 dB gain)	— — — — — — —	8.6 12.2 18 10.3 11.8 13.4	— — — — — —	MHz MHz MHz MHz MHz MHz

Output Noise	$e_{(OUT)}$	22 Hz to 22 kHz bandwidth	—	-103	—	dBu
		THAT 1250 (0 dB gain)	—	-105	—	dBu
		THAT 1253 (-3 dB gain)	—	-106	—	dBu
		THAT 1256 (-6 dB gain)	—		—	
Slew Rate	SR	$R_L = 2 \text{ k}\Omega$ ; $C_L = 300 \text{ pf}$	7	12	—	V/ $\mu$ s
Output Gain Error	$G_{ER(OUT)}$	$f = 1 \text{ kHz}$	-0.1	0	+0.1	dB
Output Voltage Swing	$V_{O+}$	$R_L = 2 \text{ k}\Omega$	$V_{CC} - 2.5$	$V_{CC} - 2$	—	V
	$V_{O-}$	$R_L = 2 \text{ k}\Omega$	—	$V_{EE} + 2$	$V_{EE} + 2.5$	V
Output Offset Voltage	$V_{OFF}$	No signal	-7	—	+7	mV
Output Short Circuit Current	$I_{SC}$	$R_L = 0 \Omega$	—	$\pm 25$	—	mA
Resistive Load	$R_L$		2	—	—	k $\Omega$
Capacitive Load	$C_L$		—	—	300	pF

<b>Package Characteristics</b>						
Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Through-hole Package</b>						
Type		See Figure 13		8-Pin PDIP		
Thermal Resistance	$\theta_{JA}$	DIP package soldered to board	-	100	-	$^{\circ}\text{C}/\text{W}$
<b>Surface Mount Package</b>						
Type		See Figure 14		8-Pin SOP		
Thermal Resistance	$\theta_{JA}$	SO package soldered to board	-	150	-	$^{\circ}\text{C}/\text{W}$
Soldering Reflow Profile				JEDEC JESD22-A113-B (220 $^{\circ}\text{C}$ )		

## Theory of Operation

The THAT1250-series ICs consist of high performance opamps with integrated, thin-film resistors. These designs take full advantage of THAT fully complementary dielectric isolation (DI) process to deliver excellent performance with low current consumption. The devices are simple to apply in many applications.

### Resistor Matching, Values, and CMRR

The 1250-series devices rely upon the inherent matching of silicon-chromium (Si-Cr), thin-film, integrated resistors to achieve a 50 dB common mode rejection ratio and tight gain accuracy. No trimming is

performed. As a result of their monolithic construction, the R3/R4 ratio generally matches within  $\pm 0.1\%$  of the R1/R2 ratio.

However, while the resistor ratios are tightly controlled, the actual value of any individual resistor is not. Lot-to-lot variations of up to  $\pm 25\%$  are to be expected.

If higher CMRR is required in a simple input stage, consider the THAT 1240-series ICs. These parts are laser trimmed to improve the inherent precision of our thin-film resistor process. For demanding applications in which the source impedance balance may be less

<sup>1</sup> All specifications are subject to change without notice.

<sup>2</sup> Unless otherwise noted,  $T_A = 25^{\circ}\text{C}$ ,  $V_{CC} = +15\text{V}$ ,  $V_{EE} = -15\text{V}$ . Test circuit is as shown in Figure 2.

<sup>3</sup> 0 dBu = 0.775Vrms.

<sup>4</sup> While specific resistor ratios are very closely matched, absolute resistance values can vary  $\pm 25\%$  from the typical values shown. Input impedance is monitored by lot sampling.

<sup>5</sup> Defined with respect to differential gain.

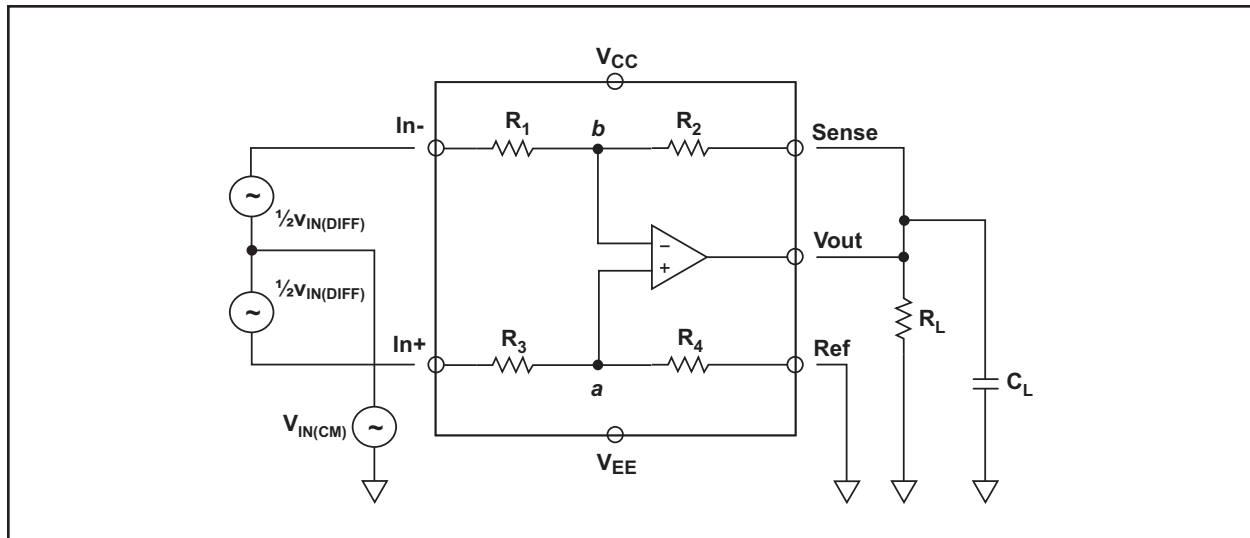


Figure 2. THAT1250 series test circuit

than perfect, the 1200-series ICs offer exceptional CMRR performance via a patented method of increasing common-mode input impedance.

### Input Considerations

The 1250-series devices are internally protected against input overload via an unusual arrangement of diodes connecting the + and - Input pins to the power supply pins. The circuit of Figure 3 shows the arrangement used for the  $R_3 / R_4$  side; a similar one applies to the other side. The zener diodes prevent the protection network from conducting until an input pin is raised at least 50 V above  $V_{CC}$  or below  $V_{EE}$ . Thus, the protection networks protect the devices without constraining the allowable signal swing at the input pins. The reference (and sense) pins are protected via more conventional reverse-biased diodes which will conduct if these pins are raised above  $V_{CC}$  or below  $V_{EE}$ .

Because the 1250-series devices are input stages, their input pins are of necessity connected to the outside world. This is likely to expose the parts to ESD when cables are connected and disconnected. Our testing indicates that the 1250-series devices will typically withstand application of up to 1,000 volts under the human body ESD model.

To reduce risk of damage from ESD, and to prevent RF from reaching the devices, THAT recommends the circuit of Figure 4.  $C_3$  through  $C_5$  should be located close to the point where the input signal comes into the chassis, preferably directly on the input connector. The unusual circuit design minimizes the unbalancing impact of differences in the values of  $C_4$  and  $C_5$  by forcing the capacitance from each input to chassis ground to depend primarily on the value of  $C_3$ . The circuit shown is approximately ten times less sensitive to mismatches between  $C_4$  and  $C_5$  than the more conventional approach in which the junction of  $C_4$  and  $C_5$  is grounded directly<sup>6</sup>.

Designers frequently seek to improve RF bypassing through the addition of R-C networks at the inputs (se-

ries resistor followed by a capacitor to ground at each input). Generally, THAT recommends keeping any such series resistances under  $50\Omega$ , so as not to upset the intrinsic balance between the 1250's internal  $R_1/R_2$  and  $R_3/R_4$  resistor ratios. Because the internal resistor absolute values are not well controlled, the external resistors can interact with the internal ones in unexpected ways. As an alternative to a resistor as additional build-out impedance, THAT recommends the use of a ferrite bead or balun instead.

If it is necessary to ac-couple the inputs of the 1250-series parts, the coupling capacitors should be sized to present negligible impedance at any frequencies of interest for common mode rejection. Regardless of the type of coupling capacitor chosen, variations in the values of the two capacitors, working against the 1250-series input impedance, can unbalance common mode input signals, converting them to balanced signals which will not be rejected by the CMRR of the devices. For this reason, THAT recommends dc-coupling the inputs of the 1250-series devices.

### Input Voltage Limitations

When configured, respectively, for -3 dB and -6 dB gain, the 1253 and 1256 devices are capable of accepting input signals above the power supply rails. This is because the internal opamp's inputs connect to the outside world only through the on-chip resistors  $R_1$  through  $R_4$  at nodes a and b as shown in Figure 2. Consider the following analysis.

#### Differential Input Signals

For differential signals ( $V_{IN(DIFF)}$ ), the limitation to signal handling will be output clipping. The outputs of all the devices typically clip at within 2V of the supply rails. Therefore, maximum differential input signal levels are directly related to the gain and supply rails.

#### Common-mode Input Signals

For common-mode input signals, there is very little output signal. The limitation on common-mode han-

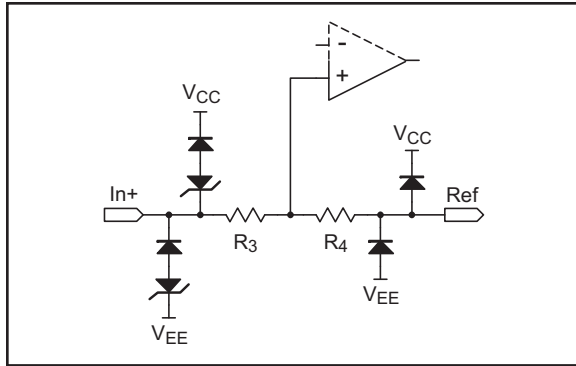


Figure 3. Representative Input Protection Circuit

ding is the point at which the inputs are overloaded. So, we must consider the inputs of the opamp.

For common-mode signals ( $V_{IN(CM)}$ ), the common-mode input current splits to flow through both  $R_1/R_2$  and through  $R_3/R_4$ . Because  $v_b$  is constrained to follow  $V_a$ , we will consider only the voltage at node a.

The voltage at a can be calculated as:

$$v_a = v_{IN(CM)} \left[ \frac{R_4}{R_3 + R_4} \right].$$

Again, solving for  $V_{IN(CM)}$ ,

$$v_{IN(CM)} = v_a \left[ \frac{R_3 + R_4}{R_4} \right].$$

For the 1250,  $(R_3 + R_4) / R_4 = 2$ . For the 1253,  $(R_3 + R_4) / R_4 = 2.4$ . For the 1256,  $(R_3 + R_4) / R_4 = 3$ . Furthermore, the same constraints apply to  $V_a$  as in the differential analysis.

Following the same reasoning as above, the maximum common-mode input signal for the 1250 is  $(2V_{CC} - 4)$  V, and the minimum is  $(2V_{EE} + 4)$  V. For the 1253, these figures are  $(2.4V_{CC} - 4.8)$  V, and  $(2.4V_{EE} + 4.8)$  V. For the 1256, these figures are  $(3V_{CC} - 6)$  V, and  $(3V_{EE} + 6)$  V.

Therefore, for common-mode signals and  $\pm 15$  V rails, the 1250 will accept up to  $\sim 26$  V in either direction. As an ac signal, this is 52 V peak-peak, 18.4 V rms, or +27.5 dBu. With the same supply rails, the 1253 will accept up to  $\sim 31$  V in either direction. As an ac signal, this is 62 V peak-peak, 21.9 V rms, or +29 dBu. With the same supply rails, the 1256 will accept up to  $\sim 39$  V in either direction. As an ac signal, this is 78 V peak-peak, 27.6 V rms, or +31 dBu.

Of course, in the real world, differential and common-mode signals combine. The maximum signal that can be accommodated will depend on the superposition of both differential and common-mode limitations.

## Output Considerations

The 1250-series devices are typically capable of supplying 25 mA into a short circuit. While they will

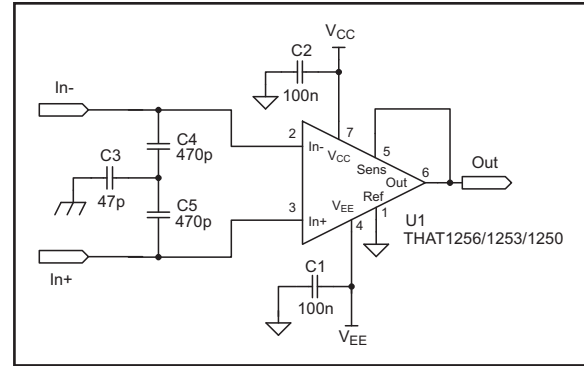


Figure 4. RFI and Supply Bypassing

survive a short, power dissipation will rise dramatically if the output is shorted. Junction temperature must be kept under 125 °C to maintain the devices' specifications.

These devices are stable with up to 300 pf of load capacitance.

## Power Supply Considerations

The 1250-series parts are not particularly sensitive to the power supply, but they *do* contain wide bandwidth opamps. Accordingly, small local bypass capacitors should be located within a few inches of the supply pins on these parts, as shown in Figure 4.

## Selecting a Gain Variation

The three different parts offer different gain structures to suit different applications. The 1256 is customarily configured for -6 dB gain, but by reversing the resistor connections, can also be configured for +6 dB. The 1253 is most often configured for -3 dB gain, but can also be configured for +3 dB. The choice of input gain is determined by the input voltage range to be accommodated, and the power supply voltages used within the circuit.

To minimize noise and maximize signal-to-noise ratio, the input stage should be selected and configured for the highest possible gain that will ensure that maximum-level input signals will not clip the input stage or succeeding stages. For example, with  $\pm 18$  V supply rails, the 1250-series parts have a maximum output signal swing of +23 dBu. In order to accommodate +24 dBu input signals, the maximum gain for the stage is -1 dB. With  $\pm 15$  V supply rails, the maximum output signal swing is  $\sim +21.1$  dBu; here, -3 dB is the maximum gain. In each case, a 1253 configured for -3 dB gain is the ideal choice. The 1250 (0dB gain only) will not provide enough headroom at its output to support a +24 dBu input signal. The 1256 (configured for -6 dB gain) will increase noise, thus reducing dynamic range, by attenuating the input signal more than necessary to support a +24 dBu input.

In fact, for most professional audio applications, THAT recommends the -3 dB input configuration possi-

<sup>6</sup>An excellent discussion of input stage grounding can be found in the June 1995 issue of the Journal of the Audio Engineering Society, Vol. 43, No. 6, in articles by Stephen Macatee, Bill Whitlock, and others.

ble only with the 1253 in order to preserve dynamic

range within a reasonable range of power supply voltages and external headroom limits.

## Applications

The THAT 1250, 1253, and 1256 are usually thought of as precision differential amplifiers with gains of zero, -3 and -6 dB respectively. These devices are primarily intended as balanced line receivers for audio applications. However, their topology lends itself to other applications as well.

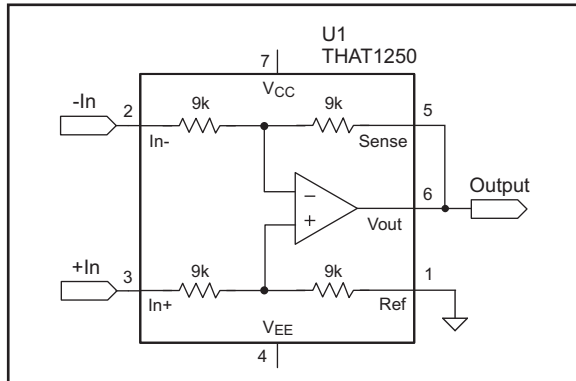


Figure 5. Zero dB line receiver

### Basic Balanced Receiver Applications

Figures 5, 6, and 7, respectively, show the THAT 1250, 1256, and 1253 configured as zero, -6 dB, and -3 dB line receivers. Figures 8 and 9, respectively, show the 1253 and 1256 configured as +3 dB and +6 dB line receivers. The higher gains are achieved by swapping the positions of the resistors within each pair in regard to signal input vs. Output. In all five cases, no external resistors are required to set the desired gain.

Figure 10 shows a THAT 1250 configured as a precision summing amplifier. This circuit uses both the In+ and Ref pins as inputs. Because of the good matching between the resistor pairs, the output voltage is precisely equal to the sum of the two input voltages.

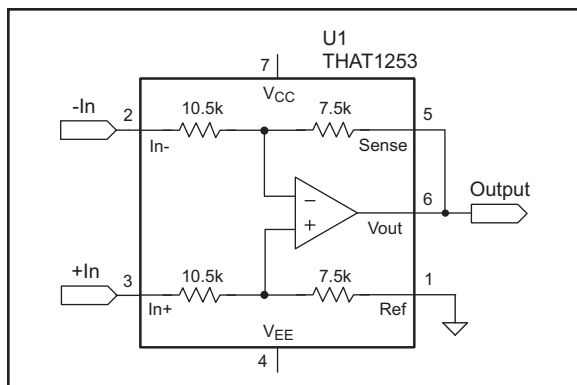


Figure 6. -3 dB line receiver

### More Complex Applications

Figure 11 shows a convenient method of driving a typical audio ADC with balanced inputs. This circuit accepts +24 dBu in. By using a pair of THAT 1256 ICs connected in anti-phase, the signal level between their respective outputs is +24 dBu. An attenuator network brings this signal down by 24 dB while attenuating the noise of the line receivers as well.

The output noise of a THAT 1256 is -106 dBu. Since there are two of them, and uncorrelated noise sources add in RMS fashion, the total noise level going into the resistive pad will be 3 dB higher, or -103 dBu. The pad reduces the noise level to -127 dBu at the input to the ADC. The noise density resulting from the line receivers will therefore be

$$e_{n \text{ line receiver}} = \frac{10^{\frac{-127 \text{ dBu}}{20}} \times 0.775}{\sqrt{20 \text{ kHz}}} = 245 \frac{\text{nV}}{\sqrt{\text{Hz}}}$$

The thermal noise of the 249Ω resistor is 2.05 nV/√Hz. We can assume that the noise contribution of R<sub>8</sub> and R<sub>19</sub> will be negligible, and therefore, the total noise density going into the input of the ADC will be

$$e_{n \text{ total}} = \sqrt{\left(245 \frac{\text{nV}}{\sqrt{\text{Hz}}}\right)^2 + \left(2.06 \frac{\text{nV}}{\sqrt{\text{Hz}}}\right)^2} = 3.2 \frac{\text{nV}}{\sqrt{\text{Hz}}}$$

The noise floor can then be calculated to be

$$\text{Noise}_{(\text{dBu})} = 20 \log \left[ \frac{3.2 \frac{\text{nV}}{\sqrt{\text{Hz}}} \times \sqrt{20 \text{ kHz}}}{0.775} \right] = -124.7 \text{ dBu}$$

Figure 12 shows the recommended method for controlling gain in a balanced system. In such circuits, designers are sometimes tempted to keep the signal balanced and use two Voltage Controlled Amplifiers (VCAs) to independently control the gain on each half of the balanced signal. Unfortunately, this can result in common-mode to differential-mode conversion (degrading CMRR) when there are even slight differences in

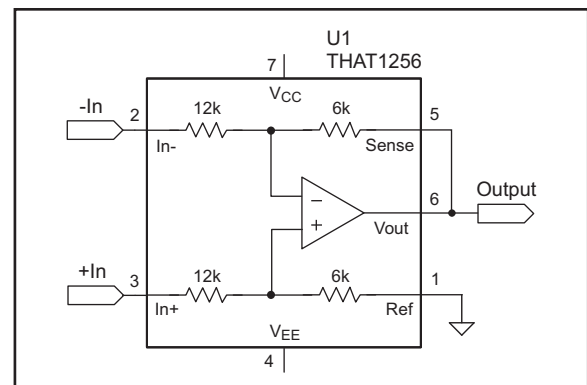


Figure 7. -6 dB line receiver

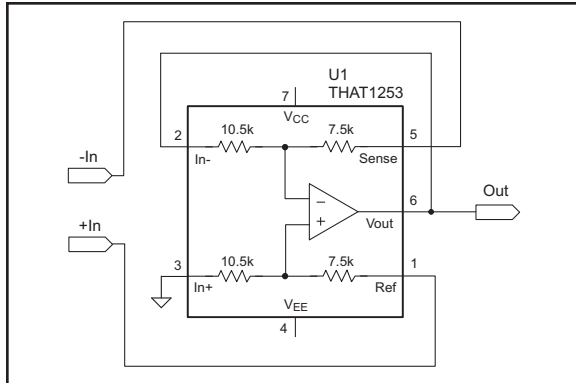


Figure 8. +3 dB line receiver

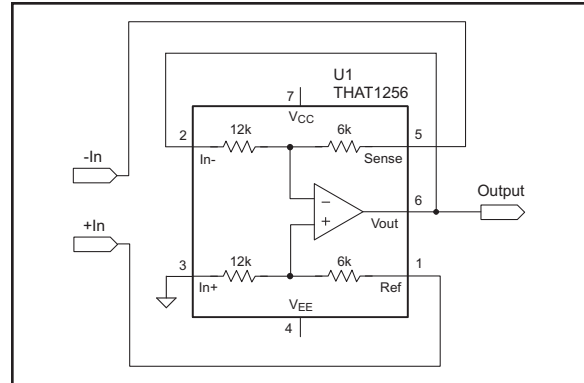


Figure 9. +6 dB line receiver

gain between the VCAs. A better approach is to convert the signal to single-ended, alter the gain, and then convert back to balanced.

In Figure 12 we use a THAT 1253 -3 dB line receiver to do the balanced-to-single-ended conversion. The VCA section also has a static gain of -3 dB due to the ratio of  $R_2$  to  $R_3$ . This circuit can accept +24 dBu at its input, since the THAT 1253 output stage is capable of delivering 21 dBu without distortion. Reducing  $R_3$  to 14 k $\Omega$  results in a 3 dB reduction in VCA output noise. This arrangement results in 3 dB greater dynamic range compared to the case where a -6 dB line receiver and a VCA with zero dB static gain are used. After the VCA, the signal is restored to 24 dBu by the THAT 1606.

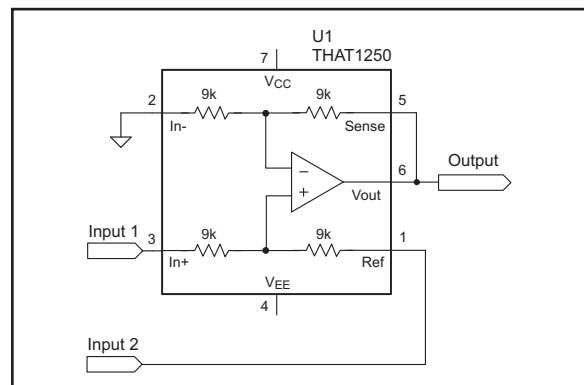


Figure 10. Precision two-input summing circuit

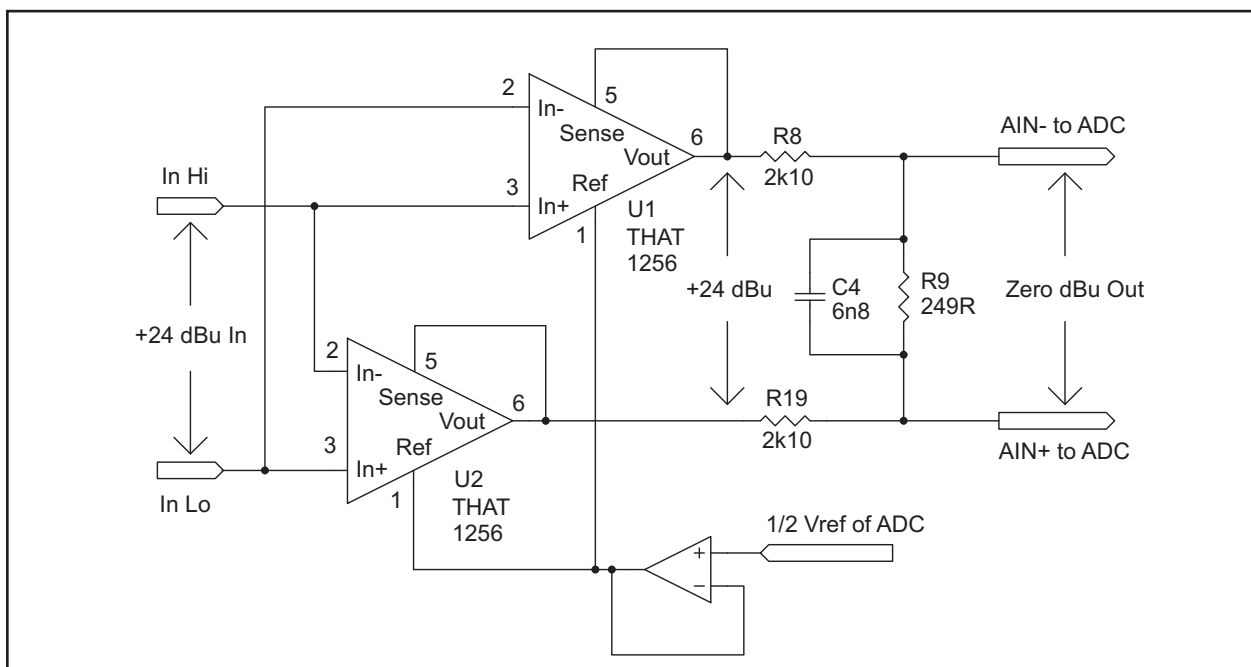


Figure 11. Circuit for audio ADCs with balanced inputs

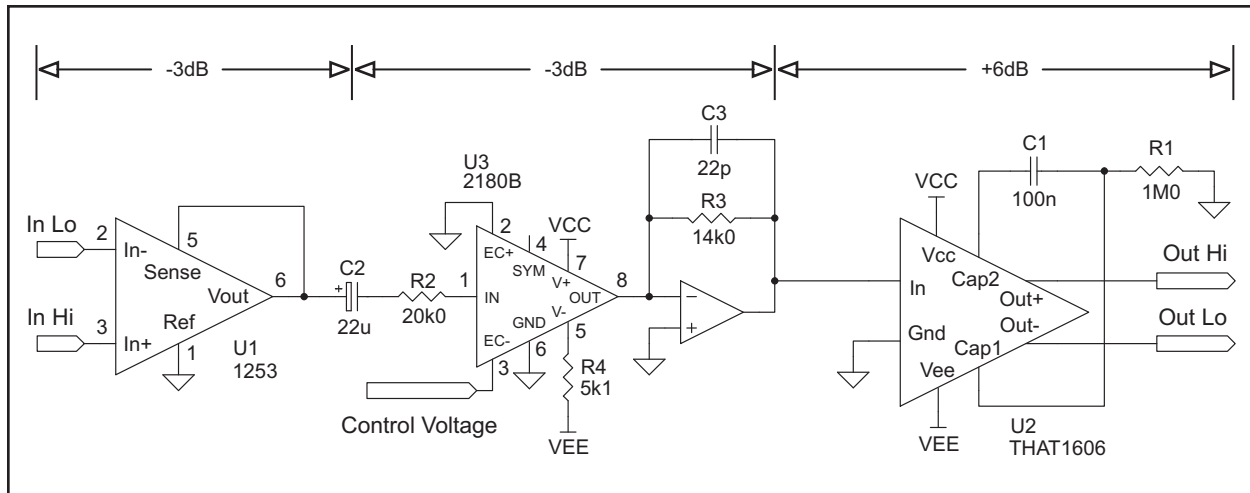


Figure 12. Automated gain control of a balanced signal

### Package and Soldering Information

The THAT 1250 series is available in both 8-pin mini-DIP and 8-pin SOIC packages. The package dimensions are shown in Figures 13 and 14 below, while pinouts are given in Table 1 on page 1.

The 1250 series is available only in lead-free, "green" packages (both SO and DIP). The lead frames are copper, plated with successive layers of nickel palladium, and gold. This approach makes it possible to solder these devices using lead-free *and* lead-bearing solders. The plastic mold compound contains no hazardous substances as specified in the RoHS directive.

The surface-mount package has been qualified using reflow temperatures as high as 260°C for 10 seconds. This makes them suitable for use in a 100% tin solder process. Furthermore, the 1250 series has been qualified to a JEDEC moisture sensitivity level of MSL1. No special humidity precautions are required prior to flow soldering the parts.

The through-hole package leads can be subjected to a soldering temperature of 300 °C for up to 10 seconds

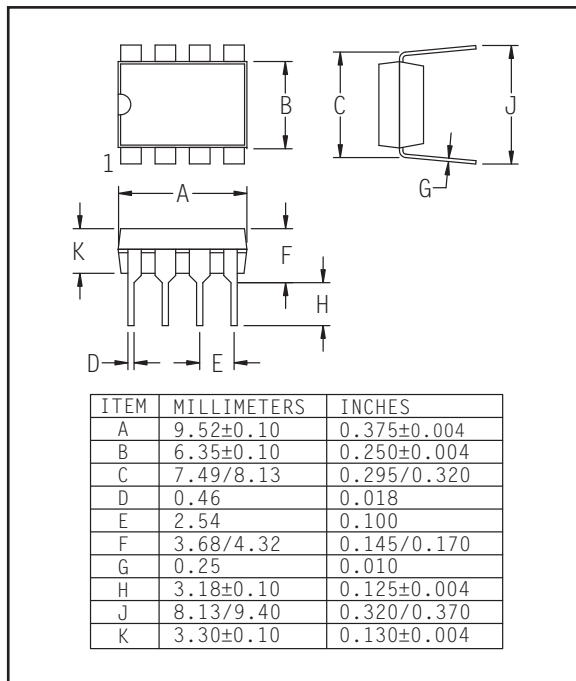


Figure 13. -P (DIP) version package outline drawing

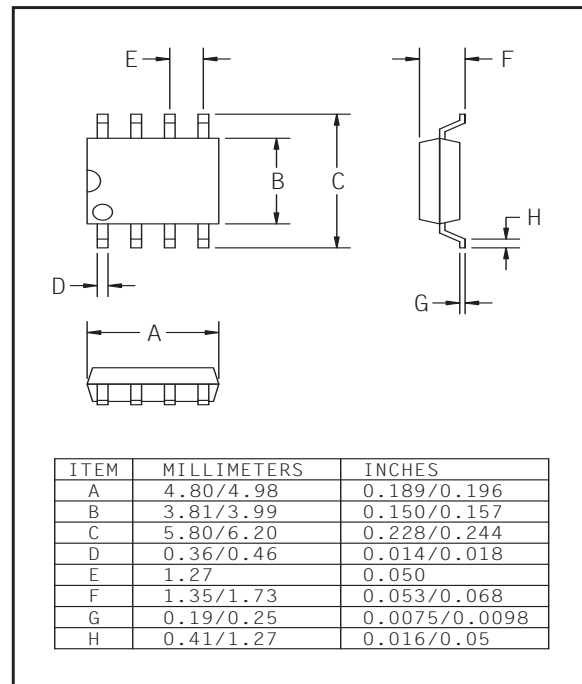


Figure 14. -S (SO) version package outline drawing