350mA, Ultra-Low V_{IN}, RF Low-Dropout Linear Regulator with Bias Pin

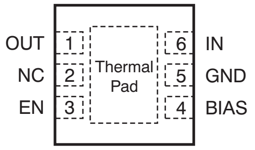
FEATURES

- **350mA High-Performance LDO**
- **Low Quiescent Current: 38µA**
- **Excellent Load Transient Response: ±15mV for I_{LOAD} = 0mA to 350mA in 1µs**
- **Excellent Line Transient Response:**
  ΔV_{OUT} = ±2mV for ΔV_{BIAS} = ±600mV in 1µs
  ΔV_{OUT} = ±200µV for ΔV_{IN} = ±400mV in 1µs
- **Low Noise: 48µV_{RMS} (10Hz to 100kHz)**
- **80dB V_{IN} PSRR (10Hz to 10kHz)**
- **70dB V_{BIAS} PSRR (10Hz to 10kHz)**
- **Fast Start-Up Time: 140µs**
- **Built-In Soft-Start with Monotonic V_{OUT} Rise and Startup Current Limited to 100mA + I_{LOAD}**
- **Over-Current and Thermal Protection**
- **Low Dropout: 110mV at I_{LOAD} = 350mA**
- **Stable with 2.2µF Output Capacitor**
- **Available in 1,33mm x 0,96mm WCSP-5 and 2mm x 2mm SON-6 Packages**

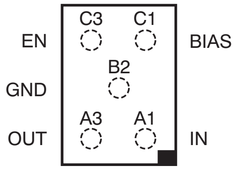
APPLICATIONS

- **Digital Cameras**
- **Cellular Camera Phones**
- **Wireless LAN**
- **Handheld Products**

TPS720xx
DRV PACKAGE
2mm x 2mm SON-6
(TOP VIEW)



TPS720xx
YZU PACKAGE
1,33mm x 0,96mm WCSP-5
(TOP VIEW)



DESCRIPTION

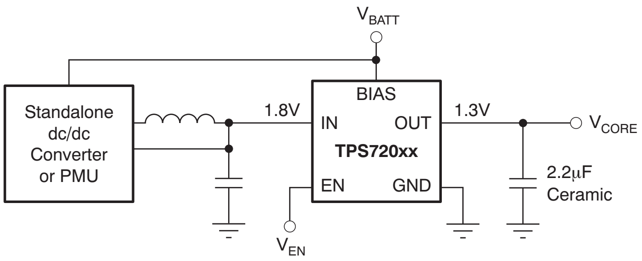
The TPS720xx family of dual rail, low-dropout linear regulators (LDOs) offers outstanding ac performance (PSRR, load and line transient response), while consuming a very low quiescent current of 38µA.

The V_{BIAS} rail that powers the control circuit of the LDO draws very low current (on the order of the quiescent current of the LDO) and can be connected to any power supply that is equal to or greater than 1.4V above the output voltage. The main power path is through V_{IN}, which can be a lower voltage than V_{BIAS}; it can be as low as V_{OUT} + V_{DO}, increasing the efficiency of the solution in many power-sensitive applications. For example, V_{IN} can be an output of a high-efficiency, dc-dc step-down regulator.

The TPS720xx supports a novel feature in which the output of the LDO regulates under light loads when the IN pin is left floating. The light-load drive current is sourced from V_{BIAS} under this condition. This feature is particularly useful in power-saving applications where the dc/dc converter connected to the IN pin is disabled but the LDO is still required to regulate the voltage to a light load.

The TPS720xx is stable with ceramic capacitors and uses an advanced BICMOS fabrication process that yields a dropout of 110mV at a 350mA output load. The TPS720xx has the unique feature of providing a monotonic V_{OUT} rise (overshoot limited to 3%) with V_{IN} inrush current limited to 100mA + I_{LOAD} with an output capacitor of 2.2µF.

The TPS720xx uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over load, line, process, and temperature extremes. An ultra-small wafer chip-scale package (WCSP) makes the TPS720xx ideal for handheld applications. The TPS720xx is also available in a SON-8 package. This family of devices is fully specified over the temperature range of T_J = –40°C to +125°C.



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ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS720***xxyyyz***	**XX** is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V). **YYY** is the package designator. **Z** is tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Output voltages from 0.9V to 3.6V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +125°C (unless otherwise noted). All voltages are with respect to GND.

PARAMETER		TPS720xx	UNIT
Input voltage range (steady-state), V_{IN}(2)		–0.3 to V_{BIAS} or +5.0(3)	V
Peak transient input voltage, V_{IN_PEAK}(4)		+5.5	V
Bias voltage range, V_{BIAS}		–0.3 to +6.0	V
Enable voltage range, V_{EN}		–0.3 to +6.0	V
Output voltage range, V_{OUT}		–0.3 to +5.0	V
Peak output current, I_{OUT}		Internally limited	
Output short-circuit duration		Indefinite	
Total continuous power dissipation, P_{DISS}		See Dissipation Ratings Table	
ESD rating	Human body model (HBM)	2000	V
	Charged device model (CDM)	500	V
	Machine model (MM)	100	V
Operating junction temperature range, T_J		–55 to +125	°C
Storage temperature range, T_{STG}		–55 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) To ensure proper operation of the device it is necessary that $V_{IN} \leq V_{BIAS}$ under all conditions.

(3) Whichever is less.

(4) For durations no longer than 1ms each, for a total of no more than 1000 occurrences over the lifetime of the device.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C	T_A = +70°C	T_A = +85°C
High-K(1)	YZU	51°C/W	248°C/W	4mW/°C	403mW	222mW	160mW
High-K(1)	DRV	20°C/W	65°C/W	15.4mW/°C	1580mW	845mW	615mW

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3- × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4V) or 2.5V (whichever is greater); $V_{IN} \geq V_{OUT}$ + 0.5V, I_{OUT} = 1mA, V_{EN} = 1.1V, C_{OUT} = 2.2µF, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range				1.1(1)		V_{BIAS} or 4.5(2)	V
V_{BIAS}	Bias voltage range				2.5		5.5	V
V_{OUT}(3)	Output voltage range(4)				0.9		3.6	V
	Output accuracy	Nominal	T_J = +25°C		–3.0		+3.0	mV
		Over V_{BIAS}, V_{IN}, I_{OUT}, T_J = –40°C to +125°C	V_{OUT} + 1.4V ≤ V_{BIAS} ≤ 5.5V, V_{OUT} + 0.5V ≤ V_{IN} ≤ 4.5V, 0mA ≤ I_{OUT} ≤ 350mA		–2.0		+2.0	%
		Over V_{BIAS}, V_{IN}, I_{OUT}, T_J = –40°C to +125°C	**DRV package only:** V_{OUT} + 1.4V ≤ V_{BIAS} ≤ 5.5V, V_{OUT} + 0.5V ≤ V_{IN} ≤ 4.5V, 0mA ≤ I_{OUT} ≤ 350mA, V_{OUT} < 1.2V		–25		+25	mV
		Over V_{BIAS}, V_{IN}, I_{OUT}, T_J = –10°C to +85°C	**YZU package only:** V_{OUT} + 1.4V ≤ V_{BIAS} ≤ 5.5V, V_{OUT} + 0.5V ≤ V_{IN} ≤ 4.5V, 0mA ≤ I_{OUT} ≤ 350mA 1.6V ≤ V_{OUT} ≤ 3.3V		–1.0		+1.0	%
		V_{IN} floating	V_{OUT} + 1.4V ≤ V_{BIAS} ≤ 5.5V, 0µA ≤ I_{OUT} ≤ 500µA			±1.0		%
$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} line regulation		V_{IN} = (V_{OUT} + 0.5V) to 4.5V, I_{OUT} = 1mA			16		µV/V
$\Delta V_{OUT}/\Delta V_{BIAS}$	V_{BIAS} line regulation		V_{BIAS} = (V_{OUT} + 1.4V) or 2.5V (whichever is greater) to 5.5V, I_{OUT} = 1mA			16		µV/V
	V_{IN} line transient		ΔV_{IN} = 400mV, t_{RISE} = t_{FALL} = 1µs			±200		µV
	V_{BIAS} line transient		ΔV_{BIAS} = 600mV, t_{RISE} = t_{FALL} = 1µs			±0.8		mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation		0mA ≤ I_{OUT} ≤ 350mA (no load to full load)			–15		µV/mA
	Load transient		0mA ≤ I_{OUT} ≤ 350mA, t_{RISE} = t_{FALL} = 1µs			±15		mV
V_{DO_IN}	V_{IN} dropout voltage(5)		V_{IN} = $V_{OUT(NOM)}$ – 0.1V, (V_{BIAS} – $V_{OUT(NOM)}$) = 1.4V, I_{OUT} = 350mA			110	200	mV
V_{DO_BIAS}	V_{BIAS} dropout voltage(6)		V_{IN} = $V_{OUT(NOM)}$ + 0.3V, I_{OUT} = 350mA			1.09	1.4	V
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(NOM)}$		420	525	800	mA
I_{GND}	Ground pin current		I_{OUT} = 100µA			38		µA
			I_{OUT} = 0mA to 350mA			54	80	µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4V, T_J = -40°C to +85°C			0.5	2	µA
PSRR	V_{IN} power-supply rejection ratio		V_{IN} – V_{OUT} ≥ 0.5V, V_{BIAS} = V_{OUT} + 1.4V, I_{OUT} = 350mA	f = 10Hz		85		dB
				f = 100Hz		85		dB
				f = 1kHz		85		dB
				f = 10kHz		80		dB
				f = 100kHz		70		dB
				f = 1MHz		50		dB

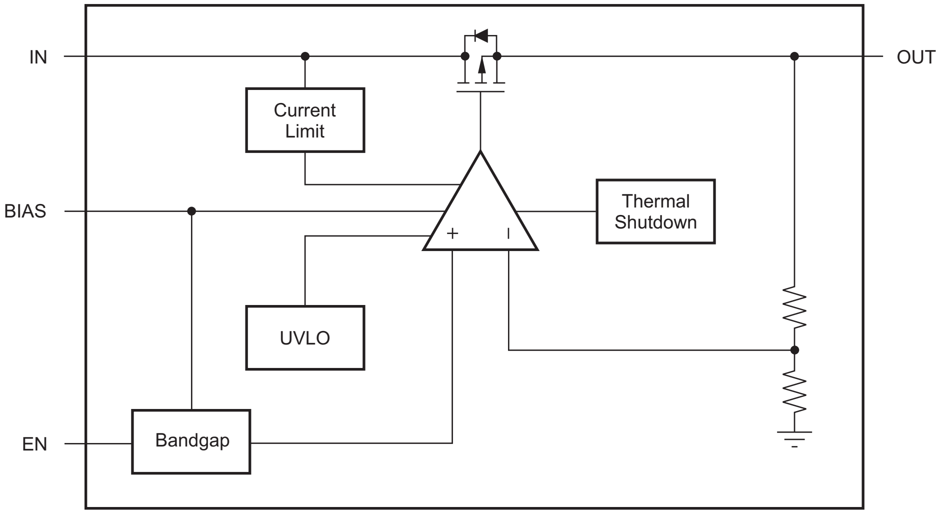
(1) Performance specifications are ensured up to a minimum V_{IN} = V_{OUT} + 0.5V.
(2) Whichever is less.
(3) Minimum V_{BIAS} = (V_{OUT} + 1.4V) or 2.5V (whichever is greater) and V_{IN}= V_{OUT} + 0.5V.
(4) V_O nominal value is factory programmable through the onchip EEPROM.
(5) Measured for devices with $V_{OUT(NOM)}$ ≥ 1.2V.
(6) V_{BIAS} – V_{OUT} with V_{OUT} = $V_{OUT(NOM)}$ – 0.1V. Measured for devices with $V_{OUT(NOM)}$ ≥ 1.8V.

ELECTRICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4V) or 2.5V (whichever is greater); $V_{IN} \geq V_{OUT}$ + 0.5V, I_{OUT} = 1mA, V_{EN} = 1.1V, C_{OUT} = 2.2µF, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PSRR	V_{BIAS} power-supply rejection ratio	$V_{IN} - V_{OUT} \geq 0.5V$, $V_{BIAS} = V_{OUT} + 1.4V$, I_{OUT} = 350mA	f = 10Hz		80		dB
			f = 100Hz		80		dB
			f = 1kHz		75		dB
			f = 10kHz		65		dB
			f = 100kHz		55		dB
			f = 1MHz		35		dB
V_N	Output noise voltage	BW = 10Hz to 100kHz, $V_{BIAS} \geq 2.5V$, $V_{IN} = V_{OUT} + 0.5V$			48		μV_{RMS}
I_{VIN_INRUSH}	Inrush current on V_{IN}	V_{BIAS} = (V_{OUT} +1.4V) or 2.5V (whichever is greater), $V_{IN} = V_{OUT} + 0.5V$			100 + I_{LOAD}		mA
t_{STR}	Startup time	V_{OUT} = 95% $V_{OUT(NOM)}$, I_{OUT} = 350mA, C_{OUT} = 2.2µF			140		µs
$V_{EN(HI)}$	Enable pin high (enabled)			1.1			V
$V_{EN(LO)}$	Enable pin low (disabled)			0		0.4	V
I_{EN}	Enable pin current	V_{EN} = 5.5V, V_{IN} = 4.5V, V_{BIAS} = 5.5V				1.0	µA
UVLO	Undervoltage lockout	V_{BIAS} rising		2.41	2.45	2.49	V
	Hysteresis	V_{BIAS} falling			150		mV
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			+160		°C
		Reset, temperature decreasing			+140		°C
T_J	Operating junction temperature			–40		+125	°C

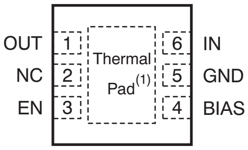
DEVICE INFORMATION



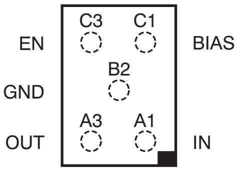
Functional Block Diagram

PIN CONFIGURATION

DRV PACKAGE
SON-6
(TOP VIEW)



YZU PACKAGE
WCSP-5
(TOP VIEW)



(1) It is recommended that the SON (DRV) package thermal pad be connected to ground.

PIN DESCRIPTIONS

TPS720xx			DESCRIPTION
NAME	DRV	YZU	
OUT	1	A3	Output pin. A 2.2μF ceramic capacitor is connected from this pin to ground, for stability and to provide load transients. See *Input and Output Capacitor Requirements* in the *Application Information* section.
NC	2	—	No connection.
EN	3	C3	Enable pin. A logic high signal on this pin turns the device on and regulates the voltage from IN to OUT. A logic low on this pin turns off the device.
BIAS	4	C1	Bias supply pin. It is recommended that this input be bypassed with a ceramic capacitor to ground for better transient performance. See *Input and Output Capacitor Requirements* in the *Application Information* section.
GND	5	B2	Ground pin.
IN	6	A1	Input pin. This pin can be a maximum of 4.5V; V_{IN} must not exceed V_{BIAS}. Bypass this input with a ceramic capacitor to ground. See *Input and Output Capacitor Requirements* in the *Application Information* section.

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4V) or 2.5V (whichever is greater); V_{IN} = V_{OUT} + 0.5V, I_{OUT} = 1mA, V_{EN} = 1.1V, C_{OUT} = 2.2µF, unless otherwise noted. Typical values are at T_J = +25°C.

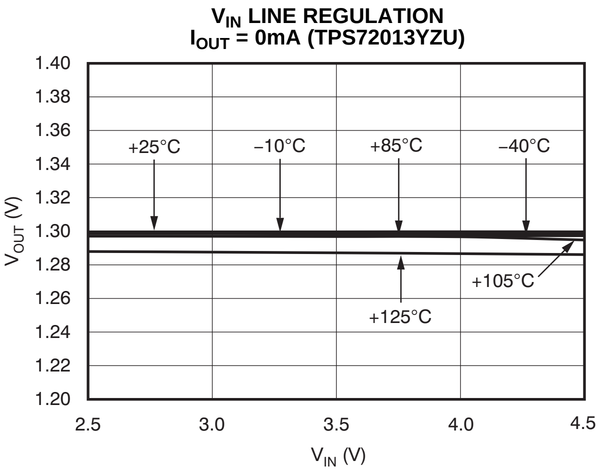


Figure 1.

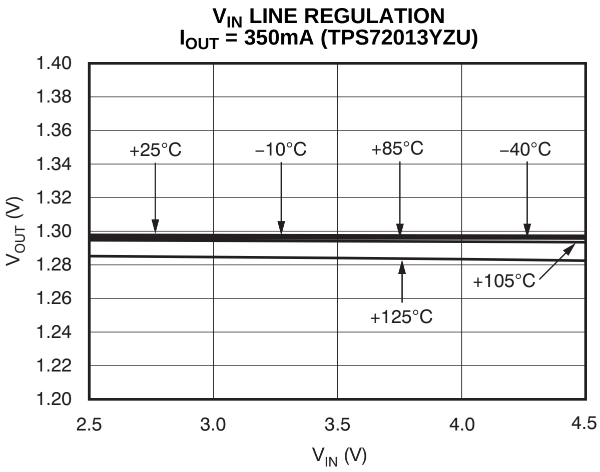


Figure 2.

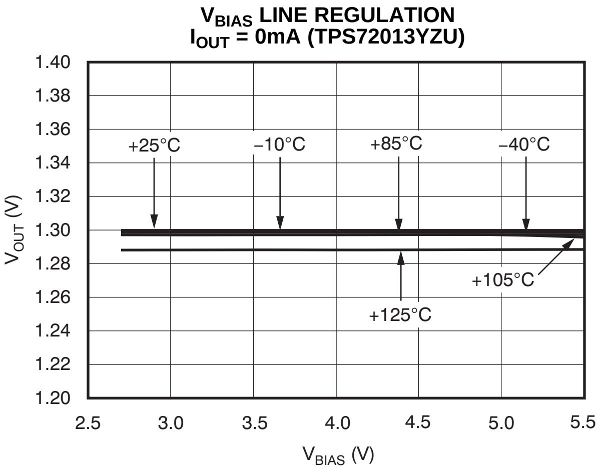


Figure 3.

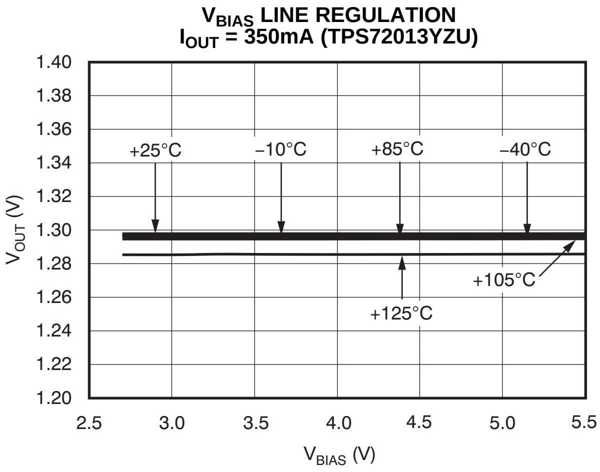


Figure 4.

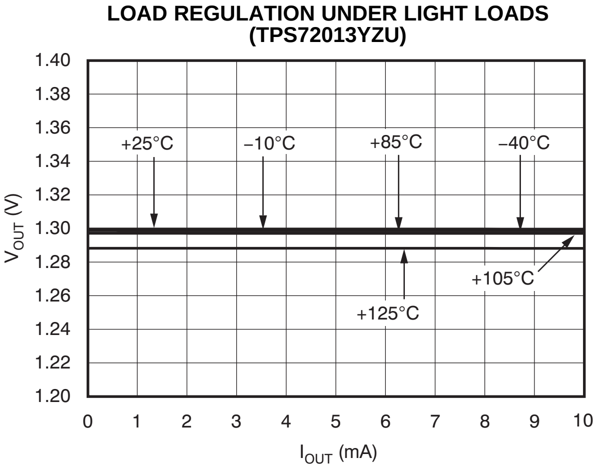


Figure 5.

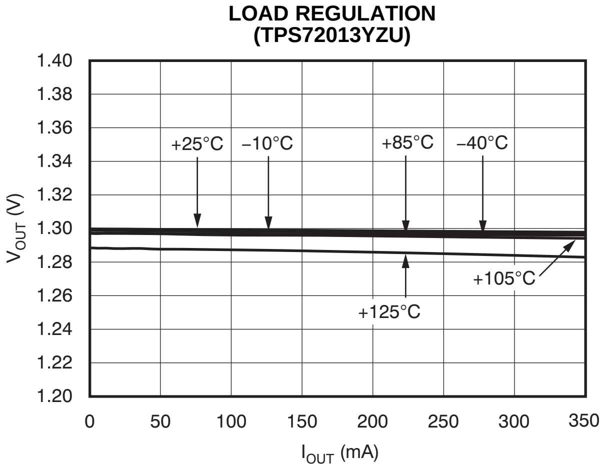


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4V) or 2.5V (whichever is greater); V_{IN} = V_{OUT} + 0.5V, I_{OUT} = 1mA, V_{EN} = 1.1V, C_{OUT} = 2.2µF, unless otherwise noted. Typical values are at T_J = +25°C.

LOAD REGULATION WITH V_{IN} FLOATING (TPS72013YZU)

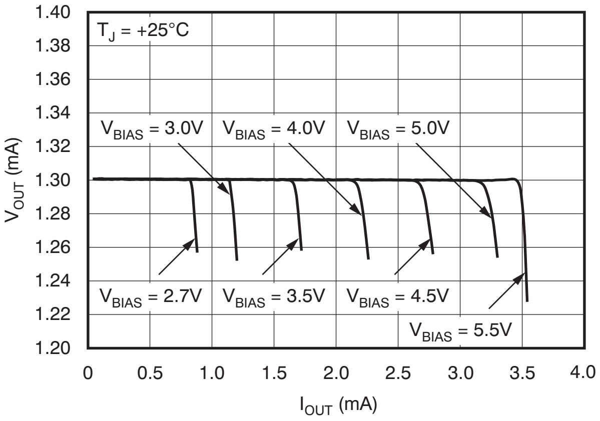


Figure 7.

LOAD REGULATION WITH V_{IN} FLOATING (TPS72013YZU)

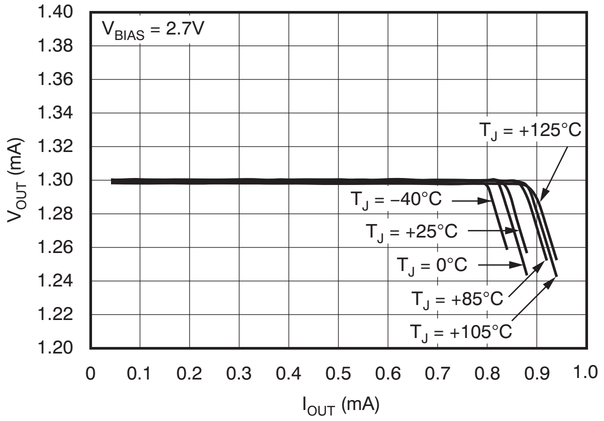


Figure 8.

V_{IN} DROPOUT VOLTAGE vs OUTPUT CURRENT (TPS72013YZU)

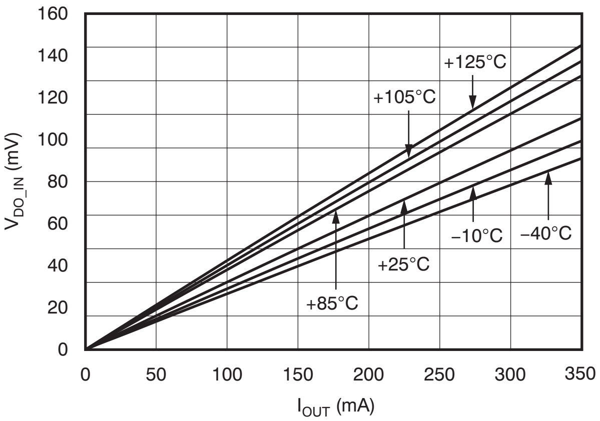


Figure 9.

V_{BIAS} DROPOUT VOLTAGE vs TEMPERATURE (TPS72033YZU)

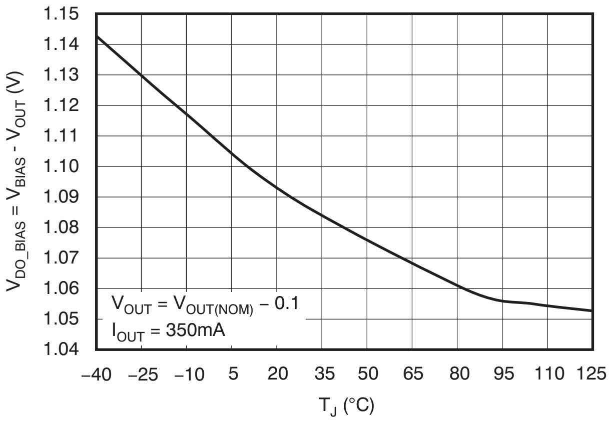


Figure 10.

OUTPUT VOLTAGE vs TEMPERATURE (TPS72013YZU)

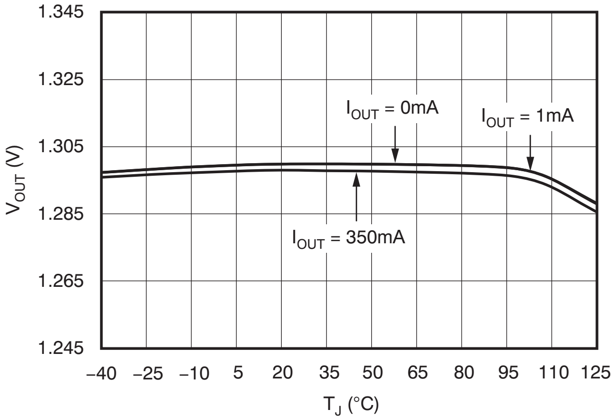


Figure 11.

GROUND PIN CURRENT vs V_{BIAS} INPUT VOLTAGE (TPS72013YZU)

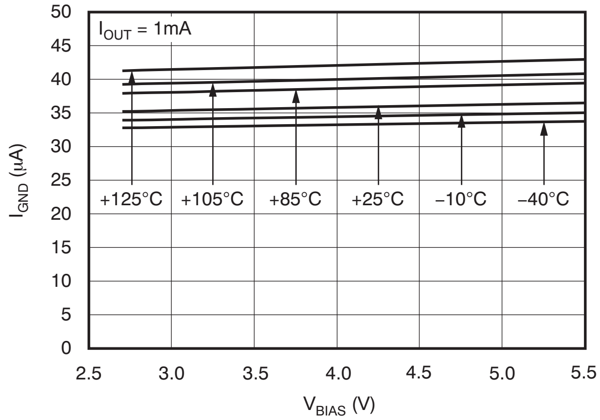


Figure 12.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4V) or 2.5V (whichever is greater); V_{IN} = V_{OUT} + 0.5V, I_{OUT} = 1mA, V_{EN} = 1.1V, C_{OUT} = 2.2µF, unless otherwise noted. Typical values are at T_J = +25°C.

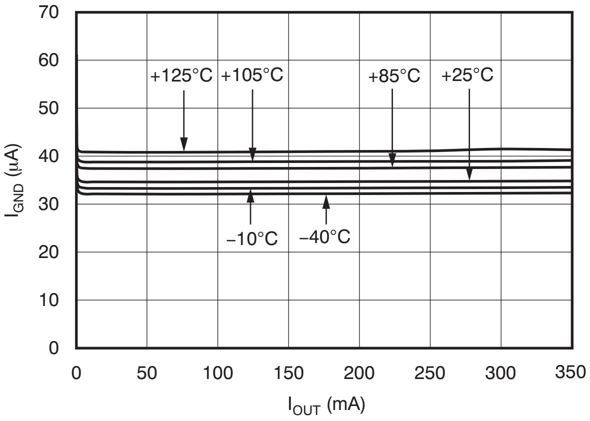

GROUND PIN CURRENT vs OUTPUT CURRENT (TPS72013YZU)

Figure 13.

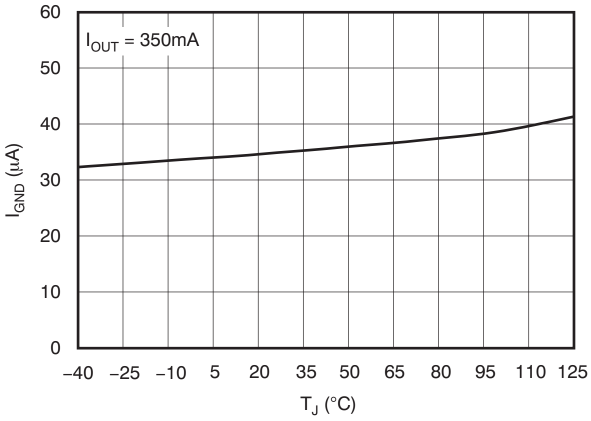

GROUND PIN CURRENT vs TEMPERATURE (TPS72013YZU)

Figure 14.

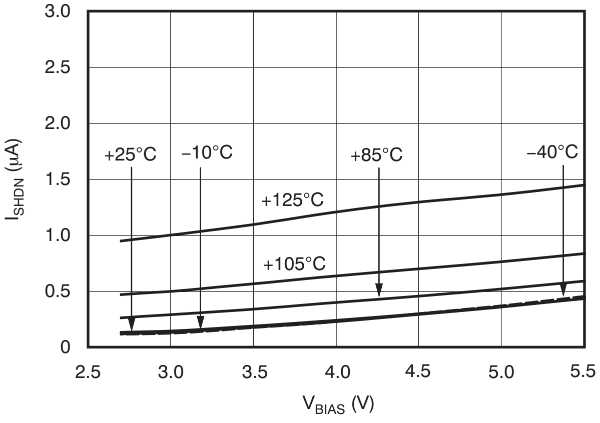

SHUTDOWN CURRENT vs V_{BIAS} INPUT VOLTAGE (TPS72013YZU)

Figure 15.

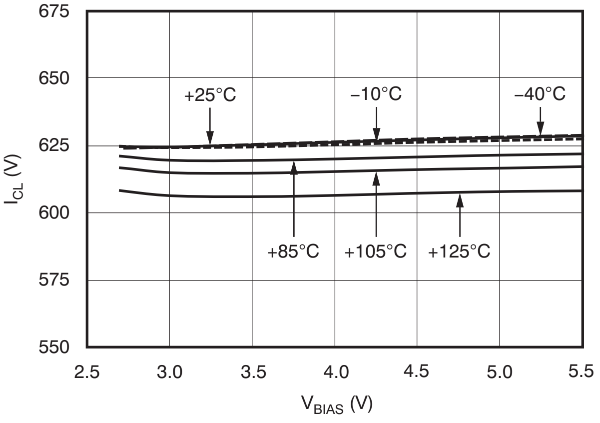

CURRENT LIMIT vs V_{BIAS} INPUT VOLTAGE (TPS72013YZU)

Figure 16.

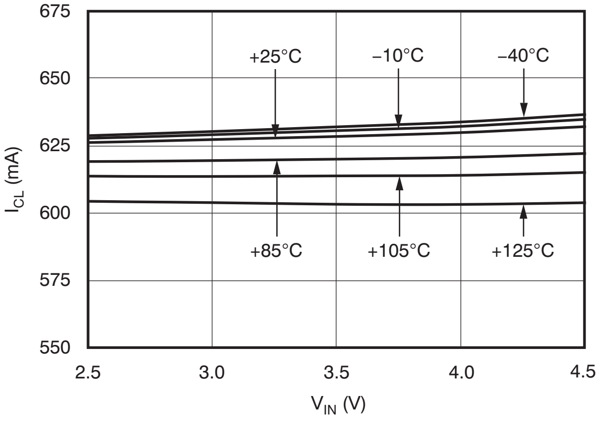

CURRENT LIMIT vs V_{IN} INPUT VOLTAGE (TPS72013YZU)

Figure 17.

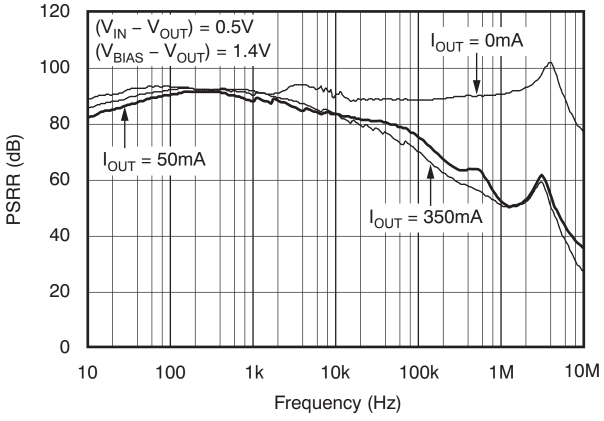

V_{IN} POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (TPS72015YZU)

Figure 18.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4V) or 2.5V (whichever is greater); V_{IN} = V_{OUT} + 0.5V, I_{OUT} = 1mA, V_{EN} = 1.1V, C_{OUT} = 2.2µF, unless otherwise noted. Typical values are at T_J = +25°C.

V_{IN} POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (TPS72015YZU)

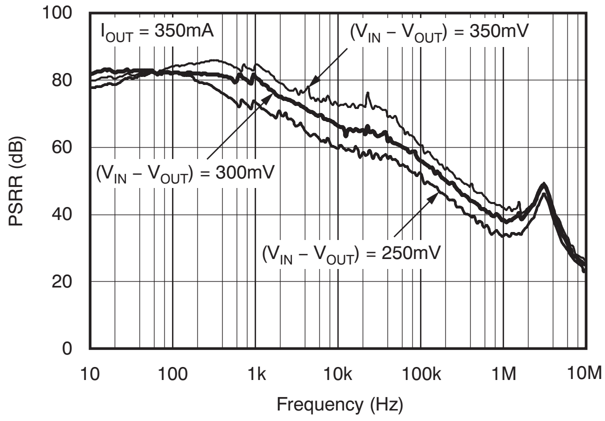


Figure 19.

V_{BIAS} POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (TPS72015YZU)

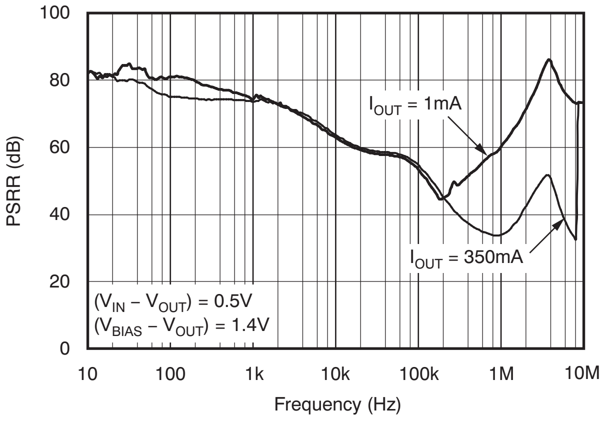


Figure 20.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY (TPS72015YZU)

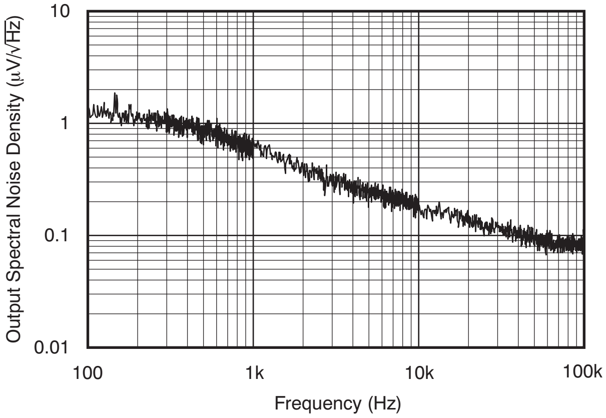


Figure 21.

V_{IN} INRUSH CURRENT
V_{IN} = 1.8V, V_{OUT} = 1.3V, V_{BIAS} = 2.7V, I_{OUT} = 0mA

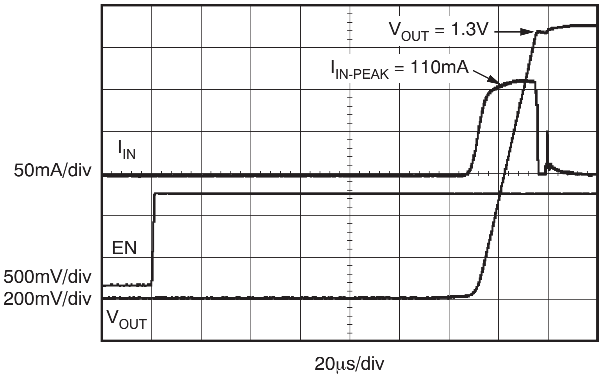


Figure 22.

V_{IN} INRUSH CURRENT
V_{IN} = 1.8V, V_{OUT} = 1.3V, V_{BIAS} = 2.7V, I_{OUT} = 350mA

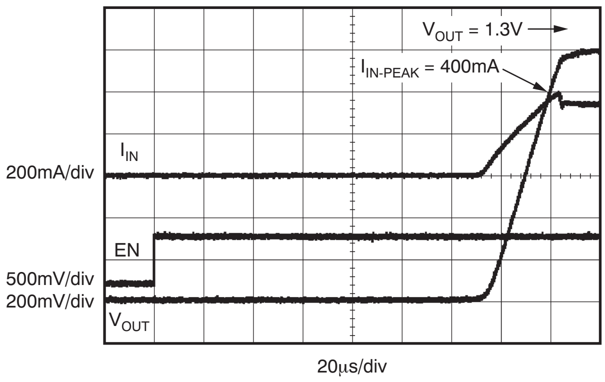


Figure 23.

V_{IN} LINE TRANSIENT RESPONSE
V_{IN} = 1.6V to 2.0V, V_{OUT} = 1.3V, V_{BIAS} = 2.7V,
V_{IN} SLEW RATE = 1V/µs, I_{OUT} = 350mA

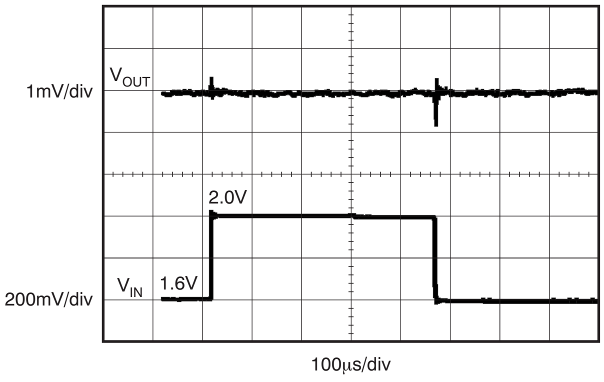


Figure 24.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4V) or 2.5V (whichever is greater); V_{IN} = V_{OUT} + 0.5V, I_{OUT} = 1mA, V_{EN} = 1.1V, C_{OUT} = 2.2µF, unless otherwise noted. Typical values are at T_J = +25°C.

V_{BIAS} LINE TRANSIENT RESPONSE
V_{IN} = 1.8V, V_{OUT} = 1.3V, V_{BIAS} = 2.7V to 3.3V,
V_{BIAS} SLEW RATE = 600m/µs, I_{OUT} = 350mA

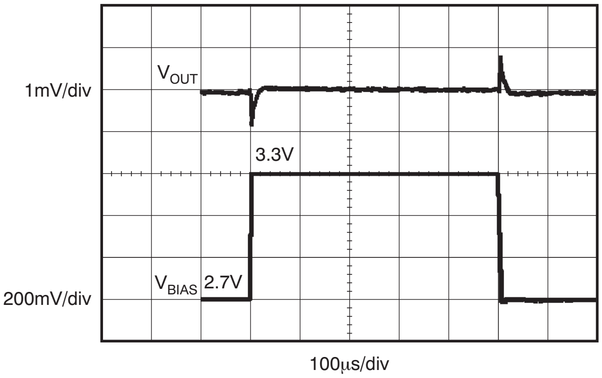


Figure 25.

LOAD TRANSIENT RESPONSE
V_{IN} = 1.8V, V_{OUT} = 1.3V, V_{BIAS} = 2.7V, t_{RISE} = 1µs

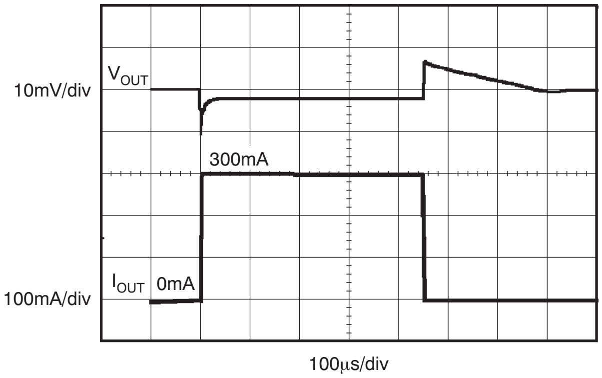


Figure 26.

APPLICATION INFORMATION

The TPS720xx belongs to a family of new generation LDO regulators that use innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR (up to 1MHz) at very low headroom ($V_{IN} – V_{OUT}$). The implementation of the BIAS pin on the TPS720xx vastly improves efficiency of low V_{OUT} applications by allowing the use of a preregulated, low-voltage input supply. The TPS720xx supports a novel feature in which the output of the LDO regulates under light loads (<500μA) when the IN pin is left floating. The light-load drive current is sourced from V_{BIAS} under this condition. This feature is particularly useful in power-saving applications where the dc/dc converter connected to the IN pin is disabled but the LDO is still required to regulate the voltage to a light load. These features, combined with low noise, low ground pin current, and ultra-small packaging, make this device ideal for portable applications. This family of regulators offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from –40°C to +125°C.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability on the IN pin, it is good analog design practice to connect a 0.1μF to 1.0μF low equivalent series resistance (ESR) capacitor across the IN pin input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located close to the power source. If source impedance is not sufficiently low, a 0.1μF input capacitor may be necessary to ensure stability.

The BIAS pin does not require an input capacitor because it does not source high currents. However, if source impedance is not sufficiently low, a small 0.1μF bypass capacitor is recommended.

The TPS720xx is designed to be stable with standard ceramic capacitors with values of 2.2μF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 250mΩ.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High equivalent series resistance (ESR) capacitors may degrade PSRR. The BIAS pin draws very little current and can be routed as a signal (make sure to shield it from high-frequency coupling).

INTERNAL CURRENT LIMIT

The TPS720xx internal current limits help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The NMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{LIMIT}$ until thermal shut down is triggered and the device is turned off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details.

The NMOS pass element in the TPS720xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current is recommended.

INRUSH CURRENT LIMIT

The TPS720xx family of LDO regulators implement a novel inrush current-limit circuit architecture: the current drawn through the IN pin is limited to a finite value. This $I_{INRUSHLIMIT}$ charges the output to its final voltage. All the current drawn through V_{IN} goes to charge the output capacitance when the load is disconnected. The following equation shows the inrush current limit performed by the circuit:

$$I_{INRUSHLIMIT}(A) = C_{OUT}(\mu F) \times 0.0454545(V/\mu s) + I_{LOAD}(A) \quad (1)$$

Assuming a C_{OUT} of 2.2μF with the load disconnected (that is, $I_{LOAD} = 0$) the $I_{INRUSHLIMIT}$ is calculated to be 100mA. The inrush current charges the LDO output capacitor. If the output of the LDO regulates to 1.3V, then the LDO charges the output capacitor to the final output value in approximately 28.6μs.

Another consideration is when a load is connected to the output of an LDO. The connected load tries to steer a portion of the current away from V_{OUT}. The TPS720xx inrush current-limit circuit employs a new technique that supplies not only the $I_{INRUSHLIMIT}$, but also the additional current needed by the load. If I_{LOAD} = 350mA, then the $I_{INRUSHLIMIT}$ calculates to be approximately 450mA (from Equation 1).

SHUTDOWN

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to the IN pin.

DROPOUT VOLTAGE

The TPS720xx uses a NMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the NMOS pass element. V_{DO} approximately scales with output current because the NMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 19 in the *Typical Characteristics* section.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

UNDERVOLTAGE LOCK-OUT (UVLO)

The TPS720xx uses an undervoltage lock-out circuit on the BIAS pin to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that it typically ignores undershoot transients on the input if they are less than 50µs duration.

MINIMUM LOAD

The TPS720xx is stable with no output load. Traditional LDOs suffer from low loop gain at very light output loads. The TPS720xx employs an innovative, low-current mode circuit under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

OUTPUT REGULATION WITH IN PIN FLOATING

The TPS720xx supports a novel feature in which the output of the LDO regulates under light loads when the IN pin is left floating. Under normal conditions, when the IN pin is connected to a power source, the BIAS pin draws only tens of milliamperes. However, when the IN pin is floating, an innovative circuit is used that allows a mximum current of 500µA to be drawn by the load through the BIAS pin, while maintaining the output in regulation. This feature is particularly useful in power-saving applications where a dc/dc converter connected to the IN pin is disabled, but the LDO is required to regulate the output voltage to a light load.

Figure 27 shows an application example where a microcontroller is not turned off (to maintain the state of the internal memory), but where the regulated supply (shown as the TPS62xxx) is turned off to reduce power. In this case, the TPS720xx BIAS pin provides sufficient load current to maintain a regulated voltage to the microcontroller.

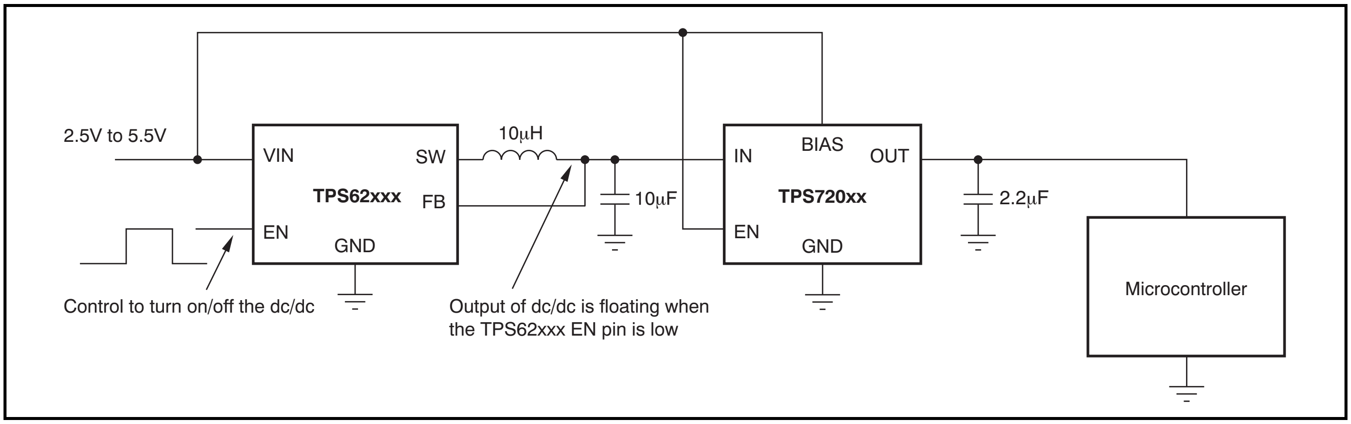


Figure 27. Example of Floating IN Pin Regulation

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS720xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS720xx into thermal shutdown degrades device reliability.

POWER DISSIPATION

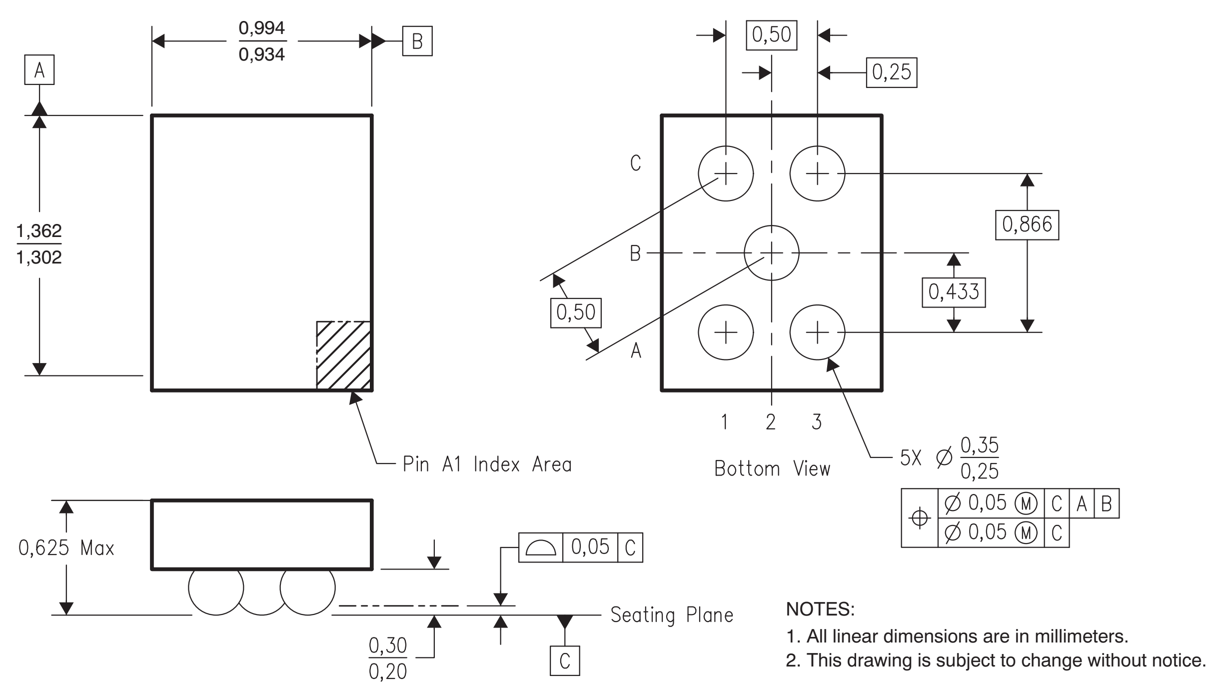
The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Dissipation Ratings* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS720xx are available from the Texas Instruments web site at www.ti.com.



NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Figure 28. YZU Wafer Chip-Scale Package Dimensions (in mm)

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September, 2008) to Revision D	Page
• Added electrical specifications for DRV package	3
• Noted electrical specifications for YZU package	3

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS720105DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS720105DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS720105YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS720105YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS72010DRVR	PREVIEW	SON	DRV	6	3000	TBD	Call TI	Call TI
TPS72010DRVT	PREVIEW	SON	DRV	6	250	TBD	Call TI	Call TI
TPS72012DRVR	PREVIEW	SON	DRV	6	3000	TBD	Call TI	Call TI
TPS72012DRVT	PREVIEW	SON	DRV	6	250	TBD	Call TI	Call TI
TPS72012YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS72012YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS72013YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS72013YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS72015DRVR	PREVIEW	SON	DRV	6	3000	TBD	Call TI	Call TI
TPS72015DRVT	PREVIEW	SON	DRV	6	250	TBD	Call TI	Call TI
TPS72015YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS72015YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS72017YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS72017YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS72018DRVR	PREVIEW	SON	DRV	6	3000	TBD	Call TI	Call TI
TPS72018DRVT	PREVIEW	SON	DRV	6	250	TBD	Call TI	Call TI
TPS72018YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS72018YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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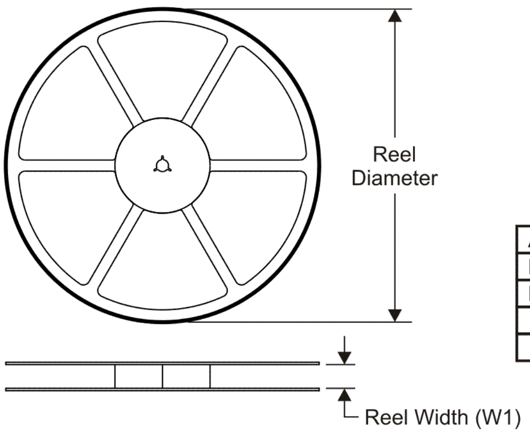
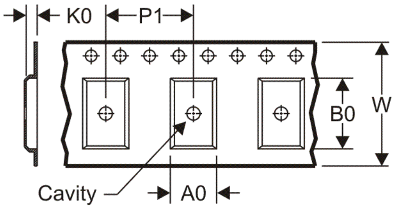
TAPE AND REEL INFORMATION

REEL DIMENSIONS

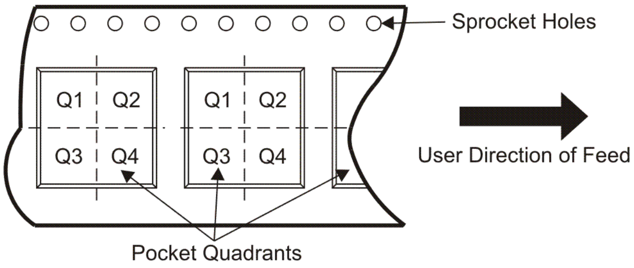


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

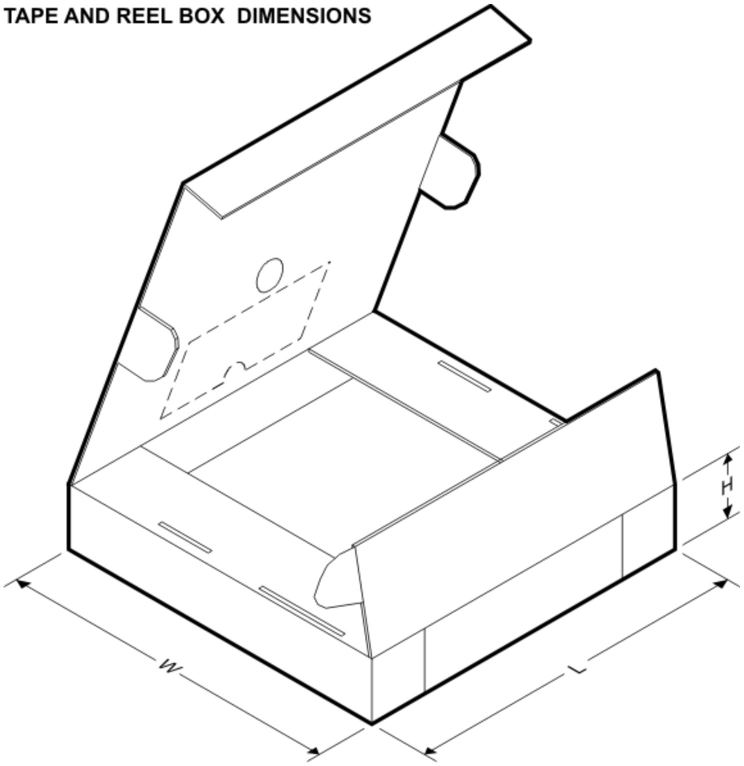
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS720105DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS720105DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS720105YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.09	1.42	0.81	4.0	8.0	Q1
TPS720105YZUT	DSBGA	YZU	5	250	180.0	8.4	1.09	1.42	0.81	4.0	8.0	Q1
TPS72012YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.09	1.42	0.81	4.0	8.0	Q1
TPS72012YZUT	DSBGA	YZU	5	250	180.0	8.4	1.09	1.42	0.81	4.0	8.0	Q1
TPS72013YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.09	1.42	0.81	4.0	8.0	Q1
TPS72013YZUT	DSBGA	YZU	5	250	180.0	8.4	1.09	1.42	0.81	4.0	8.0	Q1
TPS72015YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.09	1.42	0.81	4.0	8.0	Q1
TPS72015YZUT	DSBGA	YZU	5	250	180.0	8.4	1.09	1.42	0.81	4.0	8.0	Q1
TPS72017YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.09	1.42	0.81	4.0	8.0	Q1
TPS72017YZUT	DSBGA	YZU	5	250	180.0	8.4	1.09	1.42	0.81	4.0	8.0	Q1
TPS72018YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.09	1.42	0.81	4.0	8.0	Q1
TPS72018YZUT	DSBGA	YZU	5	250	180.0	8.4	1.09	1.42	0.81	4.0	8.0	Q1

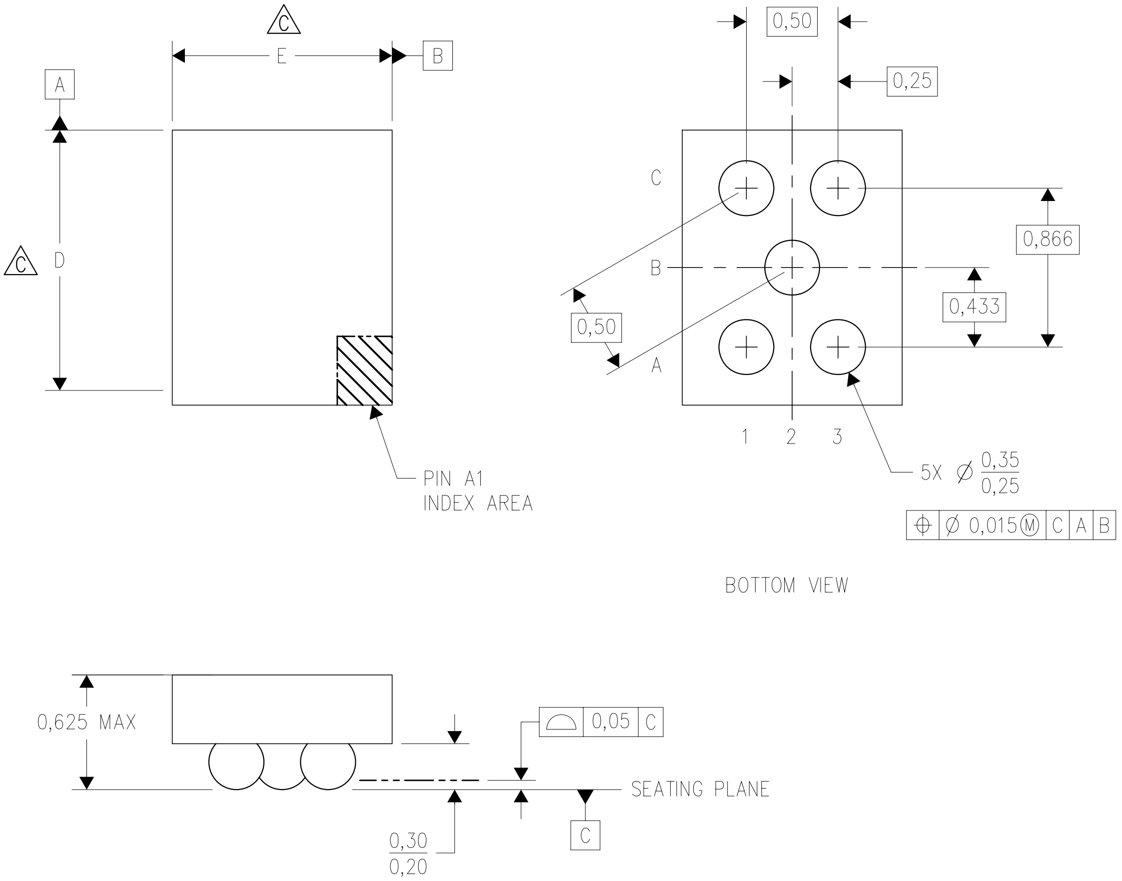
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS720105DRVR	SON	DRV	6	3000	195.0	200.0	45.0
TPS720105DRVT	SON	DRV	6	250	195.0	200.0	45.0
TPS720105YZUR	DSBGA	YZU	5	3000	190.5	212.7	31.8
TPS720105YZUT	DSBGA	YZU	5	250	190.5	212.7	31.8
TPS72012YZUR	DSBGA	YZU	5	3000	190.5	212.7	31.8
TPS72012YZUT	DSBGA	YZU	5	250	190.5	212.7	31.8
TPS72013YZUR	DSBGA	YZU	5	3000	190.5	212.7	31.8
TPS72013YZUT	DSBGA	YZU	5	250	190.5	212.7	31.8
TPS72015YZUR	DSBGA	YZU	5	3000	190.5	212.7	31.8
TPS72015YZUT	DSBGA	YZU	5	250	190.5	212.7	31.8
TPS72017YZUR	DSBGA	YZU	5	3000	190.5	212.7	31.8
TPS72017YZUT	DSBGA	YZU	5	250	190.5	212.7	31.8
TPS72018YZUR	DSBGA	YZU	5	3000	190.5	212.7	31.8
TPS72018YZUT	DSBGA	YZU	5	250	190.5	212.7	31.8

YZU (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



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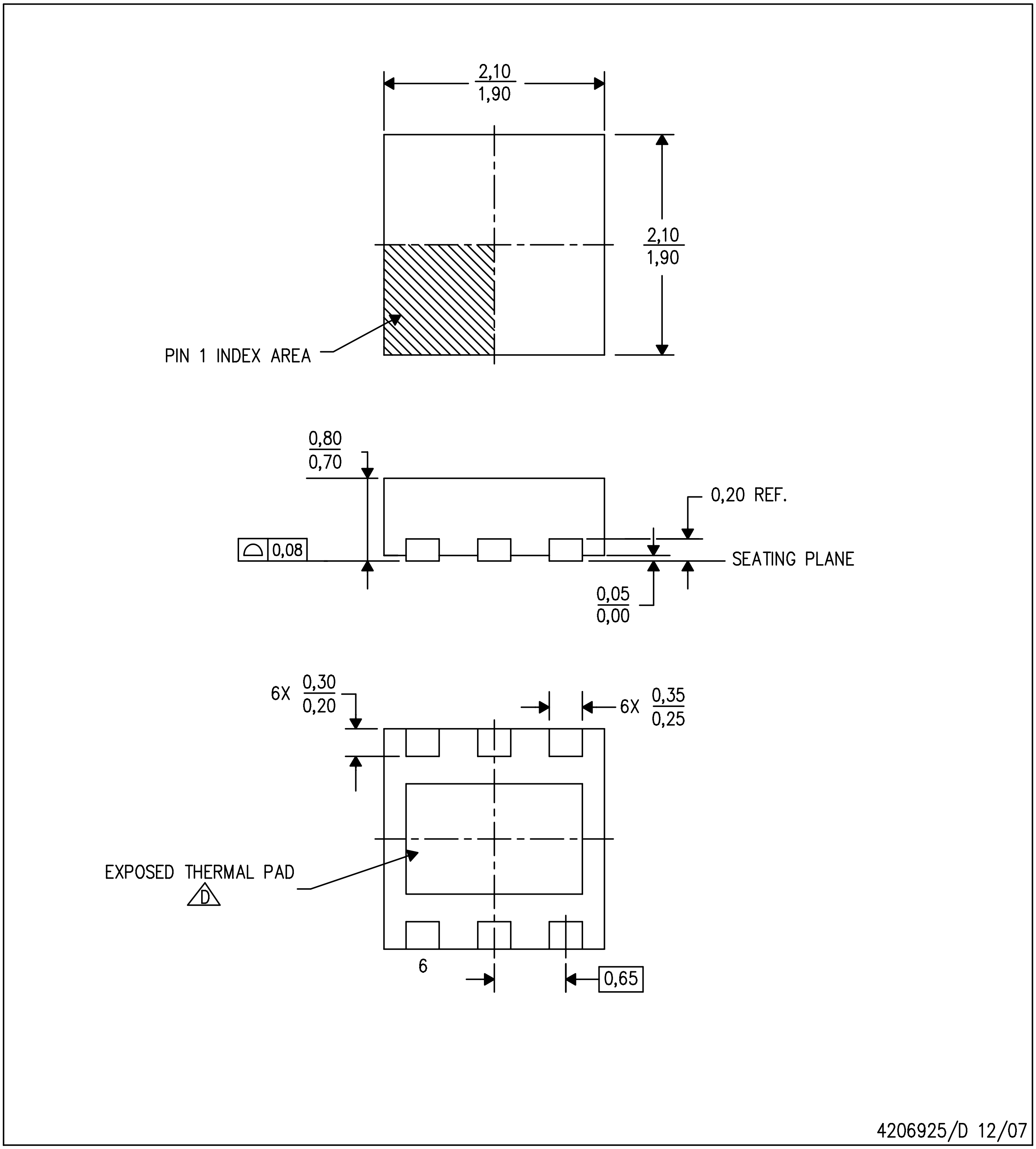
Notes:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Devices in this YZQ package can have dimension D ranging from 1.31 to 1.75 mm and dimension E ranging from 0.94 to 1.45 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
- D. NanoFree™ package configuration.
- E. This package contains lead–free balls. Refer to the 5 YEU package (drawing 4205430) for tin–lead (SnPb) balls.

NanoFree is a trademark of Texas Instruments.

DRV (S–PDSO–N6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

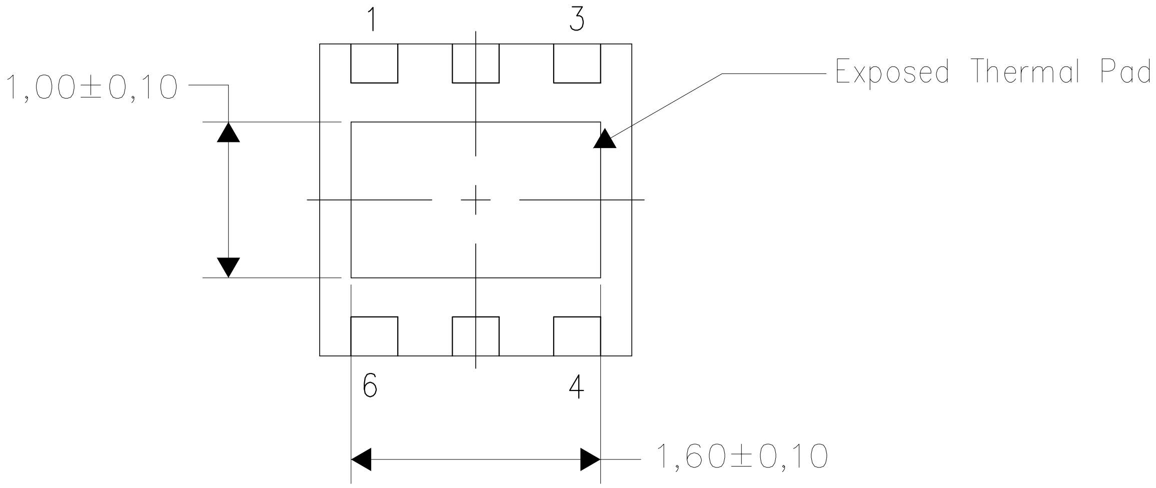
THERMAL PAD MECHANICAL DATA

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

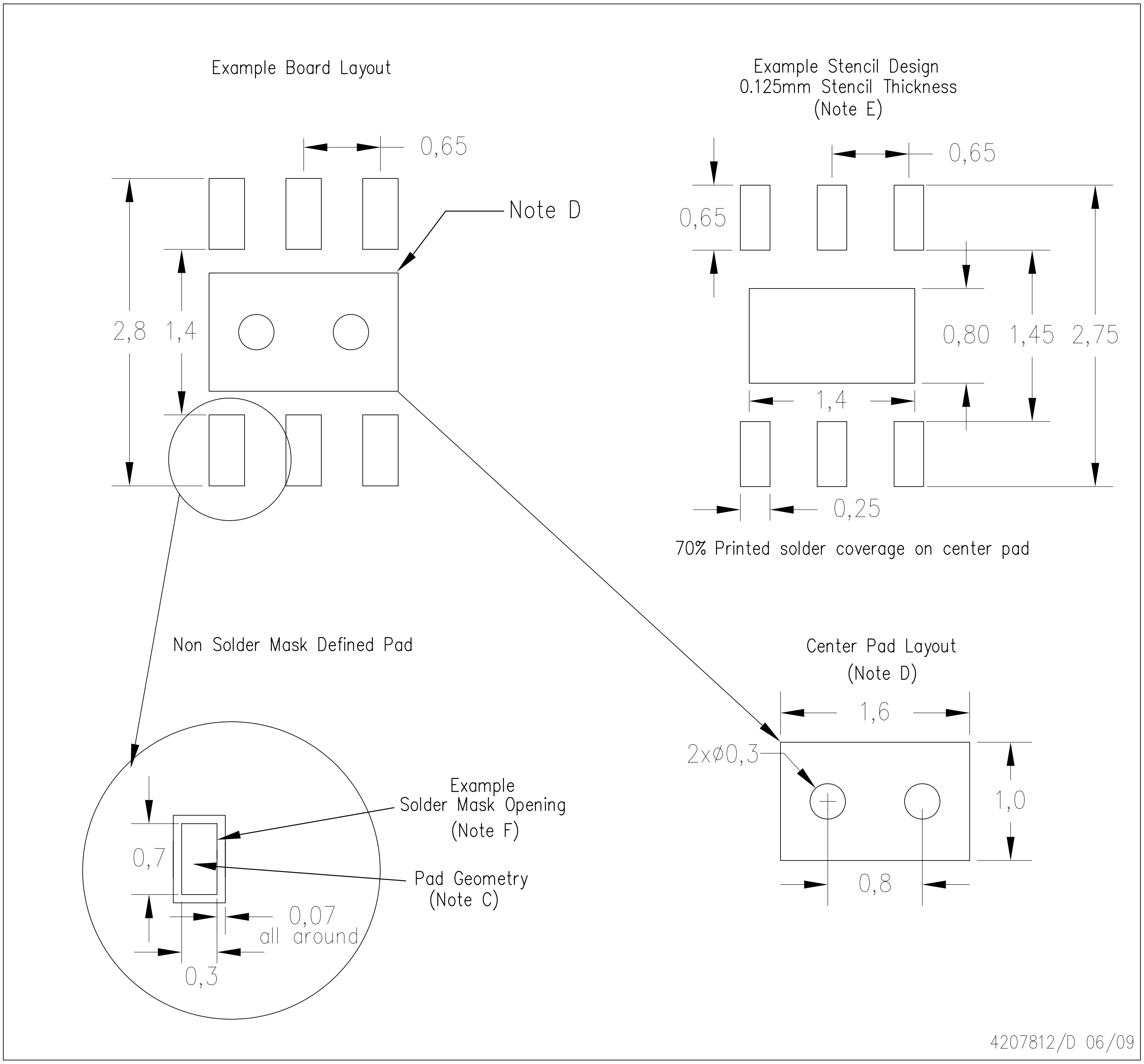


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRV (S-PWSON-N6)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

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