PRECISION ADJUSTABLE CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES

FEATURES

- Up to 1.5 A Maximum Load Current
- ±6% Current-Limit Accuracy at 1.7 A (typ)
- Meets USB Current-Limiting Requirements
- Backwards Compatible with TPS2550/51
- Adjustable Current Limit, 75 mA–1700 mA (typ)
- Constant-Current (TPS2552/53) and Latch-off (TPS2552-1/53-1) Versions
- Fast Overcurrent Response - 2-μS (typ)
- 85-mΩ High-Side MOSFET (DBV Package)
- Reverse Input-Output Voltage Protection
- Operating Range: 2.5 V to 6.5 V
- Built-in Soft-Start
- 15 kV ESD Protection per IEC 61000-4-2 (with External Capacitance)
- UL Listed – File No. E169910

APPLICATIONS

- USB Ports/Hubs
- Digital TV
- Set-Top Boxes
- VOIP Phones

DESCRIPTION

The TPS2552/53 and TPS2552-1/53-1 power-distribution switches are intended for applications where precision current limiting is required or heavy capacitive loads and short circuits are encountered and provide up to 1.5 A of continuous load current. These devices offer a programmable current-limit threshold between 75 mA and 1.7 A (typ) via an external resistor. Current-limit accuracy as tight as ±6% can be achieved at the higher current-limit settings. The power-switch rise and fall times are controlled to minimize current surges during turn on/off.

TPS2552/53 devices limit the output current to a safe level by using a constant-current mode when the output load exceeds the current-limit threshold. TPS2552-1/53-1 devices provide circuit breaker functionality by latching off the power switch during overcurrent or reverse-voltage situations. An internal reverse-voltage comparator disables the power-switch when the output voltage is driven higher than the input to protect devices on the input side of the switch. The $\overline{\text{FAULT}}$ output asserts low during overcurrent and reverse-voltage conditions.

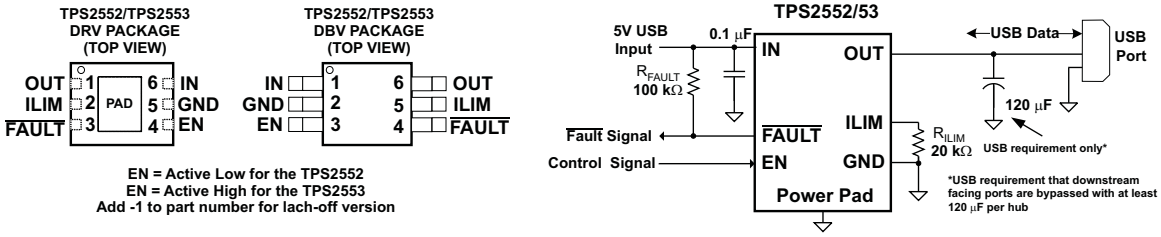


Figure 1. Typical Application as USB Power Switch

GENERAL SWITCH CATALOG

33 mΩ, single	80 mΩ, single	80 mΩ, dual	80 mΩ, dual	80 mΩ, triple	80 mΩ, quad	80 mΩ, quad
TPS201xA 0.2 A - 2 A	TPS2014 600 mA	TPS2042B 500 mA	TPS2080 500 mA	TPS2043B 500 mA	TPS2044B 500 mA	TPS2085 500 mA
TPS202x 0.2 A - 2 A	TPS2015 1 A	TPS2052B 500 mA	TPS2081 500 mA	TPS2053B 500 mA	TPS2054B 500 mA	TPS2086 500 mA
TPS203x 0.2 A - 2 A	TPS2041B 500 mA	TPS2046B 250 mA	TPS2082 500 mA	TPS2047B 250 mA	TPS2048A 250 mA	TPS2087 500 mA
	TPS2051B 500 mA	TPS2056 250 mA	TPS2090 250 mA	TPS2057A 250 mA	TPS2058 250 mA	TPS2095 250 mA
	TPS2045A 250 mA	TPS2062 1 A	TPS2091 250 mA	TPS2063 1 A		TPS2096 250 mA
	TPS2049 100 mA	TPS2066 1 A	TPS2092 250 mA	TPS2067 1 A		TPS2097 250 mA
	TPS2055A 250 mA	TPS2060 1.5 A				
	TPS2061 1 A	TPS2064 1.5 A				
	TPS2065 1 A					
	TPS2068 1.5 A					
	TPS2069 1.5 A					

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either VCC or ground. Specific guidelines for handling devices of this type are contained in the publication Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies available from Texas Instruments.

AVAILABLE OPTIONS AND ORDERING INFORMATION

DEVICE(1)	AMBIENT TEMPERATURE(2)	ENABLE	SON (3) (DRV)	SOT23(3) (DBV)	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT(2)	CURRENT-LIMIT PROTECTION
TPS2552	–40°C to 85°C	Active low	TPS2552DRV	TPS2552DBV	1.5 A	Constant-Current
TPS2553		Active high	TPS2553DRV	TPS2553DBV		
TPS2552-1		Active low	TPS2552DRV-1	TPS2552DBV-1		Latch-Off
TPS2553-1		Active high	TPS2553DRV-1	TPS2553DBV-1		

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Maximum ambient temperature is a function of device junction temperature and system level considerations, such as load current, power dissipation and board layout. See *dissipation rating table* and *recommended operating conditions* for specific information related to these devices.
(3) Add an R suffix to the device type for tape and reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1) (2)

			VALUE	UNIT
	Voltage range on IN, OUT, EN or $\overline{EN}$, ILIM, $\overline{FAULT}$		–0.3 to 7	V
	Voltage range from IN to OUT		–7 to 7	V
I_O	Continuous output current		Internally Limited	
	Continuous total power dissipation		See the Dissipation Rating Table	
	Continuous $\overline{FAULT}$ sink current		25	mA
	ILIM source current		1	mA
	ESD	HBM	2	kV
		CDM	500	V
T_J	Maximum junction temperature		–40 to 150	°C
T_{stg}	Storage temperature		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are referenced to GND unless otherwise noted.

DISSIPATION RATING TABLE

BOARD	PACKAGE	THERMAL RESISTANCE θ_{JA}	THERMAL RESISTANCE θ_{JC}	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
Low-K(1)	DBV	350°C/W	55°C/W	285 mW	2.85 mW/°C	155 mW	114 mW
High-K(2)	DBV	160°C/W	55°C/W	625 mW	6.25 mW/°C	340 mW	250 mW
Low-K(1)	DRV	140°C/W	20°C/W	715 mW	7.1 mW/°C	395 mW	285 mW
High-K(2)	DRV	75°C/W	20°C/W	1330 mW	13.3 mW/°C	730 mW	530 mW

(1) The JEDEC low-K (1s) board used to derive this data was a 3in × 3in, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in × 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{IN}	Input voltage, IN		2.5	6.5	V
V_{EN}	Enable voltage	TPS2552/52-1	0	6.5	V
$V_{\overline{EN}}$		TPS2553/53-1	0	6.5	
V_{IH}	High-level input voltage on EN or $\overline{EN}$		1.1		V
V_{IL}	Low-level input voltage on EN or $\overline{EN}$			0.66	
I_{OUT}	Continuous output current, OUT	–40 °C ≤ T_J ≤ 125 °C	0	1.2	A
		–40 °C ≤ T_J ≤ 105 °C	0	1.5	
R_{ILIM}	Current-limit threshold resistor range (nominal 1%) from ILIM to GND		15	232	kΩ
I_O	Continuous $\overline{FAULT}$ sink current		0	10	mA
	Input de-coupling capacitance, IN to GND		0.1		µF
T_J	Operating virtual junction temperature(1)	I_{OUT} ≤ 1.2 A	–40	125	°C
		I_{OUT} ≤ 1.5 A	-40	105	

(1) See "Dissipation Rating Table" and "Power Dissipation and Junction Temperature" sections for details on how to calculate maximum junction temperature for specific applications and packages.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions, $V_{/EN}$ = 0 V, or V_{EN} = V_{IN}, R_{FAULT} = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
POWER SWITCH								
$r_{DS(on)}$	Static drain-source on-state resistance	DBV package, T_J = 25 °C				85	95	mΩ
		DBV package, –40 °C ≤T_J ≤125 °C					135	
		DRV package, T_J = 25 °C				100	115	
		DRV package, –40 °C ≤T_J ≤105 °C					140	
		DRV package, –40 °C ≤T_J ≤125 °C					150	
t_r	Rise time, output	V_{IN} = 6.5 V	C_L = 1 µF, R_L = 100 Ω, (see Figure 2)			1.1	1.5	ms
		V_{IN} = 2.5 V				0.7	1	
t_f	Fall time, output	V_{IN} = 6.5 V			0.2		0.5	
		V_{IN} = 2.5 V			0.2		0.5	
ENABLE INPUT EN OR $\overline{EN}$								
	Enable pin turn on/off threshold				0.66		1.1	V
I_{EN}	Input current	V_{EN} = 0 V or 6.5 V, $V_{/EN}$ = 0 V or 6.5 V			–0.5		0.5	µA
t_{on}	Turnon time	C_L = 1 µF, R_L = 100 Ω, (see Figure 2)					3	ms
t_{off}	Turnoff time						3	ms
CURRENT LIMIT								
I_{OS}	Current-limit threshold (Maximum DC output current I_{OUT} delivered to load) and Short-circuit current, OUT connected to GND		R_{ILIM} = 15 kΩ	–40 °C ≤T_J ≤105 °C	1610	1700	1800	mA
			R_{ILIM} = 20 kΩ	T_J = 25 °C	1215	1295	1375	
				–40 °C ≤T_J ≤125 °C	1200	1295	1375	
			R_{ILIM} = 49.9 kΩ	T_J = 25 °C	490	520	550	
				–40 °C ≤T_J ≤125 °C	475	520	565	
			R_{ILIM} = 210 kΩ		110	130	150	
			ILIM shorted to IN		50	75	100	
t_{IOS}	Response time to short circuit	V_{IN} = 5 V (see Figure 3)				2		µs
REVERSE-VOLTAGE PROTECTION								
	Reverse-voltage comparator trip point (V_{OUT} – V_{IN})				95	135	190	mV
	Time from reverse-voltage condition to MOSFET turn off	V_{IN} = 5 V			3	5	7	ms

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions, $V_{/EN}$ = 0 V, or V_{EN} = V_{IN}, R_{FAULT} = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{IN_off}	Supply current, low-level output	V_{IN} = 6.5 V, No load on OUT, $V_{\overline{EN}}$ = 6.5 V or V_{EN} = 0 V			0.1	1	µA
I_{IN_on}	Supply current, high-level output	V_{IN} = 6.5 V, No load on OUT	R_{ILIM} = 20 kΩ		120	140	µA
			R_{ILIM} = 210 kΩ		100	120	µA
I_{REV}	Reverse leakage current	V_{OUT} = 6.5 V, V_{IN} = 0 V	T_J = 25 °C		0.01	1	µA
UNDERVOLTAGE LOCKOUT							
UVLO	Low-level input voltage, IN	V_{IN} rising			2.35	2.45	V
	Hysteresis, IN	T_J = 25 °C			25		mV
$\overline{FAULT}$ FLAG							
V_{OL}	Output low voltage, $\overline{FAULT}$	$I_{/FAULT}$ = 1 mA				180	mV
	Off-state leakage	$V_{/FAULT}$ = 6.5 V				1	µA
	$\overline{FAULT}$ deglitch	$\overline{FAULT}$ assertion or de-assertion due to overcurrent condition		5	7.5	10	ms
		$\overline{FAULT}$ assertion or de-assertion due to reverse-voltage condition		2	4	6	ms
THERMAL SHUTDOWN							
	Thermal shutdown threshold			155			°C
	Thermal shutdown threshold in current-limit			135			°C
	Hysteresis				10		°C

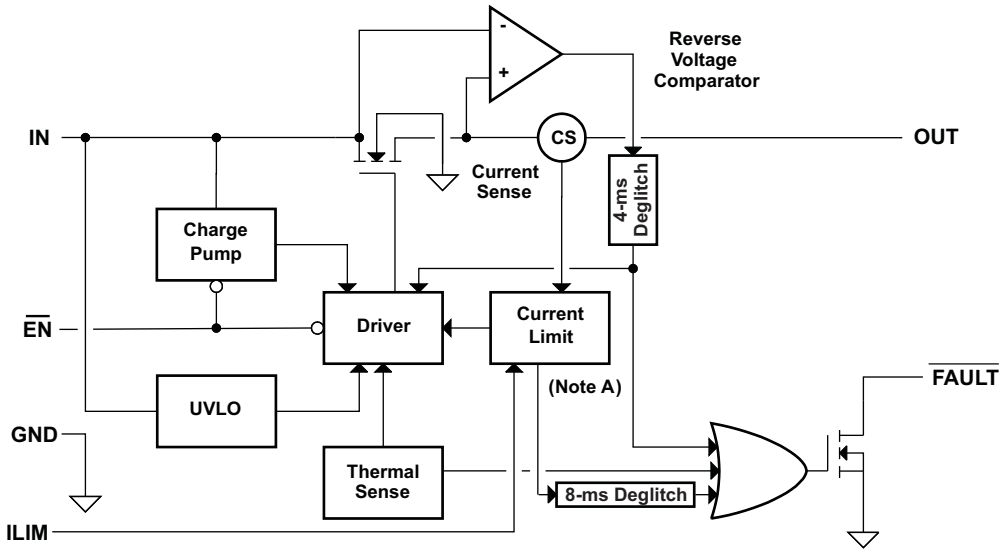
DEVICE INFORMATION

Pin Functions

PIN					I/O	DESCRIPTION
NAME	TPS2552DBV	TPS2553DBV	TPS2552DRV	TPS2553DRV		
$\overline{EN}$	3	–	4	–	I	Enable input, logic low turns on power switch
EN	–	3	–	4	I	Enable input, logic high turns on power switch
GND	2	2	5	5		Ground connection; connect externally to PowerPAD
IN	1	1	6	6	I	Input voltage; connect a 0.1 µF or greater ceramic capacitor from IN to GND as close to the IC as possible.
$\overline{FAULT}$	4	4	3	3	O	Active-low open-drain output, asserted during overcurrent, overtemperature, or reverse-voltage conditions.
OUT	6	6	1	1	O	Power-switch output
ILIM	5	5	2	2	O	External resistor used to set current-limit threshold; recommended 15 kΩ ≤ R_{ILIM} ≤ 232 kΩ.
PowerPAD™	–	–	PAD	PAD		Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND pin externally.

Add -1 for Latch-Off version

FUNCTIONAL BLOCK DIAGRAM



Note A: TPS255x parts enter constant current mode during current limit condition; TPS255x-1 parts latch off

PARAMETER MEASUREMENT INFORMATION

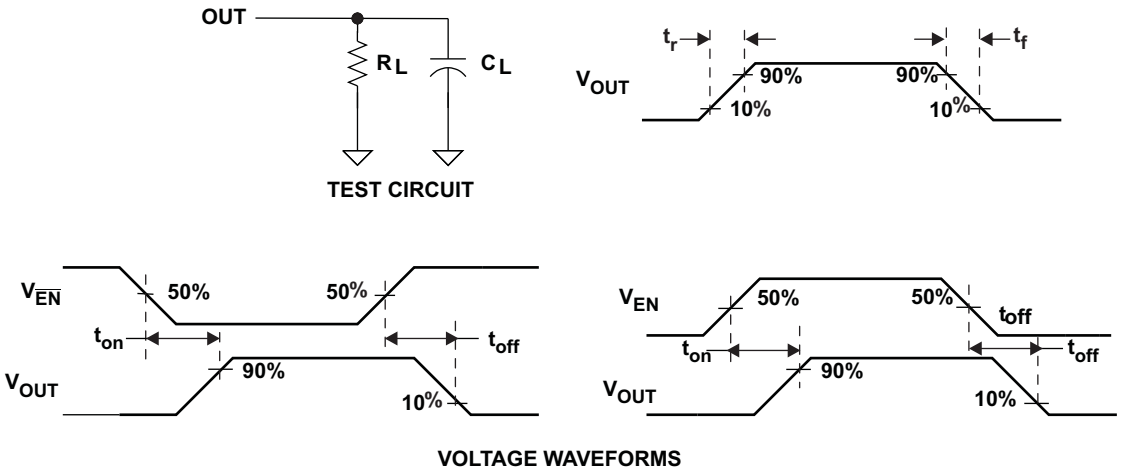


Figure 2. Test Circuit and Voltage Waveforms

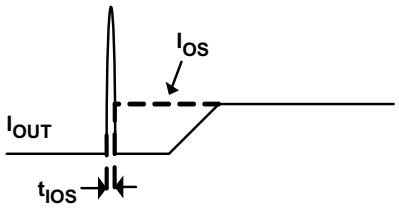


Figure 3. Response Time to Short Circuit Waveform

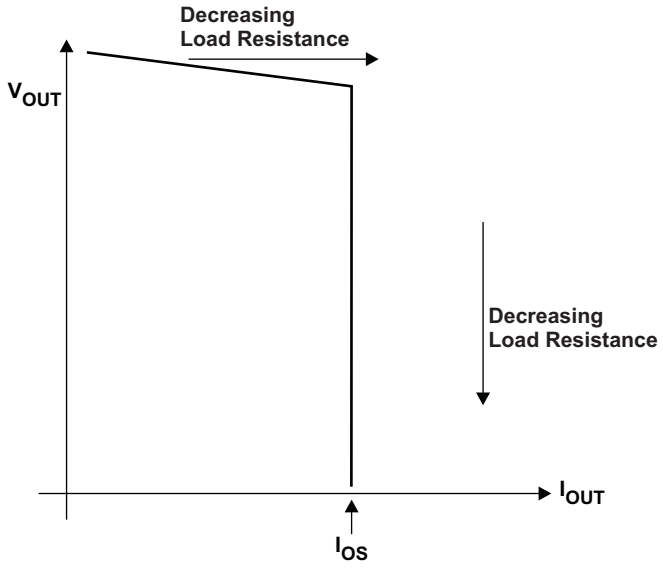


Figure 4. Output Voltage vs. Current-Limit Threshold

TYPICAL CHARACTERISTICS

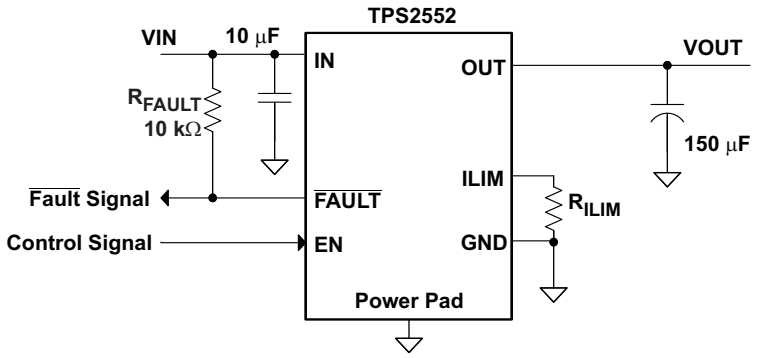


Figure 5. Typical Characteristics Reference Schematic

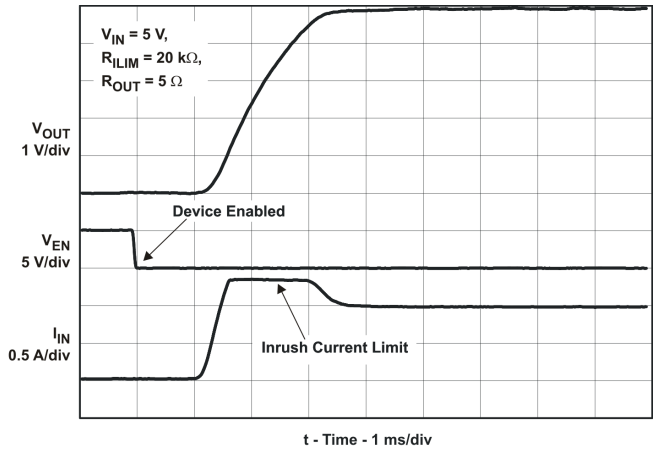


Figure 6. Turnon Delay and Rise Time

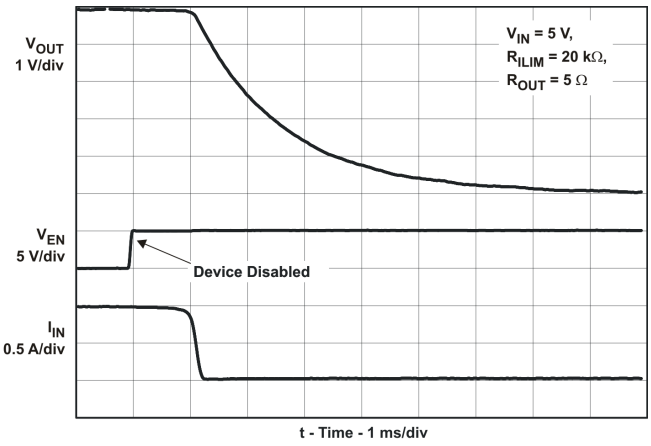


Figure 7. Turnoff Delay and Fall Time

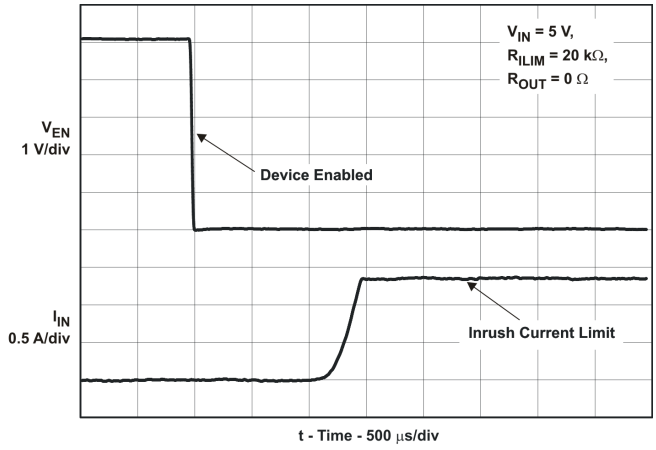


Figure 8. Device Enabled into Short-Circuit

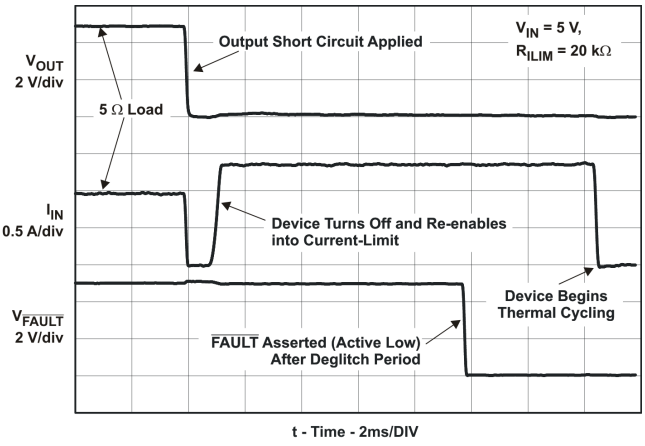


Figure 9. Full-Load to Short-Circuit Transient Response

TYPICAL CHARACTERISTICS (continued)

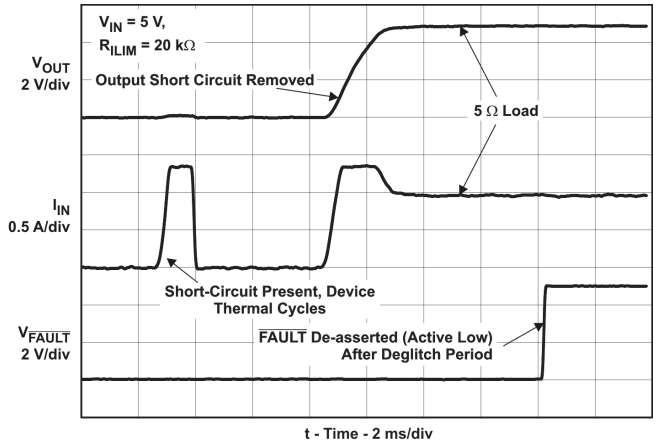


Figure 10. Short-Circuit to Full-Load Recovery Response

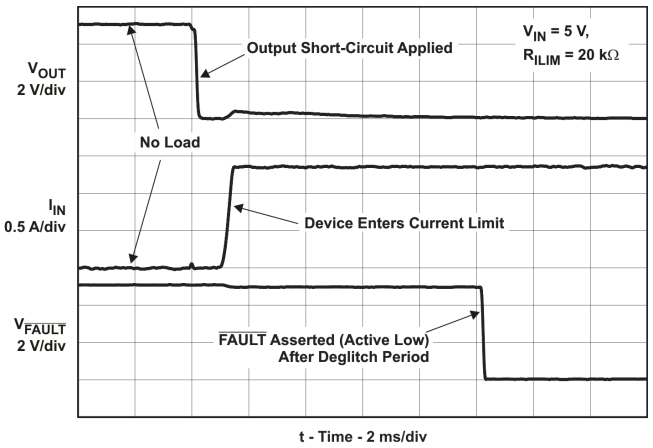


Figure 11. No-Load to Short-Circuit Transient Response

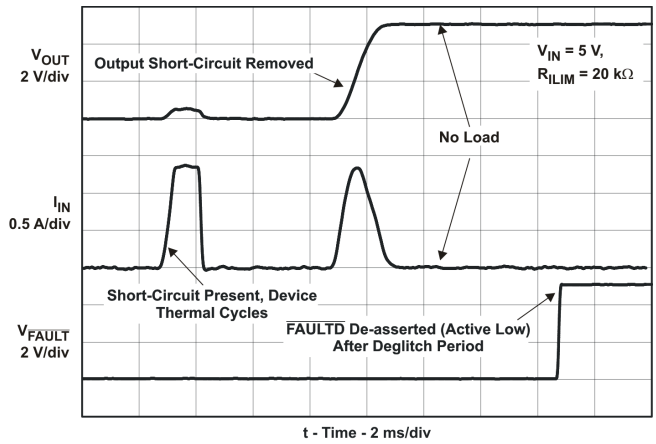


Figure 12. Short-Circuit to No-Load Recovery Response

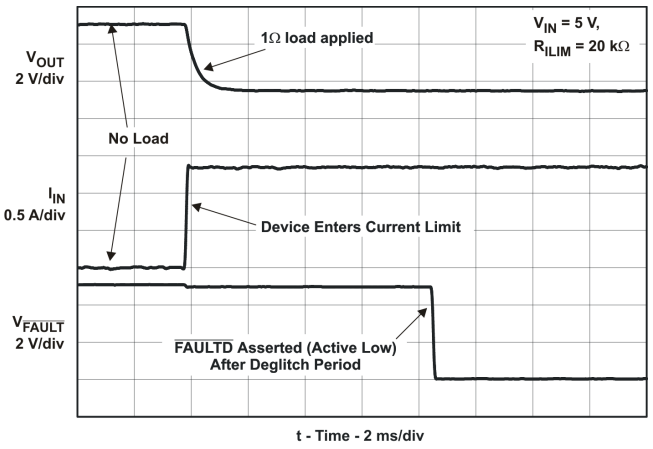


Figure 13. No Load to 1Ω Transient Response

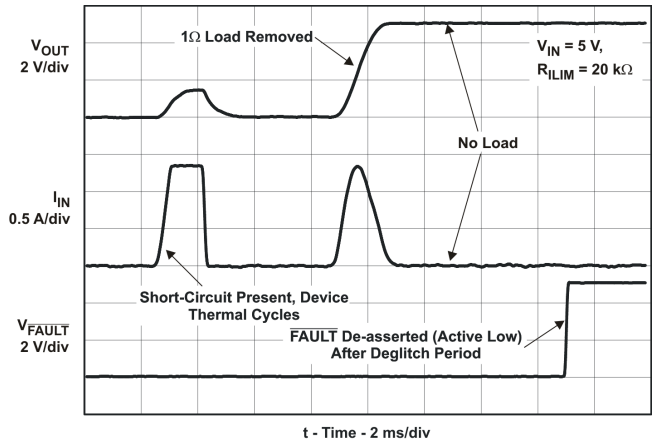


Figure 14. 1Ω to No Load Transient Response

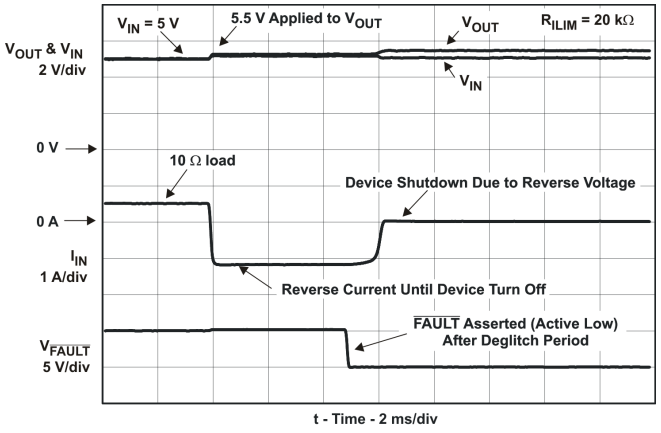


Figure 15. Reverse-Voltage Protection Response

TYPICAL CHARACTERISTICS (continued)

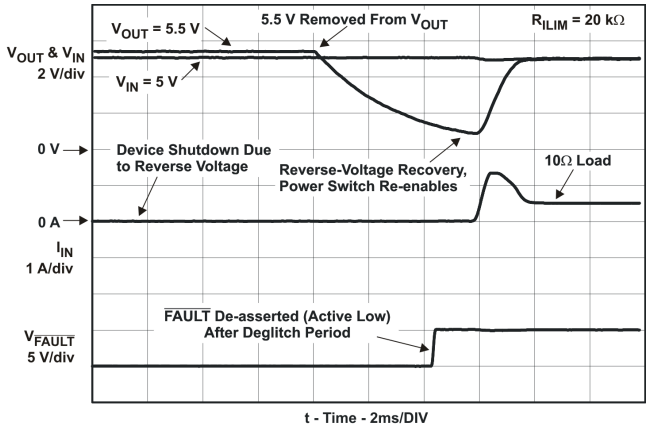


Figure 16. Reverse-Voltage Protection Recovery

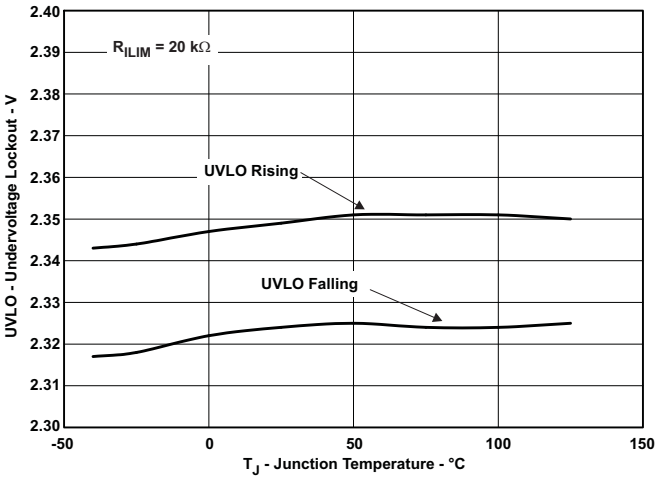


Figure 17. UVLO – Undervoltage Lockout – V

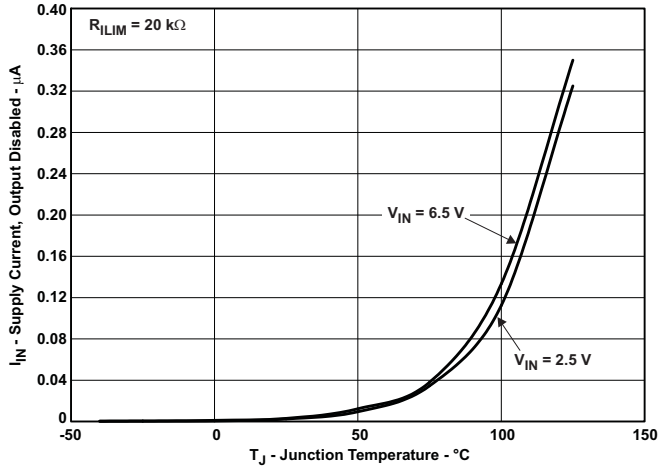


Figure 18. I_{IN} – Supply Current, Output Disabled – µA

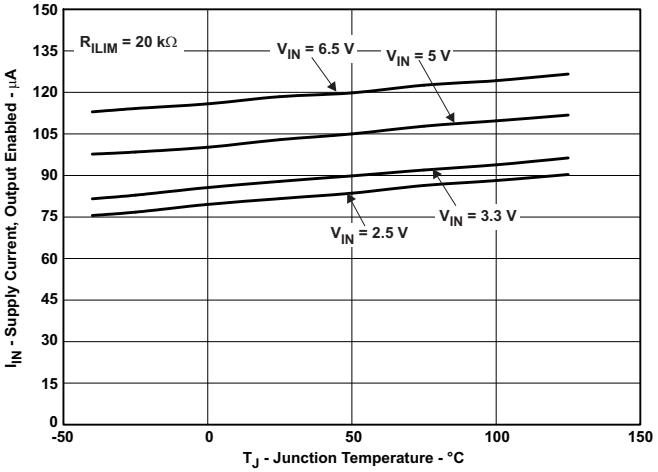


Figure 19. I_{IN} – Supply Current, Output Enabled – µA

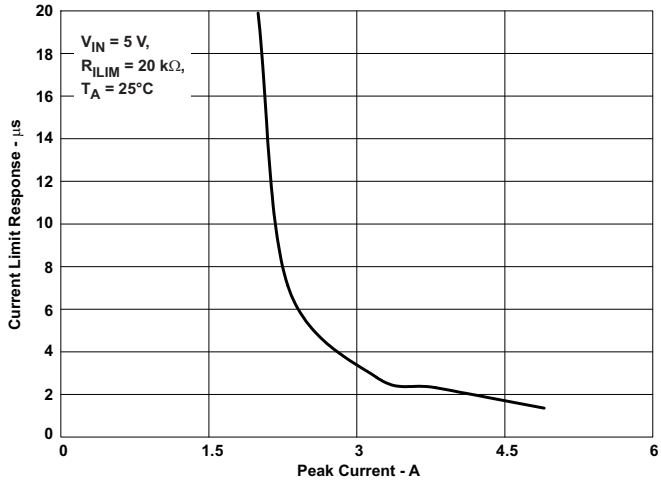


Figure 20. Current Limit Response – µs

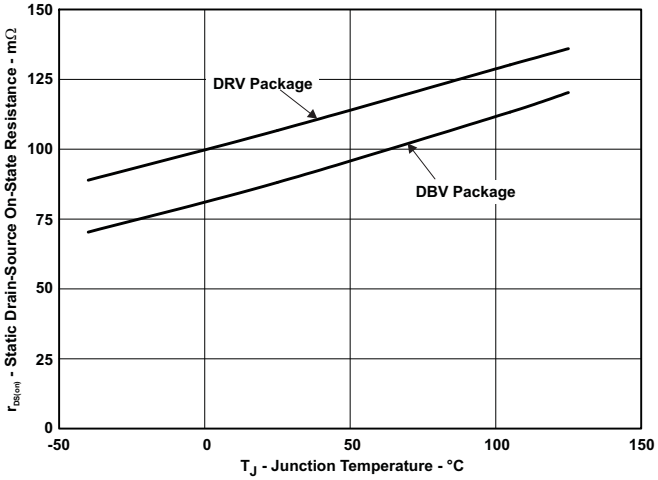


Figure 21. MOSFET $r_{DS(on)}$ Vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

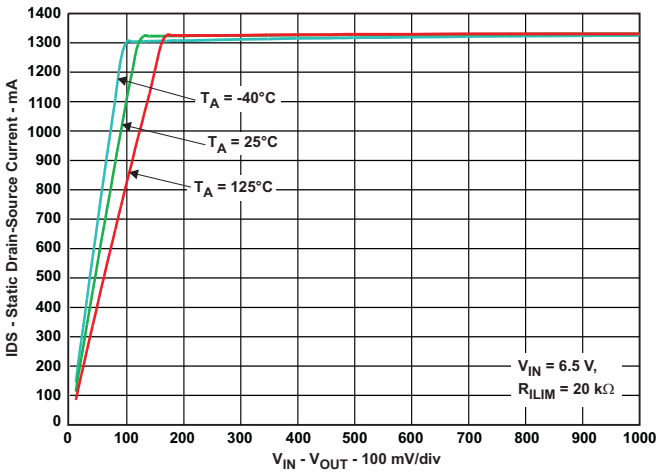


Figure 22. Switch Current Vs. Drain-Source Voltage Across Switch

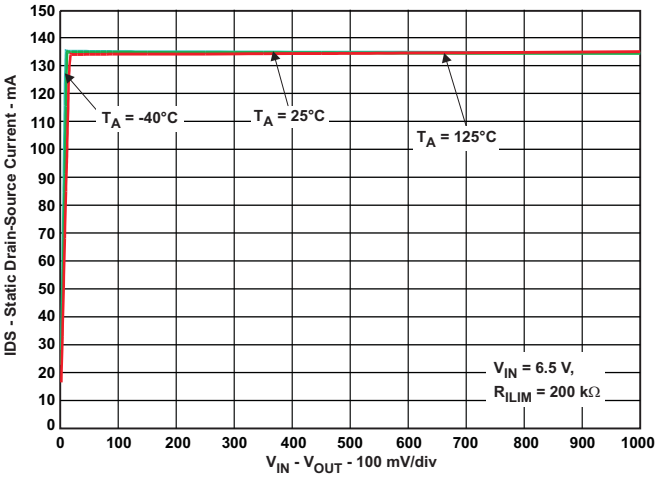


Figure 23. Switch Current Vs. Drain-Source Voltage Across Switch

DETAILED DESCRIPTION

OVERVIEW

The TPS2552/53 and TPS2552-1/53-1 are current-limited, power-distribution switches using N-channel MOSFETs for applications where short circuits or heavy capacitive loads will be encountered and provide up to 1.5 A of continuous load current. These devices allow the user to program the current-limit threshold between 75 mA and 1.7 A (typ) via an external resistor. Additional device shutdown features include overtemperature protection and reverse-voltage protection. The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.5 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. There are two device families that handle overcurrent situations differently. The TPS2552/53 family enters constant-current mode while the TPS2552-1/53-1 family latches off when the load exceeds the current-limit threshold.

OVERCURRENT CONDITIONS

The TPS2552/53 and TPS2552-1/53-1 respond to overcurrent conditions by limiting their output current to the I_{OS} levels shown in Figure 24. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS2552/53 ramps the output current to I_{OS}. The TPS2552/53 devices will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle. The TPS2552-1/53-1 devices will limit the current to I_{OS} until the overload condition is removed or the internal deglitch time (7.5-ms typical) is reached and the device is turned off . The device will remain off until power is cycled or the device enable is toggled.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time t_{IOS} (see Figure 3). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and limits the output current to I_{OS}. Similar to the previous case, the TPS2552/53 will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle; the TPS2552-1/53-1 will limit the current to I_{OS} until the overload condition is removed or the internal deglitch time is reached and the device is latched off.

The TPS2552/53 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (typ) while in current limit. The device remains off until the junction temperature cools 10°C (typ) and then restarts. The TPS2552/53 cycles on/off until the overload is removed (see Figure 10 and Figure 12) .

REVERSE-VOLTAGE PROTECTION

The reverse-voltage protection feature turns off the N-channel MOSFET whenever the output voltage exceeds the input voltage by 135 mV (typ) for 4-ms (typ). This prevents damage to devices on the input side of the TPS2552/53 and TPS2552-1/TPS2253-1 by preventing significant current from sinking into the input capacitance. The TPS2552/53 devices allow the N-channel MOSFET to turn on once the output voltage goes below the input voltage for the same 4-ms deglitch time. The TPS2552-1/53-1 devices keep the device turned off even if the reverse-voltage condition is removed and do not allow the N-channel MOSFET to turn on until power is cycled or the device enable is toggled. The reverse-voltage comparator also asserts the $\overline{\text{FAULT}}$ output (active-low) after 4-ms.

$\overline{\text{FAULT}}$ RESPONSE

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an overcurrent, overtemperature or reverse-voltage condition. The TPS2552/53 asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the device resumes normal operation. The TPS2552-1/53-1 asserts the $\overline{\text{FAULT}}$ signal during a fault condition and remains asserted while the part is latched-off. The $\overline{\text{FAULT}}$ signal is de-asserted once device power is cycled or the enable is toggled and the device resumes normal operation. The TPS2552/53 and TPS2552-1/53-1 are designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal delay "deglitch" circuit for overcurrent (7.5-ms typ) and reverse-voltage (4-ms typ) conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving fault conditions. Overtemperature conditions are not deglitched and assert the $\overline{\text{FAULT}}$ signal immediately.

UNDERVOLTAGE LOCKOUT (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges.

ENABLE ($\overline{\text{EN}}$ OR EN)

The logic enable controls the power switch, bias for the charge pump, driver, and other circuits to reduce the supply current. The supply current is reduced to less than 1-μA when a logic high is present on $\overline{\text{EN}}$ or when a logic low is present on EN. A logic low input on $\overline{\text{EN}}$ or a logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

THERMAL SENSE

The TPS2552/53 and TPS2552-1/53-1 have self-protection features using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. The TPS2552/53 device operates in constant-current mode during an overcurrent conditions, which increases the voltage drop across power-switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135°C (min) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 10 °C.

The TPS2552/53 and TPS2552-1/53-1 also have a second ambient thermal sensor. The ambient thermal sensor turns off the power-switch when the die temperature exceeds 155°C (min) regardless of whether the power switch is in current limit and will turn on the power switch after the device has cooled approximately 10 °C. Both the TPS2552/53 and TPS2552-1/53-1 families continue to cycle off and on until the fault is removed.

The open-drain fault reporting output $\overline{\text{FAULT}}$ is asserted (active low) immediately during an overtemperature shutdown condition.

APPLICATION INFORMATION

INPUT AND OUTPUT CAPACITANCE

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise de-coupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power-supply.

Placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

PROGRAMMING THE CURRENT-LIMIT THRESHOLD

The overcurrent threshold is user programmable via an external resistor. The TPS2552/53 and TPS2552-1/53-1 use an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is 15 kΩ ≤ R_{ILIM} ≤ 232 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM}. The following equations and Figure 24 can be used to calculate the resulting overcurrent threshold for a given external resistor value (R_{ILIM}). Figure 24 includes current-limit tolerance due to variations caused by temperature and process. However, the equations do not account for tolerance due to external resistor variation, so it is important to account for this tolerance when selecting R_{ILIM}. The traces routing the R_{ILIM} resistor to the TPS2552/53 and TPS2552-1/53-1 should be as short as possible to reduce parasitic effects on the current-limit accuracy.

R_{ILIM} can be selected to provide a current-limit threshold that occurs 1) above a minimum load current or 2) below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(min)}$ curve and choose a value of R_{ILIM} below this value. Programming the current limit above a minimum threshold is important to ensure start up into full load or heavy capacitive loads. The resulting maximum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(max)}$ curve.

To design below a maximum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(max)}$ curve and choose a value of R_{ILIM} above this value. Programming the current limit below a maximum threshold is important to avoid current limiting upstream power supplies causing the input voltage bus to droop. The resulting minimum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(min)}$ curve.

Current-Limit Threshold Equations (I_{OS}):

$$I_{OSmax}(mA) = \frac{22980V}{R_{ILIM}^{0.94}k\Omega}$$

$$I_{OSnom}(mA) = \frac{23950V}{R_{ILIM}^{0.977}k\Omega}$$

$$I_{OSmin}(mA) = \frac{25230V}{R_{ILIM}^{1.016}k\Omega} \quad (1)$$

where 15 kΩ ≤ R_{ILIM} ≤ 232 kΩ.

While the maximum recommended value of RILIM is 232 kΩ, there is one additional configuration that allows for a lower current-limit threshold. The ILIM pin may be connected directly to IN to provide a 75 mA (typ) current-limit threshold. Additional low-ESR ceramic capacitance may be necessary from IN to GND in this configuration to prevent unwanted noise from coupling into the sensitive ILIM circuitry.

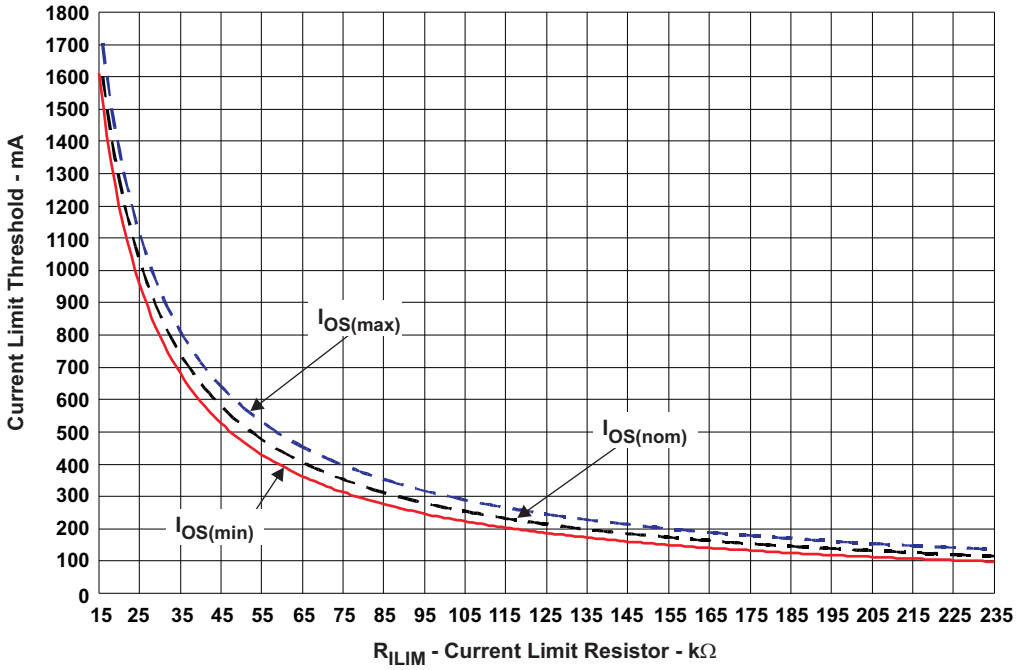


Figure 24. Current-Limit Threshold vs R_{ILIM}

APPLICATION 1: DESIGNING ABOVE A MINIMUM CURRENT LIMIT

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 1 A must be delivered to the load so that the minimum desired current-limit threshold is 1000 mA. Use the I_{OS} equations and Figure 24 to select R_{ILIM}.

$$I_{OSmin}(mA) = 1000mA$$
$$I_{OSmin}(mA) = \frac{25230V}{R_{ILIM}{}^{1.016}k\Omega}$$
$$R_{ILIM}(k\Omega) = \left(\frac{25230V}{I_{OSmin}mA}\right)^{\frac{1}{1.016}}$$
$$R_{ILIM}(k\Omega) = 24k\Omega \quad (2)$$

Select the closest 1% resistor less than the calculated value: R_{ILIM} = 23.7 kΩ. This sets the minimum current-limit threshold at 1 A . Use the I_{OS} equations, Figure 24, and the previously calculated value for R_{ILIM} to calculate the maximum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 23.7k\Omega$$
$$I_{OSmax}(mA) = \frac{22980V}{R_{ILIM}{}^{0.94}k\Omega}$$
$$I_{OSmax}(mA) = \frac{22980V}{23.7^{0.94}k\Omega}$$
$$I_{OSmax}(mA) = 1172.4mA \quad (3)$$

The resulting maximum current-limit threshold is 1172.4 mA with a 23.7 kΩ resistor.

APPLICATION 2: DESIGNING BELOW A MAXIMUM CURRENT LIMIT

Some applications require that current limiting must occur below a certain threshold. For this example, assume that the desired upper current-limit threshold must be below 500 mA to protect an up-stream power supply. Use the I_{OS} equations and Figure 24 to select R_{ILIM}.

$$I_{OSmax}(mA) = 500mA$$
$$I_{OSmax}(mA) = \frac{22980V}{R_{ILIM}{}^{0.94}k\Omega}$$
$$R_{ILIM}(k\Omega) = \left(\frac{22980V}{I_{OSmax}mA}\right)^{\frac{1}{0.94}}$$
$$R_{ILIM}(k\Omega) = 58.7k\Omega \quad (4)$$

Select the closest 1% resistor greater than the calculated value: R_{ILIM} = 59 kΩ. This sets the maximum current-limit threshold at 500 mA . Use the I_{OS} equations, Figure 24, and the previously calculated value for R_{ILIM} to calculate the minimum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 59k\Omega$$
$$I_{OSmin}(mA) = \frac{25230V}{R_{ILIM}{}^{1.016}k\Omega}$$
$$I_{OSmin}(mA) = \frac{25230V}{59^{1.016}k\Omega}$$
$$I_{OSmin}(mA) = 400.6mA \quad (5)$$

The resulting minimum current-limit threshold is 400.6 mA with a 59 kΩ resistor.

ACCOUNTING FOR RESISTOR TOLERANCE

The previous sections described the selection of R_{ILIM} given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focussed only on the TPS2552/53 and TPS2552-1/53-1 performance and assumed an exact resistor value. However, resistors sold in quantity are not exact and are bounded by an upper and lower tolerance centered around a nominal resistance. The additional R_{ILIM} resistance tolerance directly affects the current-limit threshold accuracy at a system level. The following table shows a process that accounts for worst-case resistor tolerance assuming 1% resistor values. Step one follows the selection process outlined in the application examples above. Step two determines the upper and lower resistance bounds of the selected resistor. Step three uses the upper and lower resistor bounds in the I_{OS} equations to calculate the threshold limits. It is important to use tighter tolerance resistors, e.g. 0.5% or 0.1%, when precision current limiting is desired.

Table 1. Common R_{ILIM} Resistor Selections

Desired Nominal Current Limit (mA)		Ideal Resistor (kΩ)	Closest 1% Resistor (kΩ)	Resistor Tolerance			Actual Limits		
				1% low (kΩ)	1% high (kΩ)		IOS MIN (mA)	IOS Nom (mA)	IOS MAX (mA)
75		SHORT ILIM to IN					50.0	75.0	100.0
120		226.1	226	223.7	228.3		101.3	120.0	142.1
200		134.0	133	131.7	134.3		173.7	201.5	233.9
300		88.5	88.7	87.8	89.6		262.1	299.4	342.3
400		65.9	66.5	65.8	67.2		351.2	396.7	448.7
500		52.5	52.3	51.8	52.8		448.3	501.6	562.4
600		43.5	43.2	42.8	43.6		544.3	604.6	673.1
700		37.2	37.4	37.0	37.8		630.2	696.0	770.8
800		32.4	32.4	32.1	32.7		729.1	800.8	882.1
900		28.7	28.7	28.4	29.0		824.7	901.5	988.7
1000		25.8	26.1	25.8	26.4		908.3	989.1	1081.0
1100		23.4	23.2	23.0	23.4		1023.7	1109.7	1207.5
1200		21.4	21.5	21.3	21.7		1106.0	1195.4	1297.1
1300		19.7	19.6	19.4	19.8		1215.1	1308.5	1414.9
1400		18.3	18.2	18.0	18.4		1310.1	1406.7	1517.0
1500		17.0	16.9	16.7	17.1		1412.5	1512.4	1626.4
1600		16.0	15.8	15.6	16.0		1512.5	1615.2	1732.7
1700		15.0	15.0	14.9	15.2		1594.5	1699.3	1819.4

CONSTANT-CURRENT VS. LATCH-OFF OPERATION AND IMPACT ON OUTPUT VOLTAGE

Both the constant-current devices (TPS2552/53) and latch-off devices (TPS2552-1/53-1) operate identically during normal operation, i.e. the load current is less than the current-limit threshold and the devices are not limiting current. During normal operation the N-channel MOSFET is fully enhanced, and $V_{OUT} = V_{IN} - (I_{OUT} \times r_{DS(on)})$. The voltage drop across the MOSFET is relatively small compared to V_{IN}, and $V_{OUT} \approx V_{IN}$.

Both the constant-current devices (TPS2552/53) and latch-off devices (TPS2552-1/53-1) operate identically during the initial onset of an overcurrent event. Both devices limit current to the programmed current-limit threshold set by R_{ILIM} by operating the N-channel MOSFET in the linear mode. During current-limit operation, the N-channel MOSFET is no longer fully-enhanced and the resistance of the device increases. This allows the device to effectively regulate the current to the current-limit threshold. The effect of increasing the resistance of the MOSFET is that the voltage drop across the device is no longer negligible ($V_{IN} \neq V_{OUT}$), and V_{OUT} decreases. The amount that V_{OUT} decreases is proportional to the magnitude of the overload condition. The expected V_{OUT} can be calculated by $I_{OS} \times R_{LOAD}$, where I_{OS} is the current-limit threshold and R_{LOAD} is the magnitude of the overload condition. For example, if I_{OS} is programmed to 1 A and a 1 Ω overload condition is applied, the resulting V_{OUT} is 1 V.

While both the constant-current devices (TPS2552/53) and latch-off devices (TPS2552-1/53-1) operate identically during the initial onset of an overcurrent event, they behave differently if the overcurrent event lasts longer than the internal delay "deglitch" circuit (7.5-ms typ). The constant-current devices (TPS2552/53) assert the $\overline{\text{FAULT}}$ flag after the deglitch period and continue to regulate the current to the current-limit threshold indefinitely. In practical circuits, the power dissipation in the package will increase the die temperature above the overtemperature shutdown threshold (135°C min), and the device will turn off until the die temperature decreases by the hysteresis of the thermal shutdown circuit (10°C typ). The device will turn on and continue to thermal cycle until the overload condition is removed. The constant-current devices resume normal operation once the overload condition is removed. The latch-off devices (TPS2552-1/53-1) assert the $\overline{\text{FAULT}}$ flag after the deglitch period and immediately turn off the device. The device remains off regardless of whether the overload condition is removed from the output. The latch-off devices remain off and do not resume normal operation until the surrounding system either toggles the enable or cycles power to the device.

POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated by:

$$P_D = r_{DS(on)} \times I_{OUT}^2$$

Where:

P_D = Total power dissipation (W)

$r_{DS(on)}$ = Power switch on-resistance (Ω)

I_{OUT} = Maximum current-limit threshold (A)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A$$

Where:

T_A = Ambient temperature (°C)

θ_{JA} = Thermal resistance (°C/W)

P_D = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance θ_{JA}, and thermal resistance is highly dependent on the individual package and board layout. The Dissipating Rating Table provides example thermal resistances for specific packages and board layouts.

UNIVERSAL SERIAL BUS (USB) POWER-DISTRIBUTION REQUIREMENTS

One application for this device is for current limiting in universal serial bus (USB) applications. The original USB interface was a 12-Mb/s or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). As the demand for more bandwidth increased, the USB 2.0 standard was introduced increasing the maximum data rate to 480-Mb/s. The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply. The USB specification classifies two different classes of devices depending on its maximum current draw. A device classified as low-power can draw up to 100 mA as defined by the standard. A device classified as high-power can draw up to 500 mA. It is important that the minimum current-limit threshold of the current-limiting power-switch exceed the maximum current-limit draw of the intended application. The latest USB standard should always be referenced when considering the current-limit threshold

The USB specification defines two types of devices as hubs and functions. A USB hub is a device that contains multiple ports for different USB devices to connect and can be self-powered (SPH) or bus-powered (BPH). A function is a USB device that is able to transmit or receive data or control information over the bus. A USB function can be embedded in a USB hub. A USB function can be one of three types included in the list below.

- Low-power, bus-powered function
- High-power, bus-powered function
- Self-powered function

SPHs and BPHs distribute data and power to downstream functions. The TPS2552/53 has higher current capability than required for a single USB port allowing it to power multiple downstream ports.

SELF-POWERED AND BUS-POWERED HUBS

A SPH has a local power supply that powers embedded functions and downstream ports. This power supply must provide between 4.75 V to 5.25 V to downstream facing devices under full-load and no-load conditions. SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

A BPH obtains all power from an upstream port and often contains an embedded function. It must power up with less than 100 mA. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This is accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than 100 mA. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

LOW-POWER BUS-POWERED AND HIGH-POWER BUS-POWERED FUNCTIONS

Both low-power and high-power bus-powered functions obtain all power from upstream ports. Low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 μF at power up, the device must implement inrush current limiting.

USB POWER-DISTRIBUTION REQUIREMENTS

USB can be implemented in several ways regardless of the type of USB device being developed. Several power-distribution features must be implemented.

- SPHs must:
  - Current limit downstream ports
  - Report overcurrent conditions
- BPHs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2552/53 and TPS2552-1/53-1 meets each of these requirements. The integrated current limiting and overcurrent reporting is required by self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs and the input ports for bus-powered functions.

AUTO-RETRY FUNCTIONALITY

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This *auto-retry* functionality can be implemented with an external resistor and capacitor. During a fault condition, $\overline{\text{FAULT}}$ pulls low disabling the part. The part is disabled when EN is pulled low, and $\overline{\text{FAULT}}$ goes high impedance allowing C_{RETRY} to begin charging. The part re-enables when the voltage on EN reaches the turnon threshold, and the auto-retry time is determined by the resistor/capacitor time constant. The part will continue to cycle in this manner until the fault condition is removed.

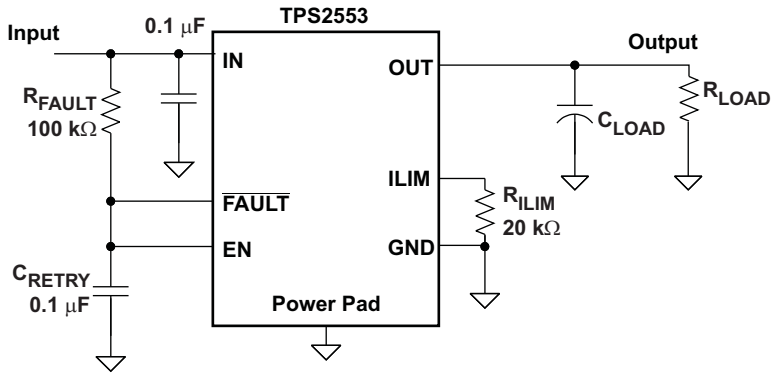


Figure 25. Auto-Retry Functionality

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. Figure 26 shows how an external logic signal can drive EN through R_{FAULT} and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

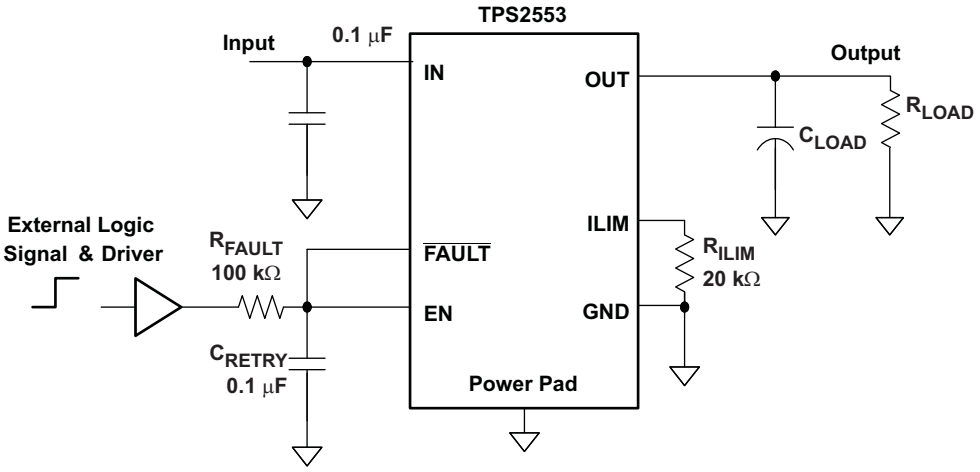


Figure 26. Auto-Retry Functionality With External EN Signal

TWO-LEVEL CURRENT-LIMIT CIRCUIT

Some applications require different current-limit thresholds depending on external system conditions. Figure 27 shows an implementation for an externally controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see the Programming the Current-Limit Threshold section). A logic-level input enables/disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND. Additional MOSFET/resistor combinations can be used in parallel to Q1/R2 to increase the number of additional current-limit levels.

NOTE:

ILIM should never be driven directly with an external signal.

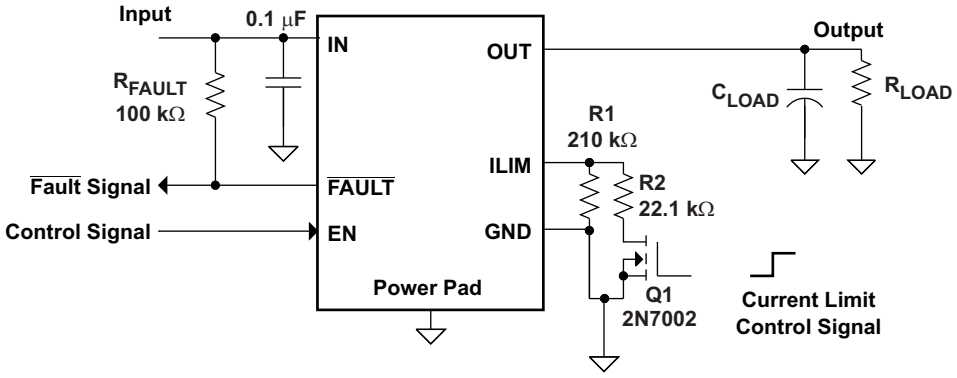


Figure 27. Two-Level Current-Limit Circuit

Revision History

Changes from Original (November 2009) to Revision A **Page**

- Changed Title from: ADJUSTABLE CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES To: PRECISION ADJUSTABLE CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES 1

Changes from Revision A (December 2009) to Revision B **Page**

- Added To Features - UL Listed – File No. E169910 1
- Changed Figure 22 Ttitle From: Current Limit Threshold Vs R_{ILM} 10
- Changed Figure 23 Ttitle From: Current Limit Threshold Vs R_{ILM} 10

Changes from Revision B (February 2009) to Revision C **Page**

- Added Feature - Up to 1.5 A Maximum Load Current 1
- Changed 1.3 A (typ) To: 1.7 A (typ) 1
- Added Text - and provide up to 1.5 A of continuous load current 1
- Changed From 1.2A to 1.5A 2
- Changed I_{OUT} values for 1.2A and 1.5A 3
- Changed T_J values for 1.2A and 1.5A 3
- Added R_{ILIM} = 15 kΩ option 3
- Changed From: 19.1 kΩ ≤ R_{ILIM} ≤ 232 kΩ To: 15 kΩ ≤ R_{ILIM} ≤ 232 kΩ. 5
- Changed Text From: current-limit threshold between 75 mA and 1.3 A (typ) To: current-limit threshold between 75 mA and 1.7 A (typ) 11
- Changed Text From: The recommended 1% resistor range for R_{ILIM} is 19.1 kΩ ≤ R_{ILIM} ≤ 232 kΩ to ensure stability To: The recommended 1% resistor range for R_{ILIM} is 15 kΩ ≤ R_{ILIM} ≤ 232 kΩ to ensure stability 13
- Changed From: where 19.1 kΩ ≤ R_{ILIM} ≤ 232 kΩ. To: where 15 kΩ ≤ R_{ILIM} ≤ 232 kΩ. 13
- Changed Figure 24 - Current-Limit Threshold vs R_{ILIM} 14
- Changed Table 1 - added rows for Current Limit of 1400 to 1700 16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS2552DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2552DBVR-1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2552DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2552DBVT-1	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2552DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2552DRVR-1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2552DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2552DRVT-1	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2553DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2553DBVR-1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2553DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2553DBVT-1	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2553DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2553DRVR-1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2553DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2553DRVT-1	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

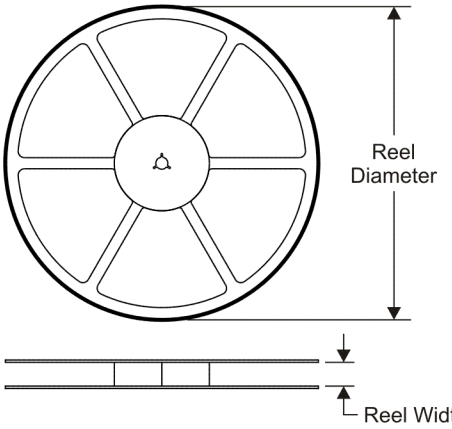
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

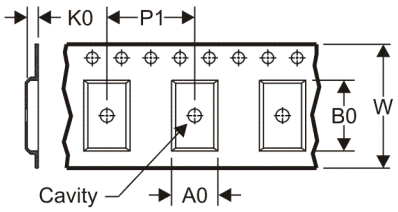
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

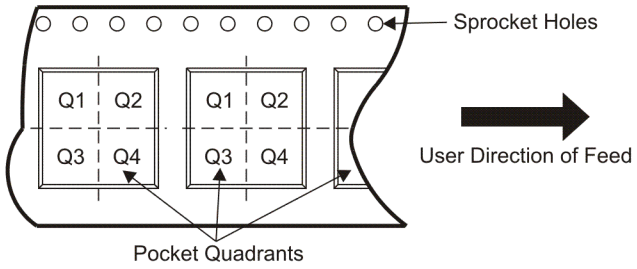


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

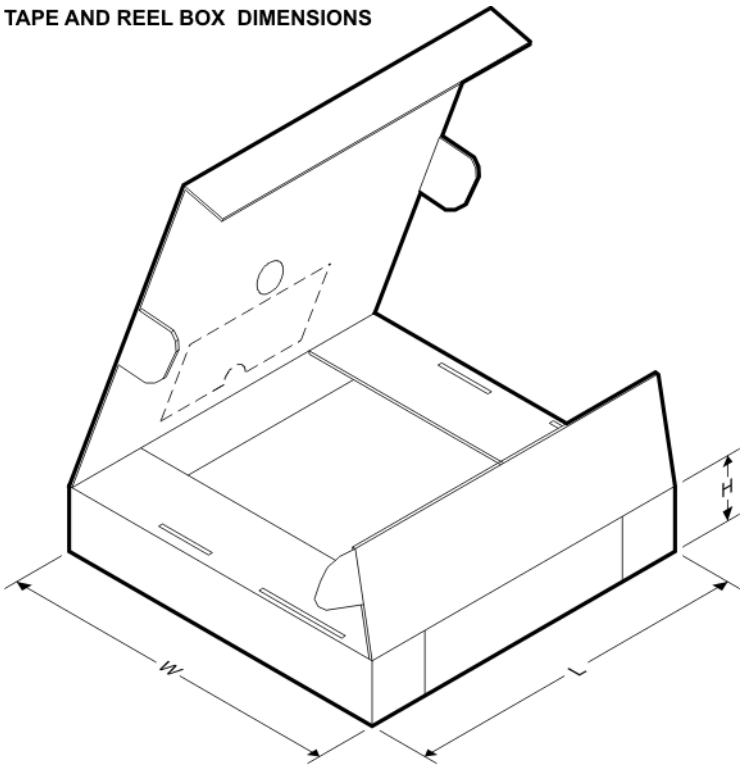
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2552DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2552DBVR-1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2552DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2552DBVT-1	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2552DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS2552DRVR-1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS2552DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS2552DRVT-1	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS2553DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2553DBVR-1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2553DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2553DBVT-1	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2553DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS2553DRVR-1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS2553DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS2553DRVT-1	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

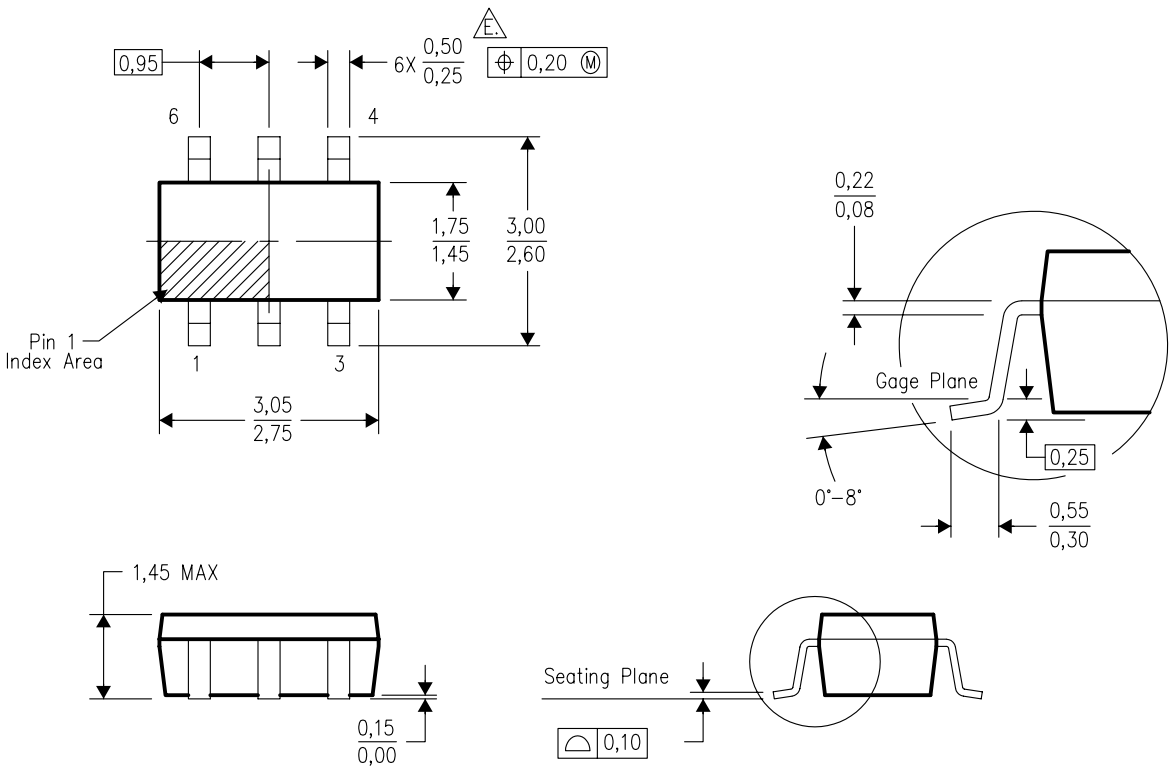
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2552DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS2552DBVR-1	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS2552DBVT	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS2552DBVT-1	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS2552DRVR	SON	DRV	6	3000	195.0	200.0	45.0
TPS2552DRVR-1	SON	DRV	6	3000	195.0	200.0	45.0
TPS2552DRVT	SON	DRV	6	250	195.0	200.0	45.0
TPS2552DRVT-1	SON	DRV	6	250	195.0	200.0	45.0
TPS2553DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS2553DBVR-1	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS2553DBVT	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS2553DBVT-1	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS2553DRVR	SON	DRV	6	3000	195.0	200.0	45.0
TPS2553DRVR-1	SON	DRV	6	3000	195.0	200.0	45.0
TPS2553DRVT	SON	DRV	6	250	195.0	200.0	45.0
TPS2553DRVT-1	SON	DRV	6	250	195.0	200.0	45.0

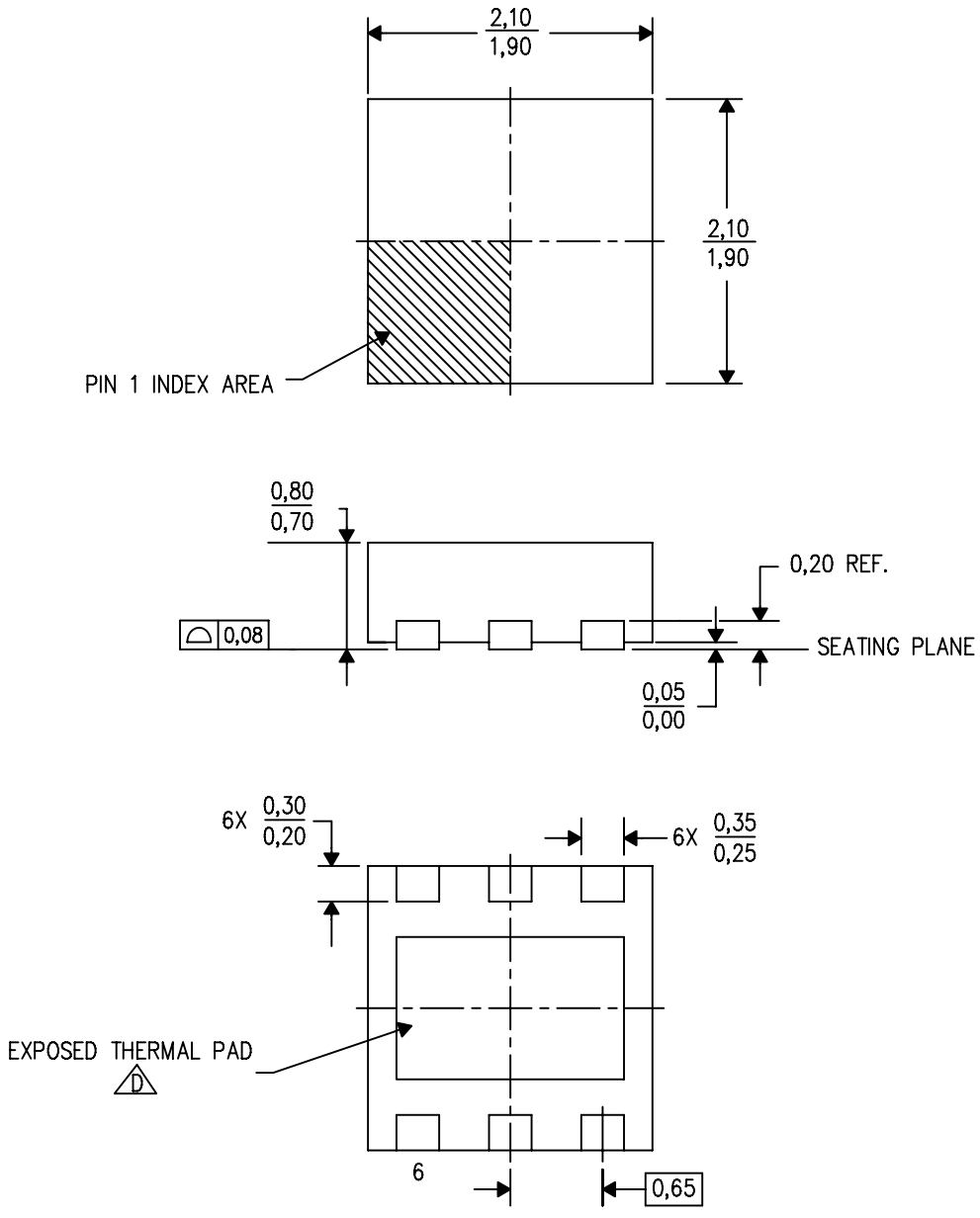
DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4073253–5/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DRV (S–PDSO–N6) PLASTIC SMALL OUTLINE



4206925/D 12/07

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

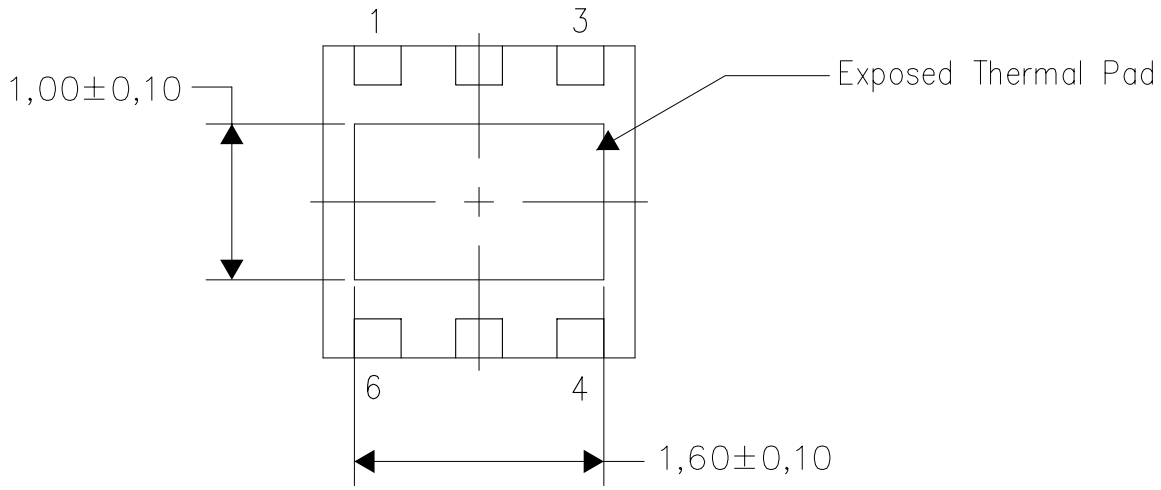
DRV (S–PWSON–N6)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

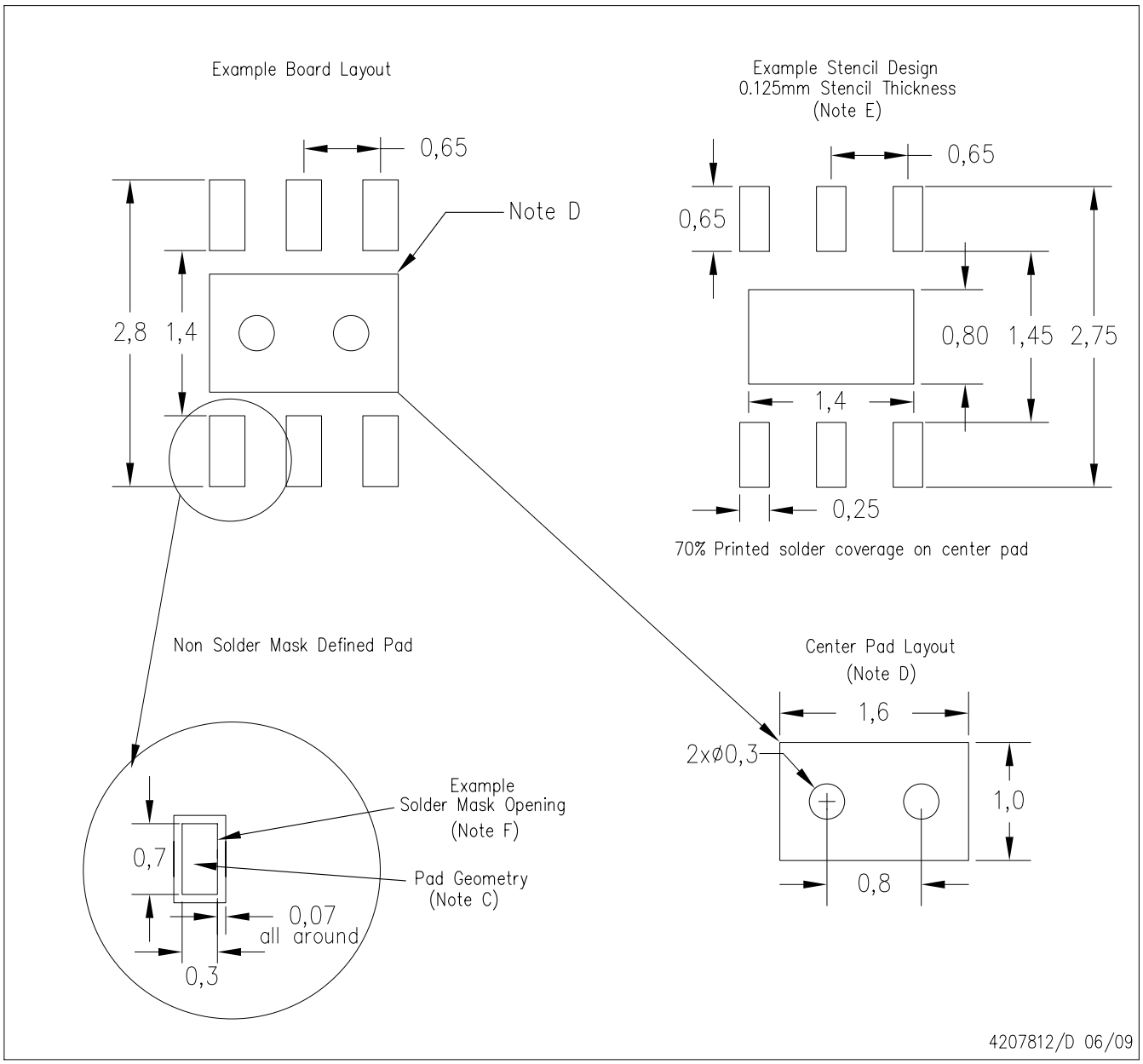


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRV (S–PWSON–N6)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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