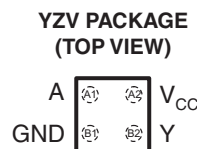
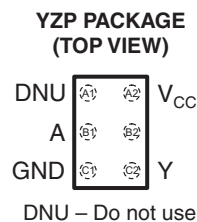
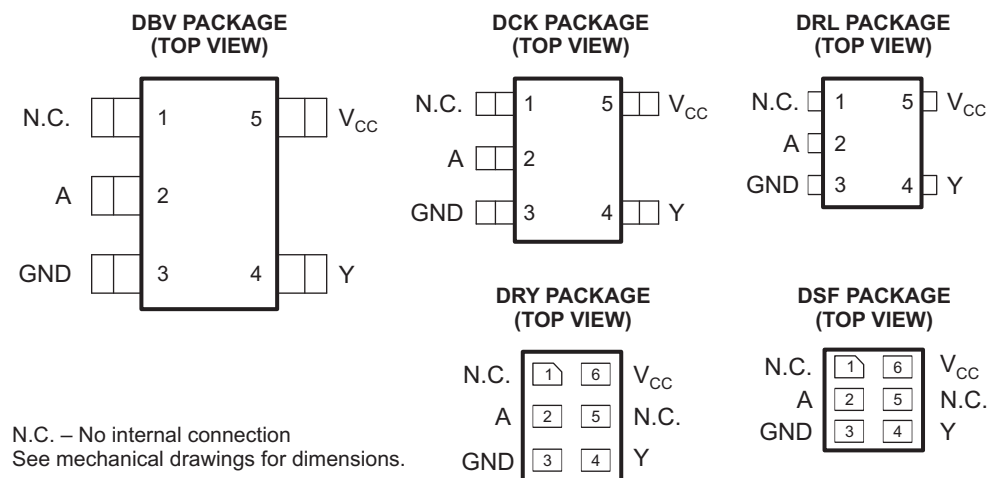


# SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT

Check for Samples: [SN74LVC1G06](#)

## FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V  $V_{CC}$  Operation
- Input and Open-Drain Output Accept Voltages up to 5.5 V
- Max  $t_{pd}$  of 4 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- $I_{off}$  Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



**Table 1. YZP PACKAGE TERMINAL ASSIGNMENTS**

	1	2
<b>A</b>	DNU	$V_{CC}$
<b>B</b>	A	No ball
<b>C</b>	GND	Y

**Table 2. YZV PACKAGE TERMINAL ASSIGNMENTS**

	1	2
<b>A</b>	A	$V_{CC}$
<b>B</b>	GND	Y



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## DESCRIPTION/ORDERING INFORMATION

This single inverter buffer/driver is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

The output of the SN74LVC1G06 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup> (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC1G06YZPR	__ _CT_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZV (Pb-free)	Reel of 3000	SN74LVC1G06YZVR	-- _CT
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G06DBVR	C06_
		Reel of 250	SN74LVC1G06DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1G06DCKR	CT_
		Reel of 250	SN74LVC1G06DCKT	
		Jumbo Tube of 10000	SN74LVC1G06DCKJ	
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1G06DRLR	CT_
	μQFN – DSF	Reel of 5000	SN74LVC1G06DSFR	CT
	QFN – DRY	Reel of 5000	SN74LVC1G06DRYR	CT

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site.  
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).  
YZV: The actual top-side marking is on two lines. Line 1 has four characters to denote year, month, day, and assembly/test site. Line 2 has two characters which show the family and function code. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

**Table 3. FUNCTION TABLE**

INPUT A	OUTPUT Y
H	L
L	Z

## LOGIC DIAGRAM (POSITIVE LOGIC) DBV, DCK, DSF, DRY, DRL, and YZP PACKAGE



## YZV PACKAGE



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	–0.5	6.5	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	–0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>	–0.5	6.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		–50 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		–50 mA
I <sub>O</sub>	Continuous output current	±50		mA
	Continuous current through V <sub>CC</sub> or GND	±100		mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DBV package		206
		DCK package		252
		DRL package		142
		YZP package		132
		YZV package		123
		DSF package		300
		DRY package		234
T <sub>stg</sub>	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5
		Data retention only	1.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
		V <sub>CC</sub> = 3 V to 3.6 V	2	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
		V <sub>CC</sub> = 3 V to 3.6 V	0.8	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.3 × V <sub>CC</sub>	
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	5.5	V
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	4	mA
		V <sub>CC</sub> = 2.3 V	8	
		V <sub>CC</sub> = 3 V	16	
			24	
		V <sub>CC</sub> = 4.5 V	32	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20	ns/V
		V <sub>CC</sub> = 3.3 V ± 0.3 V	10	
		V <sub>CC</sub> = 5 V ± 0.5 V	5	
T <sub>A</sub>	Operating free-air temperature	–40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OL</sub>		I <sub>OL</sub> = 100 µA	1.65 V to 5.5 V			0.1	V
		I <sub>OL</sub> = 4 mA	1.65 V			0.45	
		I <sub>OL</sub> = 8 mA	2.3 V			0.3	
		I <sub>OL</sub> = 16 mA	3 V			0.4	
		I <sub>OL</sub> = 24 mA				0.55	
		I <sub>OL</sub> = 32 mA	4.5 V			0.55	
I <sub>I</sub>	A input	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±1	µA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	µA
I <sub>CC</sub>		V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V			10	µA
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	µA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			4	pF
C <sub>o</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V			5	pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

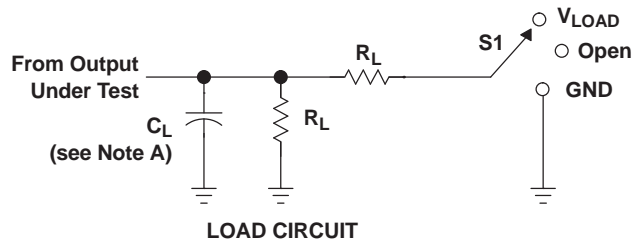
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2.2	6.5	1.1	4	1.2	4	1	3	ns

## Operating Characteristics

T<sub>A</sub> = 25°C

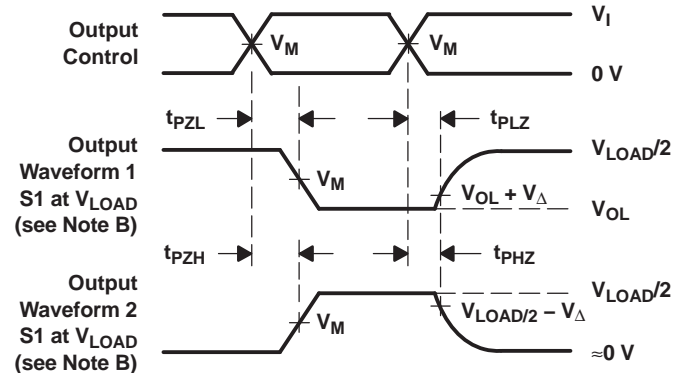
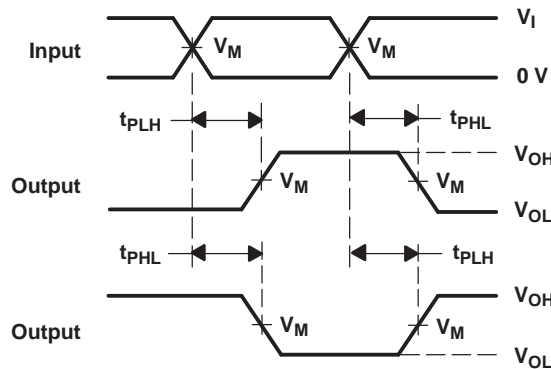
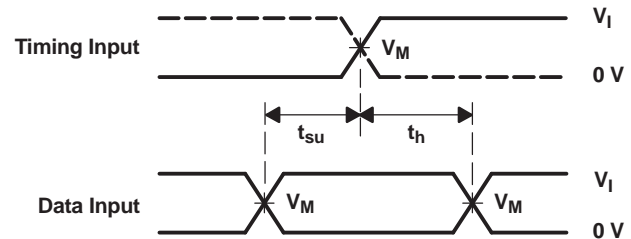
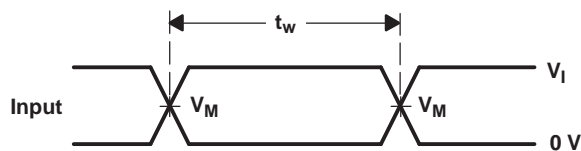
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	3	3	4	6	pF

## PARAMETER MEASUREMENT INFORMATION (OPEN DRAIN)



TEST	S1
$t_{PZL}$ (see Notes E and F)	$V_{LOAD}$
$t_{PLZ}$ (see Notes E and G)	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	$V_{LOAD}$

$V_{CC}$	INPUT		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - Since this device has open-drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{pd}$ .
  - $t_{PZL}$  is measured at  $V_M$ .
  - $t_{PLZ}$  is measured at  $V_{OL} + V_{\Delta}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## REVISION HISTORY

### Changes from Revision U (June 2011) to Revision V

### Page

- Added Jumbo Reel to ORDERING INFORMATION TABLE. .... [2](#)

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LVC1G06DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C065 ~ C06F ~ C06R ~ C06T)	<a href="#">Samples</a>
SN74LVC1G06DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C065 ~ C06F ~ C06R ~ C06T)	<a href="#">Samples</a>
SN74LVC1G06DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C065 ~ C06F ~ C06R ~ C06T)	<a href="#">Samples</a>
SN74LVC1G06DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C065 ~ C06F ~ C06R)	<a href="#">Samples</a>
SN74LVC1G06DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C065 ~ C06F ~ C06R)	<a href="#">Samples</a>
SN74LVC1G06DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C065 ~ C06F ~ C06R)	<a href="#">Samples</a>
SN74LVC1G06DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT5 ~ CTF ~ CTK ~ CTR ~ CTT)	<a href="#">Samples</a>
SN74LVC1G06DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT5 ~ CTF ~ CTK ~ CTR ~ CTT)	<a href="#">Samples</a>
SN74LVC1G06DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT5 ~ CTF ~ CTK ~ CTR ~ CTT)	<a href="#">Samples</a>
SN74LVC1G06DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT5 ~ CTF ~ CTK ~ CTR)	<a href="#">Samples</a>
SN74LVC1G06DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT5 ~ CTF ~ CTK ~ CTR)	<a href="#">Samples</a>
SN74LVC1G06DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT5 ~ CTF ~ CTK ~ CTR)	<a href="#">Samples</a>
SN74LVC1G06DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT7 ~ CTR)	<a href="#">Samples</a>
SN74LVC1G06DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT7 ~ CTR)	<a href="#">Samples</a>
SN74LVC1G06DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT	<a href="#">Samples</a>
SN74LVC1G06DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT	<a href="#">Samples</a>
SN74LVC1G06YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CT7 ~ CTN)	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LVC1G06YZVR	ACTIVE	DSBGA	YZV	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CT (7 ~ N)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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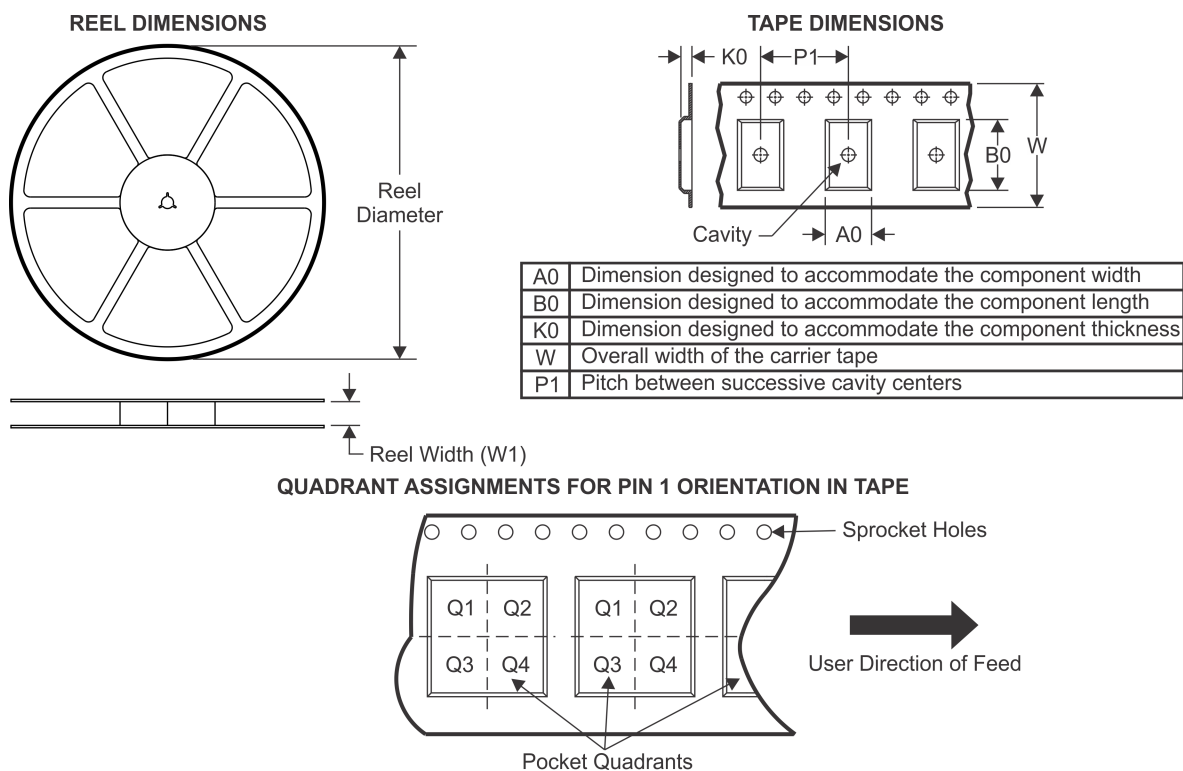
## OTHER QUALIFIED VERSIONS OF SN74LVC1G06 :

- Enhanced Product: [SN74LVC1G06-EP](#)

NOTE: Qualified Version Definitions:



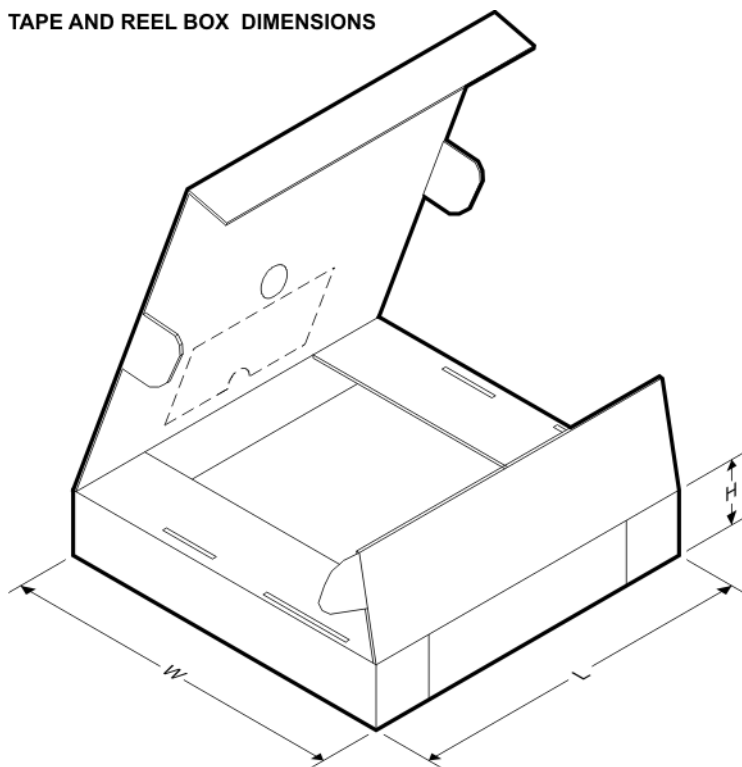
- 
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G06DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G06DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G06DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G06DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G06DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G06DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G06DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G06DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G06DRLR	SOT	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC1G06DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G06DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G06DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G06YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G06YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS

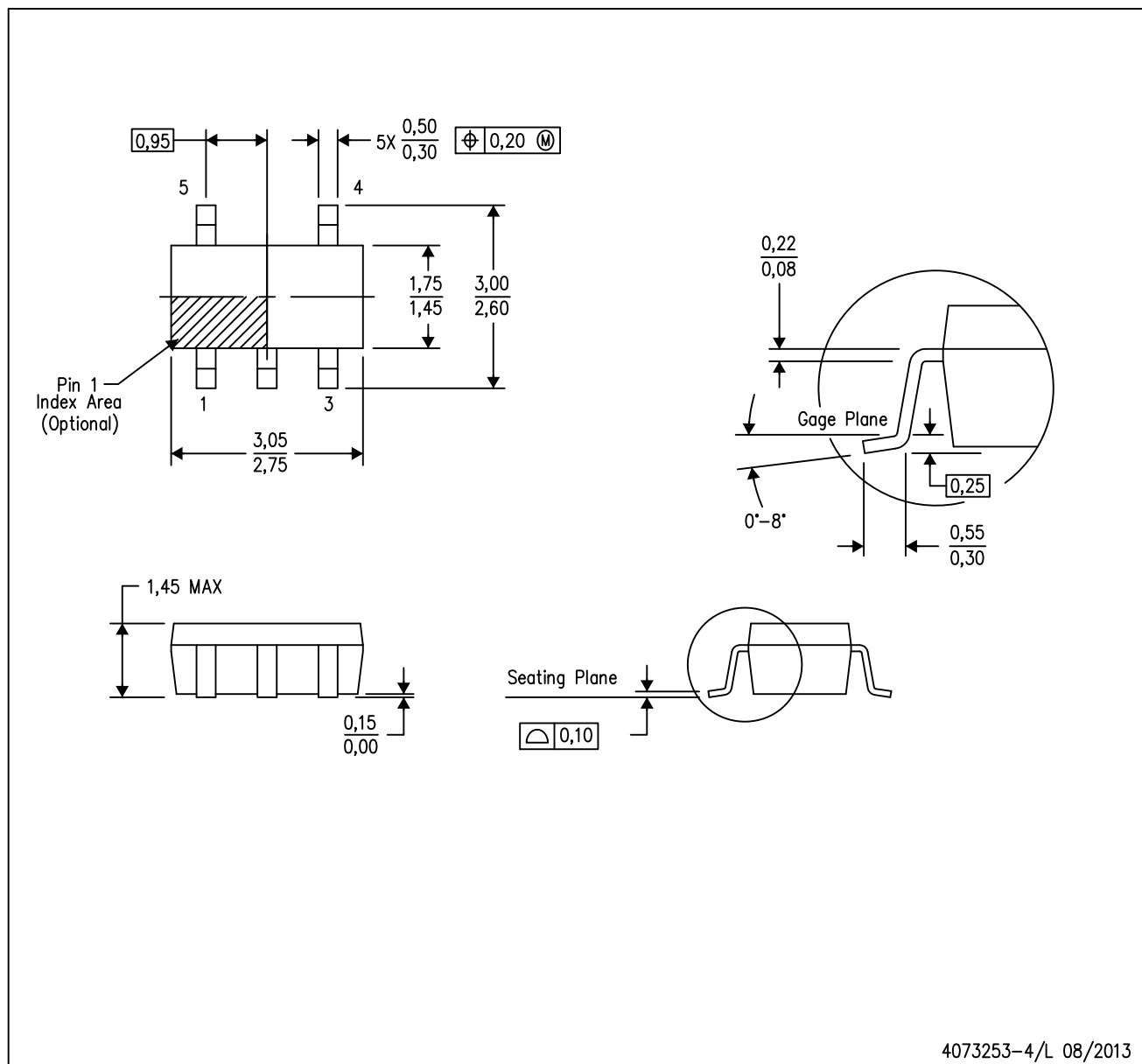


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G06DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G06DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G06DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G06DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74LVC1G06DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G06DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74LVC1G06DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DRLR	SOT	DRL	5	4000	180.0	180.0	30.0
SN74LVC1G06DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G06DRYR	SON	DRY	6	5000	180.0	180.0	30.0
SN74LVC1G06DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74LVC1G06YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G06YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0

DBV (R-PDSO-G5)

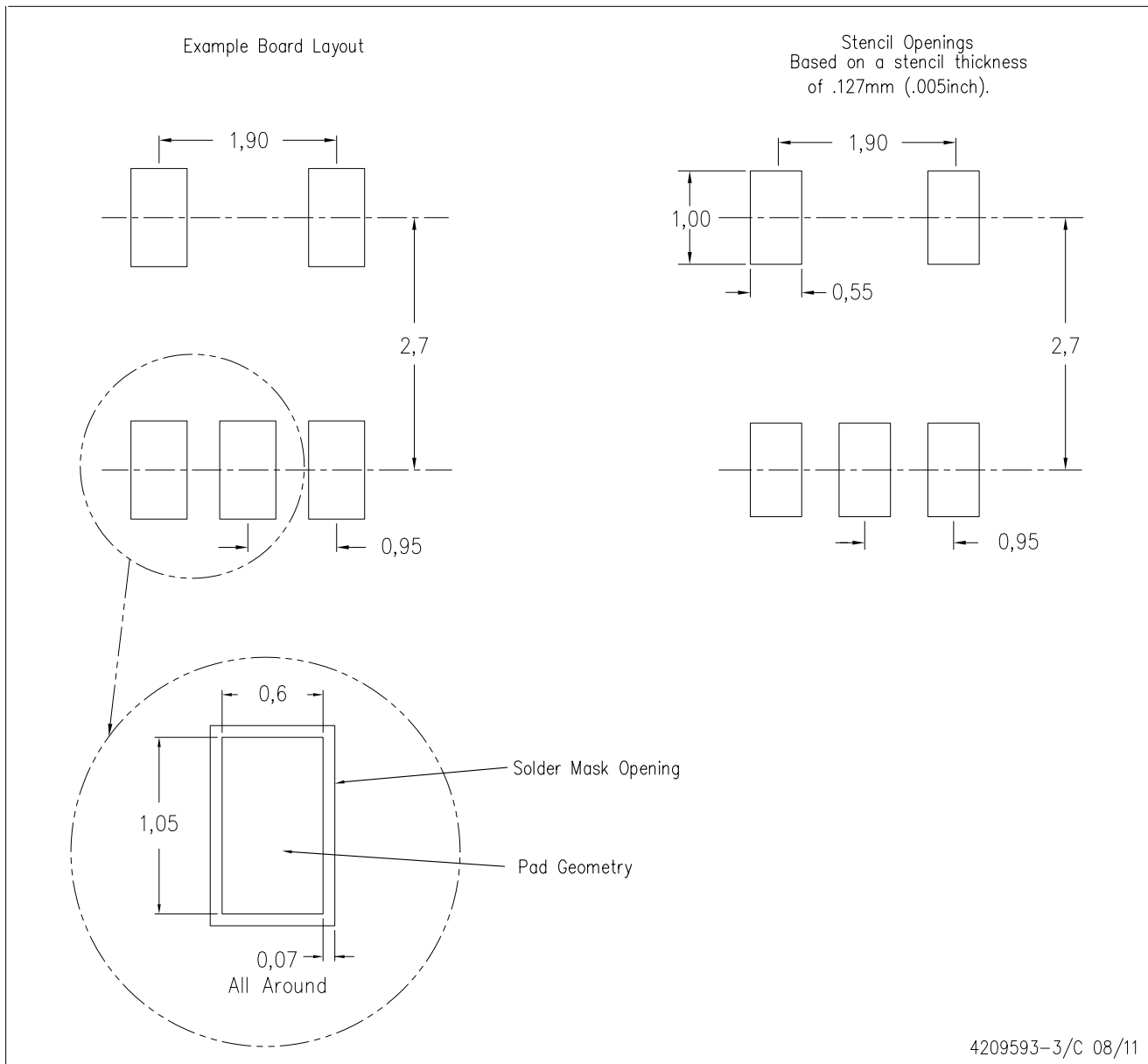
PLASTIC SMALL-OUTLINE PACKAGE



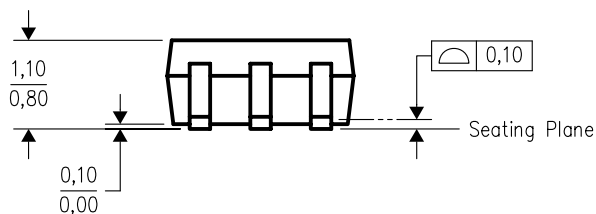
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE

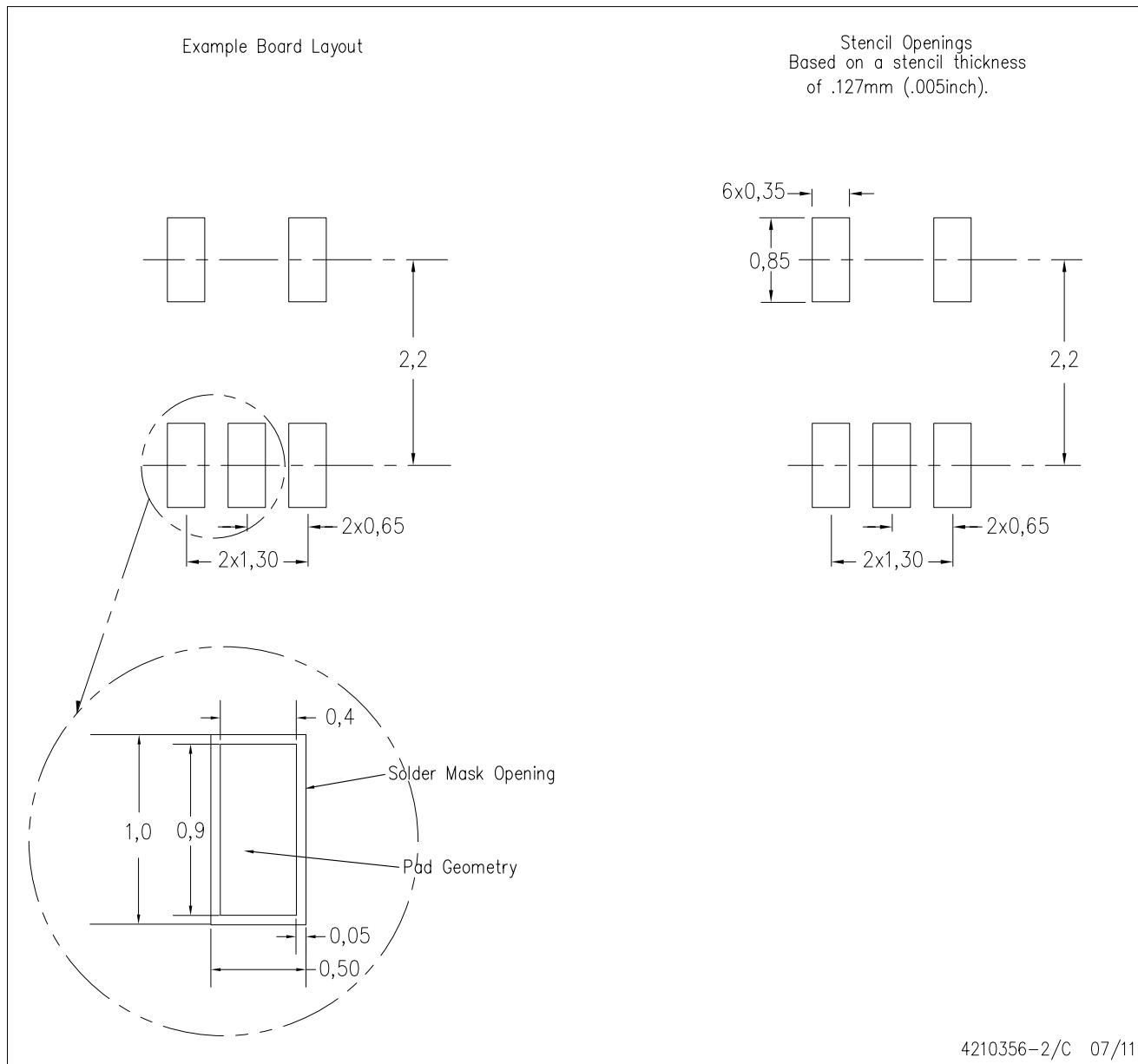


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

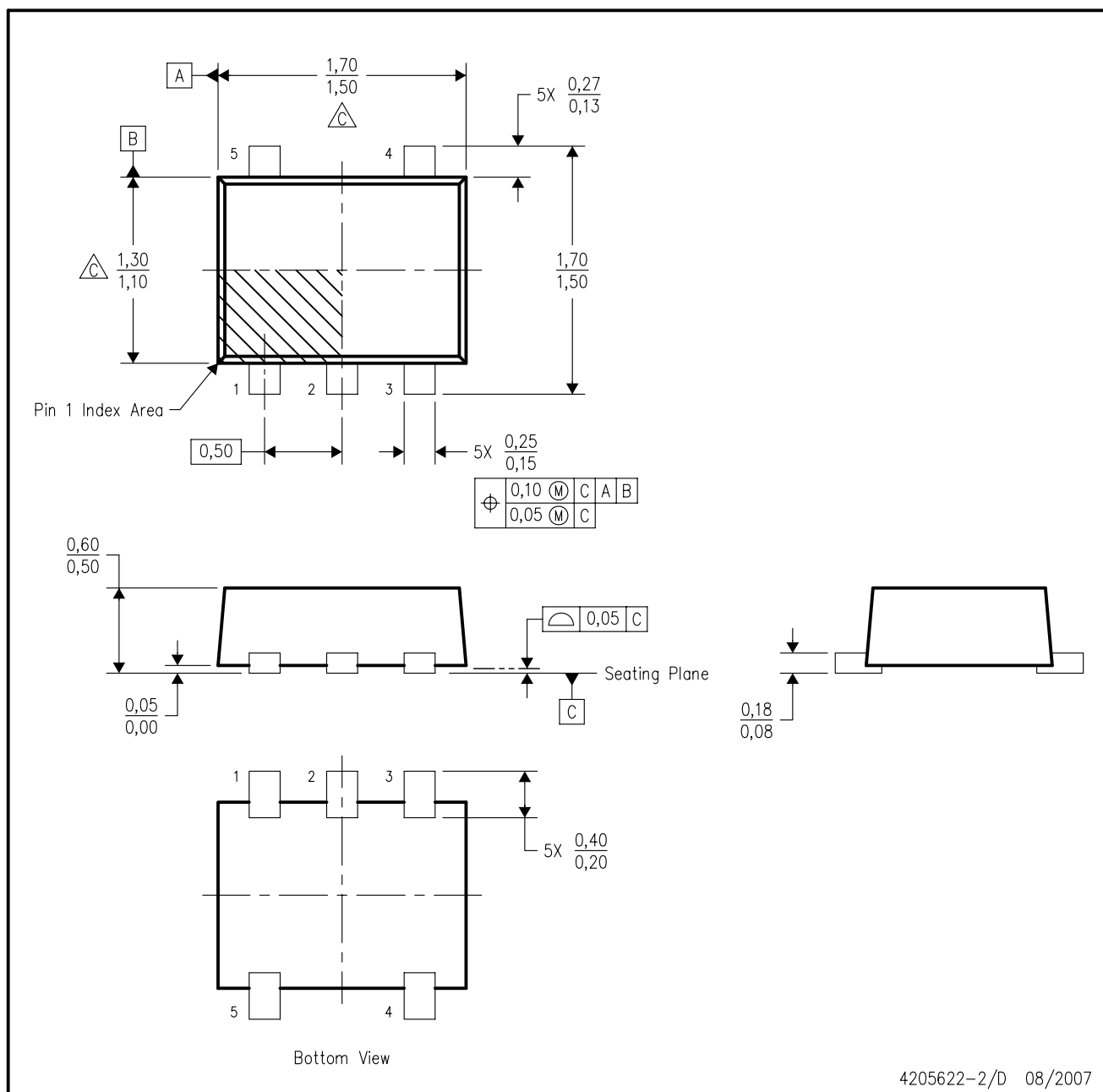


DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



4205622-2/D 08/2007

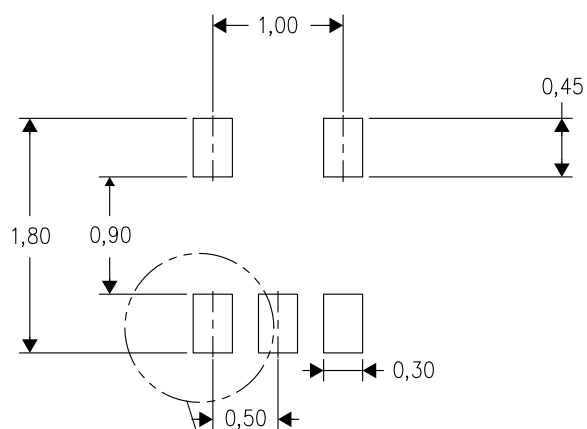
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
  - D. JEDEC package registration is pending.



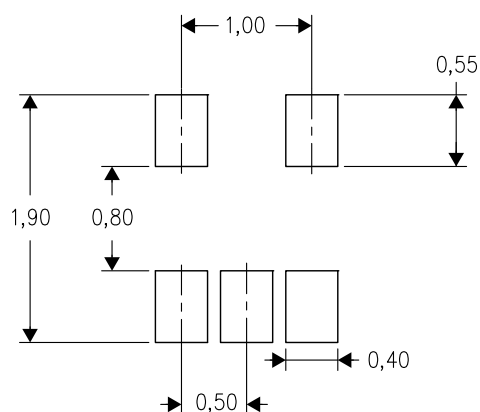
DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

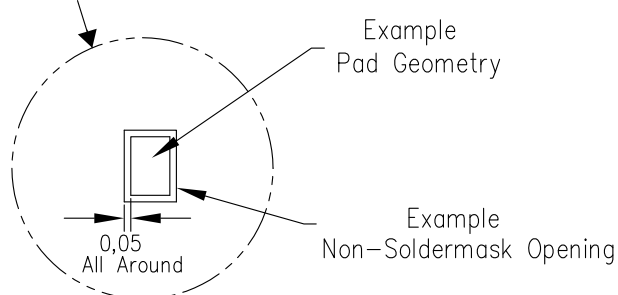
Example Board Layout



Example Stencil Design  
(Note E)



Example  
Non-Soldermask Defined Pad

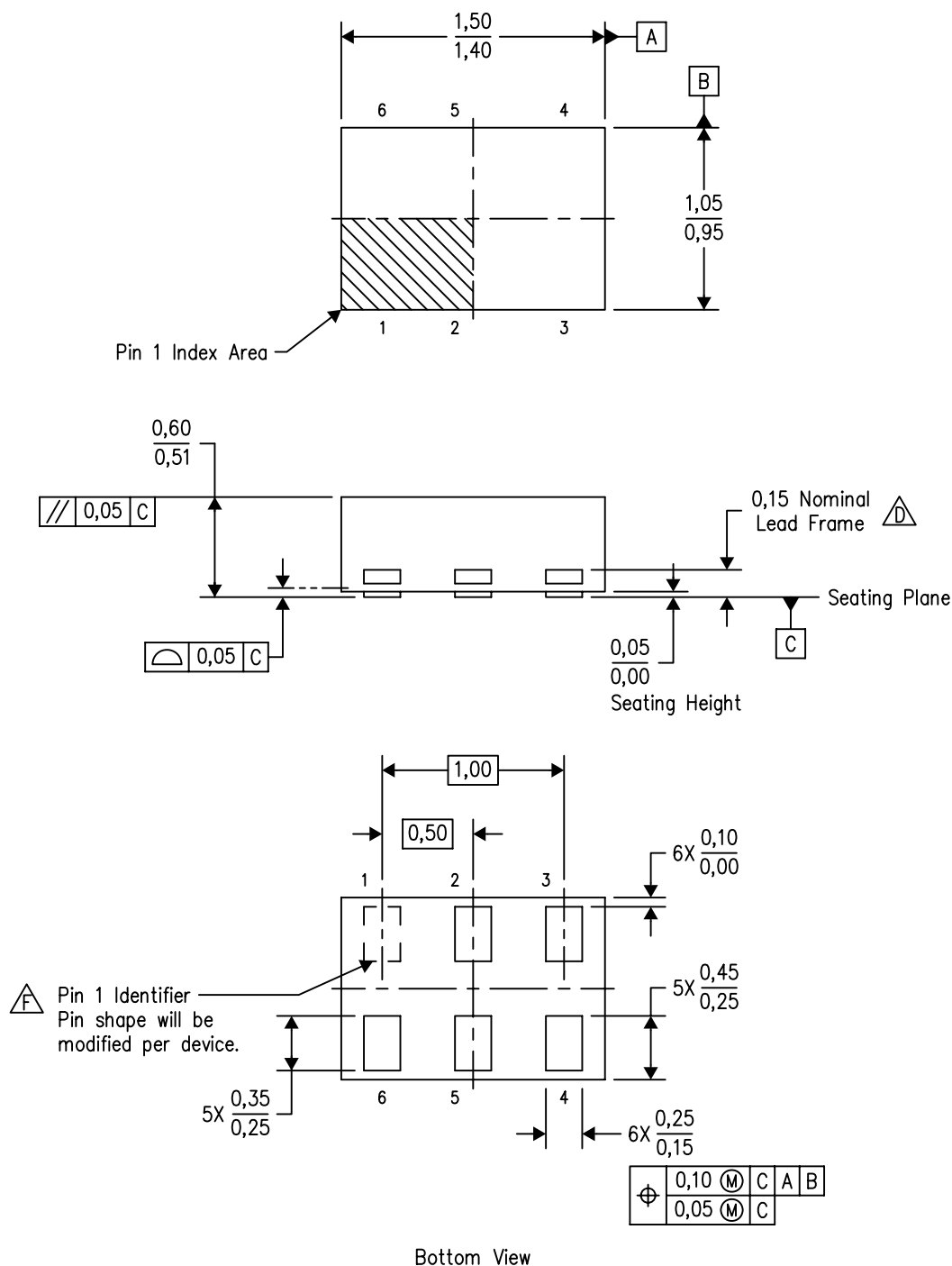


4208207-2/E 06/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



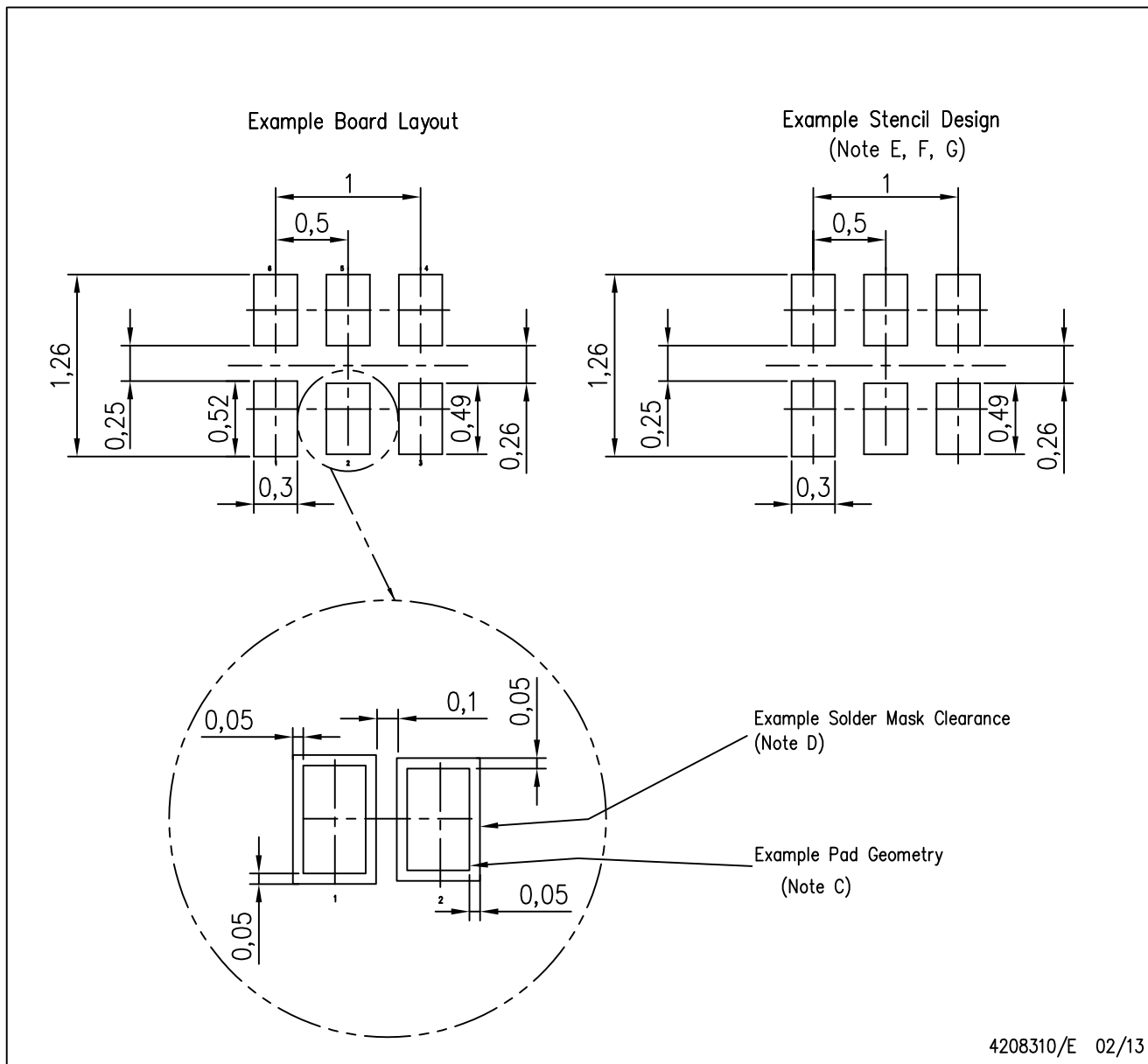
Bottom View

4207181/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
  - E. This package complies to JEDEC MO-287 variation UFAD.
  - F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

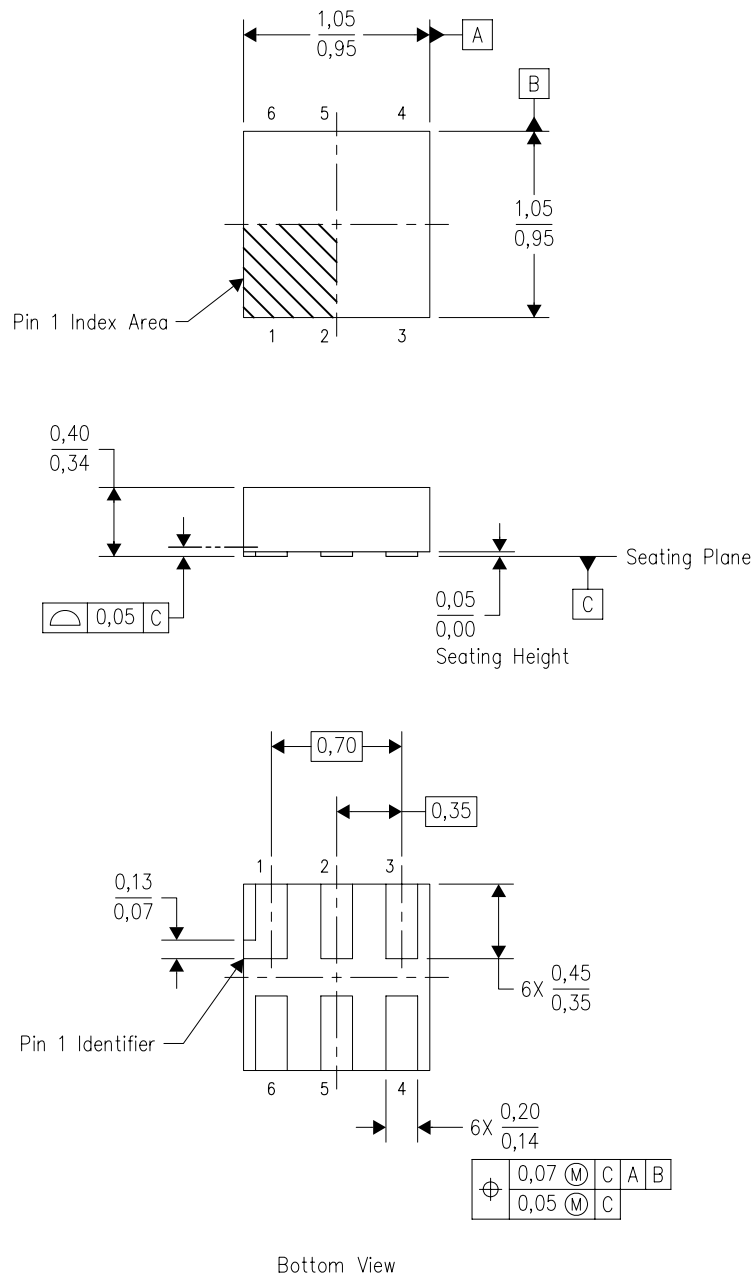
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



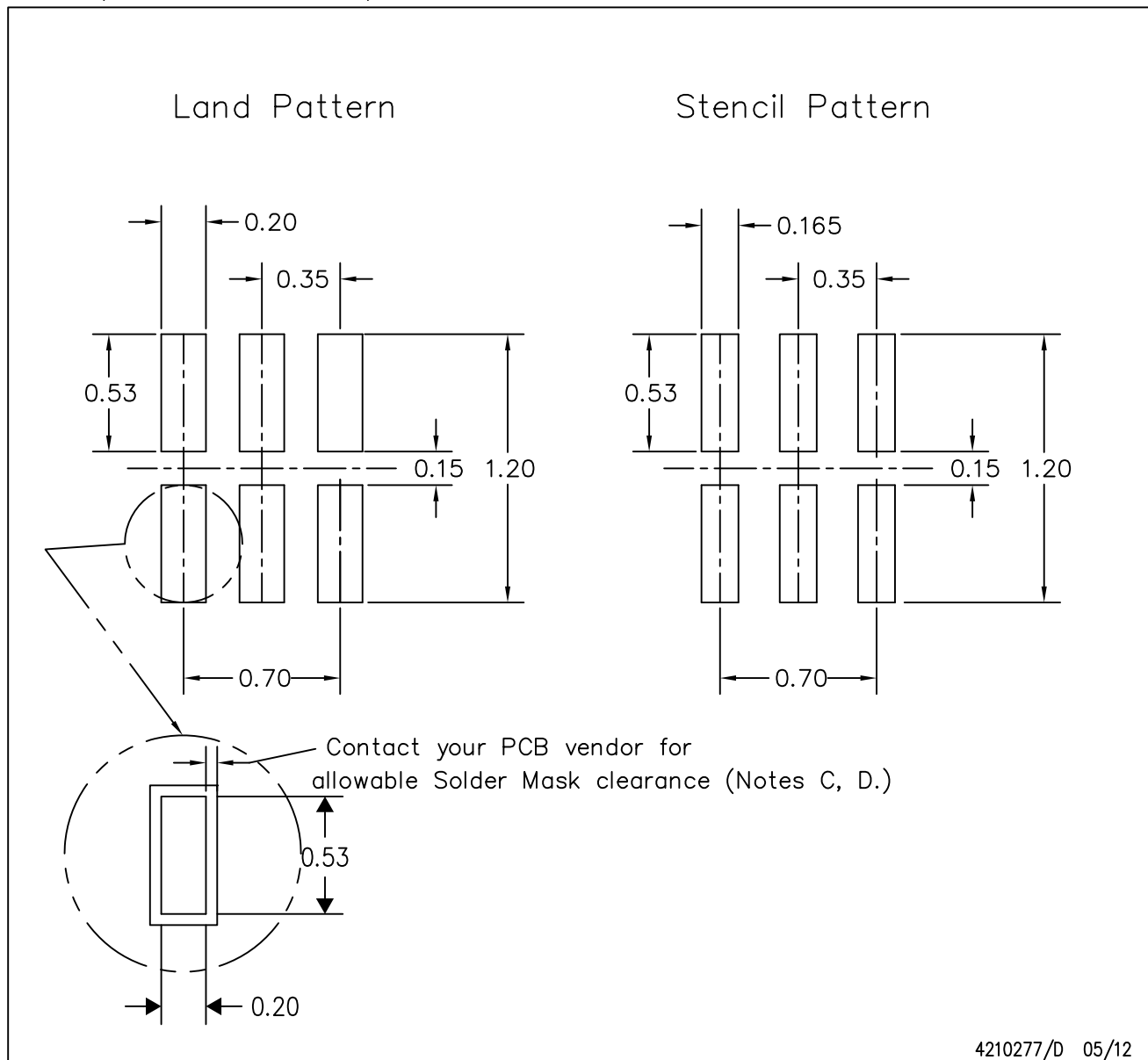
Bottom View

4208186/E 03/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - D. This package complies to JEDEC MO-287 variation X2AAF.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

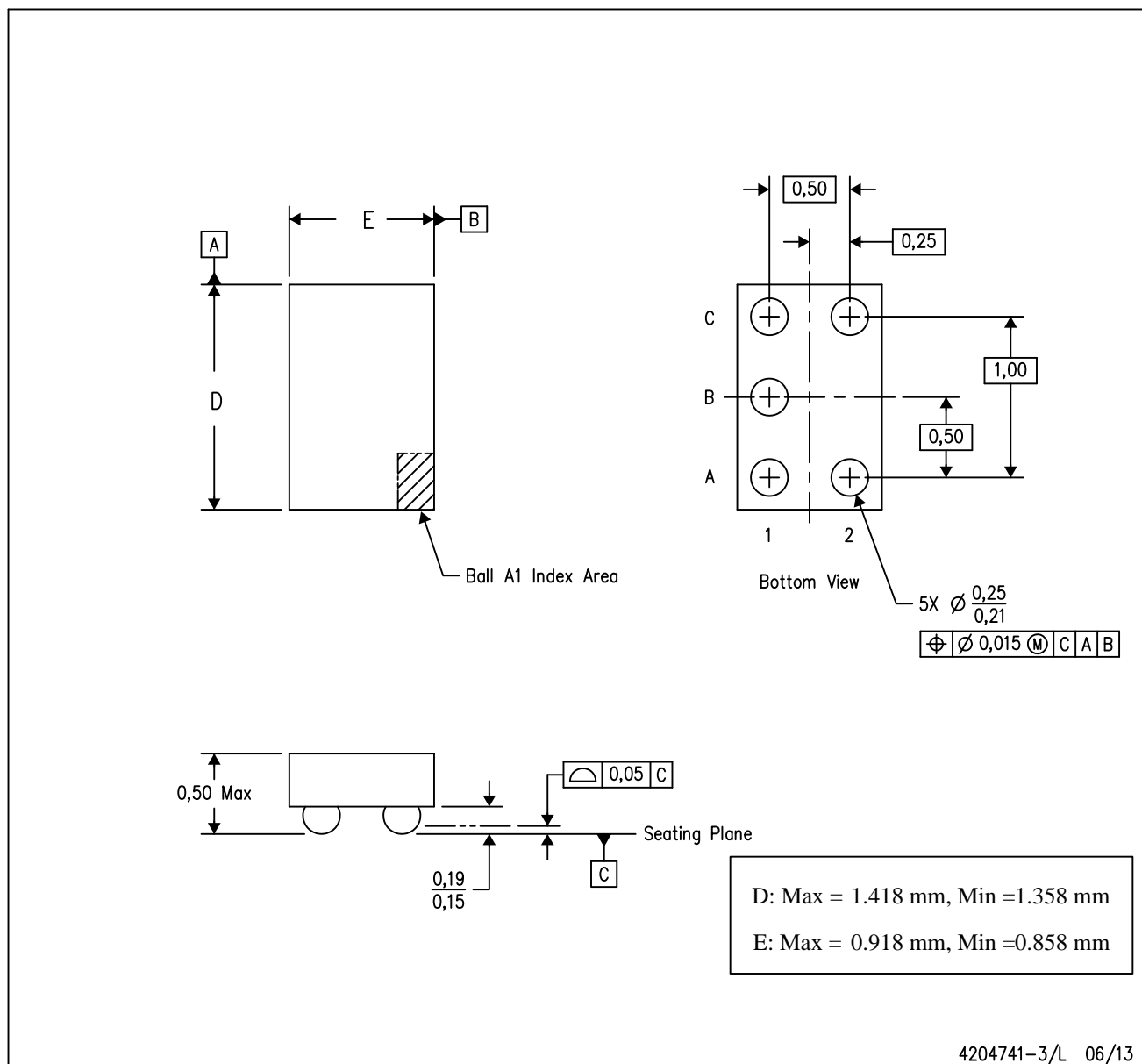


4210277/D 05/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
  - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
  - H. Component placement force should be minimized to prevent excessive paste block deformation.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY

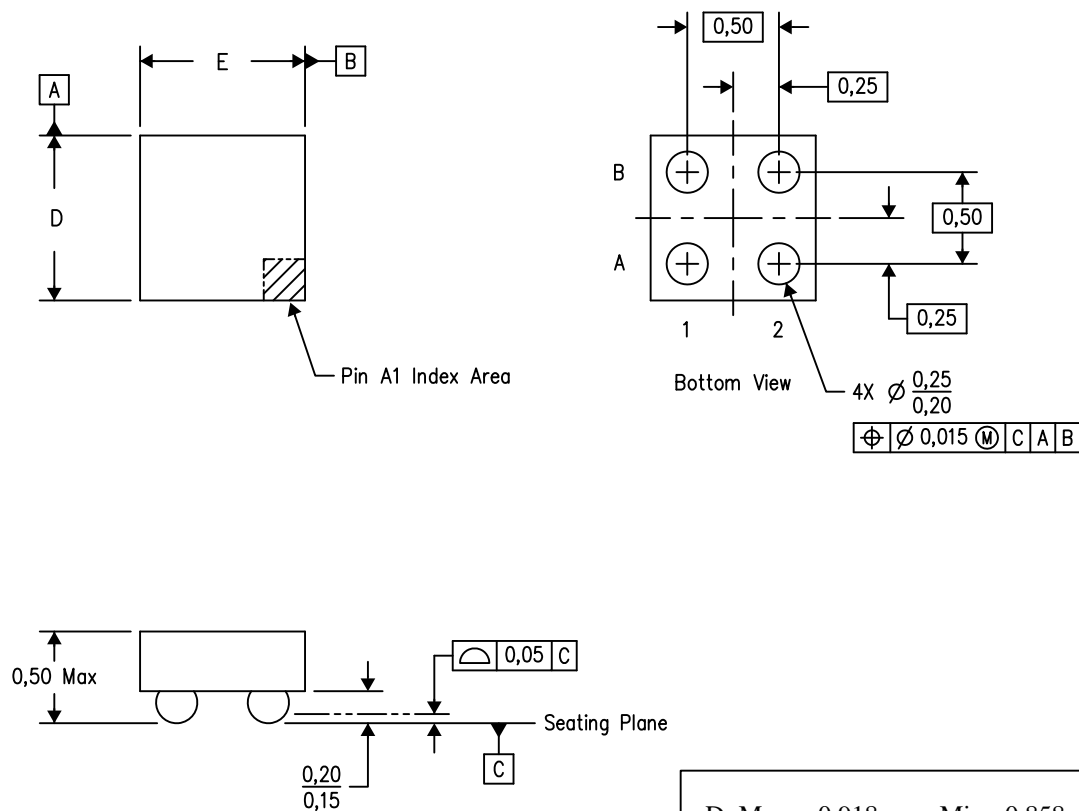


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



D: Max = 0.918 mm, Min = 0.858 mm

E: Max = 0.918 mm, Min = 0.858 mm

4206083/C 07/13

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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