SMJ27C512
524 288-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY

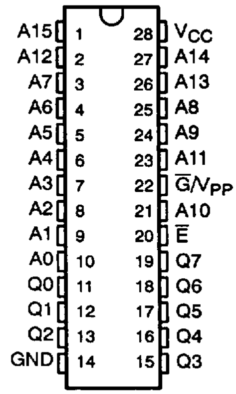
SGMS019B–SEPTEMBER 1987–REVISED FEBRUARY 1993

- **Military Operating Temperature Range . . . – 55°C to 125°C**
- **Processed to MIL-STD-883C, Class B**
- **Organization . . . 64K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 512K EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**

'27C512-20	200 ns
'27C512-25	250 ns
'27C512-30	300 ns

- **HVCMOS Technology**
- **3-State Output Buffers**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Low Power Dissipation**
  - **Active . . . 275 mW (Max)**
  - **Standby . . . 1.9 mW (Max) (CMOS Input Levels)**

J PACKAGE†
(TOP VIEW)



† Package is shown for pinout reference only.

PIN NOMENCLATURE	
A0–A15	Address Inputs
$\overline{E}$	Chip Enable/Power Down
GND	Ground
Q0–Q7	Outputs
V_{CC}	5-V Power Supply
$\overline{G}/V_{PP}$	Output Enable
GND	Ground

description

The SMJ27C512 series are 524 288-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors, and each output can drive one Series 54 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The SMJ27C512 is pin compatible with existing 28-pin 512K ROMs and EPROMs. They are offered in a 600-mil dual-in-line ceramic package (J suffix) rated for operation from –55°C to 125°C.

Since this EPROM operates from a single 5-V supply (in the read mode), it is ideal for use in microprocessor-based systems. One other 12–13 V supply is needed for programming, but all programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. Fast programming uses a V_{PP} of 12.5 V and a V_{CC} of 6 V for a nominal programming time of two minutes. SNAP! Pulse programming uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

The seven modes of operation for the SMJ27C512 are listed in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V for Fast, or 13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

TEXAS INSTRUMENTS
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FUNCTIN (PINS)	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}/V_{PP}$ (22)	V_{IL}	V_{IH}	X†	V_{PP}	V_{IL}	V_{PP}	V_{IL}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q0–Q7 (11–13, 15–19)	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	85

† X can be V_{IL} or V_{IH}.
‡ $V_H = 12\ V \pm 0.5\ V$.

read/output disable

When the outputs of two or more SMJ27C512s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the selected SMJ27C512, a low-level signal is applied to the $\overline{E}$ and $\overline{G}/V_{PP}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q0 through Q7.

power down

Active I_{CC} supply current can be reduced from 25 mA to 500 μA (TTL-level inputs) or 350 μA (CMOS-level inputs) by applying a high logic signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C512 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic 0's (lows) are programmed into the desired locations. A programmed logic 0 (low) can be erased only by ultraviolet light. The recommended minimum ultraviolet light exposure dose (UV intensity × exposure time) is 15 W•s/cm^2. A typical 12 mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C512, the window should be covered with an opaque label.

SNAP! Pulse programming

The 512K EPROM can be programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which can reduce programming time to a nominal of four seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q0 to Q7. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved with $\overline{G}/V_{PP}$ = 13 V, V_{CC} = 6.5 V, and $\overline{E} = V_{IL}$. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = 5 V, $\overline{G}/V_{PP} = V_{IL}$, and $\overline{E} = V_{IL}$.

fast programming

The 512K EPROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming, data is presented in parallel (eight bits) on pins Q0 through Q7. Once addresses and data are stable, $\overline{E}$ is pulsed. The programming mode is achieved when $\overline{G}/V_{PP}$ = 12.5 V, V_{CC} = 6 V, and $\overline{E} = V_{IL}$. More than one SMJ27C512 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = 5 V (see Figure 2).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with $\overline{G}/V_{PP}$ and $\overline{E} = V_{IL}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10); i.e., A0 = V_{IL} accesses the manufacturer code, which is output on Q0–Q7; A0 = V_{IH} accesses the device code, which is output on Q0–Q7. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q7. The manufacturer code for these devices is 97, and the device code is 85.

latchup immunity

Latchup immunity on the SMJ27C512 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

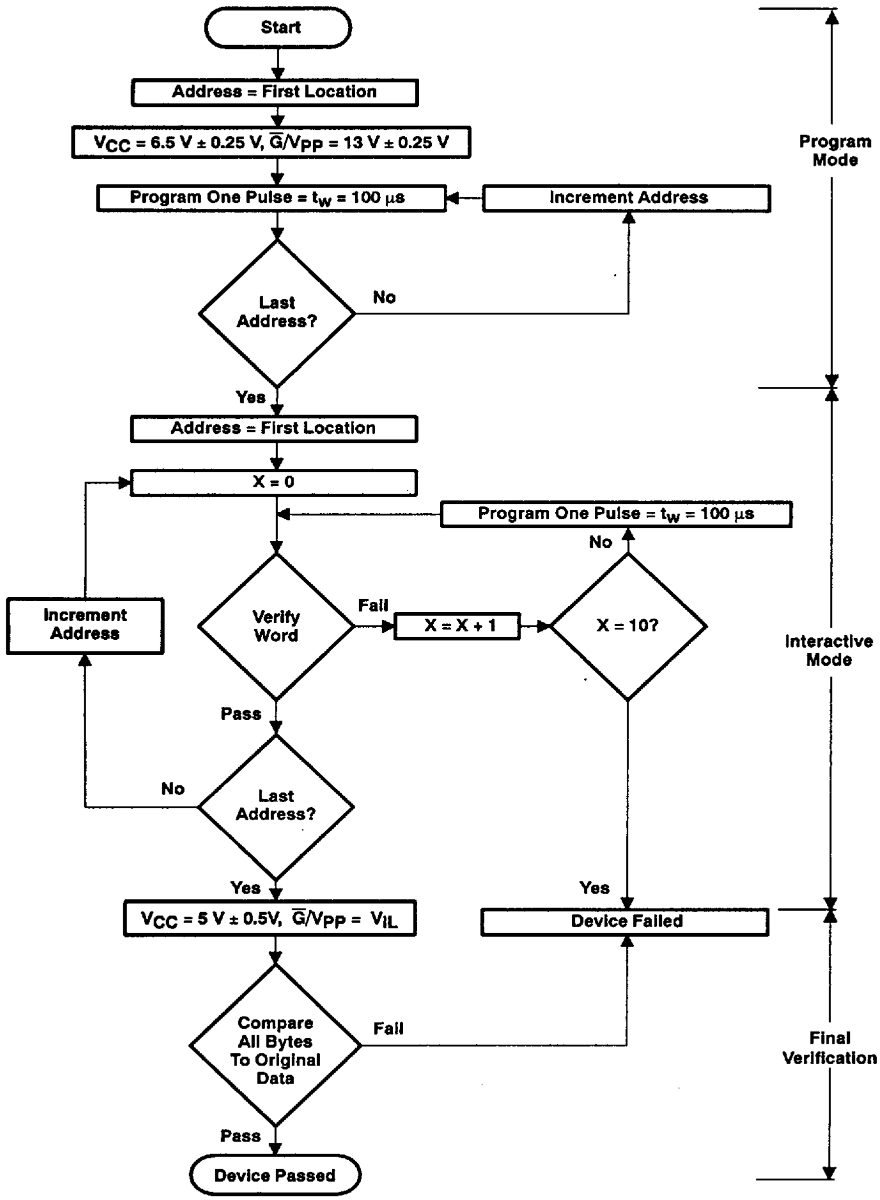


Figure 1. SNAP! Pulse Programming Flowchart

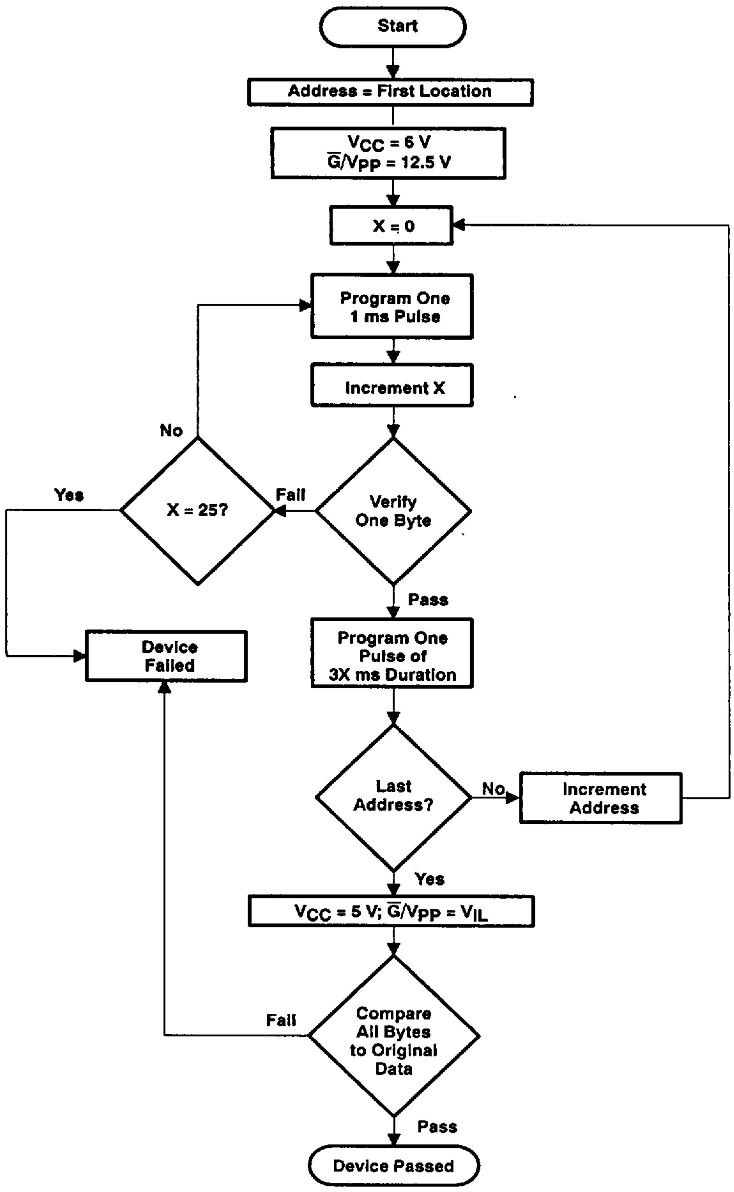
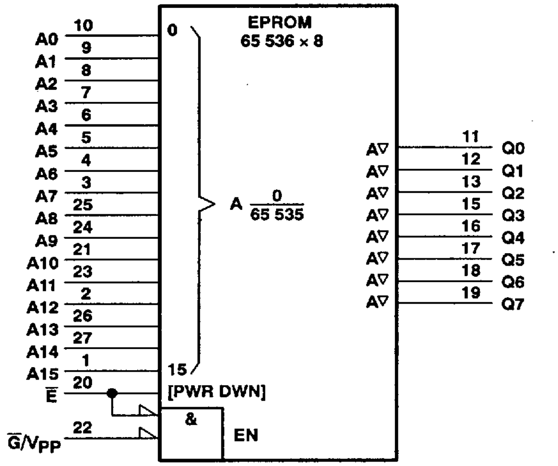


Figure 2. FAST Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1)	−0.6 V to 7 V
Supply voltage range, V_{PP}	−0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9	−0.6 V to 6.5 V
A9	−0.6 V to 13.5 V
Output voltage range (see Note 1)	−0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature	−55°C
Maximum operating case temperature	125°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			SM/SMJ27C512-20 SM/SMJ27C512-25 SM/SMJ27C512-30 MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 2)	Read mode	4.5	5	5.5	V
		Fast programming algorithm	5.75	6	6.25	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	V
$\overline{G}/V_{PP}$	Supply voltage (see Note 3)	Fast programming algorithm	12	12.5	13	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	V
		CMOS	GND −0.2		GND +0.2	V
T_A	Operating free-air temperature		−55			°C
T_C	Operating case temperature				125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as $\overline{G}/V_{PP}$ and removed after or at the same time as $\overline{G}/V_{PP}$. The device must not be inserted into or removed from the board when $\overline{G}/V_{PP}$ or V_{CC} is applied.
3. $\overline{G}/V_{PP}$ can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level ouput voltage		$I_{OH} = -400\ \mu A$	2.4			V
V_{OL}	Low-level ouput voltage		$I_{OL} = 2.1$ mA			0.4	V
I_I	Input current (leakage)		$V_I = 0$ to 5.5 V			±10	µA
I_O	Output current (leakage)		$V_O = 0$ to V_{CC}			±10	µA
I_{PP}	$\overline{G}/V_{PP}$ supply current (during program pulse)‡		$\overline{G}/V_{PP} = 13$ V		35	70	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$			500	µA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$			325	µA
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $E = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		35	50	mA

† Typical values are at $T_A = 25°C$ and nominal voltages.
‡ This parameter has been characterized at 25°C and is not production tested.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	UNIT
C_i	Input capacitance	$V_I = 0$, f = 1 MHz		6	pF
C_O	Output capacitance	$V_O = 0$, f = 1 MHz		8	pF
$C_{G/VPP}$	$\overline{G}/V_{PP}$ input capacitance	$\overline{G}/V_{PP} = 0$, f = 1 MHz		20	pF

† Typical values are at $T_A = 25°C$ and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTE 4)	'27C512-20		'27C512-25		'27C512-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	See Figure 3		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100		120	ns
tdis	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	105	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not production tested.

recommended timing requirements for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.5 and V_{PP} =13 (SNAP! Pulse), T_A = 25°C (see Note 4)

			MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	µs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			µs
$t_{dis(G)}$	Output disable time from $\overline{G}$		0		130	µs
t_{EHD}	Data valid from $\overline{E}$ low				1	µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs
$t_{r(PG)G}$	V_{PP} rise time		50			ns
$t_{h(VPP)}$	V_{PP} hold time		2			µs
$t_{rec(PG)}$	V_{PP} recovery time		2			µs

NOTE 4: For all switching characteristics and timing measurements input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference page 9, AC testing waveforms).

PARAMETER MEASUREMENT INFORMATION

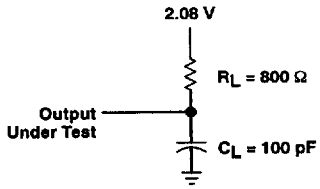


Figure 3. AC Testing Output Load Circuit

AC testing input/output wave forms

A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

PARAMETER MEASUREMENT INFORMATION

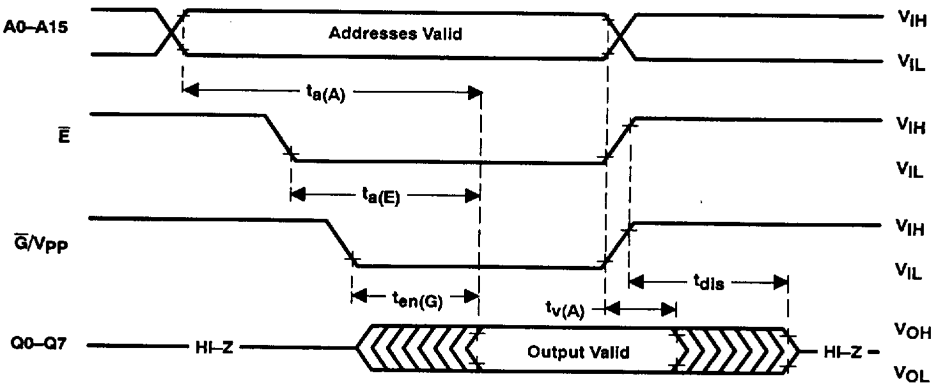
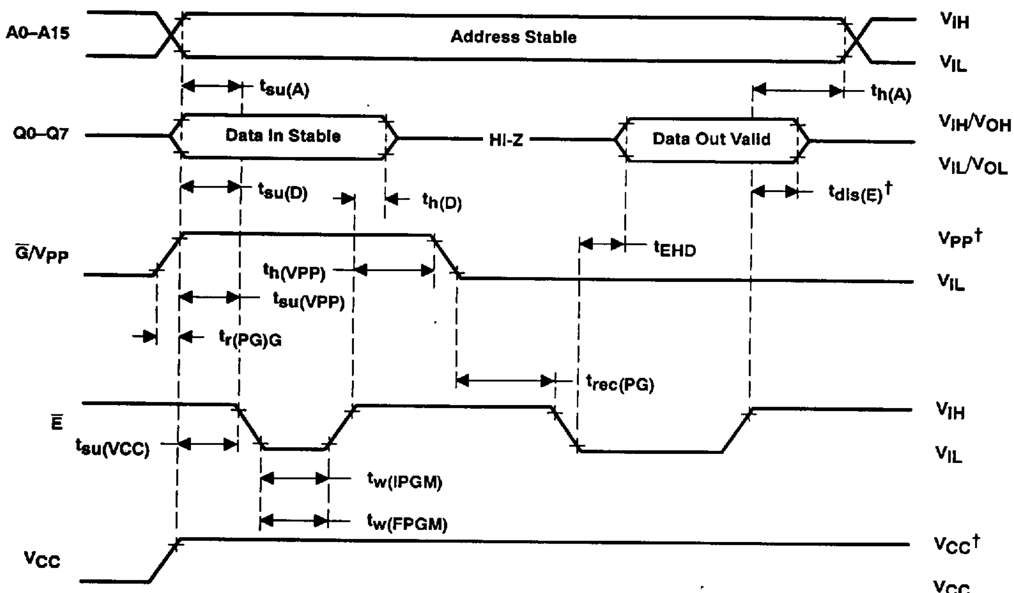


Figure 4. Read Cycle Timing



† 12.5-V V_{PP} and 6-V V_{CC} for Fast programming, 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 5. Program Cycle Timing

TYPICAL SMJ27C512 CHARACTERISTICS