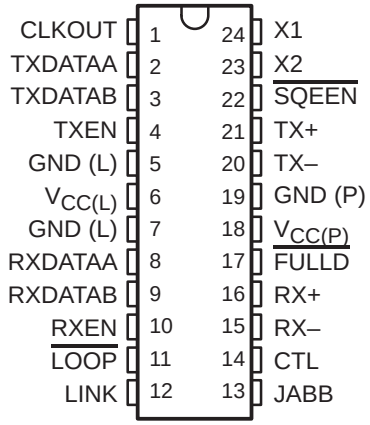
- **Meets or Exceeds the IEEE STD 802.3I, Type 10BASE-T**
- **Differential (Twisted-Pair) I/O Driver/Receiver**
- **High-Speed Receiver . . . t_{pd} = 50 ns Max**
- **Receiver Squelch Circuit Integrity Improved With Noise Filter**
- **Jabber Control Prevents Network Lockup**
- **Collision Detection for Multiple-User Networks**
- **Data Link Integrity Monitored With Link Test Pulse**
- **Externally Addressable Test Register Controls Signal Quality Error Testing**
- **CMOS and Raised ECL Compatible**
- **24-Terminal, 300-mil Dual-In-Line Package**

DW PACKAGE
(TOP VIEW)



description

The SN75LBC086 is a single-channel differential driver/receiver interface device for the medium attachment unit (MAU) used in 10-MHz twisted-pair Ethernet applications. The device uses a 5-V supply and is designed to interface with two pairs of telephone-grade twisted-pair cables coupled through isolation transformers. The functional components of the device include a differential receiver and driver, receiver squelch with noise filter, jabber controls, collision detection, data link monitor, and signal quality error (SQE) testing. The LinBiCMOS™ process technology is used in the device design to ensure analog precision, low power, and high-speed operation.

The device contains an elaborate receiver-squelch circuit† that provides an improved level of noise rejection by qualifying the incoming signal stream with three different criteria. First, the signal is compared to a set threshold voltage level. Then, the pulse duration is compared to a set time window. Last, the signal must follow a set pattern of positive and negative pulses before the circuit finally opens the receiver channel to the incoming data packet.

The jabber control is designed to prevent a defective controller from locking up the network by limiting the data packet transmission time to 20 to 30 ms. When a packet length exceeds 20 to 30 ms, the driver is turned off for about 600 ms. The driver-enable input must be made inactive by the controller during this period before the jabber control will release the driver. The JABB output is active (high) when a jabber condition exists.

Collision detection is used to arbitrate access to the multiuser network. This detection is done logically by monitoring the receive line for a valid signal during a driver transmission. When a collision is detected, this device informs the controller with an active-high CTL output. After a valid packet transmission, the device also performs a signal quality error test causing the CTL output to go active (high). This test is disabled when the $\overline{\text{SQEEN}}$ input goes inactive (high).

The device tests data-link integrity during the idle state by periodically driving the driver line with a unipolar pulse called a link-test pulse. The receiver looks for this link-test pulse on the receive line. A failed line link is indicated by a high-impedance state at the LINK output. This output drives an LED for monitoring if needed.

An internal test register is externally controlled with inputs $\overline{\text{FULLD}}$ and $\overline{\text{LOOP}}$ to select the device testing mode. When in the test mode, serial test-mode control patterns are clocked into the test register through input $\overline{\text{SQEEN}}$. These control patterns select various modes to test the internal circuits.

† Embodies technology covered by one or more Digital Equipment Corporation Patents.
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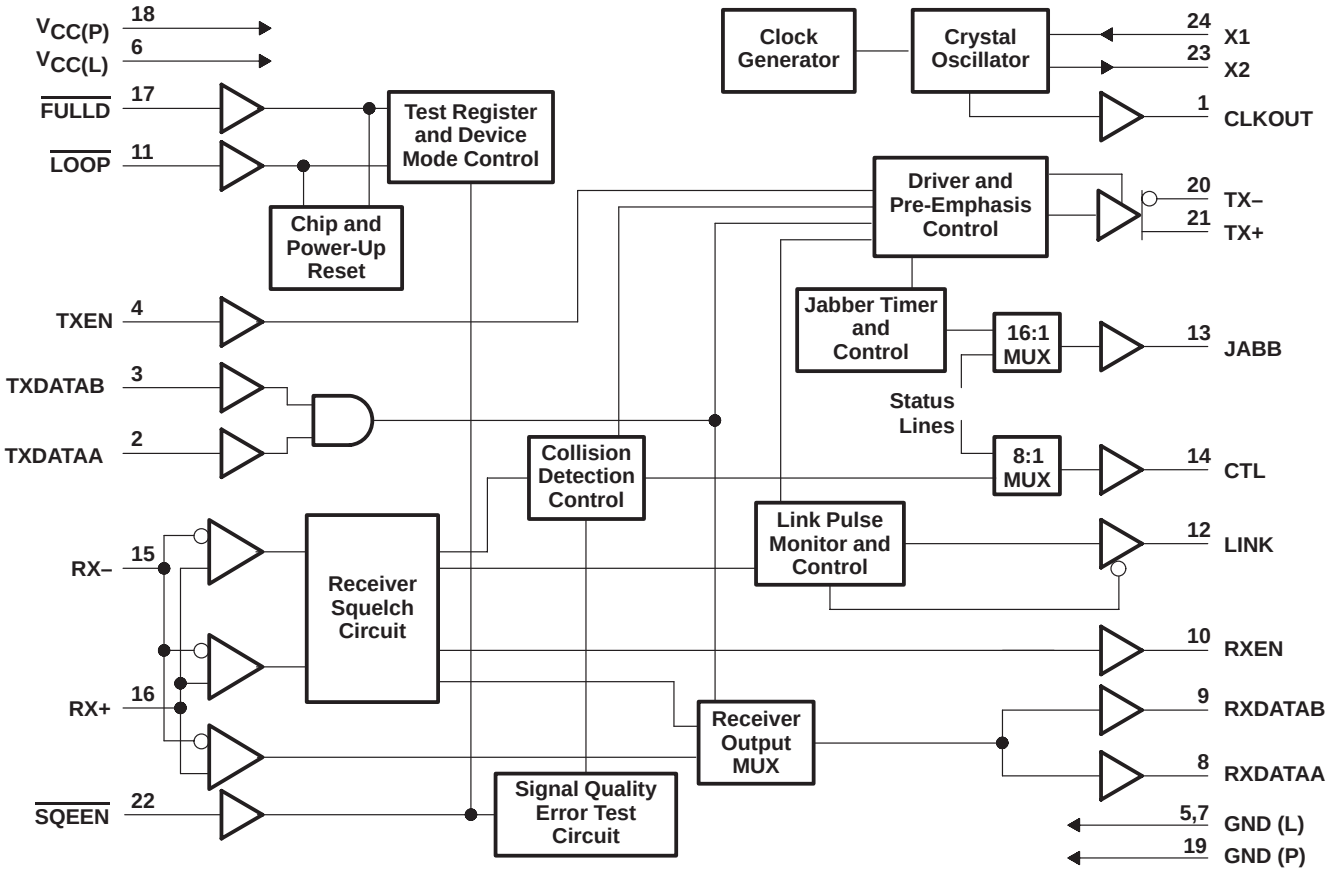
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL LEVEL	TERMINAL NO.	I/O	DESCRIPTION
CLKOUT	CMOS	1	O	Clock output. This 10-MHz buffered clock drives other interface devices.
CTL	CMOS	14	O	Control. In normal mode, CTL high indicates a collision. In test mode, status lines are muxed out.
$\overline{\text{FULLD}}$	TTL	17	I	Full-duplex mode. When active (low), the device is placed in the full-duplex operating mode for simple point-to-point communication applications. In the full-duplex mode, the receiver and driver are both active with collision detection disabled. After $\overline{\text{LOOP}}$ and $\overline{\text{FULLD}}$ go active (low), in that order, a device reset is initiated and while both are active (low), test select data clocks into the test register using a 100-ns clock at the X1 input. This terminal is held inactive (high) due to an internal pullup resistor.
GND (L)	GROUND	5 7		Logic grounds. These terminals provide a ground return for the CMOS core logic.
GND (P)	GROUND	19		Power ground. This provides a ground return for the input and output buffers, driver (transmitter), and receiver circuits.
JABB	CMOS	13	O	Jabber control. When a jabber condition exists during normal mode operation, this signal goes active (high) to report jabber-control status to the controller. In the test mode, this provides a multiplexed signal for internal timer and counter functions.
LINK	CMOS	12	O	Link status. This 3-state output indicates the status of the receiver and interface link. When driving an LED (with anode to resistor to V_{CC}), a high-impedance level indicates a failed link and the LED is off. A momentary high level indicates the device is receiving valid data and the LED is blinking on and off. A continuous low level indicates the device is receiving valid link pulses but no data, and the LED is on.
$\overline{\text{LOOP}}$	TTL	11	I	Loop-back mode. When the device is in the normal operating mode (not test mode) and $\overline{\text{LOOP}}$ is active (low), the driver (transmit) data is directed to the receive data path to put the device in the loop-back mode and the driver is turned off. After $\overline{\text{LOOP}}$ and $\overline{\text{FULLD}}$ go active (low), in that order, a device reset is initiated and while both are active (low), test select data clocks into the test register using a 100-ns clock at the X1 input. This terminal is held inactive (high) due to an internal pullup resistor.
RX+		16	I	Differential receiver inputs
RX–		15	I	
RXEN	CMOS	10	O	Receiver squelch status. This provides squelch status information to the controller. When active (high), this signal indicates that the data path is valid or open from the receive channel through the device. An inactive (low) indicates that the receive channel is squelched or closed. This signal is capable of driving an LED monitor.
RXDATAA RXDATAB	CMOS ECL	8 9	O O	Received-data serial outputs. These outputs provide a choice of logic levels and serial data either from the differential receiver input (RX+ and RX–) or data from the controller (TXDATAA or TXDATAB) when in the loop-back mode. When the receiver is idle, these output levels are normally high. These terminals are held inactive (high) due to an internal pullup resistor.
$\overline{\text{SQEEN}}$	TTL	22	I	Signal-quality error-test enable. In normal operating mode, this enables the SQE test function performed at the end of a data packet transmission. In the test mode, $\overline{\text{SQEEN}}$ is used (with X1 clock) as a serial data input port to load test patterns or selections into the test register. This terminal is held inactive (high) due to an internal pullup resistor.
TX+		21	O	Differential driver outputs
TX–		20	O	
TXEN	TTL	4	I	Transmitter (driver) enable. When TXEN is active (high), serial data at the TXDATA inputs starts and stops the driver. When TXEN is inactive (low), the driver begins transmitting an idle signal independent of the TXDATA inputs.
TXDATAA TXDATAB	CMOS ECL	2 3	I I	Transmit-data inputs. A choice of logic-level inputs provide Manchester-encoded serial data to the driver. Internal pullup resistors are included.
$V_{CC(L)}$	SUPPLY	6		V_{CC} logic power supply. This provides power to the CMOS core logic.
$V_{CC(P)}$	SUPPLY	18		V_{CC} power supply. This provides power to the input and output buffers, drivers, and receivers.
X1 X2	CMOS	24 23	I O	Crystal input/output. X1 provides an input from an external 10-MHz crystal or another external clock source when the crystal is disconnected. X2 provides an oscillator output.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range at any input, V_I . . . . . –0.5 V to 5.5 V
Output voltage range at any output, V_O . . . . . –0.5 V to 7 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to device ground pins GND(L) and GND(P) shorted together.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.25	V
High-level output voltage, V_{IH}	TXDATAA, X1		3.15			V
	TXDATAB (see Figure 1)	T_A = 0°C	$0.984V_{CC}-0.922$		$0.984V_{CC}-0.763$	
		T_A = 25°C	$0.984V_{CC}-0.877$		$0.984V_{CC}-0.727$	
		T_A = 70°C	$0.984V_{CC}-0.825$		$0.984V_{CC}-0.645$	
	$\overline{\text{TXEN}}$, $\overline{\text{LOOP}}$, $\overline{\text{FULLD}}$, SQEEN		2			
Low-level output voltage, V_{IH}	TXDATAA, X1				0.8	V
	TXDATAB (see Figure 1)	T_A = 0°C	$0.75V_{CC}-0.59$		$0.75V_{CC}-0.375$	
		T_A = 25°C	$0.75V_{CC}-0.55$		$0.75V_{CC}-0.35$	
		T_A = 70°C	$0.75V_{CC}-0.531$		$0.75V_{CC}-0.324$	
	$\overline{\text{TXEN}}$, $\overline{\text{LOOP}}$, $\overline{\text{FULLD}}$, SQEEN				0.8	
Differential input voltage, V_{ID}			0.586		2.8	V
Common-mode input voltage, V_{IC}			1.8		3.2	V
Operating free-air temperature, T_A			0		70	°C

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

drivers

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	CLKOUT, RXDATAA, RXEN, JABB, CTL	I_{OH} = –12 mA		3.7			V
		RXDATAB	See Figure 1	T_A = 0°C	0.984 V_{CC}–0.922		0.984 V_{CC}–0.763	V
				T_A = 25°C	0.984 V_{CC}–0.877		0.984 V_{CC}–0.727	
				T_A = 70°C	0.984 V_{CC}–0.825		0.984 V_{CC}–0.645	
V_{OL}	Low-level output voltage	CLKOUT, RXDATAA, RXEN, JABB, CTL	I_{OL} = 16 mA				0.5	V
		RXDATAB	See Figure 1	T_A = 0°C	0.75 V_{CC}–0.59		0.75 V_{CC}–0.375	V
				T_A = 25°C	0.75 V_{CC}–0.55		0.75 V_{CC}–0.35	
				T_A = 70°C	0.75 V_{CC}–0.531		0.75 V_{CC}–0.324	
		LINK	I_{OL} = 12 mA				0.5	V
V_{OD}	Differential-output voltage (peak)		See Figure 2		2.2		2.8	V
V_{OD}	Differential-output voltage (step)		See Figure 2		1.53		1.982	V
	Common-mode driver impedance	TX+, TX–			2	5	8	Ω

receivers

PARAMETER			TEST CONDITIONS†	MIN	MAX	UNIT
I_{IH}	High-level input current	TXDATAA, TXEN, $\overline{\text{LOOP}}$, $\overline{\text{FULLD}}$, $\overline{\text{SQEEN}}$	V_I = 5.25 V		20	µA
		X1			100	
		TXDATAB	V_{IH} = MAX		400	
I_{IL}	Low-level input current	TXDATAA, TXEN, $\overline{\text{LOOP}}$, $\overline{\text{FULLD}}$, $\overline{\text{SQEEN}}$	V_I = 0		–20	µA
		X1			–100	
		TXDATAB	V_{IL} = MIN		–400	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

drivers and receivers

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current	$V_{CC(L)}$, $V_{CC(P)}$	$V_{CC(L)}$ = 5.25 V, $V_{CC(P)}$ = 5.25 V		180	mA

switching characteristics

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time	RX+, RX–	RXEN	See Figure 4			5 bit times	
t_{pd2}	Propagation delay time at startup	RX+, RX–	RXDATAA or RXDATAB high	See Figure 4			75	ns
$t_{sk(o)}$	Output skew time	RXEN high	RXDATAA or RXDATAB low	See Figure 4			±10	ns
t_{pd3}	Propagation delay time after startup	RX+, RX–	RXDATAA or RXDATAB high	See Figure 4			50	ns
$t_{sk(p)}$	Pulse skew time ($\lvert t_{pd3(LH)} - t_{pd3(HL)} \rvert$)	RX+, RX–	RXDATAA or RXDATAAB	See Figure 4		2		ns
t_{pd4}	Propagation delay time	RX+, RX–	RXEN low	See Figure 5	155		250	ns
t_{pd5}	Propagation delay time	TXDATA or TXDATAB	TX+, TX–	See Figure 6			75	ns
$t_{sk(p)}$	Pulse skew time ($t_{pd5(LH)} - t_{pd5(HL)}$)	TXDATAA or TXDATAB	TX+, TX–	See Figure 6		2		ns
t_{pd6}	Propagation delay time in loop mode	TXDATAA or TXDATAB	RXDATAA, RXDATAB	See Figure 7			50	ns
t_{pd7}	Propagation delay time in loop mode	TXEN high	RXEN high	See Figure 7			50	ns
t_{pd8}	Propagation delay time in loop mode	$\overline{\text{LOOP}}$ low	RXEN low	See Figure 7			30	ns
t_{pd10}	Propagation delay time	TXEN low	RXEN low	See Figure 8			350	ns
t_{pd11}	Propagation delay time	TXEN low	TX+, TX– high	See Figure 8			50	ns
t_{p1}	Precompensation pulse duration		TX+, TX–	See Figure 6	45		55	ns
t_{p2}	Receiver link-beat minimum pulse duration			See Figure 9	80		120	ns
t_{en1}	Enable time	TXDATAA or TXDATAB	TX+, TX–	See Figure 6			75	ns
t_{en2}	Enable time	TXEN	TX+, TX–	See Figure 6			75	ns
t_{dis1}	Disable time, caused by TXDATAA or TXDATAB high or TXEN low	TX+, TX– high	TX+, TX– at 585-mV level	See Figure 8	250			ns
t_{pd12}	Propagation delay time to looped RXEN	TXEN high	RXEN high	See Figure 6			100	ns
t_{pd13}	Propagation delay time for looped back data	TXDATAA or TXDATAB	RXDATAA RXDATAB	See Figure 6			75	ns

timing requirements

	TEST CONDITIONS	MIN	MAX	UNIT
Setup time, test mode, $\overline{\text{SQEEN}}$ before X1↑, t_{su1}	See Figure 10	30		ns
Setup time, test mode, $\overline{\text{LOOP}}$ low before FULLD↓, t_{su2}	See Figure 10	25		ns
Hold time, test mode, $\overline{\text{SQEEN}}$ after X1↑, t_{h1}	See Figure 10	25		ns

PARAMETER MEASUREMENT INFORMATION

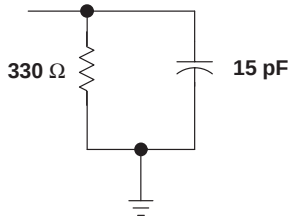


Figure 1. ECL Load Circuit

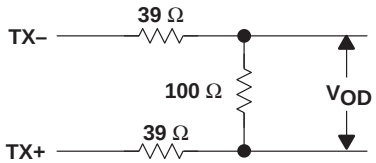


Figure 2. Differential Load CIrcuit

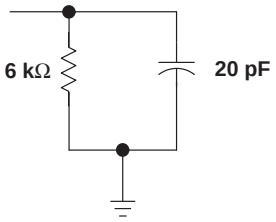


Figure 3. CMOS Load Circuit

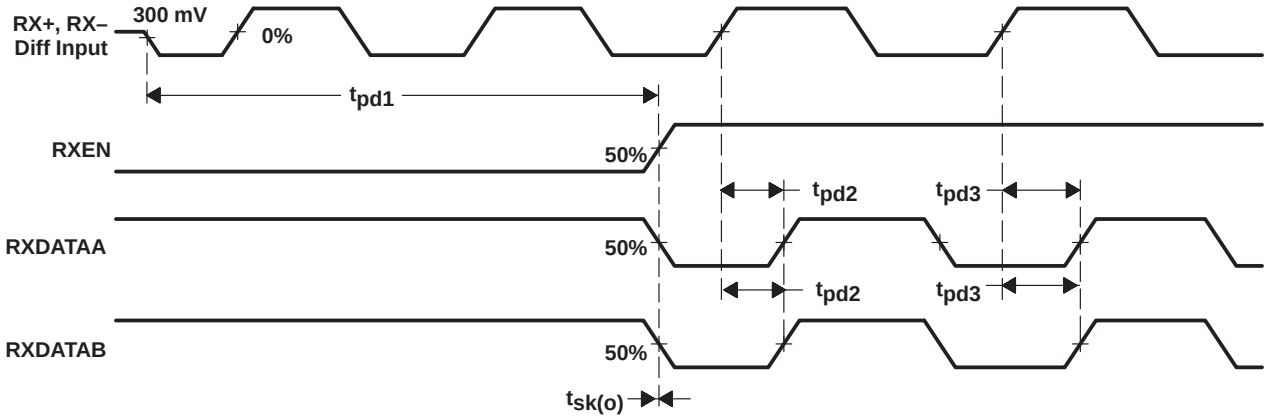


Figure 4. Receiver Startup Waveforms

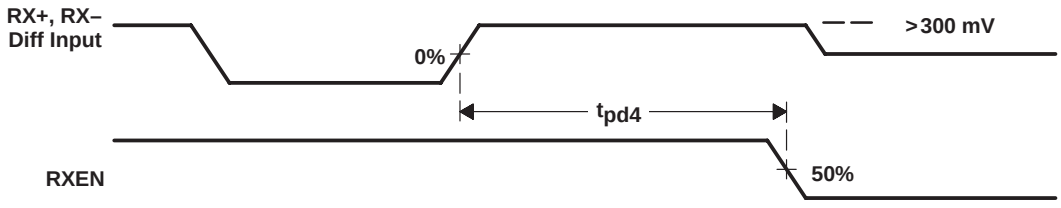


Figure 5. Receiver Shutdown Waveforms

PARAMETER MEASUREMENT INFORMATION

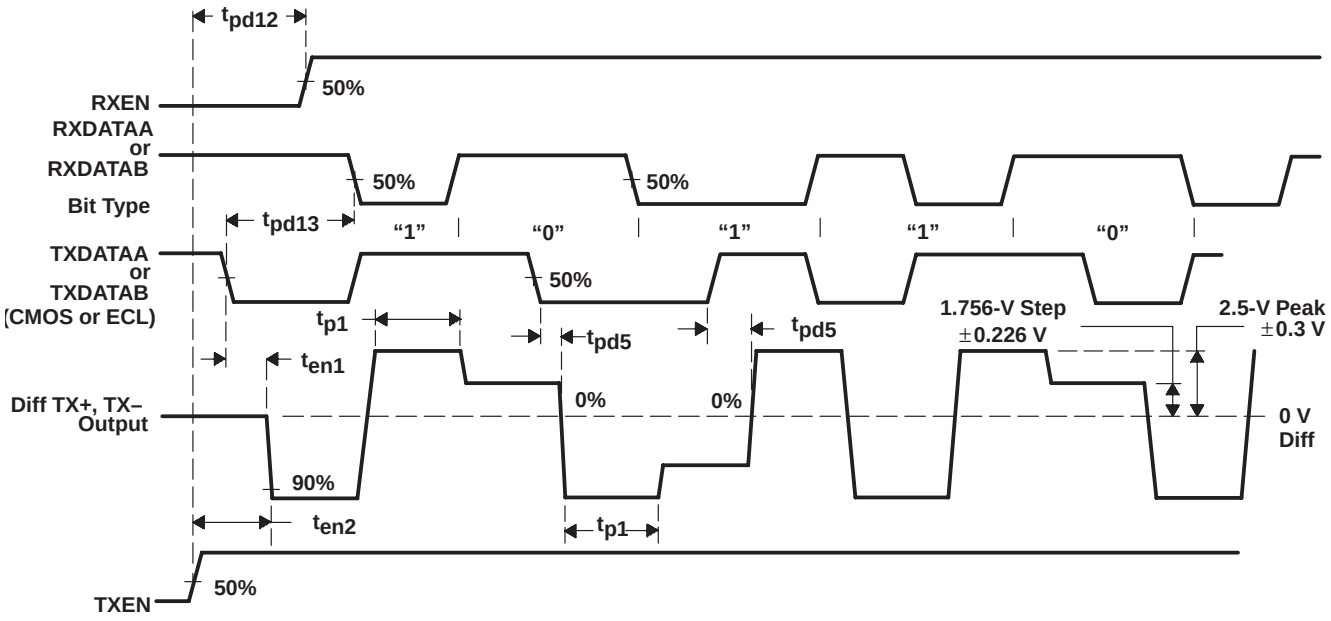


Figure 6. Driver Startup Waveforms

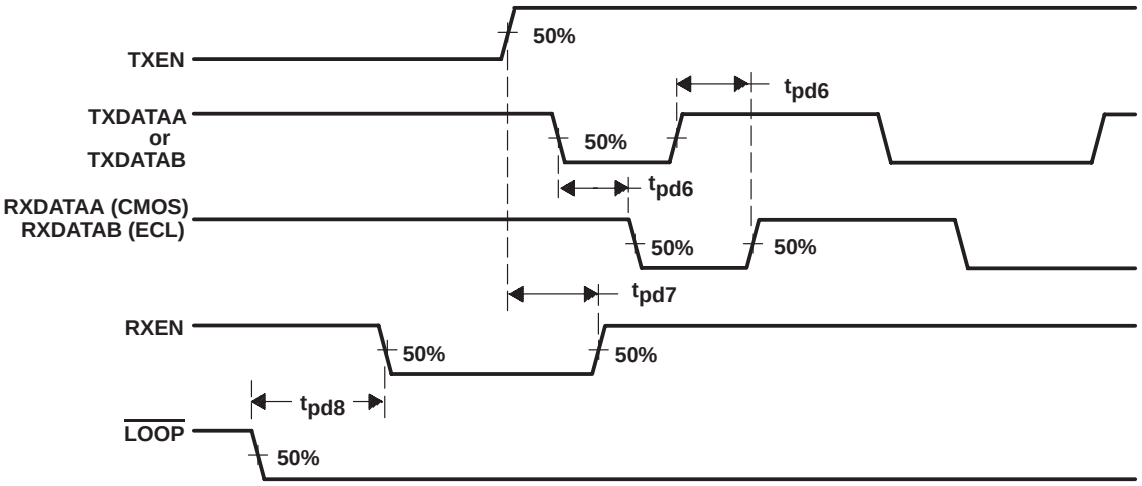


Figure 7. Propagation Delay Waveforms in Loop Mode

PARAMETER MEASUREMENT INFORMATION

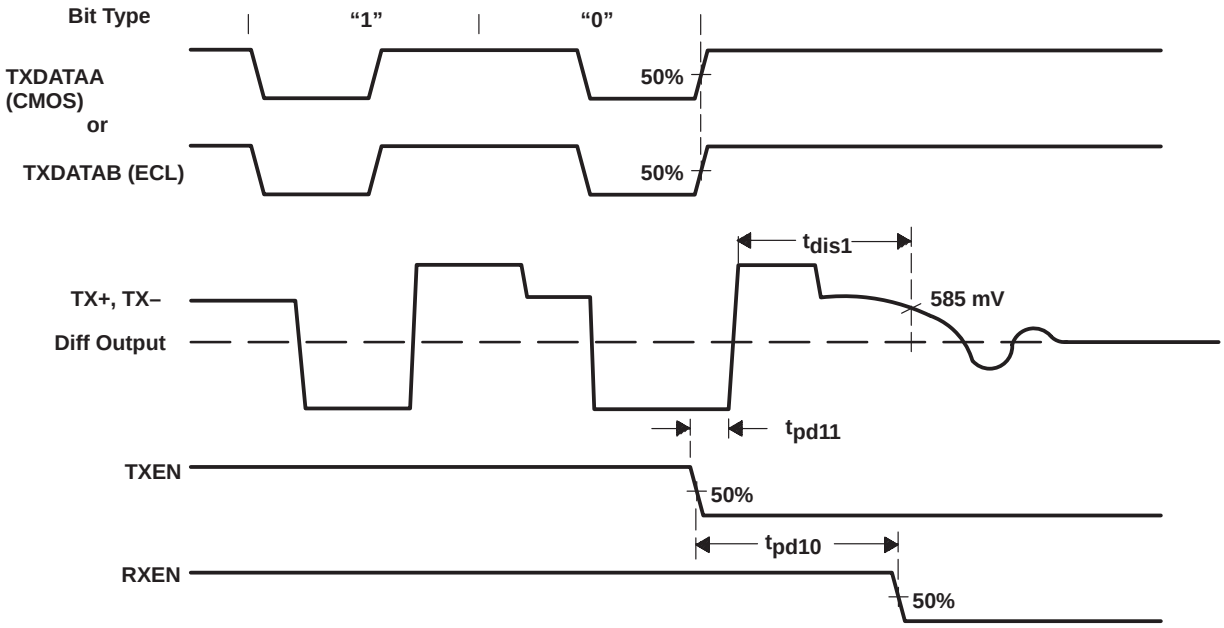


Figure 8. Driver Shutdown Waveforms

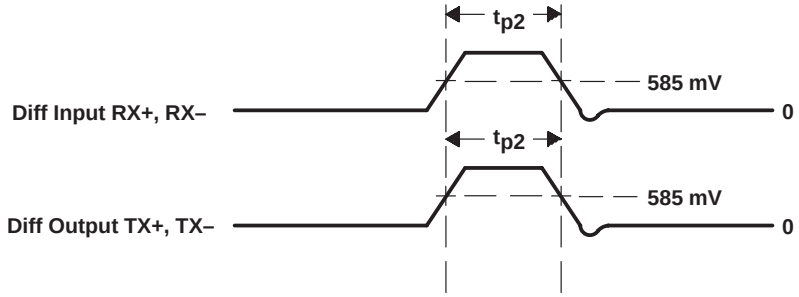


Figure 9. Link Beat Pulse Duration Waveform

PARAMETER MEASUREMENT INFORMATION

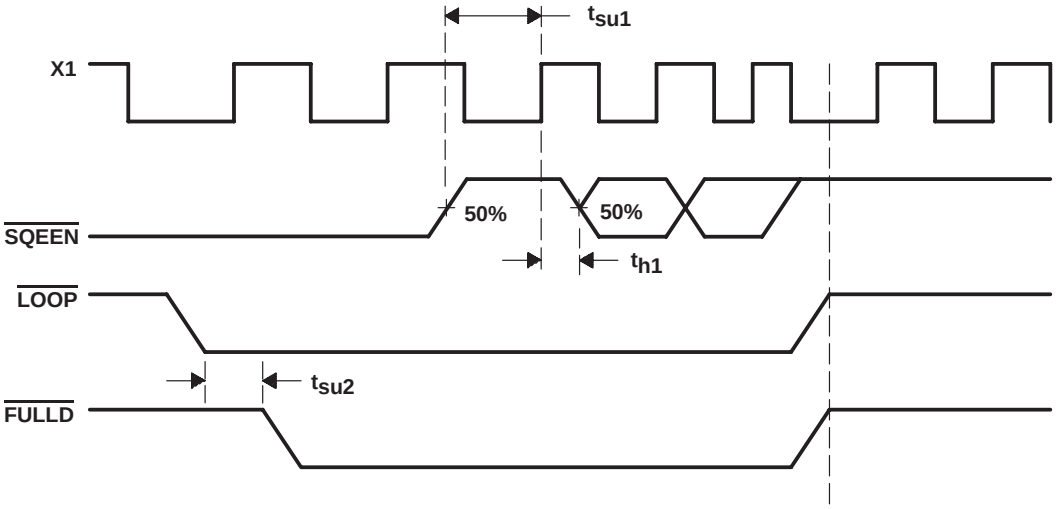


Figure 10. Setup and Hold Time Waveforms

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