

SN54LVTH373, SN74LVTH373 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS689H – MAY 1997 – REVISED OCTOBER 2003

- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Unregulated Battery Operation Down to 2.7 V
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

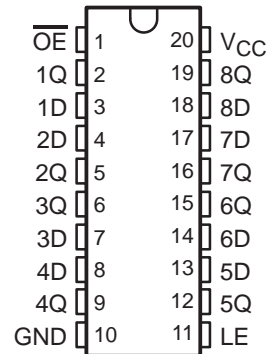
description/ordering information

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

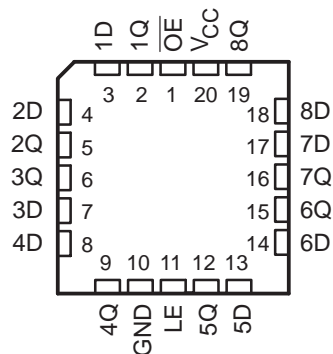
While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

SN54LVTH373 . . . J OR W PACKAGE
SN74LVTH373 . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LVTH373 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – DW	Tube	SN74LVTH373DW	LVTH373
		Tape and reel	SN74LVTH373DWR	
	SOP – NS	Tape and reel	SN74LVTH373NSR	LVTH373
	SSOP – DB	Tape and reel	SN74LVTH373DBR	LXH373
-55°C to 125°C	TSSOP – PW	Tube	SN74LVTH373PW	LXH373
		Tape and reel	SN74LVTH373PWR	
	CDIP – J	Tube	SNJ54LVTH373J	SNJ54LVTH373J
	CFP – W	Tube	SNJ54LVTH373W	SNJ54LVTH373W
	LCCC – FK	Tube	SNJ54LVTH373FK	SNJ54LVTH373FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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description/ordering information (continued)

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

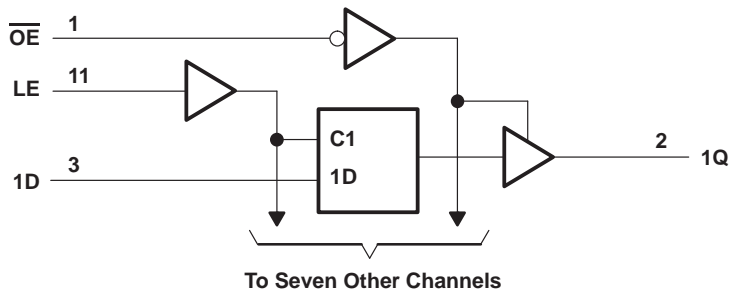
Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_{OL} : SN54LVTH373	96 mA
SN74LVTH373	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH373	48 mA
SN74LVTH373	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
DW package	58°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		SN54LVTH373		SN74LVTH373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTH373			SN74LVTH373			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2			-1.2			V	
V_{OH}	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V	
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4			2.4				
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2			2				
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$	0.2			0.2			V	
		$I_{OL} = 24\text{ mA}$	0.5			0.5				
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$	0.4			0.4				
		$I_{OL} = 32\text{ mA}$	0.5			0.5				
		$I_{OL} = 48\text{ mA}$	0.55			0.55				
		$I_{OL} = 64\text{ mA}$				0.55				
I_I	$V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$		10			10			μA	
	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1			± 1			
	Data inputs	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$		1			1		
			$V_I = 0$		-5			-5		
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$					± 100			μA	
$I_I(\text{hold})$	Data inputs	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	75			75			μA
			$V_I = 2\text{ V}$	-75			-75			
		$V_{CC} = 3.6\text{ V}\ddagger$, $V_I = 0\text{ to }3.6\text{ V}$					500 -750			
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$		5			5			μA	
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$		-5			-5			μA	
I_{OZPU}	$V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = \text{don't care}$		$\pm 100^*$			± 100			μA	
I_{OZPD}	$V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = \text{don't care}$		$\pm 100^*$			± 100			μA	
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19			mA
		Outputs low		5			5			
		Outputs disabled		0.19			0.19			
$\Delta I_{CC}\S$	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND		0.2			0.2			mA	
C_i	$V_I = 3\text{ V or }0$		3			3			pF	
C_o	$V_O = 3\text{ V or }0$		7			7			pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	SN54LVTH373				SN74LVTH373				UNIT
	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high				3	3	3	3	ns
t _{su}	Setup time, data before LE↓				1.1	0.4	1.1	0.4	ns
t _h	Hold time, data after LE↓				1.7	2	1.4	1.4	ns

switching characteristics over recommended free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH373				SN74LVTH373				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	D	Q	1.4	4.1	4.7		1.5	2.6	3.9	4.5		ns
t _{PHL}			1.4	4.1	4.7		1.5	2.6	3.9	4.5		
t _{PLH}	LE	Q	1.6	4.4	5.1		1.7	2.7	4.2	4.9		ns
t _{PHL}			1.6	4.4	5.1		1.7	2.7	4.2	4.9		
t _{PZH}	$\overline{\text{OE}}$	Q	1.2	5	6.1		1.3	3	4.8	5.9		ns
t _{PZL}			1.2	5	5.7		1.3	3	4.8	5.5		
t _{PHZ}	$\overline{\text{OE}}$	Q	1.6	5.5	5.7		1.9	3	4.6	4.9		ns
t _{PLZ}			0.8	4.8	4.9		1.9	3	4.5	4.6		

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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WITH 3-STATE OUTPUTS

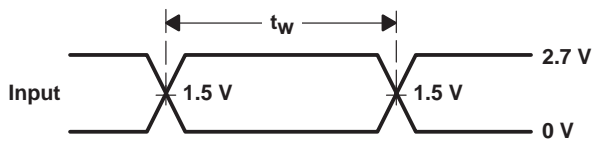
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PARAMETER MEASUREMENT INFORMATION

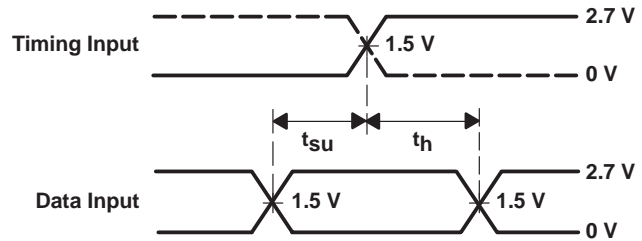


LOAD CIRCUIT

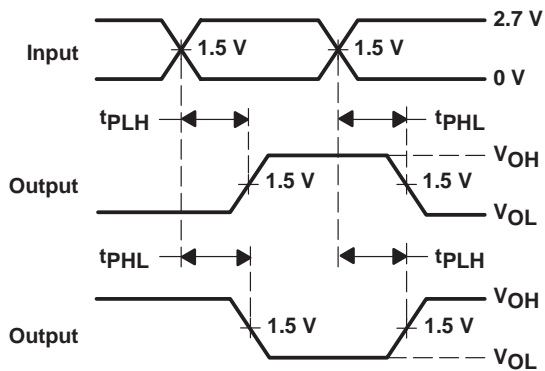
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



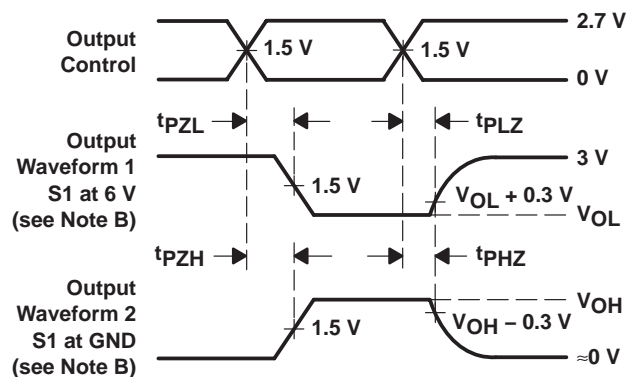
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

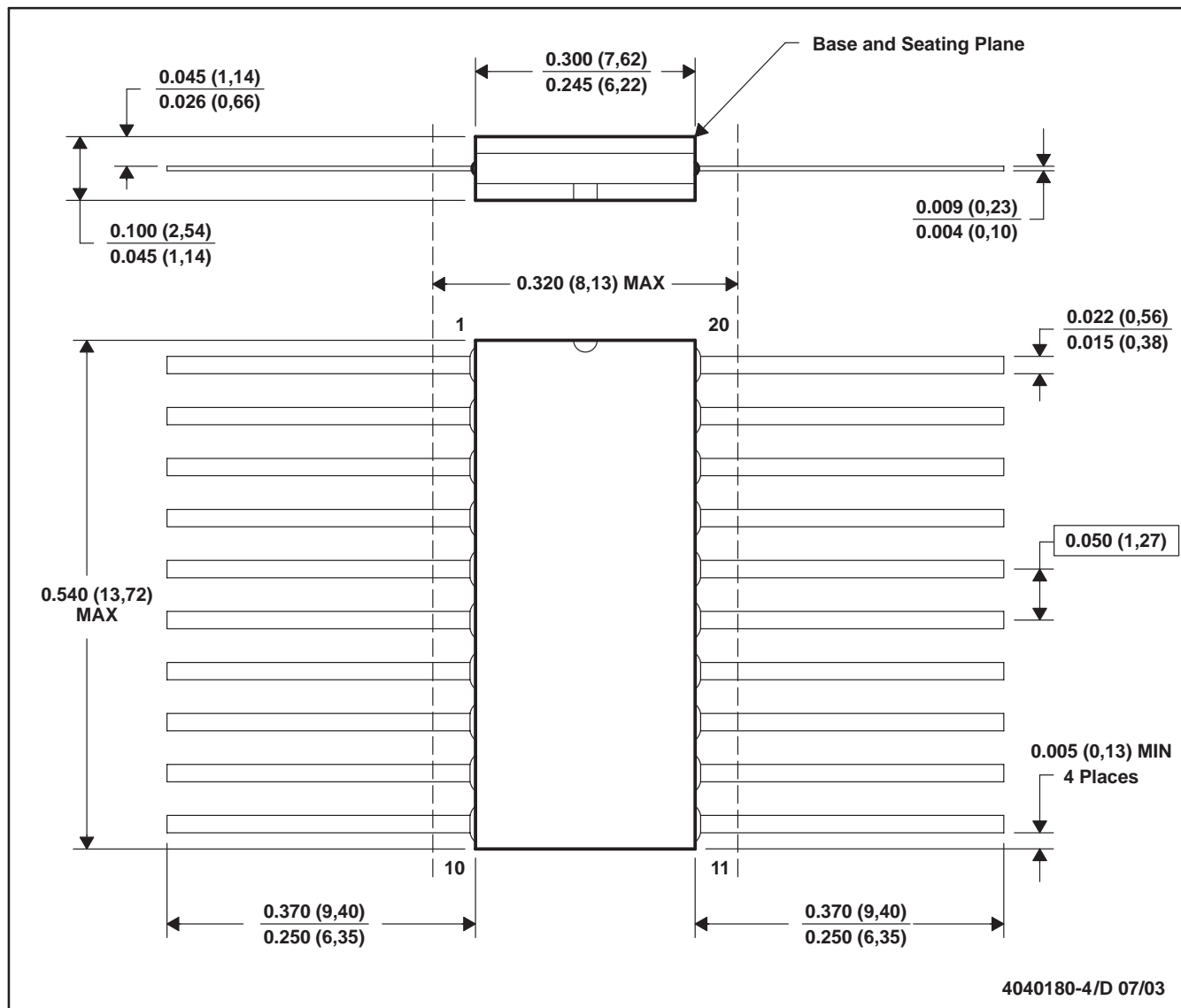


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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