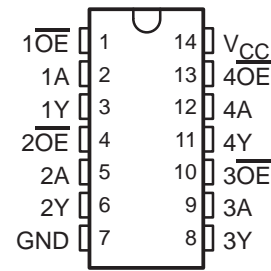# SN74LVT125
3.3-V ABT QUADRUPLE BUS BUFFER
WITH 3-STATE OUTPUTS

SCBS133F – MAY 1992 – REVISED OCTOBER 2003

- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

D, DB, NS, OR PW PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	14	V_{CC}
1A	2	13	4$\overline{OE}$
1Y	3	12	4A
2$\overline{OE}$	4	11	4Y
2A	5	10	3$\overline{OE}$
2Y	6	9	3A
GND	7	8	3Y

description/ordering information

This bus buffer is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN74LVT125 features independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable ($\overline{OE}$) input is high.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC – D	Tube	SN74LVT125D	LVT125
		Tape and reel	SN74LVT125DR	
	SOP – NS	Tape and reel	SN74LVT125NSR	LVT125
	SSOP – DB	Tape and reel	SN74LVT125DBR	LX125
	TSSOP – PW	Tube	SN74LVT125PW	LX125
		Tape and reel	SN74LVT125PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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TEXAS INSTRUMENTS

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FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O .... 128 mA
Current into any output in the high state, I_O (see Note 2) .... 64 mA
Input clamp current, I_{IK} (V_I < 0) .... −50 mA
Output clamp current, I_{OK} (V_O < 0) .... −50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package .... 86°C/W
　　　　　　　　　　　　　　　　　　　　　　 DB package .... 96°C/W
　　　　　　　　　　　　　　　　　　　　　　 NS package .... 76°C/W
　　　　　　　　　　　　　　　　　　　　　　 PW package .... 113°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
　functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
　implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES:　1.　The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
　　　　　2.　This current flows only when the output is in the high state and $V_O > V_{CC}$.
　　　　　3.　The package thermal impedance is calculated in accordance with JESD 51-7.

TEXAS INSTRUMENTS

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage			5.5	V
I_{OH}	High-level output current			−32	mA
I_{OL}	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = MIN to MAX[‡],	I_{OH} = −100 µA		V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = −8 mA		2.4			
	V_{CC} = 3 V	I_{OH} = −32 mA		2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2	V
		I_{OL} = 24 mA				0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4	
		I_{OL} = 32 mA				0.5	
		I_{OL} = 64 mA				0.55	
I_I	V_{CC} = 0 or MAX[‡],	V_I = 5.5 V				10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control inputs			±1	
		V_I = V_{CC}	Data inputs			1	
		V_I = 0				−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V				±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			µA
		V_I = 2 V		−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.19	mA
			Outputs low		4.5	7	
			Outputs disabled		0.12	0.19	
ΔI_{CC}[§]	V_{CC} = 3 V to 3.6 V,	One input at V_{CC} − 0.6 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	V_I = 3 V or 0					4	pF
C_o	V_O = 3 V or 0					8	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V $\pm$ 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.7	4		4.5	ns
t_{PHL}			1	2.9	3.9		4.9	
t_{PZH}	$\overline{OE}$	Y	1	3.4	4.7		6	ns
t_{PZL}			1.1	3.4	4.7		6.5	
t_{PHZ}	$\overline{OE}$	Y	1.8	3.7	5.1		5.7	ns
t_{PLZ}			1.3	2.6	4.5		4	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION
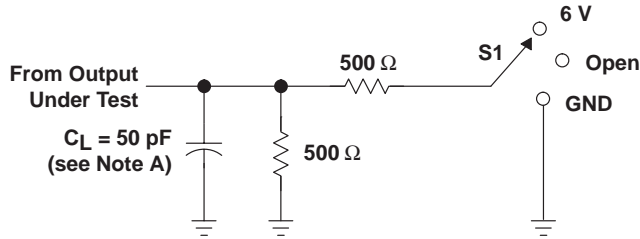
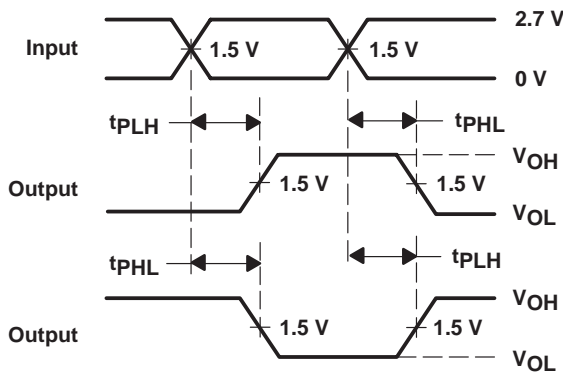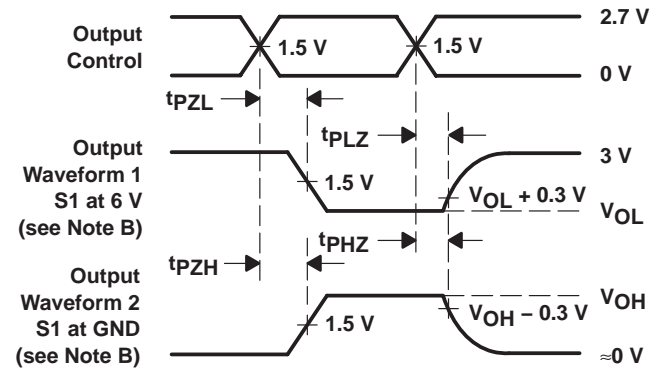| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT FOR OUTPUTS
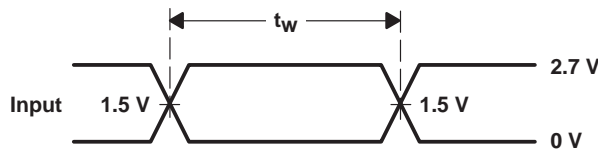
VOLTAGE WAVEFORMS
PULSE DURATION
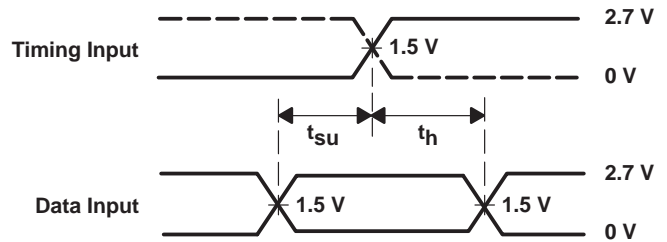
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

D (R−PDSO−G14)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1   7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/F   07/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−012 variation AB.

NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS **	14	16	20	24	28	30	38
DIM							
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
              B. This drawing is subject to change without notice.
              C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
              D. Falls within JEDEC MO-150

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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