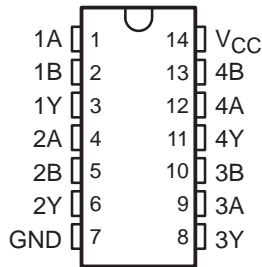


# SN54LV32A, SN74LV32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

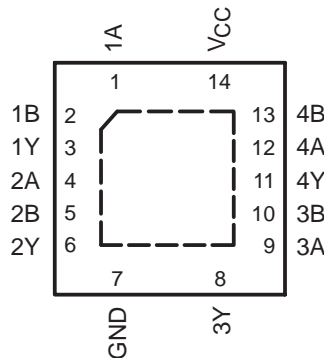
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- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 6.5 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

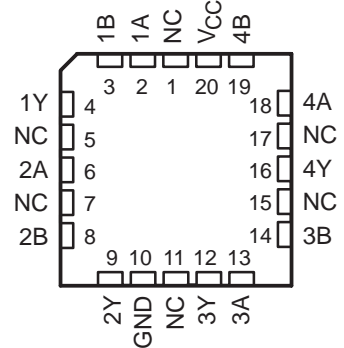
SN54LV32A . . . J OR W PACKAGE  
SN74LV32A . . . D, DB, DGV, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LV32A . . . RGY PACKAGE  
(TOP VIEW)



SN54LV32A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These quadruple 2-input positive-OR gates are designed for 2-V to 5.5-V  $V_{CC}$  operation.

The 'LV32A devices perform the Boolean function  $Y = A + B$  or  $Y = \overline{A} \cdot \overline{B}$  in positive logic.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV32ARGYR	LV32A
	SOIC – D	Tube of 50	SN74LV32AD	LV32A
		Reel of 2500	SN74LV32ADR	
	SOP – NS	Reel of 2000	SN74LV32ANSR	74LV32A
	SSOP – DB	Reel of 2000	SN74LV32ADBR	LV32A
	TSSOP – PW	Tube of 90	SN74LV32APW	LV32A
		Reel of 2000	SN74LV32APWR	
Reel of 250		SN74LV32APWT		
TVSOP – DGV	Reel of 2000	SN74LV32ADGVR	LV32A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV32AJ	SNJ54LV32AJ
	CFP – W	Tube of 150	SNJ54LV32AW	SNJ54LV32AW
	LCCC – FK	Tube of 55	SNJ54LV32AFK	SNJ54LV32AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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# SN54LV32A, SN74LV32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

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## description/ordering information (continued)

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

## logic diagram, each gate (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±25 mA
Continuous current through $V_{CC}$ or GND .....	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package .....	86°C/W
(see Note 3): DB package .....	96°C/W
(see Note 3): DGV package .....	127°C/W
(see Note 3): NS package .....	76°C/W
(see Note 3): PW package .....	113°C/W
(see Note 4): RGY package .....	47°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 5.5 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.  
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

# SN54LV32A, SN74LV32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

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## recommended operating conditions (see Note 5)

		SN54LV32A		SN74LV32A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2	5.5	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5	0.5	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		$V_{CC} \times 0.3$	$V_{CC} \times 0.3$	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		$V_{CC} \times 0.3$	$V_{CC} \times 0.3$	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		$V_{CC} \times 0.3$	$V_{CC} \times 0.3$	
$V_I$	Input voltage	0	5.5	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$		-50	-50	$\mu\text{A}$
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		-2	-2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		-6	-6	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		-12	-12	
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$		50	50	$\mu\text{A}$
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		2	2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		6	6	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		12	12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		200	200	ns/V
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		100	100	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		20	20	
$T_A$	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$

NOTE 5: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	SN54LV32A			SN74LV32A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	2 V to 5.5 V	$V_{CC}-0.1$			$V_{CC}-0.1$			V
	$I_{OH} = -2\ \text{mA}$	2.3 V	2			2			
	$I_{OH} = -6\ \text{mA}$	3 V	2.48			2.48			
	$I_{OH} = -12\ \text{mA}$	4.5 V	3.8			3.8			
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	2 V to 5.5 V					0.1		V
	$I_{OL} = 2\ \text{mA}$	2.3 V					0.4		
	$I_{OL} = 6\ \text{mA}$	3 V					0.44		
	$I_{OL} = 12\ \text{mA}$	4.5 V					0.55		
$I_I$	$V_I = 5.5\text{ V or GND}$	0 to 5.5 V			$\pm 1$			$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}\text{ or GND, } I_O = 0$	5.5 V			20			20	$\mu\text{A}$
$I_{off}$	$V_I\text{ or }V_O = 0\text{ to }5.5\text{ V}$	0			5			5	$\mu\text{A}$
$C_i$	$V_I = V_{CC}\text{ or GND}$	3.3 V		3.3		3.3			pF
		5 V		3.3		3.3			

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# SN54LV32A, SN74LV32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

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switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV32A		SN74LV32A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	$C_L = 15\text{ pF}$	7.1*	12.8*	1*	16*	1	15	ns	
			$C_L = 50\text{ pF}$	9.6	16.2	1	20	1	19		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV32A		SN74LV32A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	$C_L = 15\text{ pF}$	5*	7.9*	1*	9.5*	1	9.5	ns	
			$C_L = 50\text{ pF}$	6.9	11.4	1	13	1	13		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV32A		SN74LV32A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	$C_L = 15\text{ pF}$	3.6*	5.5*	1*	6.5*	1	6.5	ns	
			$C_L = 50\text{ pF}$	4.9	7.5	1	8.5	1	8.5		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 6)

PARAMETER		SN74LV32A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.1	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		3.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.99		V

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics,  $T_A = 25^\circ\text{C}$

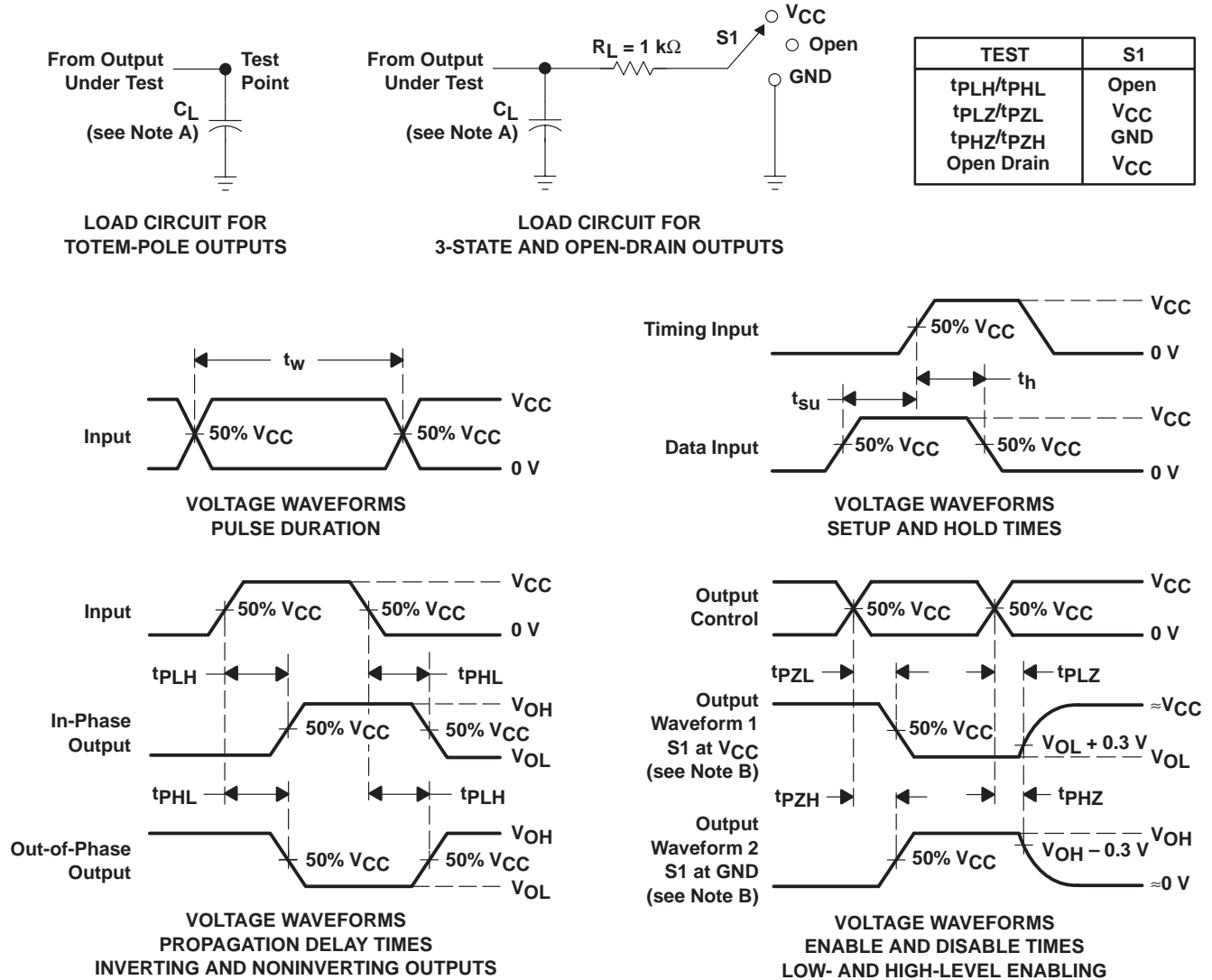
PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	9.5	pF
			5 V	11.5	

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

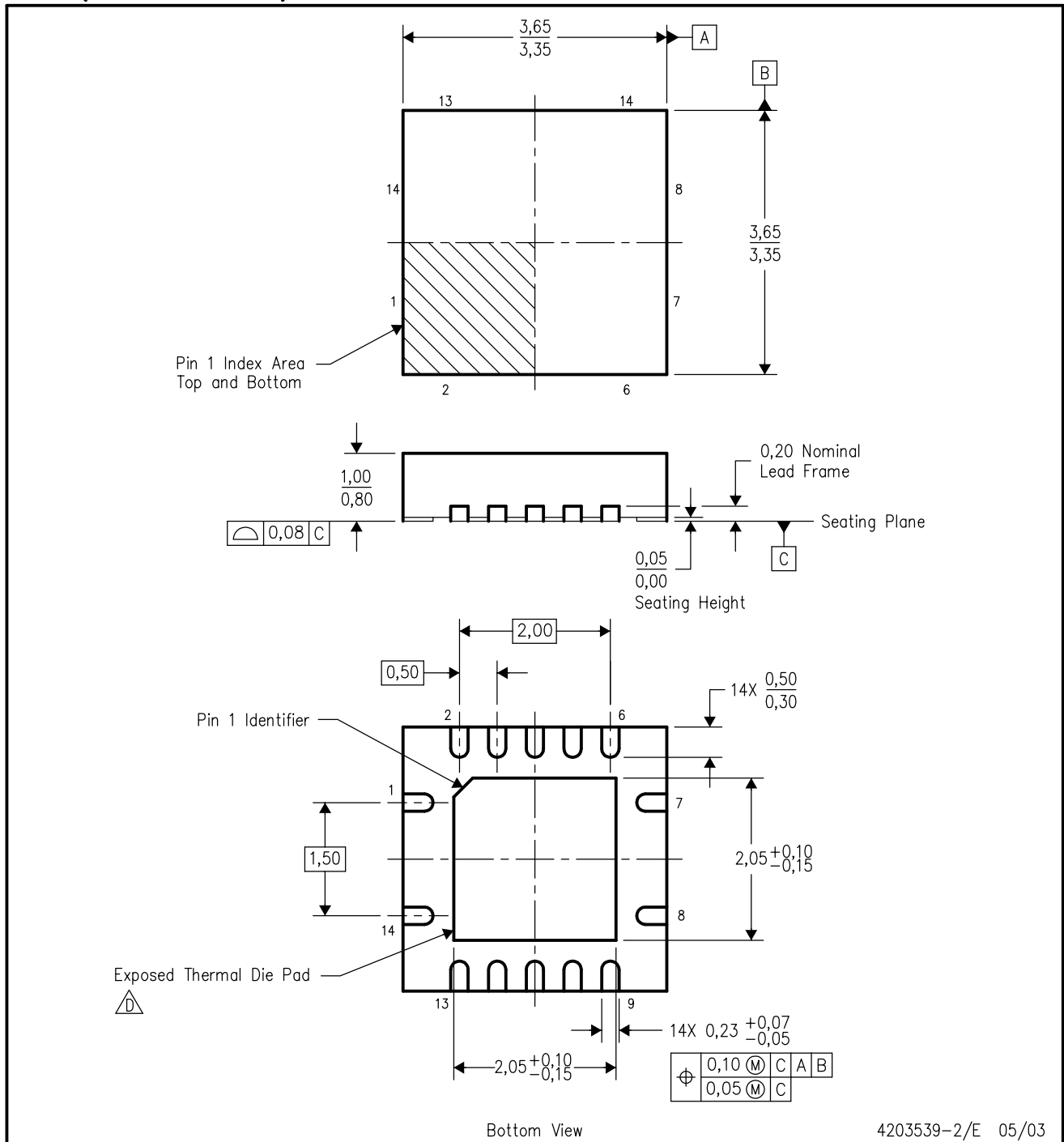
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



4203539-2/E 05/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
  - E. Package complies to JEDEC MO-241 variation BA.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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