

SN74CBTLV16292

LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS055K – MARCH 1998 – REVISED OCTOBER 2003

- Member of the Texas Instruments Widebus™ Family
- 4-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Make-Before-Break Feature
- Internal 500-Ω Pulldown Resistors to Ground
- Latch-Up Performance Exceeds 250 mA Per JESD 17

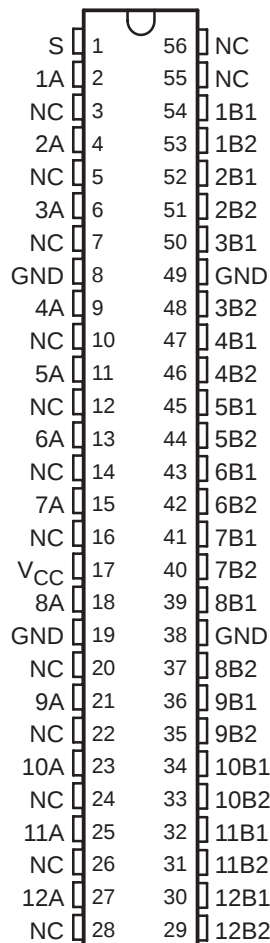
description/ordering information

The SN74CBTLV16292 is a 12-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1, and R_{INT} is connected to port B2. When S is high, port A is connected to port B2, and R_{INT} is connected to port B1.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBTLV16292DL	CBTLV16292
		Tape and reel	SN74CBTLV16292DLR	
	TSSOP – DGG	Tape and reel	SN74CBTLV16292GR	CBTLV16292
	TVSOP – DGV	Tape and reel	SN74CBTLV16292VR	CN292

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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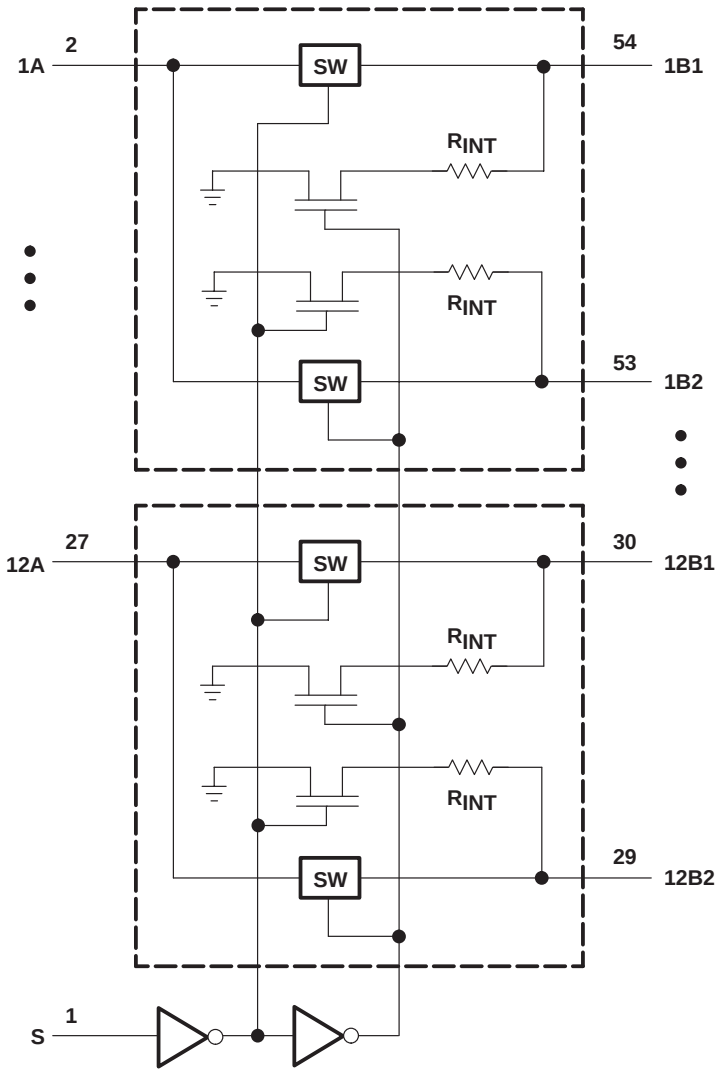
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FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R _{INT} = B2 port
H	A port = B2 port R _{INT} = B1 port

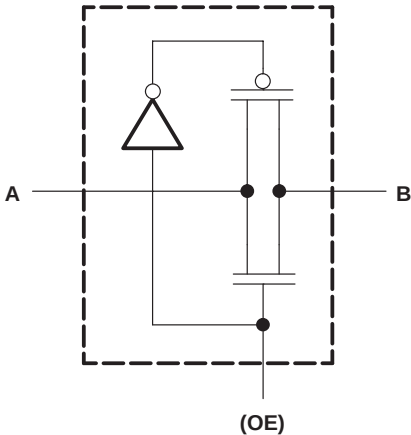
logic diagram (positive logic)



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simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}		–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		–0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		
V_{IL}	Low-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP [†]	MAX	UNIT	
V _{IK}		V _{CC} = 3 V,	I _I = −18 mA				−1.2	V	
I _I		V _{CC} = 3.6 V,	V _I = V _{CC} or GND				±1	μA	
I _{off}		V _{CC} = 0,	V _I or V _O = 0 to 3.6 V				10	μA	
I _{CC}		V _{CC} = 3.6 V,	I _O = 0, V _I = V _{CC} or GND				10	μA	
ΔI _{CC} [‡]	Control input	V _{CC} = 3.6 V,	One input at 3 V, Other inputs at V _{CC} or GND				300	μA	
C _i	Control input	V _I = 3.3 V or 0					3.5	pF	
C _{io}	A or B port	V _O = 3.3 V or 0					22.5	pF	
r _{on} [§]		V _{CC} = 2.3 V, TYP at V _{CC} = 2.5 V	V _I = 0	I _I = 64 mA			5	8	Ω
				I _I = 24 mA			5	8	
			V _I = 1.7 V, I _I = 15 mA				11	40	
		V _{CC} = 3 V	V _I = 0	I _I = 64 mA			3	7	
				I _I = 24 mA			3	7	
			V _I = 2.4 V, I _I = 15 mA				7	15	

[†] All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^\text{¶}$	A or B	B or A		0.15		0.25	ns
$t_{pd}^\#$	S	A	2.5	7.1	2.5	6.7	ns
t_{en}	S	B	1	5.6	1	5	ns
t_{dis}	S	B	1	5	1	4.5	ns

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

[#] This propagation delay was measured by observing the change of voltage on the A output introduced by static levels equal to 3 V or 0 for $3.3\text{ V} \pm 0.3\text{ V}$ or V_{CC} or 0 for $2.5\text{ V} \pm 0.2\text{ V}$ on B1 and B2 to achieve the desired transition.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	DESCRIPTION	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
$t_{mbb}^\text{ }$	Make-before-break time	0	2	0	2	ns

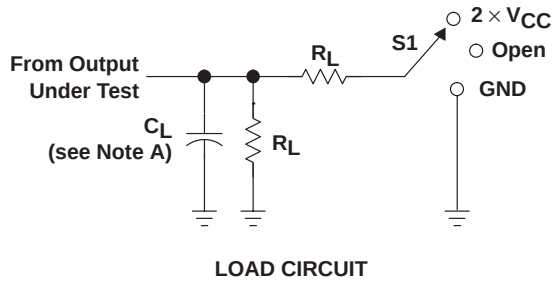
^{||} The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.

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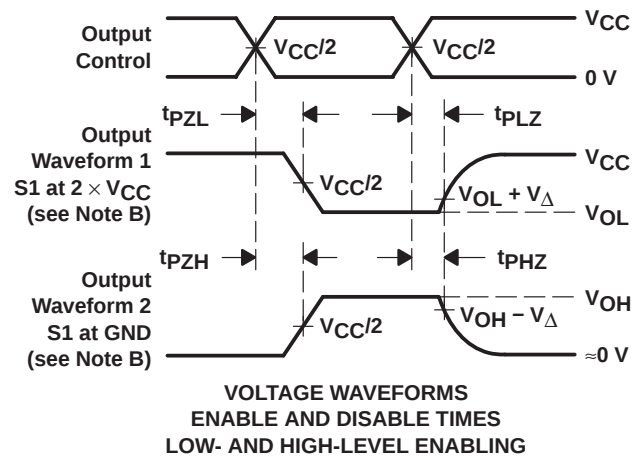
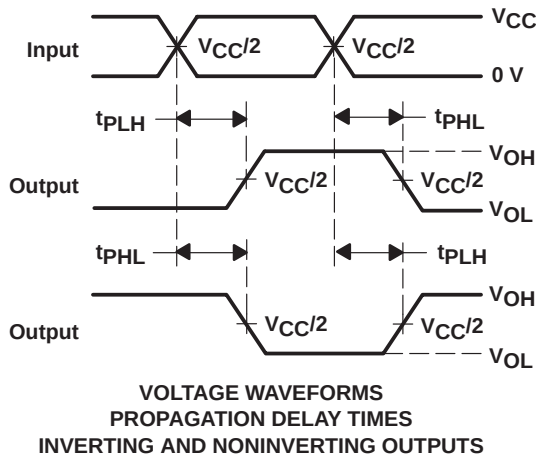
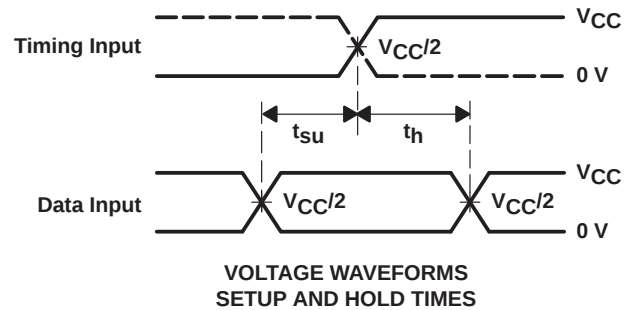
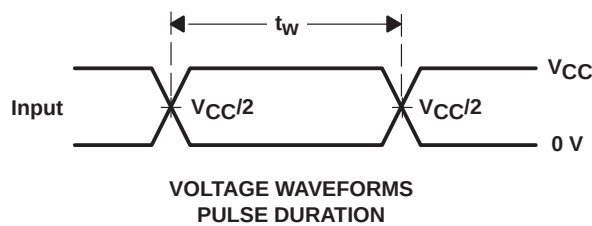
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	50 pF	500 Ω	0.3 V



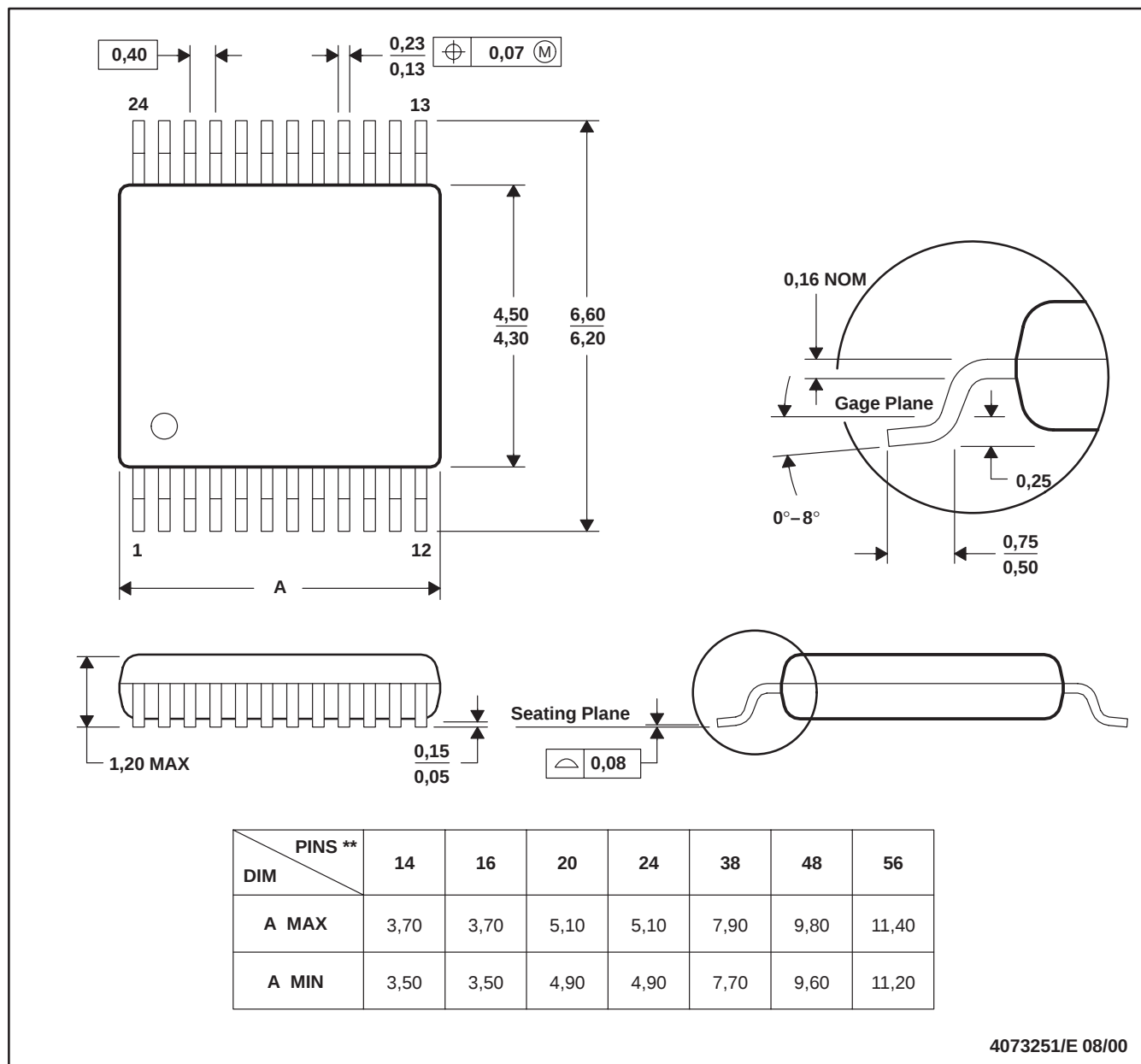
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

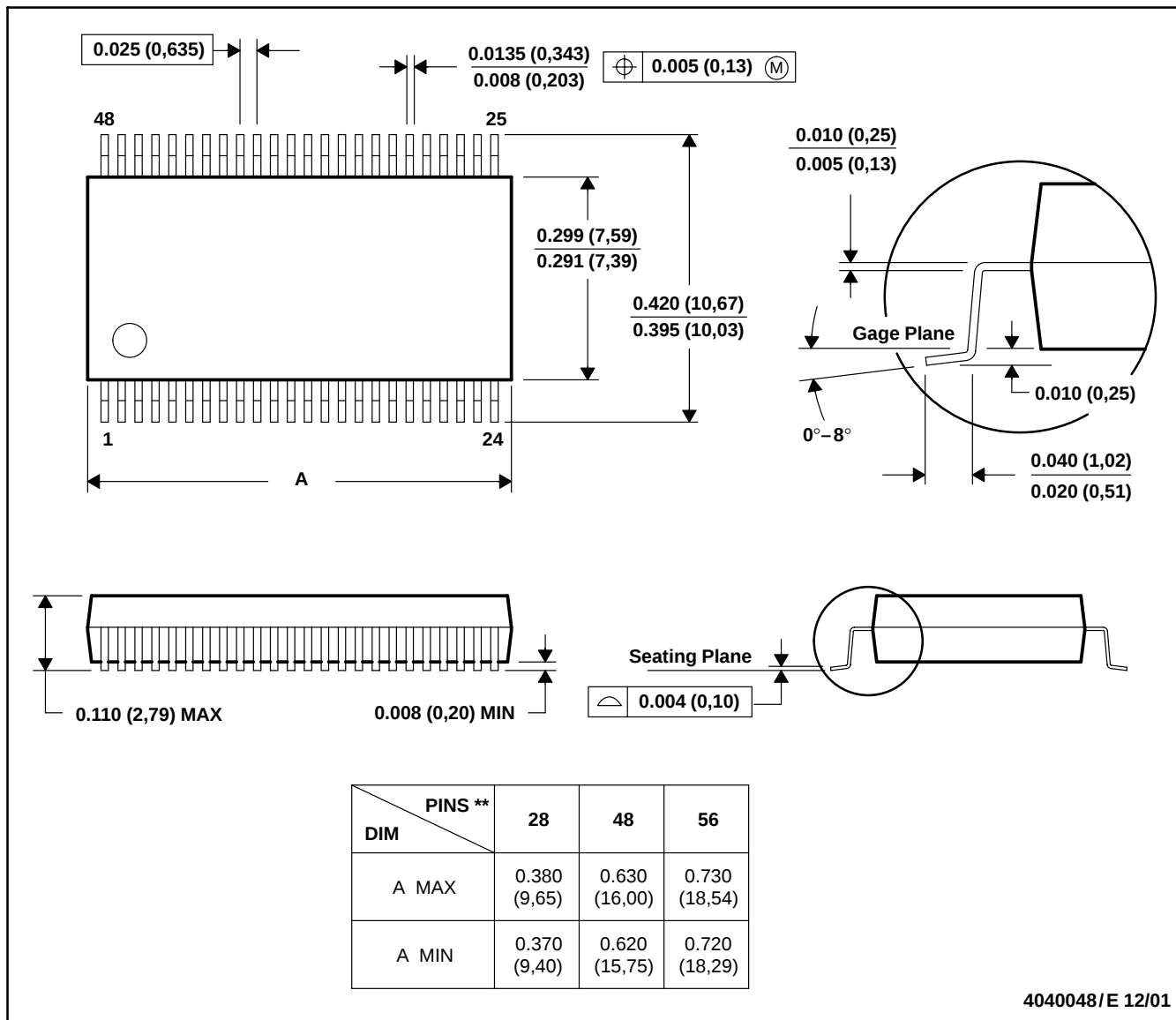


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

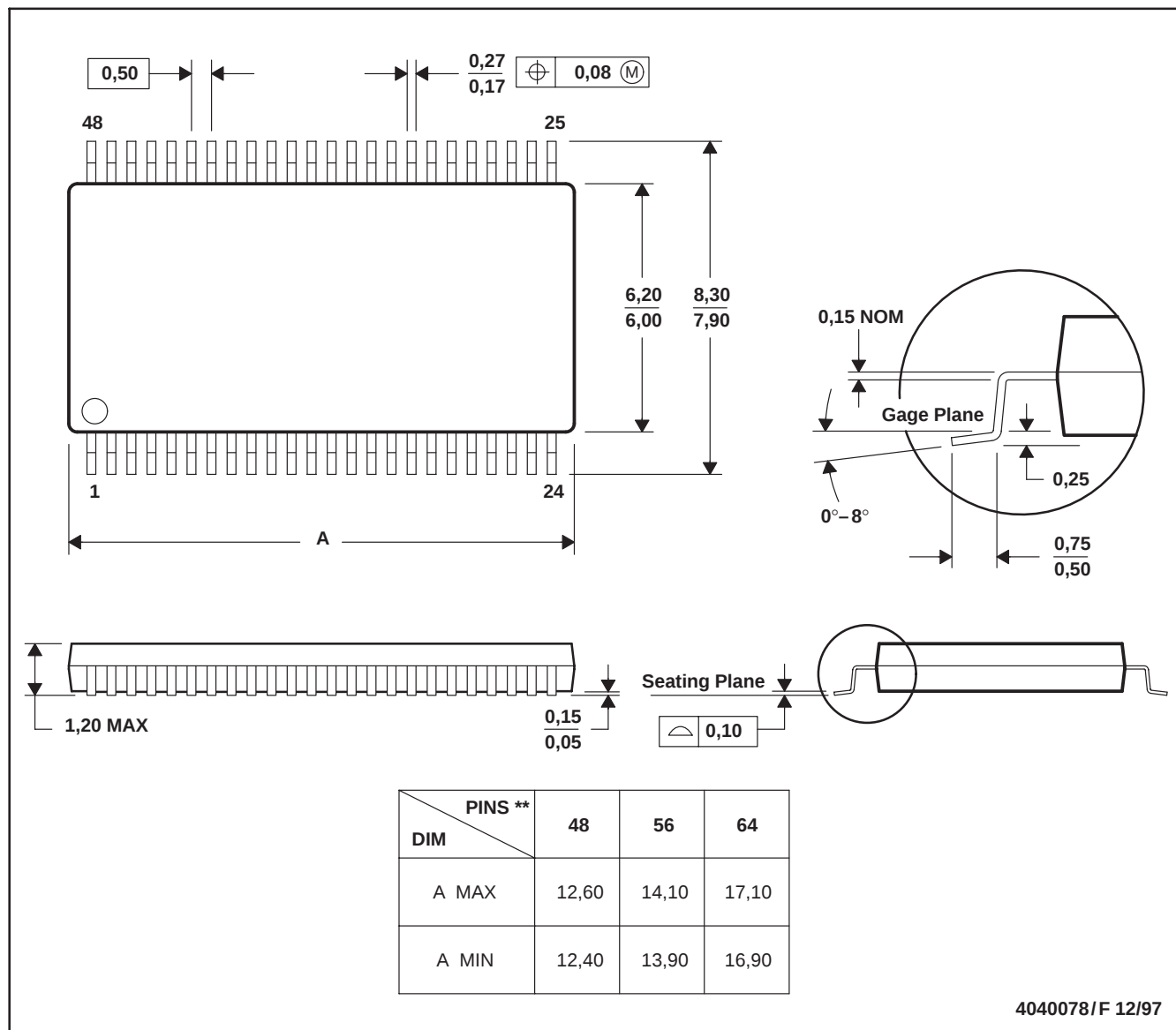


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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