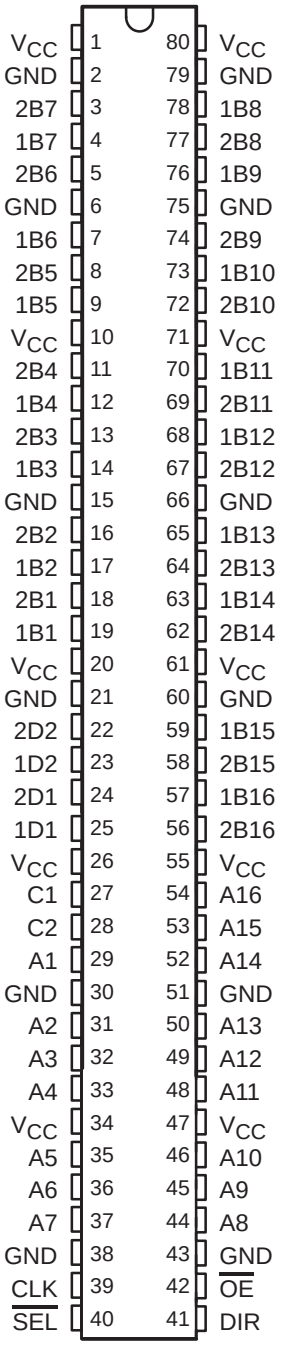
- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Sub-Micron Process**
- **A-Port Outputs Have Equivalent 50-Ω Series Resistors and B-Port Outputs Have Equivalent 20-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Thin Very Small-Outline Package**

NOTE: For order entry:
The DBB package is abbreviated to G.

For tape and reel:
The DBBR package is abbreviated to GR.

DBB PACKAGE
(TOP VIEW)



description

The SN74ALVCHG162280 is a 16-bit to 32-bit registered bus exchanger. This device is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3-V) V_{CC} operation.

The device provides synchronous data exchange between the two ports, A and B. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input. For data transfer in the B-to-A direction, the select ($\overline{SEL}$) input selects 1B or 2B data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output-enable ($\overline{OE}$) and direction-control (DIR) inputs. DIR is registered to synchronize the bus direction changes with the clock.

description (continued)

Two mask bits are provided for both data bytes. The data (D) outputs are controlled by $\overline{OE}$.

The A-port N-channel output transistors are sized at 450 μm and the P-channel output transistors are sized at 700 μm. All A-port outputs have equivalent 50-Ω series resistors. The B-port N-channel output transistors are sized at 225 μm, and the P-channel output transistors are sized at 560 μm. All B-port outputs have equivalent 20-Ω series resistors.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The switching characteristics are based on 25-pF (A port) and 80-pF (B and D ports) loads, but are tested with the standard 50-pF load.

The SN74ALVCHG162280 is characterized for operation from 0°C to 70°C.

Function Tables

A-TO-B STORAGE
($\overline{OE}$ = L, DIR = H)

INPUTS			OUTPUTS	
$\overline{SEL}$	CLK	A	1B	2B
H	X	X	$1B_0$†	$2B_0$†
L	↑	L	L‡	L
L	↑	H	H‡	H

† Output level before indicated steady-state input conditions were established
‡ Two CLK edges are needed to propagate the data.

B-TO-A STORAGE
($\overline{OE}$ = L, DIR = L)

INPUTS				OUTPUT A
CLK	$\overline{SEL}$	1B	2B	
↑	H	X	L	L§
↑	H	X	H	H§
↑	L	L	X	L
↑	L	H	X	H

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when $\overline{SEL}$ is low and propagates to the second register when $\overline{SEL}$ is high.

C-TO-D STORAGE
($\overline{OE}$ = L)

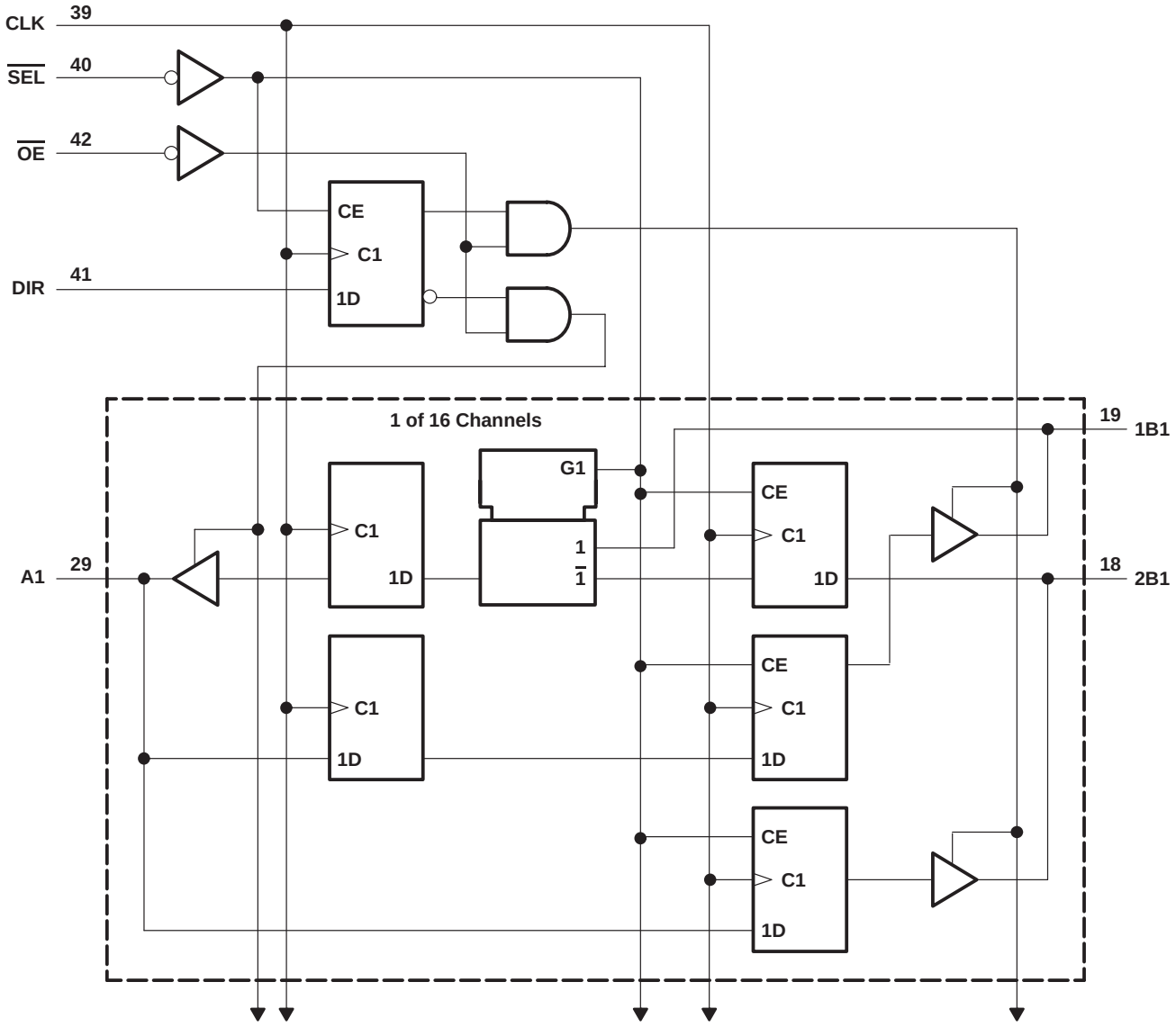
INPUTS			OUTPUTS	
$\overline{SEL}$	CLK	C	1D	2D
H	X	X	$1D_0$†	$2D_0$†
L	↑	L	L‡	L
L	↑	H	H‡	H

† Output level before indicated steady-state input conditions were established
‡ Two CLK edges are needed to propagate the data.

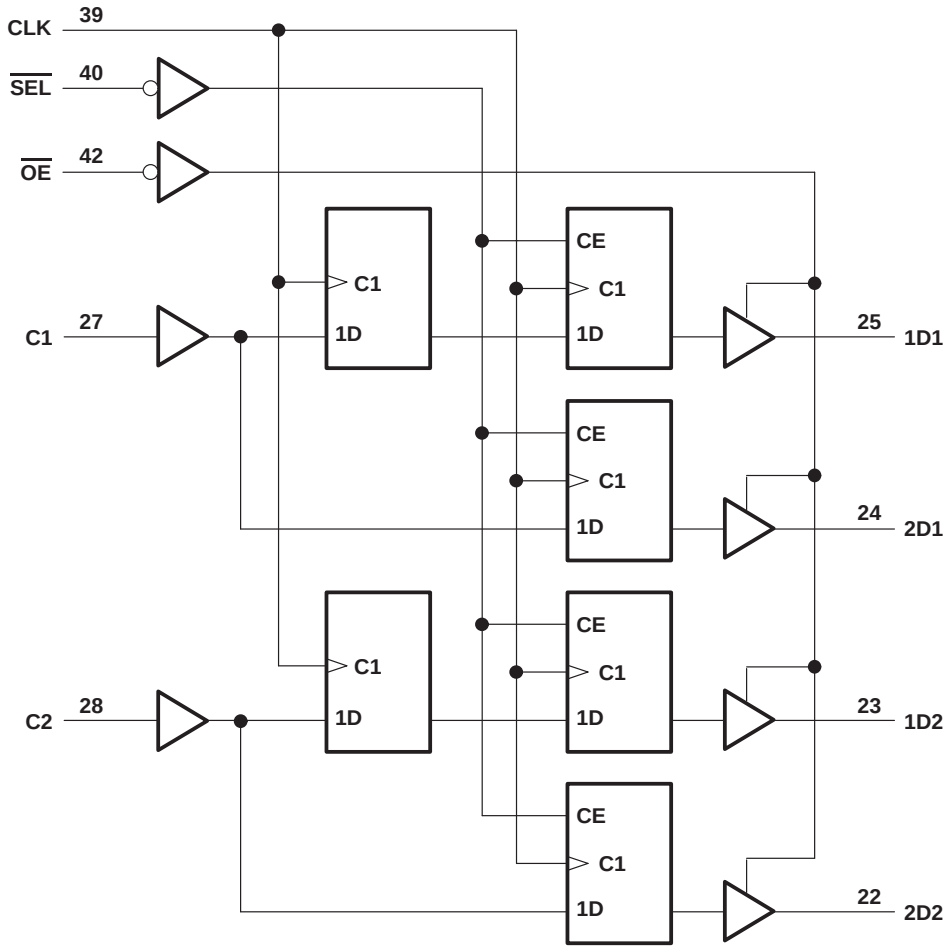
OUTPUT ENABLE

INPUTS			OUTPUTS		
CLK	$\overline{OE}$	DIR	A	1B, 2B	1D, 2D
↑	H	X	Z	Z	Z
↑	L	H	Z	Active	Active
↑	L	L	Active	Z	Active

logic diagram, A and B ports (positive logic)



logic diagram, C and D ports (positive logic)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I: Except I/O ports (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
I/O ports (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Continuous output current, I_O . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 106°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			3	3.6	V
V_{IH}	High-level input voltage		V_{CC} = 3 V to 3.6 V	2		V
V_{IL}	Low-level input voltage		V_{CC} = 3 V to 3.6 V		0.8	V
V_I	Input voltage			0	V_{CC}	V
V_O	Output voltage			0	V_{CC}	V
I_{OH}	High-level output current	A to B	V_{CC} = 3 V		8	mA
		B to A	V_{CC} = 3 V		6	
I_{OL}	Low-level output current	A to B	V_{CC} = 3 V		8	mA
		B to A	V_{CC} = 3 V		6	
$\Delta t/\Delta v$	Input transition rise or fall rate				10	ns/V
T_A	Operating free-air temperature			0	70	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		3 V to 3.6 V	V_{CC}–0.2			V
	A to B	I_{OH} = –8 mA		3 V	2			
	B to A	I_{OH} = –6 mA		3 V	2			
V_{OL}		I_{OL} = 100 μA		3 V to 3.6 V			0.2	V
	A to B	I_{OL} = 8 mA		3 V			0.8	
	B to A	I_{OL} = 6 mA		3 V			0.8	
I_I		V_I = V_{CC} or GND		3.6 V			±5	μA
$I_{I(hold)}$		V_I = 0.8 V		3 V	75			μA
		V_I = 2 V		3 V	–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	μA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		4		pF
	C port					8.5		
C_o	D port	V_O = V_{CC} or GND		3.3 V		7		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		8.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

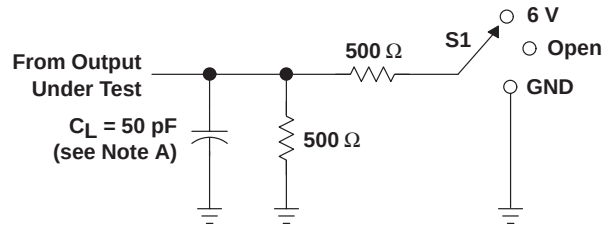
timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	
f_{clock}	Clock frequency			160	MHz
t_w	Pulse duration, CLK high or low		2.3		ns
t_{su}	Setup time, high or low	A data before CLK↑	1.4		ns
		B data before CLK↑	2		
		C data before CLK↑	1.3		
		DIR before CLK↑	2		
		$\overline{SEL}$ before CLK↑	2		
t_h	Hold time, high or low	A data after CLK↑	0.3		ns
		B data after CLK↑	0.3		
		C data after CLK↑	0.3		
		DIR after CLK↑	0.3		
		$\overline{SEL}$ after CLK↑	0.3		

switching characteristics over recommended operating free-air temperature range, C_L = 25 pF (A port), 80 pF (B and D ports) (unless otherwise noted) (see Figure 1)

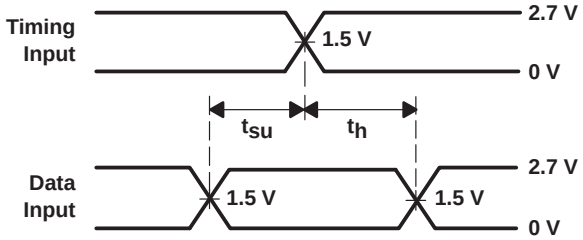
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	
f_{max}			160		MHz
t_{pd}	CLK	A	1.5	5	ns
		B	1.5	7.4	
		D	1.5	7.2	
t_{en}	CLK	A	1.5	6.2	ns
		B	1.5	9.4	
	$\overline{OE}$	A	1.5	6	
		B	1.5	9.5	
		D	1.5	7.9	
t_{dis}	CLK	A	1.5	6.4	ns
		B	1.5	7.8	
	$\overline{OE}$	A	1.5	5	
		B	1.5	7.6	
		D	1.5	6.7	

PARAMETER MEASUREMENT INFORMATION

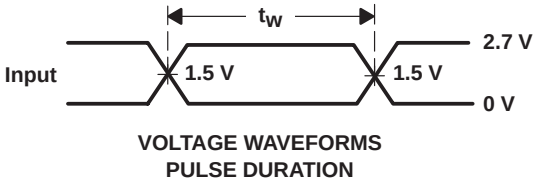


LOAD CIRCUIT

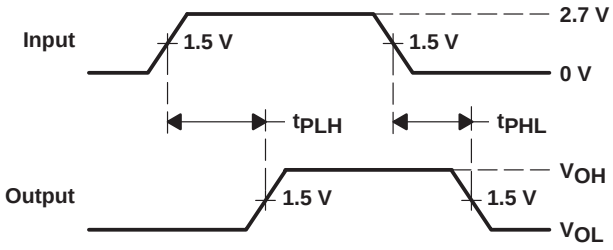
TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



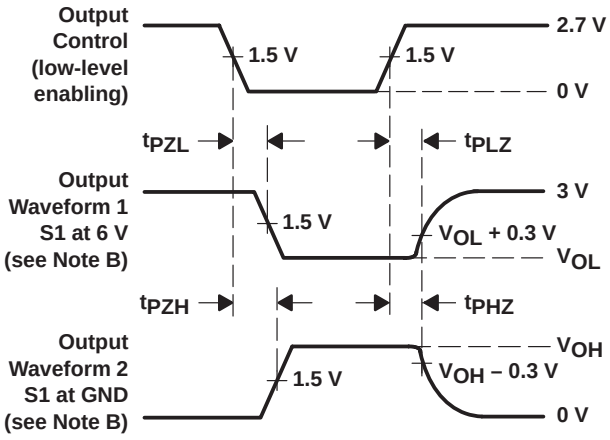
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

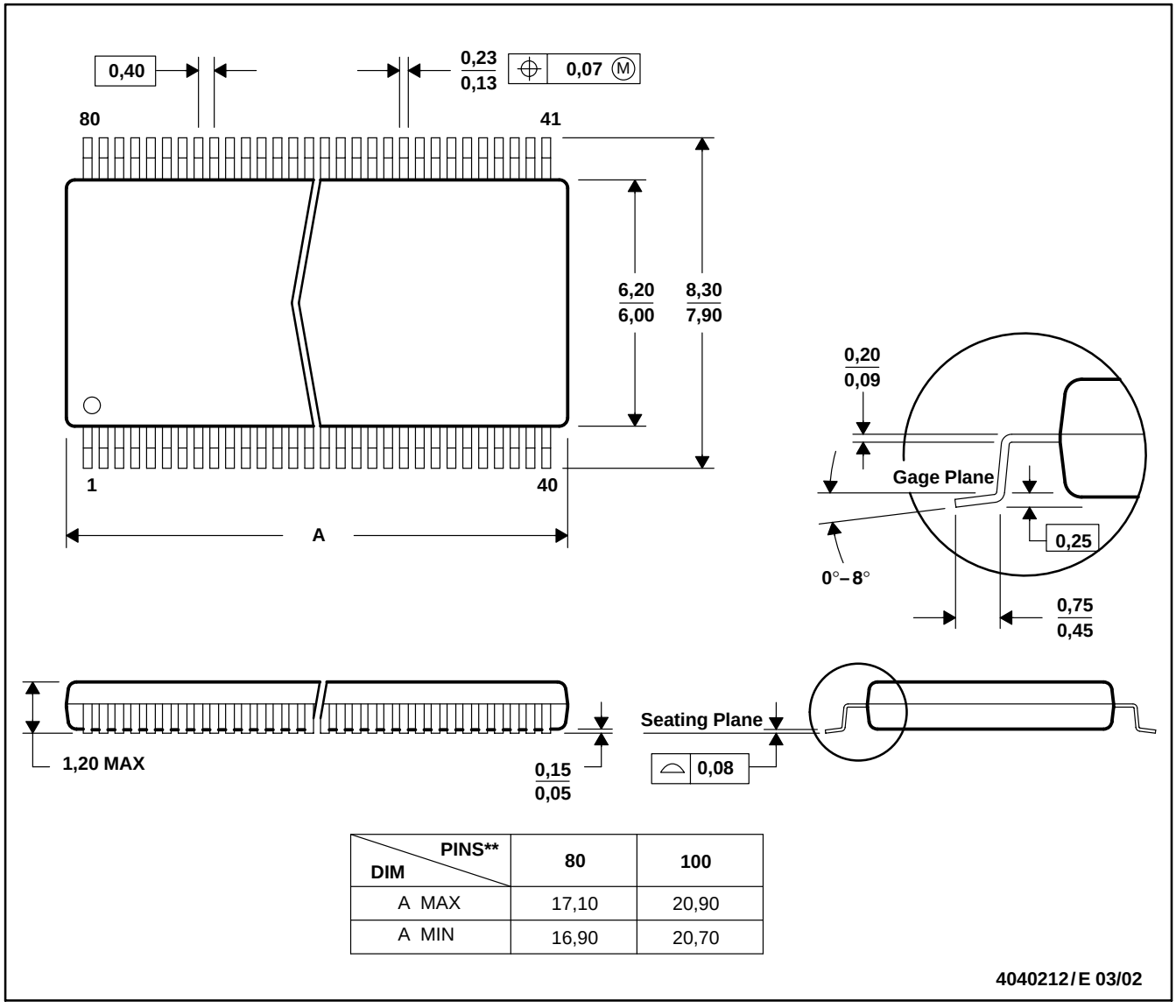
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The output is measured with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

MTSS005D – JANUARY 1995 – REVISED MARCH 2002

DBB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

80 PINS SHOWN



DIM \ PINS**	80	100
A MAX	17,10	20,90
A MIN	16,90	20,70

4040212/E 03/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC : 80 Pin – MO-153 Variation FF
100 Pin – MO-194 Variation BB

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265