SCBS678C - SEPTEMBER 1996 - REVISED JANUARY 2001

- Member of Texas Instruments' Widebus™ **Family**
- State-of-the-Art Advanced Low-Voltage BiCMOS (ALB) Technology Design for 3.3-V Operation
- Schottky Diodes on All Inputs to Eliminate **Overshoot and Undershoot**
- **Industry Standard '16245 Pinout**
- Distributed V_{CC} and GND Pins Minimize **High-Speed Switching Noise**
- Flow-Through Architecture Optimizes PCB Layout

description

The SN74ALB16245 is a 16-bit transceiver designed for high-speed, low-voltage (3.3-V) V_{CC} operation. This device is intended to replace the conventional transceiver in any speed-critical path. The small propagation delay is achieved using a unity-gain amplifier on the input and feedback resistors from input to output, which allows the output to track the input with a small offset voltage.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated.

DGG, DGV, OR DL PACKAGE (TOP VIEW)

		_			
1DIR [1	U	48	h	1 <u>OE</u>
1B1				6	1A1
1B2			46	6	1A2
GND [4		45	þ	GND
1B3 [5		44	þ	1A3
1B4			43		1A4
v _{cc} [42		V_{CC}
1B5			41	_	1A5
1B6			40	_	1A6
GND [10			_	GND
1B7	11		38		1A7
1B8	12		37	р	1A8
2B1	13		36	р	2A1
2B2 [14		35	0	2A2
GND[15		34	D	GND
2B3 [16		33	р	2A3
2B4 [17		32	0	2A4
v _{cc} [18		31		V_{CC}
2B5 [19		30	0	2A5
2B6 [20		29	р	2A6
GND[21		28		GND
2B7	22		27		2A7
2B8 [23		26	β	2A8
2DIR	24		25		2 <mark>OE</mark>
	1				

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SSOP – DL	Tube	SN74ALB16245DL	ALB16245
-40°C to 85°C	330F - DL	Tape and reel	SN74ALB16245DLR	ALD 10245
	TSSOP – DGG	Tape and reel	SN74ALB16245DGGR	ALB16245
	TVSOP - DGV	Tape and reel	SN74ALB16245DGVR	AV245

[†]Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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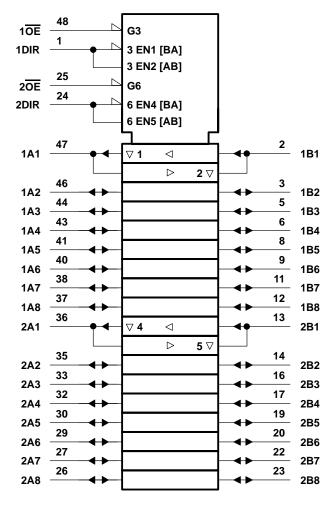
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FUNCTION TABLE (each 8-bit section)

INP	UTS	OPERATION				
OE	DIR	OPERATION				
L	L	B data to A bus				
L	Н	A data to B bus				
Н	Χ	Isolation				

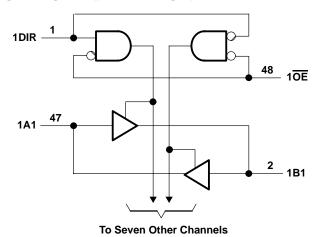
logic symbol†

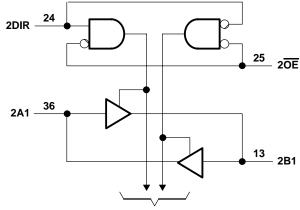


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)





To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see N	lote 1)
I/O ports (see Notes 1 a	and 2)0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_{ C } < 0)$	
Output clamp current, IOK (VO < 0 or VO > VCC)) ±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	DGG package 70°C/W
	DGV package 58°C/W
	DL package 63°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	V _{CC} Supply voltage		3	3.6	V
I _{OH} [‡] High-level output current				-25	mA
l _{OL} ‡	I _{OL} [‡] Low-level output current			25	mA
Δt/Δν	Input transition rise or fall rate Outputs enal	oled		5	ns/V
TA	Operating free-air temperature		-40	85	°C

[‡] See Figures 1 and 2 for typical I/O ranges.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
\/u.c	A or B ports	Voc - 2 V	I _I = 18 mA	I _I = 18 mA I _I = -18 mA		3.7	V _{CC} +1.2	V
VIK	A or B ports	ACC = 3 A	I _I = -18 mA			-0.9	-1.2	V
	Control inputs	$V_{CC} = 3.6 \text{ V},$	$V_I = V_{CC}$ or GND				±10	μΑ
		VCC = 3.6 V	VV	OE low		0.4	0.6	mA
l _l	A or P porto		$A^{I} = A^{CC}$	OE high			25	μΑ
	A or B ports		V _I = 0	OE low		-0.7	-1	mA
				OE high			-60	μΑ
lozh	$V_{CC} = 3.6 \text{ V}, \qquad V_{O} = 3 \text{ V}$			0.7	20	μΑ		
lozL		$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V			-0.2	- 50	μΑ
I _{CC} /bi	uffer	$V_{CC} = 3.6 \text{ V},$	I _O = 0,	$V_I = V_{CC}$ or GND		3.7	5.6	mA
ICCZ	$V_{CC} = 3.6 \text{ V}$, Control inputs = V_{CC} or GND				0.8	mA		
∆lcc [‡]	:	$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$	$CC = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND				600	μΑ
Ci		V _I = 3 V or 0				3.5		pF
C _{io}		V _O = 3 V or 0				7.5		pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM	ТО	V_{CC} = 3.3 V \pm 0.3 V			UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP [†]	MAX	UNII
^t pd	A or B	B or A	0.6	1.3	2	ns
t _{en}	ŌĒ	A or B	1.5	3.2	6	ns
^t dis	ŌĒ	A or B	1.8	2.8	4.2	ns

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

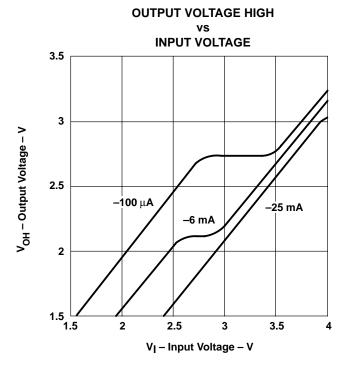


Figure 1. $V_{\mbox{OH}}$ Over Recommended Free-Air Temperature Range

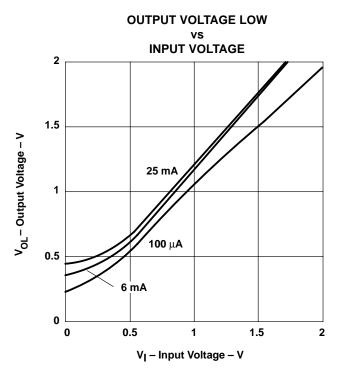
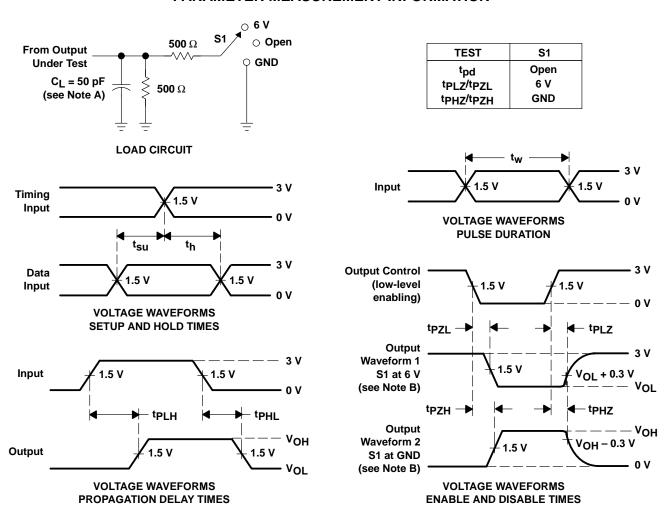


Figure 2. $V_{\mbox{\scriptsize OL}}$ Over Recommended Free-Air Temperature Range



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



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