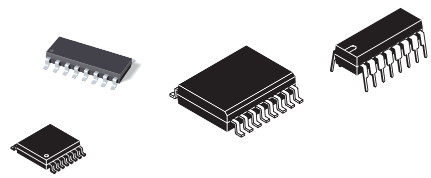


SLUS272C − FEBRUARY 2000 − REVISED JUNE 2003

LOW−POWER, DUAL-OUTPUT, CURRENT-MODE PWM CONTROLLER

FEATURES

- **BiCMOS Version of UC3846 Family**
- **1.4-mA Maximum Operating Current**
- **100-µA Maximum Startup Current**
- **±0.5-A Peak Output Current**
- **125-ns Circuit Delay**
- **Easier Parallelability**
- **Improved Benefits of Current Mode Control**

DESCRIPTION

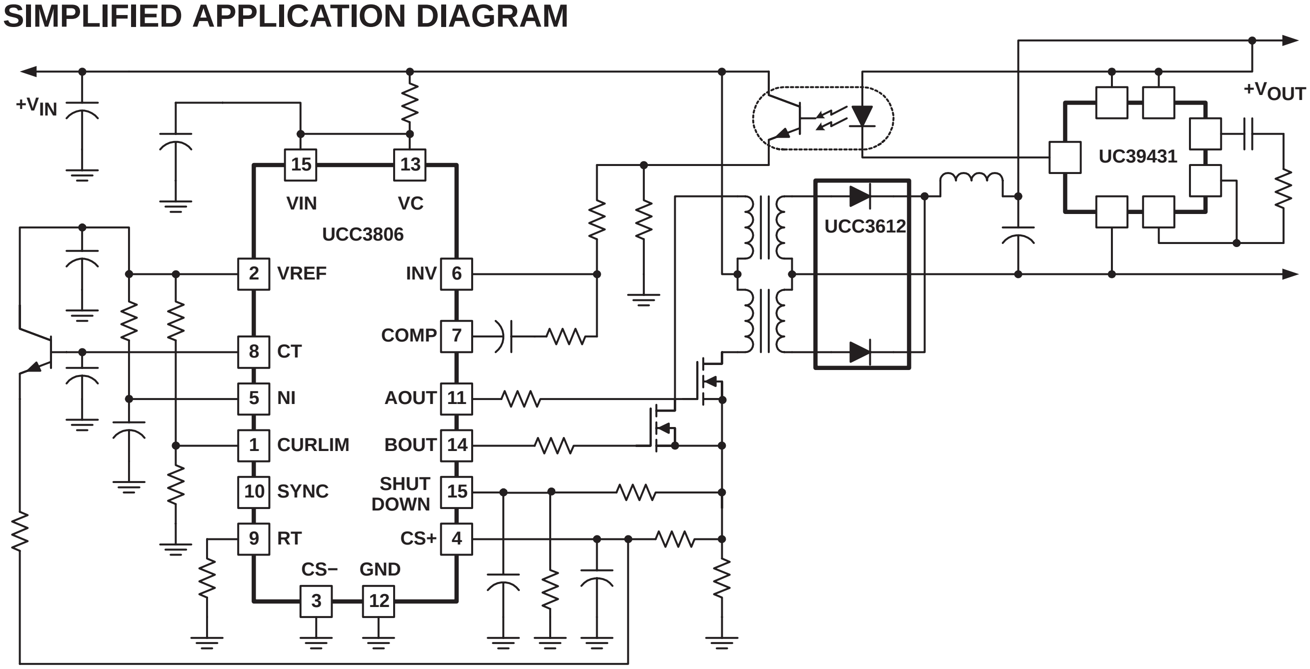
The UCC3806 family of BiCMOS PWM controllers offers exceptionally improved performance with a familiar architecture. With the same block diagram and pinout of the popular UC3846 series, the UCC3806 line features increased switching frequency capability while greatly reducing the bias current used within the device. With a typical startup current of 50 µA and a well defined voltage threshold for turn-on, these devices are favored for applications ranging from off-line power supplies to battery operated portable equipment. Dual high-current, MOSFET driving outputs and a fast current sense loop further enhance device versatility.

All the benefits of current mode control including simpler loop closing, voltage feed-forward, parallelability with current sharing, pulse-by-pulse current limiting, and push/pull symmetry correction are readily achievable with the UCC3806 series.

These devices are available in multiple package options for both through-hole and surface mount applications; and in commercial, industrial, and military temperature ranges.

The UCC3806 is specified for operation from −55°C to 125°C, the UCC2806 is specified for operation from −40°C to 85°C, and the UCC3806 is specified for operation from 0°C to 70°C.

SIMPLIFIED APPLICATION DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UCx806	UNIT
Supply voltage, V_{IN}	VIN, low impedance	15	V
Supply current, I_{IN}	VIN, high impedance	25	mA
Output supply voltage	VC	18	V
Output current	Continuous source or sink	± 200	mA
	Gate drive	± 500	
	SYNC	± 30	
	COMP	± 10 to −(self-limiting)	
Analog input voltage range	CS−, CS+, NI, INV, SHUTDOWN	−0.3 to (V_{IN} + 0.3)	V
Storage temperature, T_{stg}		−65 to 150	°C
Operating temperature, T_J		−55 to 150	°C
Lead temperature, T_{sol}, 1,6 mm (1/16 inch) from case for 10 seconds		300	°C

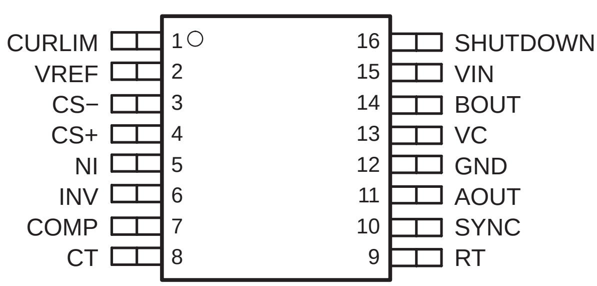
(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal.

RECOMMENDED OPERATING CONDITIONS

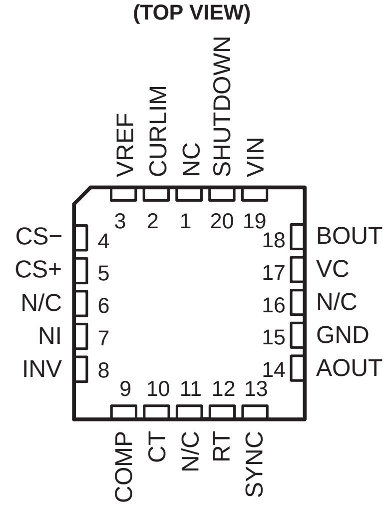
		MIN	NOM	MAX	UNIT
Input voltage, V_{IN}		8.0		14.5	V
Operating junction temperature, T_J	UCC1806	−55		125	°C
	UCC2806	−40		85	
	UCC3806	0		70	

PACKAGE DESCRIPTION

D, DW, J, M, N OR PW PACKAGE
(TOP VIEW)



Q OR L PACKAGE
(TOP VIEW)



N/C − No connection

ORDERING INFORMATION

PACKAGED DEVICES				$T_A = T_J$		
DESIGNATOR	TYPE	OPTION	QUANTITY	− 55°C to 125°C	− 40°C to 85°C	0°C to 70°C
D	SOIC−16	Tube	40	–	UCC2806D	–
		Reeled	2,500	–	UCC2806DTR	–
DW	SOICW−16	Tube	40	–	UCC2806DW	UCC3806DW
		Reeled	2,000	–	UCC2806DWTR	UCC3806DWTR
J	CDIP−16	Tube	25	UCC1806J	UCC2806J	UCC3806J
L	CLCC−20	Tube	55	UCC1806L	–	–
M	SSOP−16	Reeled	2,500	–	UCC2806MTR	–
N	PDIP−16	Tube	25	–	UCC2806N	UCC3806N
PW	TSSOP−16	Tube	90	–	UCC2806PW	UCC3806PW
		Reeled	2,000	–	UCC2806PWTR	UCC3806PWTR
Q	PLCC−20	Tube	46	–	UCC2806Q	UCC3806Q
		Reeled	1,000	–	UCC2806QTR	UCC3806QTR

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, R_T = 33 kΩ, C_T = 330 pF, C_{BYPASS} on V_{REF} = 0.01 µF, −55°C < T_A < 125°C for the UCC1806, −40°C < T_A < 85°C for the UCC2806, 0°C < T_A < 70°C for the UCC3806, and T_A = T_J (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE							
V_{REF}	Supply, UVLO, turn-on	UCC1806 UCC2806		5.02	5.10	5.17	V
		UCC3806		5.00	5.10	5.20	V
	Load regulation		0.2 mA ≤ I_{OUT} ≤ 5 mA		3	25	mV
	Total output variation (1)(2)		Line, load, temperature	−150		150	mV
	Output noise voltage (2)		10 Hz ≤ f_{OSC} ≤ 10 kHz, T_J = 25°C		70		µV
	Long term stability (2)		T_A = 125°C, 1000 hours		5	25	mV
	Output short circuit			−10		−30	mA
OSCILLATOR							
	Initial accuracy		T_J = 25°C	42	47	52	kHz
	Temperature stability (2)		T(min) ≤ T_A ≤ T(max)		2%		
	Amplitude				2.35		V
t_{DELAY}	Delay-to-output time, SYNC	UCC1806 UCC2806	V_{CT} = 0 V, V_{RT} = V_{REF} 0.8 V ≤ V_{SYNC} ≤ 2.0 V		50	125	ns
		UCC3806	V_{CT} = 0 V, V_{RT} = V_{REF} 0.8 V ≤ V_{SYNC} ≤ 2.0 V		50	100	ns

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, R_T = 33 kΩ, C_T = 330 pF, C_{BYPASS} on V_{REF} = 0.01 µF, −55°C < T_A < 125°C for the UCC1806, −40°C < T_A < 85°C for the UCC2806, 0°C < T_A < 70°C for the UCC3806, and T_A = T_J (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR (continued)							
I_{DCHG}	Discharge current		T_J = 25°C, V_{CT} = 2.0 V		2		mA
V_{OL}	Low-level output voltage, SYNC		I_{OUT} = 1 mA			0.4	V
V_{OH}	High-level output voltage, SYNC		I_{OUT} = −4 mA	2.4			
V_{IL}	Low-level input voltage, SYNC		V_{CT} = 0 V, V_{RT} = V_{REF}			0.8	
V_{IH}	High-level input voltage, SYNC		V_{CT} = 0 V, V_{RT} = V_{REF}	2.0			
I_{SYNC}	Input current, SYNC			−1		1	µA
ERROR AMPLIFIER							
	Input offset voltage	UCC1806 UCC2806				5	mV
		UCC3806				10	
I_{BIAS}	Input bias current					−1	µA
I_{OFSET}	Input offset current					500	nA
CMR	Common mode range(1)			0		V_{IN}−2	V
A_{VOL}	Open loop gain		1 V ≤ V_{OUT} ≤ 4 V	80	100		dB
GBW	bandwidth			1			MHz
I_{COMP_SINK}	Output sink current		V_{ID} < −20 mV, V_{COMP} = 1 V	1			mA
I_{COMP_SRC}	Output source current		V_{ID} < 20 mV, V_{COMP} = 3 V	−80	−120		µA
V_{COMP_L}	Low-level output voltage		V_{ID} = −50 mV			0.5	V
V_{COMP_H}	High-level output voltage		V_{ID} = −50 mV	4.5			
CURRENT SENSE AMPLIFIER							
A	Amplifier gain(3)(4)		V_{CS-} = 0 V, V_{CURLIM} = V_{REF}	2.75	3.00	3.35	V/V
	Maximum differential input signal (V_{CS+} − V_{CS-})		V_{CURLIM} = V_{NI} = V_{REF}, V_{INV} = 0V	1.1			V
	Input offset voltage	UCC1806 UCC2806	V_{CURLIM} = 0.5 V, V_{COMP} = OPEN		10	30	µA
		UCC3806	V_{CURLIM} = 0.5 V, V_{COMP} = OPEN		10	50	mV
CMRR	Common mode rejection ratio		0 V ≤ V_{CM} ≤ (V_{IN} − 3.5 V)	60			dB
PSRR	Power supply rejection ratio			56			dB
I_{BIAS}	Input bias current (3)		V_{CURLIM} = 0.5 V, V_{COMP} = OPEN			−1	µA
	Input offset current (3)		V_{CURLIM} = 0.5 V, V_{COMP} = OPEN			1	µA
	Delay-to-output time (5)		V_{NI} = V_{REF}, V_{INV} = 0 V, V_{CURLIM} = 2.75 V, (V_{CS+} − V_{CS-}) = 0 V to 1.5 V step		125	175	ns
CURRENT LIMIT ADJUST							
	Current limit offset		V_{CS-} = V_{CS+} = 0 V, V_{COMP} = OPEN	0.4	0.5	0.6	V
I_{BIAS}	Input bias current					1	µA
	Minimum latching current			300	200		
	Maximum non-latching current				200	80	

(1) Line range = 10 V to 15 V, load range = 0.2 mA to 5 mA
(2) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, R_T = 33 kΩ, C_T = 330 pF, C_{BYPASS} on V_{REF} = 0.01 µF, −55°C to 125°C for the UCC1806, −40°C < T_A < 85°C for the UCC2806, 0°C < T_A < 70°C for the UCC3806, and T_A = T_J (unless otherwise noted)

SHUTDOWN TERMINAL							
	Threshold voltage	UCC1806 UCC2806		0.94	1.00	1.06	V
		UCC3806		0.9	1.0	1.1	
	Input voltage range			0		V_{IN}	
t_{DLY}	Delay-to-output time		0 V ≤ $V_{SHUTDOWN}$ ≤ 1.3 V		75	150	ns
OUTPUT							
	Output supply voltage			2.5		15.0	V
	Low-level output voltage	UCC1806 UCC2806	I_{SINK} = 20 mA		100	300	
			I_{SINK} = 100 mA		0.4	1.1	
		UCC3806	I_{SINK} = 20 mA		100	200	
			I_{SINK} = 100 mA		0.4	1.1	
	High-level output voltage		I_{SRC} = −20 mA	11.6	11.9		
			I_{SRC} = −100 mA	11.0	11.6		
t_{RISE}	Rise time		T_J = 25°C, C_{LOAD} = 1000 pF		35	65	ns
t_{FALL}	Fall time		T_J = 25°C, C_{LOAD} = 1000 pF		35	65	
UNDERVOLTAGE LOCKOUT (UVLO)							
V_{START}	Startup threshold voltage			6.5	7.5	8.0	V
	Threshold hysteresis				0.75		V
I_{START}	Startup current		V_{IN} < V_{START}		50	100	µA
I	Operating supply current				1.0	1.4	mA
	V_{IN} shunt voltage		I_{VIN} = 10 mA	15.0		17.5	

(1) Line range = 10 V to 15 V, load range = 0.2 mA to 5 mA
(2) Ensured by design. Not production tested.
(3) Parameters measured at trip point of latch with V_{NI} = VREF , V_{INV} = 0V.
(4) Amplifier gain defined as: G = delta change at COMP /delta change forced at CS+ delta voltage at CS+ = 0 to 1V
(5) Current-sense amplifier output is slew rate limited to provide noise immunity.

THERMAL RESISTANCE TABLE

PACKAGE DESIGNATOR	PACKAGE TYPE	θ_{JC} (°C/W)	θ_{JA} (°C/W)
D	SOIC−16	35	50 to 120(1)
DW	SOICW−16	27	50 to 100(1)
J	CDIP−16	28	80 to 120
L	CLCC−20	20	70 to 80
M	SSOP−16	38	144 to 172(2)
N	PDIP−16	45	90(1)
PW	TSSOP−16	15	123 to 147(2)
Q	PLCC−20	34	43 to 75(1)

(1) Specified θ_{JA} (junction to ambient) is for devices mounted to 5 in^2 FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 in^2 aluminum PC board. Test PWB was 0.062 in thick and typically used 0.635 mm trace widths for power packages and 1.3 mm trace widths for non-power packages with a 100x100 mil probe land area at the end of each trace.
(2) Modeled data. If value range given for θ_{JA}, the lower value is for 3x3 inch1 oz internal copper ground plane, and the higher value is for 1x1 inch ground plane. All model data assumes only one trace for each non-fused lead.

TERMINAL FUNCTIONS

TERMINAL NAME	PACKAGES D/DW/J/M /N/PW	PACKAGES L,Q	I/O	DESCRIPTION
AOUT	11	14	O	High-current gate drive for the external MOSFETs
BOUT	14	18		
COMP	7	9	O	Output of the error amplifier
CS−	3	4	I	Inverting input of the 3×, differential current sense amplifier
CS+	4	5	I	Non-inverting input of the 3×, differential current sense amplifier
CT	8	10	I	Oscillator timing capacitor connection point
CURLIM	1	2	I	Programs the primary current limit threshold that determins latching or retry after an overcurrent situation
GND	12	15	−	Reference ground and power ground for all functions of this device
INV	6	8	I	Inverting input of the error amplifier.
NI	5	7	I	Non-nverting input of the error amplifier.
RT	9	12	I	Connection point for the oscillator timing resistor
SHUTDOWN	16	20	I	Provided for enhanced protection. When SHUTDOWN is driven above 1 V, AOUT and BOUT are forced low.
SYNC	10	13	I/O	Allows providing external synchronization with TTL compatible thresholds.
VC	13	17	I	Input supply connection for the FET drive outputs.
VIN	15	19	I	Input supply connection for this device.
VREF	2	3	O	Reference output.

DETAILED PIN DESCRIPTIONS

AOUT and BOUT: AOUT and BOUT provide alternating high current gate drive for the external MOSFETs. Duty cycle can be varied from 0% to 50% where minimum dead time is a function of CT. Both outputs use MOS transistor switches with inherent anti-parallel body diodes to clamp voltage swings to the supply rails, allowing operation without the use of clamp diodes.

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier is a low output impedance, 2-MHz operational amplifier which allows sinking or sourcing of current at the COMP pin. The error amplifier is internally current limited, so that zero duty cycle can be commanded by externally forcing COMP to GND.

CS−: CS− is the inverting input of the 3× differential current sense amplifier.

CS+: CS+ is the non-inverting input of the 3× differential current sense amplifier.

CT: CT is the oscillator timing capacitor connection point, which is charged by the current set by RT. CT is discharged to GND through a 2.6-mA current sink. This causes a linear discharge of CT to 0 V which then initiates the next switching cycle. Dead time occurs during the discharge of CT, forcing AOUT and BOUT low. Switching frequency (f_S) and dead time (t_D) are approximated by:

$$f_S = \frac{1}{2 \times R_T \times C_T + t_D} \quad \text{and} \quad t_D = 961 \times C_T \qquad (1)$$

DETAILED PIN DESCRIPTIONS (continued)

CURLIM: CURLIM programs the primary current limit threshold and determines whether the device latches off or retries after an overcurrent condition. When a shutdown signal is generated, a 200-µA current source to ground pulls down on CURLIM. If the voltage on the pin remains above 350 mV the device remains latched and the power must be cycled to restart. If the voltage on the pin falls below 350 mV, the device attempts a restart. The voltage threshold is typically set by a resistor divider from V_{REF} to ground. To calculate the current limit adjust voltage threshold the following equations can be used.

Current limit adjust latching mode voltage is calculated in equation (2)

$$V = \frac{V_{REF} - (R1 \times 300\ \mu A \times 3)}{1 + \left(\frac{R1}{R2}\right)} > 350\ mV \qquad (2)$$

Current limit adjust non-latching mode voltage is calculated in equation (3)

$$V = \frac{V_{REF} - (R1 \times 80\ \mu A \times 3)}{1 + \left(\frac{R1}{R2}\right)} < 350\ mV \qquad (3)$$

where

- R1 is the resistance from the VREF to CURLIM
- R2 is the resistance from CURLIM to GND

GND: GND is the reference ground and power ground for all functions of this part. Bypass and timing capacitors should be connected as close as possible to GND.

RT: RT is the connection point for the oscillator timing resistor. It has a low impedance input and is nominally at 1.25 V. The current through RT is mirrored to the timing capacitor pin, CT. This causes a linear charging of CT from 0 V to 2.35 V. Note that the current mirror is limited to a maximum of 100 µA so R_T must be greater than 12.5 kΩ.

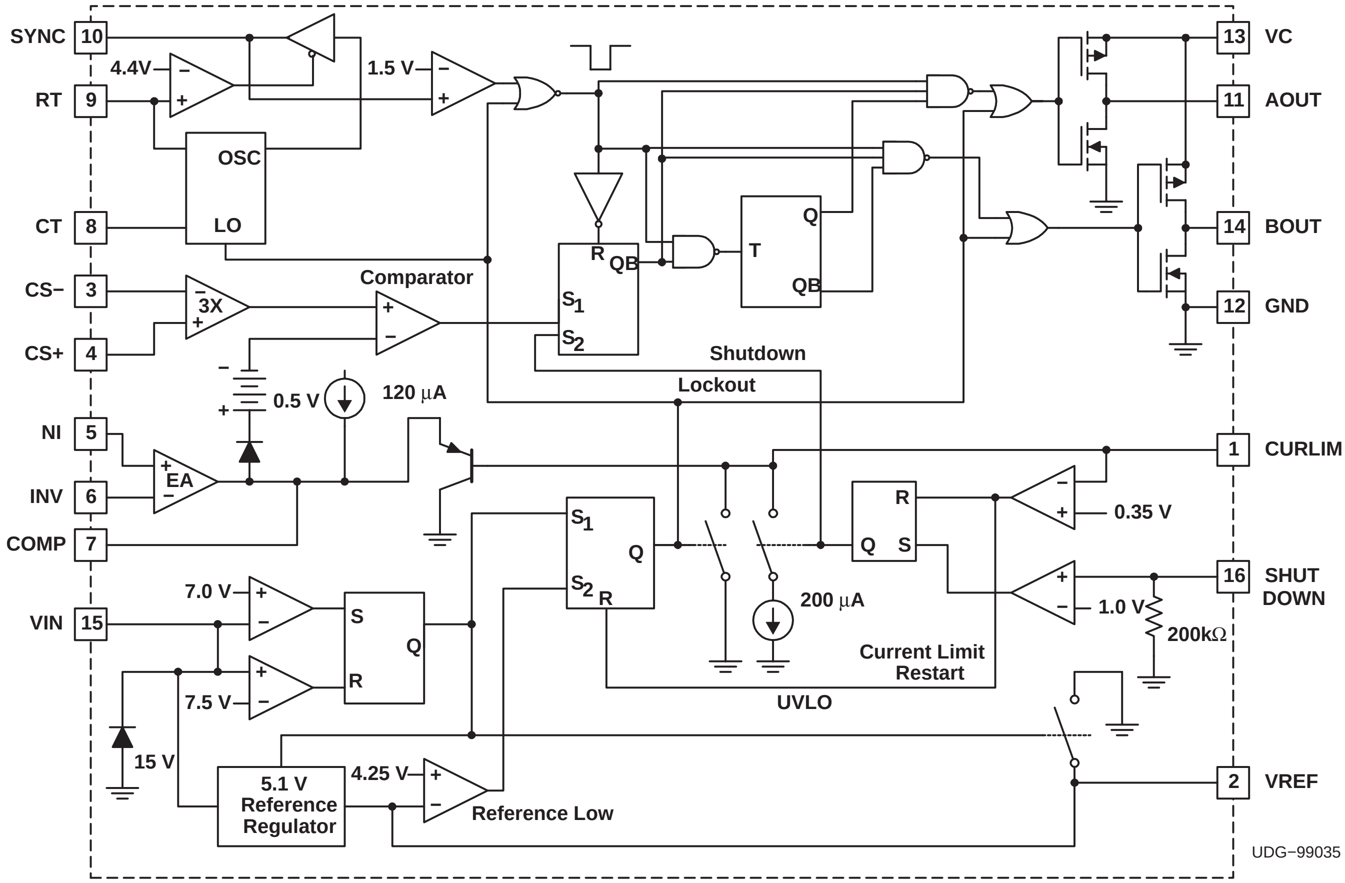
SYNC: SYNC is a bi-directional pin, allowing or providing external synchronization with TTL compatible thresholds. In a typical application RT is connected through a timing resistor to GND which allows the internal oscillator to free run. In this mode SYNC outputs a TTL compatible pulse during the oscillator dead time (when CT is being discharged). If RT is forced above 4.4 V, SYNC acts as an input with TTL compatible thresholds and the internal oscillator is disabled. When SYNC is high, greater than 2 V the outputs are held active low. When SYNC returns low, the outputs may be high until the on−time is terminated by the normal peak current signal, a fault seen at SHUTDOWN or the next high assertion of SYNC. Multiple UCC3806s can be synchronized by a single master UCC3806 or external clock.

VC: VC is the input supply connection for the FET drive outputs and has an input range from 2.5 V to 15 V. VC should be capacitively bypassed for proper operation.

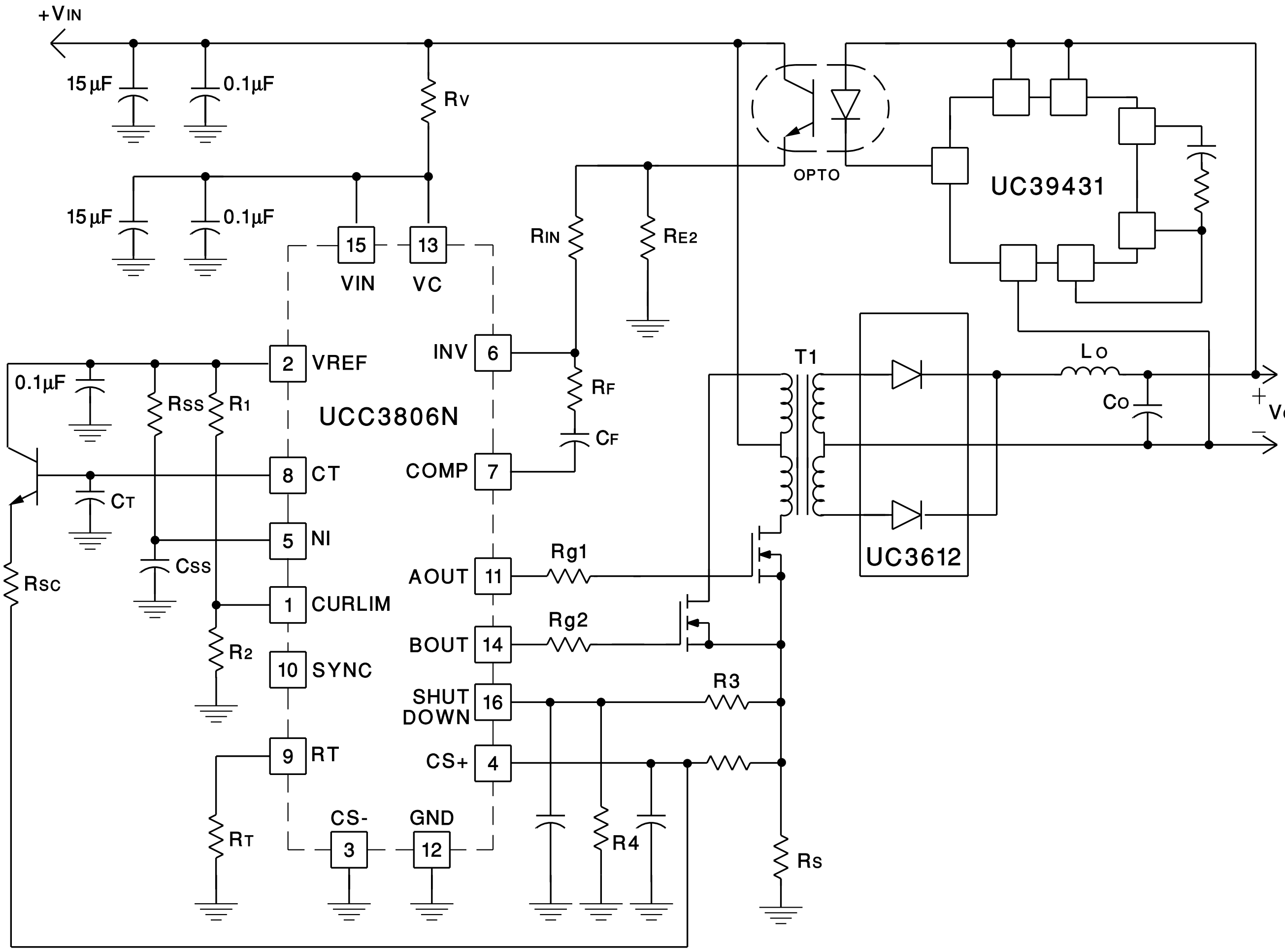
VIN: VIN is the input supply connection for this device. The UCC1806 has a maximum startup threshold of 8 V and internally limited by means of a 15 V shunt regulator. The shunted supply current must be limited to 2.5 mA. For proper operation, VIN must be bypassed to GND with at least a 0.01-µF ceramic capacitor

VREF: VREF is a 5.1 V ±1% trimmed reference output with a 5 mA maximum available current. VREF must be bypassed to GND with at least a 0.1-µF ceramic capacitor for proper operation.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION DIAGRAM



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TYPICAL CHARACTERISTICS

Design equations for oscillator are described in the following equations.

$$f_{OSC} = \frac{1}{t_{RAMP} + t_{FALL}} \tag{4}$$

$$t_{RAMP} = 1.92 \times R_T \times C_T \tag{5}$$

$$t_{FALL} = \frac{2.4 \times C_T}{\left(0.002 - \left(\frac{1.25}{R_T}\right)\right)} \tag{6}$$

$$t_{DEAD} = t_{FALL} \tag{7}$$

TYPICAL CHARACTERISTICS

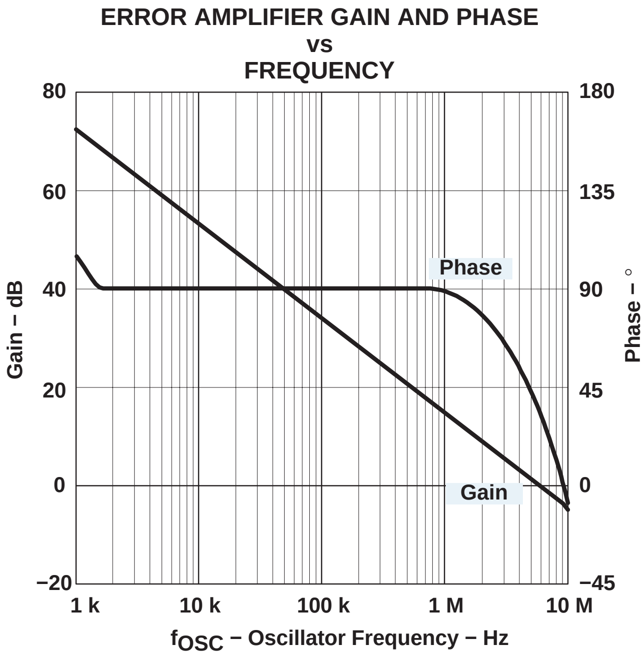

Figure 1.

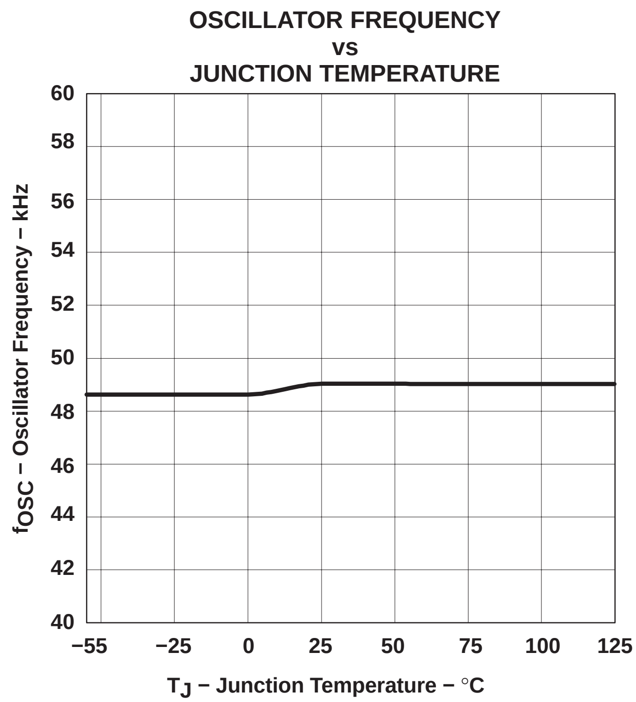

Figure 2.

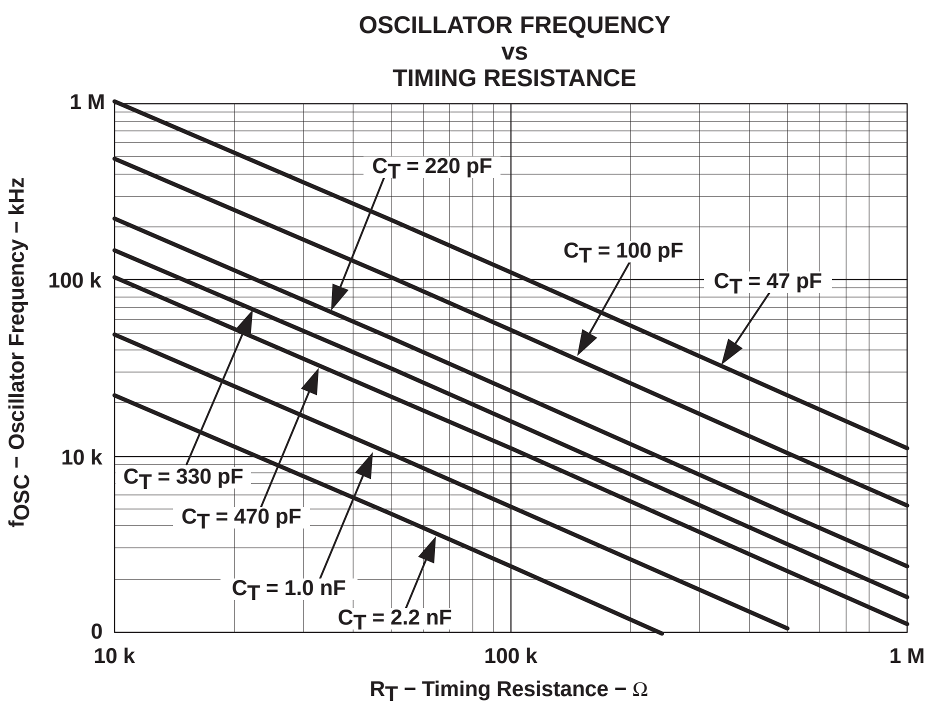

Figure 3.

IMPORTANT NOTICE

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