34-Channel Symmetric Row Driver

Ordering Information

Device	Package Options			
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack	44 J-Lead Quad Ceramic Chip Carrier (MIL-Std-883 Processed*)
HV7022-C	HV7022DJ-C	HV7022PJ-C	HV7022X-C	RBHV7022DJ-C

*For Hi-Rel process flows, refer to page 5-3 of the databook.

Features

- ❑ Processed with HVCMOS® technology
- ❑ Symmetric row drive (reduces latent imaging in ACTFEL displays)
- ❑ Output voltages up to 230V
- ❑ Low-power level shifting
- ❑ Source/Sink current 70mA (min.)
- ❑ Shift register speed 4MHz
- ❑ Pin-programmable shift direction
- ❑ 44-lead plastic & ceramic surface-mount packages
- ❑ Hi-Rel processing available

General Description

The HV7022-C is a low-voltage serial to high-voltage parallel converter with push-pull outputs. It is especially suited for use as a symmetric row driver in AC thin-film electroluminescent (ACTFEL) displays. The HV70 offers 34 output lines, a direction (DIR) pin to give CW or CCW shift register loading, output enable (OE), and polarity (POL) control. After DATA INPUT is entered (on the falling edge of CLOCK), a logic high will cause the output to swing to V_{PP} if POL is high, or to GND if POL is low.

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.3V to +15V
Supply voltage, V_{PP}[1]		-0.3V to +250V
Logic input levels[1]		-0.3V to V_{DD} +0.3V
Ground current[2]		1.5A
Continuous total power dissipation[3]:	Plastic	1200mW
	Ceramic	1500mW
Operating temperature range	Plastic	-40°C to +85°C
	Ceramic	-55°C to 125°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. All voltages are referenced to GND.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to maximum operating temperature at 25mW/°C for plastic and at 15mW/°C for ceramic.

For Detailed circuit and application information, please refer to Application Note AN-H3.

Electrical Characteristics

(over recommended operating conditions of V_{DD} = 12V, T_A = 25°C and V_{PP} = 230V unless otherwise noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			10	mA	f_{CLK} = 4MHz
I_{PP}	High voltage supply current			4	mA	1 Output high[1]
				100	μA	All Outputs low or High-Z
				750	μA	All Outputs low or High-Z (125°C)
I_{DDQ}	Quiescent V_{DD} supply current			100	μA	All V_{IN} = GND or V_{DD}
V_{OH}	High-level output	HV_{OUT}	195		V	I_O= -70mA (-50mA)[2]
		Data out	11		V	I_O= -500μA
V_{OL}	Low-level output	HV_{OUT}		30	V	I_O= 70mA (+50mA)[2]
		Data out		1	V	I_O= 500μA
I_{IH}	High-level logic input current			1	μA	V_{IH} = 12V
I_{IL}	Low-level logic input current			-1	μA	V_{IL} = 0V

Notes:

1. The total number of ON outputs times the duty cycle must not exceed the allowable package power disspation.
2. Over military temperature range (-55°C to 125°C).

AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		4	MHz	
t_W	Pulse duration clock high or low	125		ns	
t_{SUD}	Data set-up time before falling clock	100		ns	
t_{HD}	Data hold time after falling clock	100		ns	
t_{SUC}	Setup time clock low before V_{PP}↑ or GND↓	300		ns	
t_{SUE}	Setup time enable high before V_{PP}↑ or GND↓	300		ns	
t_{SUP}	Setup time polarity high or low before V_{PP}↑ or GND↓	300		ns	
t_{HC}	Hold time clock high after V_{PP}↑ or GND↓	500		ns	
t_{HE}	Hold time enable high after V_{PP}↑ or GND↓	300		ns	
t_{HP}	Hold time polarity high or low after V_{PP}↑ or GND↓	300		ns	
t_{DHL}	Delay time high to low level output from clock		150	ns	C_L = 10pF
t_{DLH}	Delay time low to high level output from clock		200	ns	C_L = 10pF
t_{THL}	Transition time high to low level serial output		200	ns	C_L = 15pF
t_{TLH}	Transition time low to high level serial output		100	ns	C_L = 15pF
t_{ONH}	High level turn-on time Q outputs from enable		500	ns	I_O = -50 mA, V_{OH} =195V R_L = 2 kΩ to 95V
t_{ONL}	Low level turn-on time Q outputs from enable		500	ns	I_O = 50 mA, V_{OH} =130V R_L = 2 kΩ to 30V
t_{OFFH}	High level turn-off time Q outputs from enable		1000	ns	I_O = -50 mA, V_{OH} =195V R_L = 2 kΩ to 95V
t_{OFFL}	Low level turn-off time Q outputs from enable		500	ns	I_O = 50 mA, V_{OH} =130V R_L = 2 kΩ to 30V
	Slew rate, V_{PP} or GND		45	V/μs	With one active output driving a 4.7 nF load to V_{PP} or GND

Recommended Operating Conditions

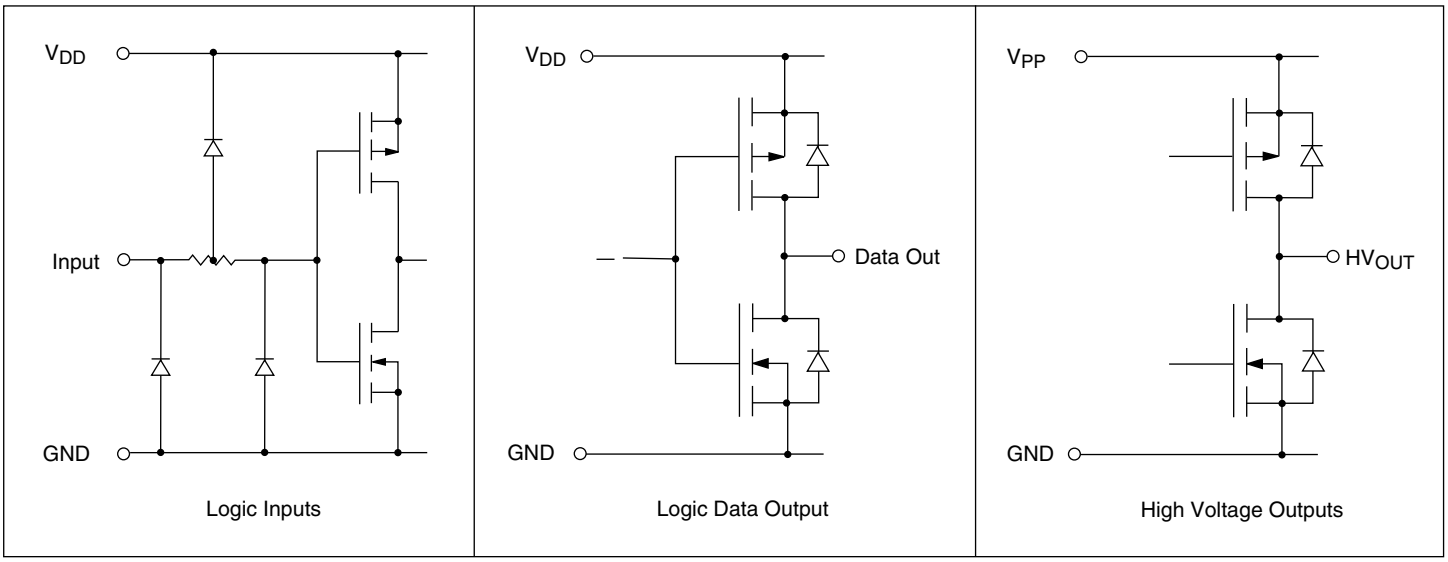
Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	High voltage supply			230	V
V_{IH}	High-level input voltage	V_{DD} = 10.8V	8.1		V
		V_{DD} = 13.2V	9.9		
V_{IL}	Low-level input voltage	V_{DD} = 10.8V		2.7	V
		V_{DD} = 13.2V		3.3	
f_{CLK}	Clock frequency			4	MHz
T_A	Operating free-air temperature	Plastic	-40	+85	°C
		Ceramic	-55	+125	°C
I_{OD}	Allowable pulse current through output diodes			±300	mA

Note:
Power-up sequence should be the following:

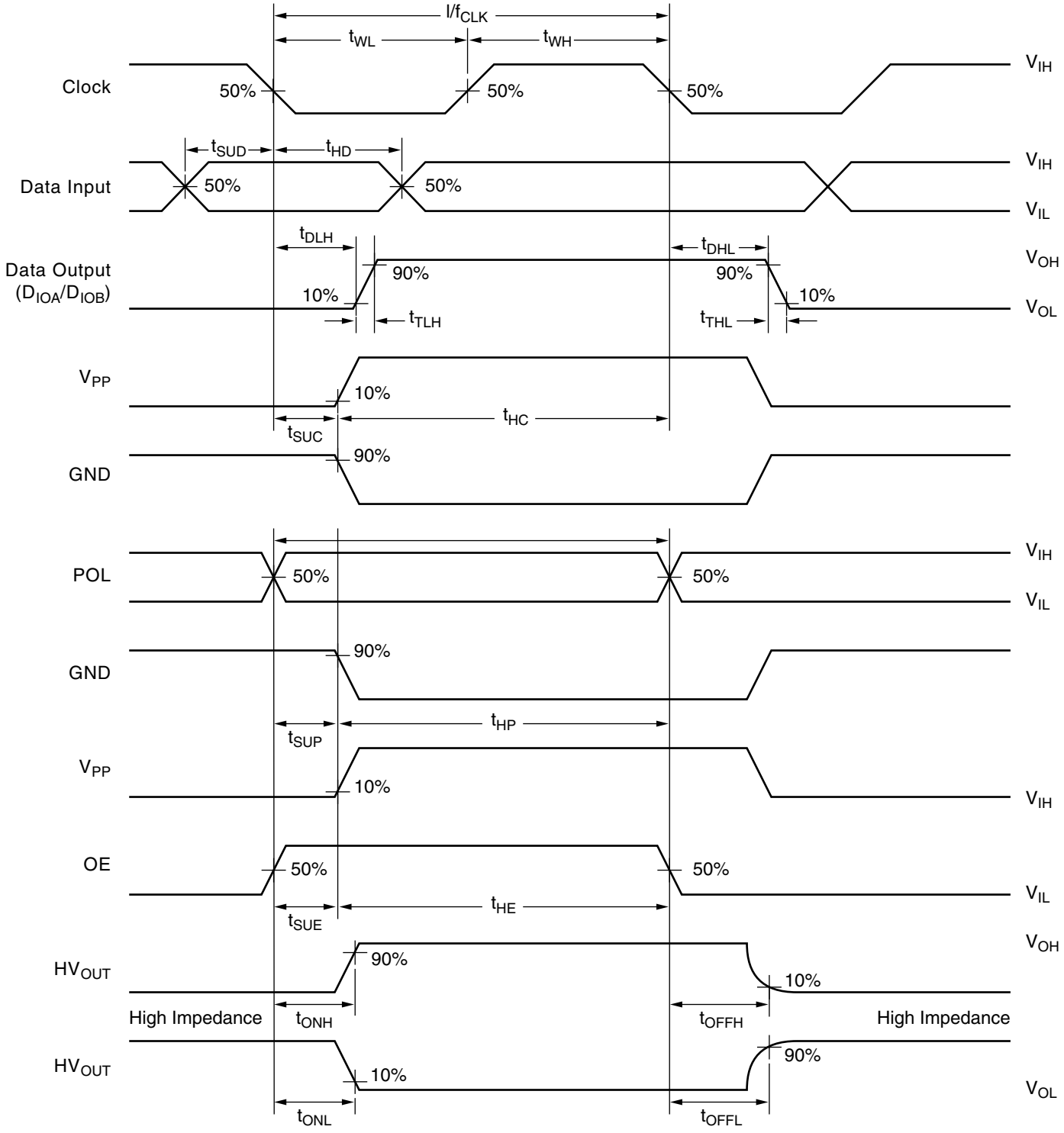
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.
5. The V_{PP} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.

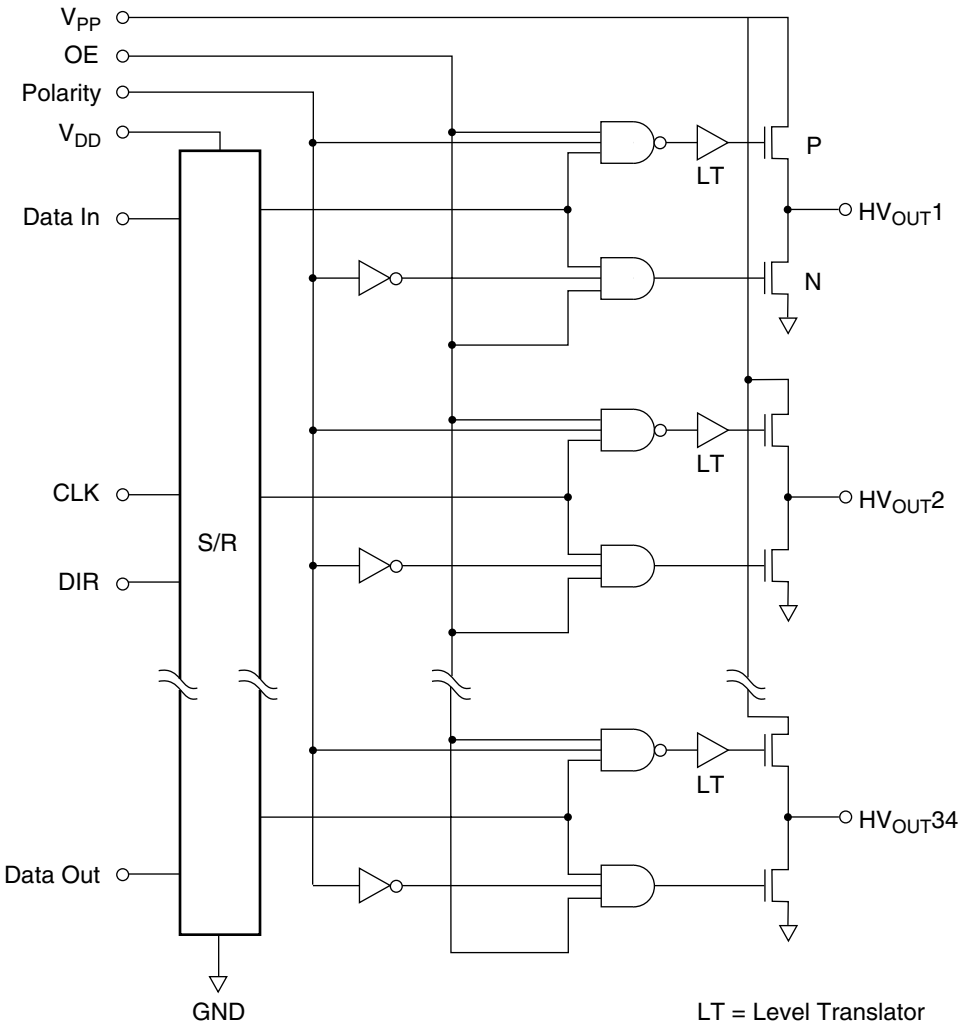
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

I/O Relations	Inputs					Outputs		
	CLK	DIR	Data	POL	OE	Shift Reg	HV Outputs	Data Out
O/P HIGH	X	X	H	H	H	*	H	
O/P OFF	X	X	L	H	H	*	HIGH-Z	*
O/P LOW	X	X	H	L	H	*	L	*
O/P OFF	X	X	L	L	H	*	HIGH-Z	*
O/P OFF	X	X	X	X	L	*	All O/P HIGH-Z	*
Load S/R, set DIR	↓	L	X	X	X	$Q_n \rightarrow Q_{n+1}$	*	Q_{34}
	↓	H	X	X	X	$Q_n \rightarrow Q_{n-1}$	*	Q_1
	No ↓	X	X	X	X	*	No Change	No Change

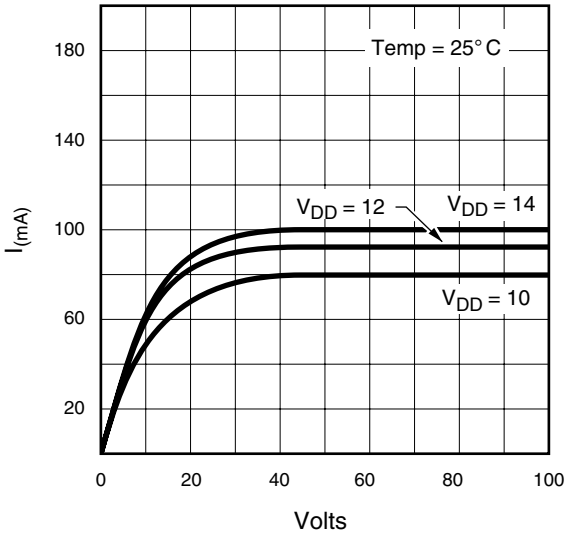
Notes:

H = logic high level, L = logic low level, X = irrelevant, ↓ = high-to-low transition,

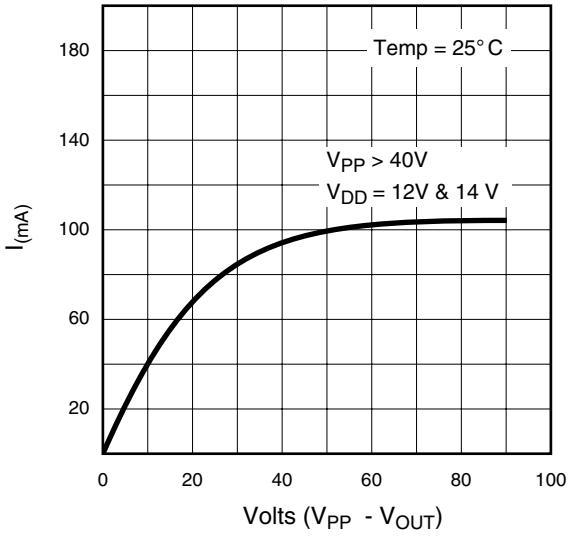
$Q_1 = HV_{OUT}$ 1, $Q_n = HV_{OUT}(n)$, etc.

* = dependent on previous state and whether an O/P or S/R command occured.

HV_{OUT} Characteristics



Output N-Channel Characteristics through FET



Output P-Channel Characteristics through FET

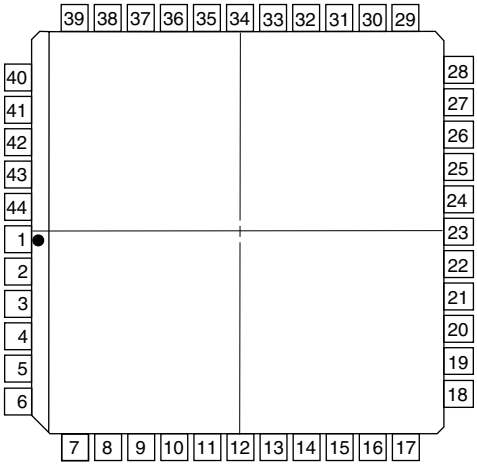
Pin Configurations

HV70
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 18/17	23	DIR
2	HV_{OUT} 17/18	24	V_{DD}
3	HV_{OUT} 16/19	25	Polarity
4	HV_{OUT} 15/20	26	Data In
5	HV_{OUT} 14/21	27	V_{PP}
6	HV_{OUT} 13/22	28	N/C
7	HV_{OUT} 12/23	29	HV_{OUT} 34/1
8	HV_{OUT} 11/24	30	HV_{OUT} 33/2
9	HV_{OUT} 10/25	31	HV_{OUT} 32/3
10	HV_{OUT} 9/26	32	HV_{OUT} 31/4
11	HV_{OUT} 8/27	33	HV_{OUT} 30/5
12	HV_{OUT} 7/28	34	HV_{OUT} 29/6
13	HV_{OUT} 6/29	35	HV_{OUT} 28/7
14	HV_{OUT} 5/30	36	HV_{OUT} 27/8
15	HV_{OUT} 4/31	37	HV_{OUT} 26/9
16	HV_{OUT} 3/32	38	HV_{OUT} 25/10
17	HV_{OUT} 2/33	39	HV_{OUT} 24/11
18	HV_{OUT} 1/34	40	HV_{OUT} 23/12
19	Data Out	41	HV_{OUT} 22/13
20	Output Enable	42	HV_{OUT} 21/14
21	Clock	43	HV_{OUT} 20/15
22	GND	44	HV_{OUT} 19/16

Note:
Pin designation for DIR L/H
Example: For DIR = L, pin 1 is HV_{OUT} 18
For DIR = H, pin 1 is HV_{OUT} 17

Package Outline



top view
44-pin J-Lead Package

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