



N-Channel Depletion-Mode Vertical DMOS FETs

Features

- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage

Applications

- ☐ Normally-on switches
- ☐ Solid state relays
- ☐ Converters
- ☐ Constant current sources
- ☐ Power supply circuits
- ☐ Telecom

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSX}
Drain-to-Gate Voltage	BV_{DGX}
Gate-to-Source Voltage	$\pm 20V$
Operating and Storage Temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering Temperature*	$300^{\circ}C$

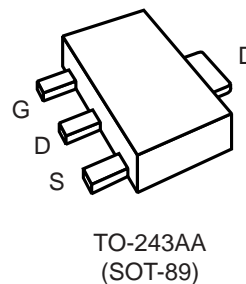
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These depletion-mode (normally-on) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See Package Outline section for dimensions.

Ordering Information

BV_{DSX} / BV_{DGX}	$R_{DS(ON)}$ (max)	I_{DSS} (min)	Order Number / Package
			TO-243AA*
450V	60 Ω	120mA	DN3145N8

* Same as SOT-89. Product shipped on 2000 piece carrier tape reels.

Product marking for TO-243AA:

DN1M*

Where * = 2-week alpha date code

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	θ_{JC} $^\circ\text{C/W}$	θ_{JA} $^\circ\text{C/W}$	I_{DR}^*	I_{DRM}
TO-243AA	100mA	300mA	1.3W†	34	97†	100mA	300mA

* I_D (continuous) is limited by max rated T_J .

† Mounted on FR4 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

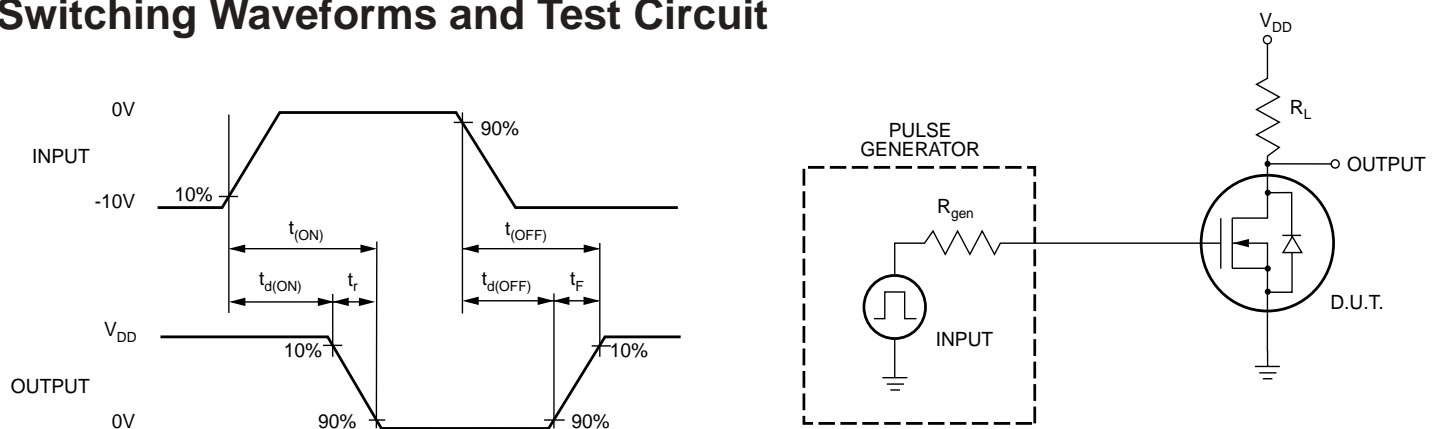
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSX}	Drain-to-Source Breakdown Voltage	450			V	$V_{GS} = -5V$, $I_D = 100\mu\text{A}$
$V_{GS(OFF)}$	Gate-to-Source OFF Voltage	-1.5		-3.5	V	$V_{DS} = 15V$, $I_D = 10\mu\text{A}$
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with Temperature			4.5	mV/ $^\circ\text{C}$	$V_{DS} = 15V$, $I_D = 10\mu\text{A}$
I_{GSS}	Gate Body Leakage Current			100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
$I_{D(OFF)}$	Drain-to-Source Leakage Current			1.0	μA	$V_{GS} = -5.0V$, $V_{DS} = \text{Max Rating}$
				1.0	mA	$V_{GS} = -5.0V$, $V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
I_{DSS}	Saturated Drain-to-Source Current	120			mA	$V_{GS} = 0V$, $V_{DS} = 15V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			60	Ω	$V_{GS} = 0V$, $I_D = 100\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.1	%/ $^\circ\text{C}$	$V_{GS} = 0V$, $I_D = 100\text{mA}$
G_{FS}	Forward Transconductance	140			mS	$I_D = 100\text{mA}$, $V_{DS} = 10V$
C_{ISS}	Input Capacitance			120	pF	$V_{GS} = -5.0V$, $V_{DS} = 25V$ $f = 1.0 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance			15		
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = 25V$, $I_D = 100\text{mA}$, $R_{GEN} = 25\Omega$
t_r	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			20		
t_f	Fall Time			35		
V_{SD}	Diode Forward Voltage Drop			1.8	V	$V_{GS} = -5.0V$, $I_{SD} = 100\text{mA}$
t_{rr}	Reverse Recovery Time		800		ns	$V_{GS} = -5.0V$, $I_{SD} = 100\text{mA}$

Notes:

- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



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