ST-NXP Wireless

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ST-NXP Wireless

ISP1504A1; ISP1504C1

ULPI Hi-Speed Universal Serial Bus On-The-Go transceiver

Rev. 01 — 6 August 2007 Product data sheet

1. General description

The ISP1504A1; ISP1504C1 (ISP1504x1) is a Universal Serial Bus (USB) On-The-Go (OTG) transceiver that is fully compliant with *Universal Serial Bus Specification Rev. 2.0*, *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.2* and *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

The ISP1504x1 can transmit and receive USB data at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s), and provides a pin-optimized, physical layer front-end attachment to the USB host, peripheral and OTG devices.

It is ideal for use in portable electronic devices, such as mobile phones, digital still cameras, digital video cameras, Personal Digital Assistants (PDAs) and digital audio players. It allows USB Application-Specific Integrated Circuits (ASICs), Programmable Logic Devices (PLDs) and any system chip set to interface with the physical layer of the USB through a 12-pin interface.

The ISP1504x1 can interface to devices with digital I/O voltages in the range of 1.65 V to 3.6 V.

The ISP1504x1 is available in TFBGA36 package.

2. Features

- Fully complies with:
  - *Universal Serial Bus Specification Rev. 2.0*
  - *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.2*
  - *UTMI+ Low Pin Interface (ULPI) Specification Rev 1.1*
- Interfaces to host, peripheral and OTG device cores; optimized for portable devices or system ASICs with built-in USB OTG device core
- Complete Hi-Speed USB physical front-end solution that supports high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s)
  - Integrated 45 Ω ± 10 % high-speed termination resistors, 1.5 kΩ ± 5 % full-speed device pull-up resistor, and 15 kΩ ± 5 % host termination resistors
  - Integrated parallel-to-serial and serial-to-parallel converters to transmit and receive
  - USB clock and data recovery to receive USB data at ±500 ppm
  - USB data synchronization from 60 MHz input to 480 MHz output during transmit
  - Insertion of stuff bits during transmit and discarding of stuff bits during receive
  - Non-Return-to-Zero Inverted (NRZI) encoding and decoding
  - Supports bus reset, suspend, resume and high-speed detection handshake (chirp)
- Complete USB OTG physical front-end that supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)

- Supports external charge pump or 5 V V_{BUS} switch
- Complete control over bus resistors
- Data line and V_{BUS} pulsing session request methods
- Integrated V_{BUS} voltage comparators
- Integrated cable (ID) detector

- Highly optimized ULPI-compliant interface
  - 60 MHz, 8-bit interface between the core and the transceiver
  - Integrated Phase-Locked Loop (PLL) supporting input clock frequency of 19.2 MHz for ISP1504A1, and 26 MHz for ISP1504C1
  - Fully programmable ULPI-compliant register set
  - Internal Power-On Reset (POR) circuit
- Flexible system integration and very low current consumption, optimized for portable devices
  - Power-supply input range is 3.0 V to 4.5 V
  - Internal voltage regulator supplies 3.3 V and 1.8 V
  - Supports external V_{BUS} charge pump or 5 V supply:

    External V_{BUS} source is controlled using the PSW_N pin; open-drain PSW_N allows per-port or ganged power control

    Digital FAULT input to monitor the external V_{BUS} supply status
  - Pin CS_N/PWRDN 3-states the ULPI interface, allowing bus reuse for other applications
  - Supports power-down mode when $V_{CC(I/O)}$ is not present or when pin CS_N/PWRDN is HIGH
  - Supports wide range interfacing I/O voltage of 1.65 V to 3.6 V; separate I/O voltage pins minimize crosstalk
  - Typical operating current of 10 mA to 48 mA, depending on the USB speed and bus utilization
  - Typical suspend current of 50 μA
  - Typical power-down current of 0.5 μA
- Full industrial grade operating temperature range from −40 °C to +85 °C
- ElectroStatic Discharge (ESD) compliance
  - JESD22-A114D 2 kV contact Human Body Model (HBM)
  - JESD22-A115-A 200 V Machine Model (MM)
  - JESD22-C101-C 500 V Charge Device Model (CDM)
- Available in a small TFBGA36 (3.5 mm × 3.5 mm) Restriction of Hazardous Substances (RoHS) compliant, halogen-free and lead-free package

3. Applications

- Digital still camera
- Digital TV
- Digital Versatile Disc (DVD) recorder
- External storage device, for example:
  - Zip drive
  - Magneto-Optical (MO) drive
  - Optical drive: CD-ROM, CD-RW, CD-DVD

- Mobile phone
- MP3 player
- PDA
- Printer
- Scanner
- Set-Top Box (STB)
- Video camera

4. Ordering information

Table 1. Ordering information

Part			Package		
Type number	**Marking**	**Crystal or clock frequency**	**Name**	**Description**	**Version**
ISP1504A1ET	504M[1]	19.2 MHz	TFBGA36	plastic thin fine-pitch ball grid array package; 36 balls; body 3.5 × 3.5 × 0.8 mm	SOT912-1
ISP1504C1ET	504P[1]	26 MHz			

[1] The package marking is the first line of text on the IC package and can be used for IC identification.

5. Block diagram

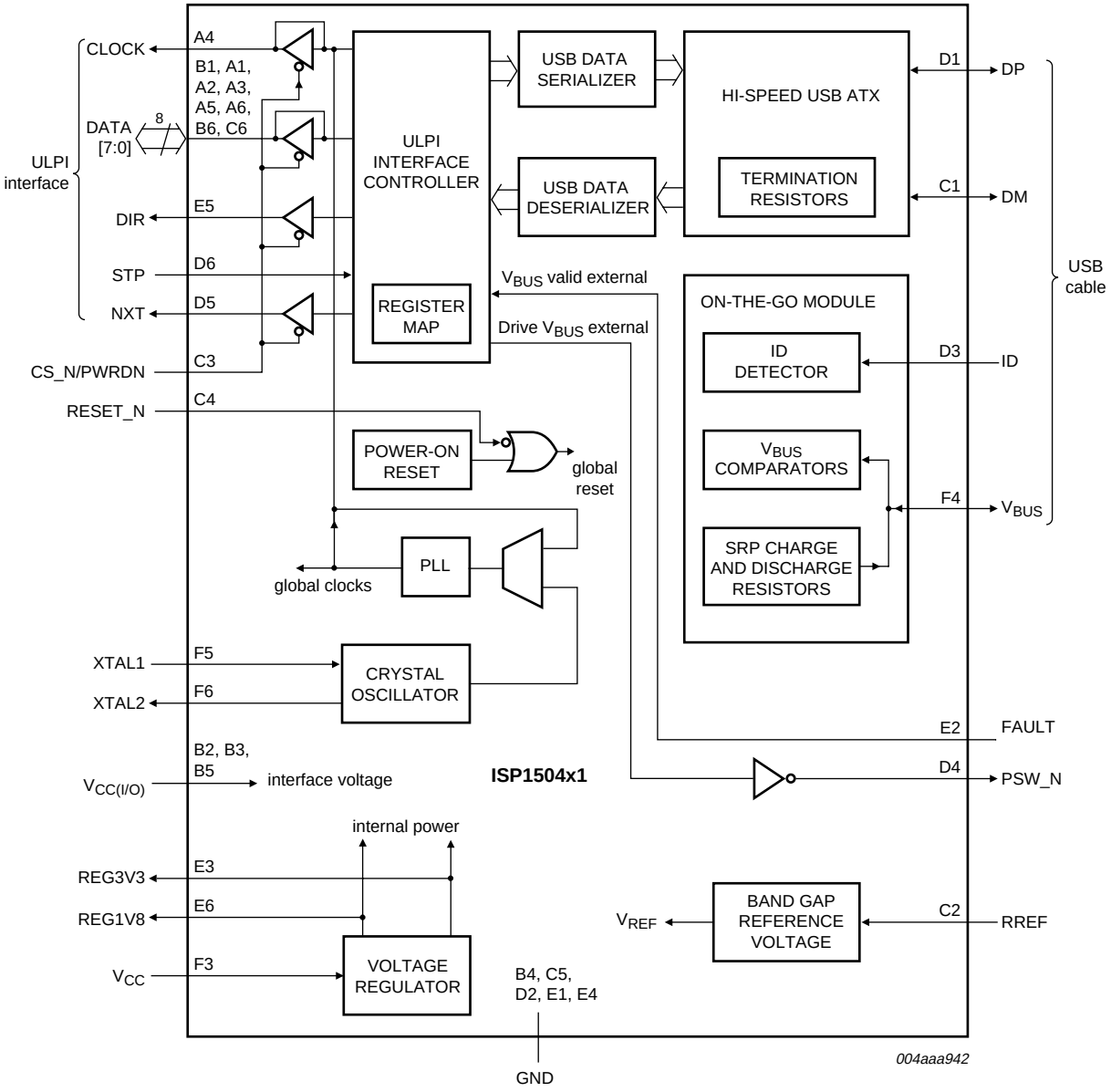


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

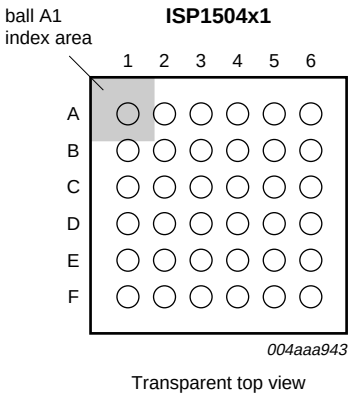


Fig 2. Pin configuration TFBGA36; top view

6.2 Pin description

Table 2. Pin description

Symbol[1][2]	Pin	Type[3]	Description[4]
DATA1	A1	I/O	pin 1 of the bidirectional ULPI data bus slew rate controlled output (1 ns); plain input; programmable pull down
DATA2	A2	I/O	pin 2 of the bidirectional ULPI data bus slew rate controlled output (1 ns); plain input; programmable pull down
DATA3	A3	I/O	pin 3 of the bidirectional ULPI data bus slew rate controlled output (1 ns); plain input; programmable pull down
CLOCK	A4	O	60 MHz clock output for ULPI slew rate controlled output (1 ns)
DATA4	A5	I/O	pin 4 of the bidirectional ULPI data bus slew rate controlled output (1 ns); plain input; programmable pull down
DATA5	A6	I/O	pin 5 of the bidirectional ULPI data bus slew rate controlled output (1 ns); plain input; programmable pull down
DATA0	B1	I/O	pin 0 of the bidirectional ULPI data bus slew rate controlled output (1 ns); plain input; programmable pull down
$V_{CC(I/O)}$	B2, B3, B5	P	input I/O supply voltage; allowable range 1.65 V to 3.6 V; a 0.1 µF decoupling capacitor is recommended
GND	B4, C5, D2, E1, E4	P	ground supply
DATA6	B6	I/O	pin 6 of the bidirectional ULPI data bus slew rate controlled output (1 ns); plain input; programmable pull down
DM	C1	AI/O	data minus (D–) pin of the USB cable
RREF	C2	AI/O	resistor reference; connect through 12 kΩ ± 1 % to GND

Table 2. Pin description *...continued*

Symbol[1][2]	Pin	Type[3]	Description[4]
CS_N/ PWRDN	C3	I	active LOW chip select • When this pin is HIGH, ULPI pins will be 3-stated and the chip is in power-down mode. • When this pin is LOW, ULPI pins will operate normally. plain input
RESET_N	C4	I	active LOW, asynchronous reset input If this pin is not used, it must directly be connected to $V_{CC(I/O)}$. plain input
DATA7	C6	I/O	pin 7 of the bidirectional ULPI data bus slew rate controlled output (1 ns); plain input; programmable pull down
DP	D1	AI/O	data plus (D+) pin of the USB cable
ID	D3	I	identification (ID) pin of the micro-USB cable; see Section 7.6.1 If this pin is not used, it is recommended to connect it to REG3V3. plain input; TTL level
PSW_N	D4	OD	active LOW external V_{BUS} power switch or external charge pump enable open-drain output; 5 V tolerant
NXT	D5	O	ULPI next signal slew rate controlled output (1 ns)
STP	D6	I	ULPI stop signal plain input; programmable pull up
FAULT	E2	I	input pin for the external V_{BUS} digital overcurrent or the fault detector signal If this pin is not used, it must be connected to ground. plain input; 5 V tolerant
REG3V3	E3	P	3.3 V regulator output requiring parallel 0.1 µF and 4.7 µF capacitors; internally powers OTG, analog core and ATX; cannot be externally used as a power source
DIR	E5	O	ULPI direction signal slew rate controlled output (1 ns)
REG1V8	E6	P	1.8 V regulator output requiring parallel 0.1 µF and 4.7 µF capacitors; internally powers digital core and analog core; cannot be externally used as a power source
n.c.	F1, F2	-	not connected
V_{CC}	F3	P	input supply voltage or battery source; 3.0 V to 4.5 V
V_{BUS}	F4	AI/O	must be connected to the V_{BUS} pin of the USB cable; required in all configurations, except when the ISP1504x1 is used as a host-only with an external 5 V source
XTAL1	F5	AI/O	crystal oscillator or clock input; 1.8 V peak input allowed; frequency is 19.2 MHz for ISP1504A1, and 26 MHz for ISP1504C1
XTAL2	F6	AI/O	crystal oscillator output; if crystal is not in use, leave this pin open

[1] Symbol names ending with underscore N, for example, NAME_N, indicate active LOW signals.

[2] For details on external components required on each pin, see bill of materials and application diagrams in Section 15.

[3] I = input; O = output; I/O = digital input/output; OD = open-drain output; AI/O = analog input/output; P = power or ground pin.

[4] A detailed description of these pins can be found in Section 7.9.

7. Functional description

7.1 ULPI interface controller

The ISP1504x1 provides a 12-pin interface that is compliant with *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*. This interface must be connected to the USB link.

The ULPI interface controller provides the following functions:

- ULPI-compliant interface and register set
- Allows full control over the USB peripheral, host and OTG functionality
- Parses the USB transmit and receive data
- Prioritizes the USB receive data, USB transmit data, interrupts and register operations
- Low-power mode
- Control of the V_{BUS} external power source
- V_{BUS} monitoring, charging and discharging
- 6-pin serial mode and 3-pin serial mode
- Generates RXCMDs; status updates
- Maskable interrupts
- Control over the ULPI bus state, allowing pins to 3-state or attach active weak pull-down resistors

For more information on the ULPI protocol, see Section 9.

7.2 USB data serializer and deserializer

The USB data serializer prepares data to transmit on the USB bus. To transmit data, the USB link sends a transmit command and data on the ULPI bus. The serializer performs parallel-to-serial conversion, bit stuffing and NRZI encoding. For packets with a PID, the serializer adds a SYNC pattern to the start of the packet, and an EOP pattern to the end of the packet. When the serializer is busy and cannot accept any more data, the ULPI interface controller de-asserts NXT.

The USB data deserializer decodes data received from the USB bus. When data is received, the deserializer strips the SYNC and EOP patterns, and then performs serial-to-parallel conversion, NRZI decoding and discarding of stuff bits on the data payload. The ULPI interface controller sends data to the USB link by asserting DIR, and then asserting NXT whenever a byte is ready. The deserializer also detects various receive errors, including bit stuff errors, elasticity buffer underrun or overrun, and byte-alignment errors.

7.3 Hi-Speed USB (USB 2.0) ATX

The Hi-Speed USB ATX block is an analog front-end containing the circuitry needed to transmit, receive and terminate the USB bus in high-speed, full-speed and low-speed, for USB peripheral, host and OTG implementations. The following circuitry is included:

- Differential drivers to transmit data at high-speed, full-speed and low-speed

- Differential and single-ended receivers to receive data at high-speed, full-speed and low-speed
- Squelch circuit to detect high-speed bus activity
- High-speed disconnect detector
- 45 Ω high-speed bus terminations on DP and DM
- 1.5 kΩ pull-up resistor on DP
- 15 kΩ pull-down resistor on DP and DM

For details on controlling resistor settings, see Table 8.

7.4 Voltage regulator

The ISP1504x1 contains a built-in voltage regulator that conditions the V_{CC} supply for use inside the ISP1504x1. The voltage regulator:

- Supports input supply range of 3.0 V < V_{CC} < 4.5 V
- Can be supplied from a battery with a voltage range of 3.0 V to 4.5 V
- Supplies internal circuitry with 1.8 V and 3.3 V
- Automatically bypasses the internal 3.3 V regulator when V_{CC} < 3.5 V, drawing power directly from the V_{CC} pin

To save current, the voltage regulator will be shut down, if $V_{CC(I/O)}$ is not present or if pin CS_N/PWRDN is at a HIGH level.

Remark: The REG1V8 and REG3V3 pins require an external 0.1 µF capacitor in parallel with a 4.7 µF capacitor. For details, see Section 15.

7.5 Crystal oscillator and PLL

The ISP1504x1 has a built-in crystal oscillator and a Phase-Locked Loop (PLL) for clock generation.

The crystal oscillator takes a sine-wave input from an external crystal, on the XTAL1 pin, and converts it to a square wave clock for internal use. Alternatively, a square wave clock of the same frequency can also be directly driven into the XTAL1 pin. Using an existing square wave clock can save the cost of the crystal and also reduce the board size. The input clock or crystal frequency supported is 19.2 MHz or 26 MHz.

The PLL produces the following frequencies, irrespective of the clock source:

- 60 MHz clock for the ULPI interface controller
- 1.5 MHz for the low-speed USB data
- 12 MHz for the full-speed USB data
- 480 MHz for the high-speed USB data
- Other internal frequencies for data conversion and data recovery

7.6 OTG module

This module contains several sub-blocks that provide all the functionality required by the USB OTG specification. Specifically, it provides the following circuits:

- The ID detector to sense the ID pin of the micro-USB cable. The ID pin dictates which device is initially configured as the host and which as the peripheral.
- V_{BUS} comparators to determine the V_{BUS} voltage level. This is required for the V_{BUS} detection, SRP and HNP.
- Resistors to temporarily charge and discharge V_{BUS}. This is required for SRP.

Remark: The ISP1504x1 does not include the 5 V charge pump to power V_{BUS}.

7.6.1 ID detector

The ID detector detects which end of the micro-USB cable is plugged in. The detector must first be enabled by setting the ID_PULLUP register bit to logic 1. If the ISP1504x1 senses a value on ID that is different from the previously reported value, an RXCMD status update will be sent to the USB link, or an interrupt will be asserted.

- If the micro-B end of the cable is plugged in, the ISP1504x1 will report that ID_GND is logic 1. The USB link must change to peripheral mode.
- If the micro-A end of the cable is plugged in, the ISP1504x1 will report that ID_GND is logic 0. The USB link must change to host mode.

7.6.2 V_{BUS} comparators

The ISP1504x1 provides three comparators, V_{BUS} valid comparator, session valid comparator and session end comparator, to detect the V_{BUS} voltage level.

7.6.2.1 V_{BUS} valid comparator

This comparator is used by hosts and OTG A-devices to determine whether the voltage on V_{BUS} is at a valid level for operation. The ISP1504x1 threshold for the V_{BUS} valid comparator is $V_{A\_VBUS\_VLD}$. Any voltage on V_{BUS} below $V_{A\_VBUS\_VLD}$ is considered a fault. During power-up, it is expected that the comparator output will be ignored.

7.6.2.2 Session valid comparator

The session valid comparator is a TTL-level input that determines when V_{BUS} is high enough for a session to start. Peripherals, A-devices and B-devices use this comparator to detect when a session is started. The A-device also uses this comparator to determine when a session is completed. The session valid threshold of the ISP1504x1 is $V_{A\_SESS\_VLD}$, with a hysteresis of $V_{hys(A\_SESS\_VLD)}$.

7.6.2.3 Session end comparator

The ISP1504x1 session end comparator determines when V_{BUS} is below the B-device session end threshold. The B-device uses this threshold to determine when a session has ended. The session end threshold of the ISP1504x1 is $V_{B\_SESS\_END}$.

7.6.3 SRP charge and discharge resistors

The ISP1504x1 provides on-chip resistors for short-term charging and discharging of V_{BUS}. These are used by the B-device to request a session, prompting the A-device to restore the V_{BUS} power. First, the B-device makes sure that V_{BUS} is fully discharged from the previous session by setting the DISCHRG_VBUS register bit to logic 1 and waiting for SESS_END to be logic 1. Then the B-device charges V_{BUS} by setting the CHRG_VBUS register bit to logic 1. The A-device sees that V_{BUS} is charged above the session valid threshold and starts a session by turning on the V_{BUS} power.

7.7 Band gap reference voltage

The band gap circuit provides a stable internal voltage reference to bias analog circuitry. The band gap requires an accurate external reference resistor. Connect a 12 kΩ ± 1 % resistor between the RREF pin and GND.

7.8 Power-On Reset (POR)

The ISP1504x1 has an internal POR circuit that resets all internal logic on power-up. The ULPI interface is also reset on power-up.

Remark: When CLOCK starts toggling after power-up, the USB link must issue a reset command over the ULPI bus to ensure correct operation of the ISP1504x1.

7.9 Detailed description of pins

7.9.1 DATA[7:0]

Bidirectional data bus. The USB link must drive DATA[7:0] to LOW when the ULPI bus is idle. When the link has data to transmit to the PHY, it drives a nonzero value.

The data bus can be reconfigured to carry various data types, as given in Section 8 and Section 9.

The DATA[7:0] pins can be 3-stated by driving pin CS_N/PWRDN to HIGH. Weak pull-down resistors are incorporated into the DATA[7:0] pins as part of the interface protect feature. For details, see Section 9.3.1.

7.9.2 $V_{CC(I/O)}$

The input voltage that sets the I/O voltage level. The ISP1504x1 supports nominal I/O voltages in the range of 1.8 V to 3.3 V. A 0.1 µF decoupling capacitor is recommended. $V_{CC(I/O)}$ provides power to on-chip pads of the following pins:

- CLOCK
- CS_N/PWRDN
- DATA[7:0]
- DIR
- NXT
- RESET_N
- STP

If $V_{CC(I/O)}$ is not present while V_{CC} is present, the chip is put in power-down mode.

7.9.3 RREF

Resistor reference analog I/O pin. A 12 kΩ ± 1 % resistor must be connected between RREF and GND, as shown in Section 15. This provides an accurate voltage reference that biases internal analog circuitry. Less accurate resistors cannot be used and will render the ISP1504x1 unusable.

7.9.4 DP and DM

DP (data plus) and DM (data minus) are USB differential data pins. These must be connected to the D+ and D– pins of the USB receptacle.

7.9.5 FAULT

If an external V_{BUS} overcurrent or fault circuit is used, the output fault indicator of that circuit can be connected to the ISP1504x1 FAULT input pin. The ISP1504x1 will inform the link of V_{BUS} fault events by sending RXCMDs on the ULPI bus. To use the FAULT pin, the link must set the USE_EXT_VBUS_IND register bit to logic 1, and the polarity of the external fault signal must be set using the IND_COMPL register bit.

7.9.6 ID

For OTG implementations, the ID (identification) pin is connected to the ID pin of the micro-USB receptacle. As defined in *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.2*, the ID pin dictates the initial role of the link. If ID is detected as HIGH, the link must assume the role of a peripheral. If ID is detected as LOW, the link must assume a host role. Roles can be swapped at a later time by using HNP.

If the ISP1504x1 is not used as an OTG PHY, but as a standard USB host or peripheral PHY, it is recommended to connect the ID pin to REG3V3.

7.9.7 V_{CC}

V_{CC} is the main input supply voltage for the ISP1504x1. A 0.1 µF decoupling capacitor is recommended. For details, see Section 15.

7.9.8 PSW_N

PSW_N is an active LOW, open-drain output pin. This pin can be connected to an active LOW, external V_{BUS} switch or charge pump enable circuit to control the external V_{BUS} power source.

If the link is in host mode, it can enable the external power switch by setting the DRV_VBUS_EXT bit in the OTG Control register to logic 1. The ISP1504x1 will drive PSW_N to LOW to enable the external switch. If the link detects an overcurrent condition (the V_{BUS} state in RXCMD is not 11b), it must disable the external V_{BUS} supply by setting DRV_VBUS_EXT to logic 0.

An external pull-up resistor, R_{pullup}, is required when PSW_N is used. This pin is open-drain, allowing ganged mode power control for multiple USB ports.

7.9.9 V_{BUS}

This pin acts as an input to V_{BUS} comparators, and also as a power pin for SRP charge and discharge resistors.

The V_{BUS} pin requires a capacitive load. Table 3 provides the recommended capacitor for various applications.

Table 3. Recommended V_{BUS} capacitor value

Application	V_{BUS} capacitor (C_{VBUS})
OTG	1 µF to 6.5 µF, 10 V
Standard host	120 µF ± 20 %, 10 V
Standard peripheral	1 µF to 10 µF, 10 V

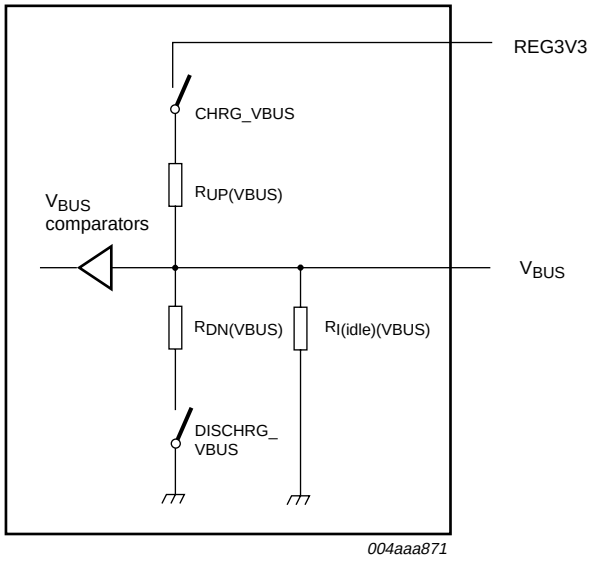


Fig 3. Application circuit components

7.9.10 REG3V3 and REG1V8

Regulator output voltage. These supplies are used to power the ISP1504x1 internal digital and analog circuits, and must not be used to power external circuits.

For correct operation of the regulator, it is recommended that you connect REG3V3 and REG1V8 to a 0.1 µF capacitor in parallel with a 4.7 µF capacitor. For examples, see Section 15.

7.9.11 XTAL1 and XTAL2

XTAL1 is the crystal input, and XTAL2 is the crystal output. The allowed frequency on the XTAL1 pin is 19.2 MHz or 26 MHz.

Either a crystal must be attached, or a clock of the same frequency must be driven into XTAL1, with XTAL2 left floating.

If a crystal is attached, it requires capacitors to GND on each terminal of the crystal. For details, see Section 15.

7.9.12 RESET_N

An active LOW asynchronous reset pin that resets all circuits in the ISP1504x1. The RESET_N pin must be connected to $V_{CC(I/O)}$, if not used. The ISP1504x1 contains an internal power-on reset circuit, and therefore using the RESET_N pin is optional.

For details on using RESET_N, see Section 9.3.2.

7.9.13 DIR

ULPI direction output pin. Controls the direction of the data bus. By default, the ISP1504x1 holds DIR at LOW, causing the data bus to be an input. When DIR is LOW, the ISP1504x1 listens for data from the link. The ISP1504x1 pulls DIR to HIGH only when it has data to send to the link, which is for one of two reasons:

- To send the USB receive data, RXCMD status updates and register read data to the link.
- To block the link from driving the data bus during power-up, reset and low-power mode (suspend).

For details on DIR usage, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

7.9.14 STP

ULPI stop input pin. The link must assert STP to signal the end of a USB transmit packet or a register write operation. When DIR is asserted, the link can optionally assert STP to abort the ISP1504x1, causing it to de-assert DIR in the next clock cycle. A weak pull-up resistor is incorporated into the STP pin as part of the interface protect feature. For details, see Section 9.3.1.

For details on STP usage, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

7.9.15 NXT

ULPI next data output pin. The ISP1504x1 holds NXT at LOW, by default. When DIR is LOW and the link is sending data to the ISP1504x1, NXT will be asserted to notify the link to provide the next data byte. When DIR is HIGH and the ISP1504x1 is sending data to the link, NXT will be asserted to notify the link that another valid byte is on the bus. NXT is not used for register read data or the RXCMD status update.

For details on NXT usage, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

7.9.16 CLOCK

A 60 MHz interface clock to synchronize the ULPI bus.

7.9.17 CS_N/PWRDN

Active LOW chip select pin. When CS_N/PWRDN is HIGH, ULPI output pins DATA[7:0], CLOCK, DIR and NXT are 3-stated and ignored. All internal circuits, including the internal regulator, are powered down. When CS_N/PWRDN is LOW, the ISP1504x1 will wake up and the ULPI bus will operate normally.

If CS_N/PWRDN is not used, it must be connected to LOW. For more information on using CS_N/PWRDN, see Section 9.3.3.

7.9.18 GND

Power and signal ground. To ensure correct operation of the ISP1504x1, GND must be soldered to the cleanest ground available.

8. Modes of operation

8.1 ULPI modes

The ISP1504x1 ULPI bus can be programmed to operate in five modes. Each mode reconfigures the signals on the data bus as described in the following subsections. Setting more than one mode will lead to undefined behavior.

8.1.1 Synchronous mode

This is default mode. At power-up, and when CLOCK is stable, the ISP1504x1 will enter synchronous mode. The link must synchronize all ULPI signals to CLOCK, meeting the set-up and hold times as defined in Section 14. A description of the ULPI pin behavior in synchronous mode is given in Table 4.

This mode is used by the link to perform the following tasks:

- High-speed detection handshake (chirp)
- Transmit and receive USB packets
- Read and write to registers
- Receive USB status updates (RXCMDs)

For more information on various synchronous mode protocols, see Section 9.

Table 4. ULPI signal description

Signal name	Direction on ISP1504x1	Signal description
CLOCK	O	**60 MHz interface clock**: During low-power and serial modes, the clock can be turned off to save power.
DATA[7:0]	I/O	**8-bit data bus**: In synchronous mode, the link drives DATA[7:0] to LOW by default. The link initiates transfers by sending a nonzero data pattern called TXCMD (transmit command). In synchronous mode, the direction of DATA[7:0] is controlled by DIR. Contents of DATA[7:0] lines must be ignored for exactly one clock cycle whenever DIR changes value. This is called the turnaround cycle. Data lines have fixed direction and different meaning in low-power and serial modes.

Table 4. ULPI signal description *…continued*

Signal name	Direction on ISP1504x1	Signal description
DIR	O	**Direction**: Controls the direction of data bus DATA[7:0]. In synchronous mode, the ISP1504x1 drives DIR to LOW by default, making the data bus an input so that the ISP1504x1 can listen for TXCMDs from the link. The ISP1504x1 drives DIR to HIGH only when it has data for the link. When DIR and NXT are HIGH, the byte on the data bus contains decoded USB data. When DIR is HIGH and NXT is LOW, the byte contains status information called RXCMD (receive command). The only exception to this rule is when the PHY returns register read data, where NXT is also LOW, replacing the usual RXCMD byte. Every change in DIR causes a turnaround cycle on the data bus, during which DATA[7:0] is not valid and must be ignored by the link. DIR is always asserted during low-power and serial modes.
STP	I	**Stop**: In synchronous mode, the link drives STP to HIGH for one cycle after the last byte of data is sent to the ISP1504x1. The link can optionally assert STP to force DIR to be de-asserted. In low-power and serial modes, the link holds STP at HIGH to wake up the ISP1504x1, causing the ULPI bus to return to synchronous mode.
NXT	O	**Next**: In synchronous mode, the ISP1504x1 drives NXT to HIGH to throttle data. If DIR is LOW, the ISP1504x1 asserts NXT to notify the link to place the next data byte on DATA[7:0] in the following clock cycle. If DIR is HIGH, the ISP1504x1 asserts NXT to notify the link that a valid USB data byte is on DATA[7:0] in the current cycle. The ISP1504x1 always drives an RXCMD when DIR is HIGH and NXT is LOW, unless register read data is to be returned to the link in the current cycle. NXT is not used in low-power or serial mode.

8.1.2 Low-power mode

When the USB is idle, the link can place the ISP1504x1 into low-power mode (also called suspend mode). In low-power mode, the data bus definition changes to that shown in Table 5. To enter low-power mode, the link sets the SUSPENDM bit in the Function Control register to logic 0. To exit low-power mode, the link asserts the STP signal. The ISP1504x1 will draw only suspend current from the V_{CC} supply (see Table 46).

During low-power mode, the clock on XTAL1 may be stopped. The clock must be started again before asserting STP to exit low-power mode. After exiting low-power mode, the ISP1504x1 will send an RXCMD to the link if a change was detected in any interrupt source, and the change still exists. An RXCMD may not be sent if the interrupt condition is removed before exiting.

For more information on low-power mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 5. Signal mapping during low-power mode

Signal	Maps to	Direction	Description
LINESTATE0	DATA0	O	combinatorial LINESTATE0 directly driven by the analog receiver
LINESTATE1	DATA1	O	combinatorial LINESTATE1 directly driven by the analog receiver
Reserved	DATA2	O	reserved; the ISP1504x1 will drive this pin to LOW
INT	DATA3	O	active HIGH interrupt indication; will be asserted whenever any unmasked interrupt occurs

8.1.3 6-pin full-speed or low-speed serial mode

If the link requires a 6-pin serial interface to transmit and receive full-speed or low-speed USB data, it can set the ISP1504x1 to 6-pin serial mode. In 6-pin serial mode, the data bus definition changes to that shown in Table 6. To enter 6-pin serial mode, the link sets the 6PIN_FSLS_SERIAL bit in the Interface Control register to logic 1. To exit 6-pin serial mode, the link asserts STP. This is provided primarily for links that contain legacy full-speed or low-speed functionality, providing a more cost-effective upgrade path to high-speed. An interrupt pin is also provided to inform the link of USB events. If the link requires CLOCK to be running during 6-pin serial mode, the CLOCK_SUSPENDM register bit must be set to logic 1.

For more information on 6-pin serial mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 6. Signal mapping for 6-pin serial mode

Signal	Maps to	Direction	Description
TX_ENABLE	DATA0	I	active HIGH transmit enable
TX_DAT	DATA1	I	transmit differential data on DP and DM
TX_SE0	DATA2	I	transmit single-ended zero on DP and DM
INT	DATA3	O	active HIGH interrupt indication; will be asserted whenever any unmasked interrupt occurs
RX_DP	DATA4	O	single-ended receive data from DP
RX_DM	DATA5	O	single-ended receive data from DM
RX_RCV	DATA6	O	differential receive data from DP and DM
Reserved	DATA7	O	reserved; the ISP1504x1 will drive this pin to LOW

8.1.4 3-pin full-speed or low-speed serial mode

If the link requires a 3-pin serial interface to transmit and receive full-speed or low-speed USB data, it can set the ISP1504x1 to 3-pin serial mode. In 3-pin serial mode, the data bus definition changes to that shown in Table 7. To enter 3-pin serial mode, the link sets the 3PIN_FSLS_SERIAL bit in the Interface Control register to logic 1. To exit 3-pin serial mode, the link asserts STP. This is provided primarily for links that contain legacy full-speed or low-speed functionality, providing a more cost-effective upgrade path to high-speed. An interrupt pin is also provided to inform the link of USB events. If the link requires CLOCK to be running during 3-pin serial mode, the CLOCK_SUSPENDM register bit must be set to logic 1.

For more information on 3-pin serial mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 7. Signal mapping for 3-pin serial mode

Signal	Maps to	Direction	Description
TX_ENABLE	DATA0	I	active HIGH transmit enable
DAT	DATA1	I/O	transmit differential data on DP and DM when TX_ENABLE is HIGH receive differential data from DP and DM when TX_ENABLE is LOW
SE0	DATA2	I/O	transmit single-ended zero on DP and DM when TX_ENABLE is HIGH receive single-ended zero from DP and DM when TX_ENABLE is LOW
INT	DATA3	O	active HIGH interrupt indication; will be asserted whenever any unmasked interrupt occurs
Reserved	DATA[7:4]	O	reserved; the ISP1504x1 will drive these pins to LOW

8.1.5 Power-down mode

In this mode, the PHY will 3-state the DATA[7:0], CLOCK, NXT and DIR pins. The link can reuse the 3-stated pins for other purposes. To enter power-down mode, the link must drive the CS_N/PWRDN pin to HIGH. To exit power-down mode, the link must drive the CS_N/PWRDN pin to LOW.

In this mode, the ISP1504x1 will do the following:

- All internal circuits, including the internal regulator, are powered down. The total current from V_{CC} is less than 10 μA.
- The DATA[7:0], NXT, CLOCK and DIR pins are 3-stated and ignored. The STP pin is ignored.
- The pull-down resistors on DATA[7:0] are disabled.
- USB wake-up events cannot be detected. The link must first wake up the ISP1504x1 by driving CS_N/PWRDN to LOW.

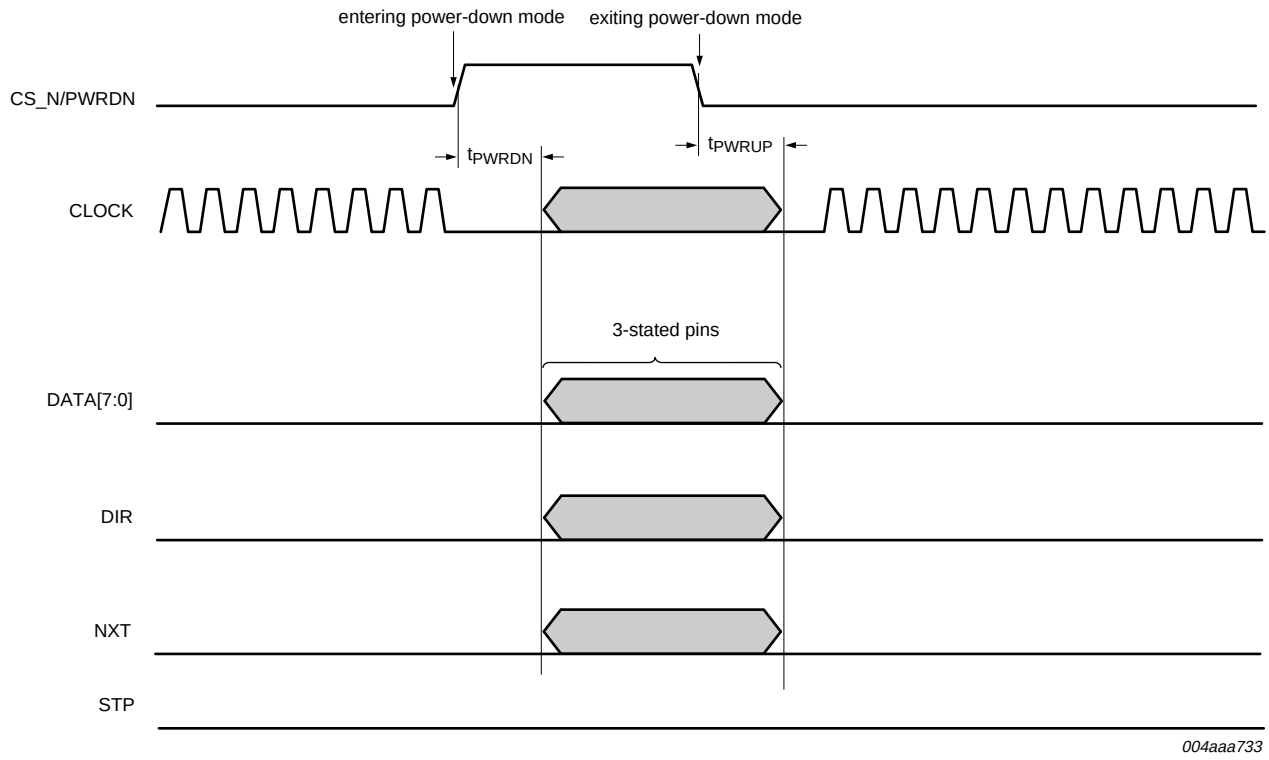


Fig 4. Entering and exiting 3-state in normal mode

8.2 USB state transitions

A Hi-Speed USB host or an OTG device handles more than one electrical state as defined in *Universal Serial Bus Specification Rev. 2.0* and *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.2*. The ISP1504x1 accommodates various states through the register bit settings of XCVRSELECT[1:0], TERMSELECT, OPMODE[1:0], DP_PULLDOWN and DM_PULLDOWN.

Table 8 summarizes operating states. The values of register settings in Table 8 will force resistor settings as also given in Table 8. Resistor setting signals are defined as follows:

- RPU_DP_EN enables the 1.5 kΩ pull-up resistor on DP
- RPD_DP_EN enables the 15 kΩ pull-down resistor on DP
- RPD_DM_EN enables the 15 kΩ pull-down resistor on DM
- HSTERM_EN enables the 45 Ω termination resistors on DP and DM

It is up to the link to set the desired register settings.

Table 8. Operating states and corresponding resistor settings

Signaling mode	Register settings					Internal resistor settings			
	XCVR SELECT [1:0]	TERM SELECT	OPMODE [1:0]	DP_ PULL DOWN	DM_ PULL DOWN	RPU_DP _EN	RPD_DP _EN	RPD_ DM_EN	HSTERM_ EN
General settings									
3-state drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b
Power up or V_{BUS} < $V_{B\_SESS\_END}$	01b	0b	00b	1b	1b	0b	1b	1b	0b
Host settings									
Host chirp	00b	0b	10b	1b	1b	0b	1b	1b	1b
Host high-speed	00b	0b	00b	1b	1b	0b	1b	1b	1b
Host full-speed	X1b	1b	00b	1b	1b	0b	1b	1b	0b
Host high-speed or full-speed suspend	01b	1b	00b	1b	1b	0b	1b	1b	0b
Host high-speed or full-speed resume	01b	1b	10b	1b	1b	0b	1b	1b	0b
Host low-speed	10b	1b	00b	1b	1b	0b	1b	1b	0b
Host low-speed suspend	10b	1b	00b	1b	1b	0b	1b	1b	0b
Host low-speed resume	10b	1b	10b	1b	1b	0b	1b	1b	0b
Host Test J or Test K	00b	0b	10b	1b	1b	0b	1b	1b	1b
Peripheral settings									
Peripheral chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b
Peripheral high-speed	00b	0b	00b	0b	0b	0b	0b	0b	1b
Peripheral full-speed	01b	1b	00b	0b	0b	1b	0b	0b	0b
Peripheral high-speed or full-speed suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b
Peripheral high-speed or full-speed resume	01b	1b	10b	0b	0b	1b	0b	0b	0b
Peripheral Test J or Test K	00b	0b	10b	0b	0b	0b	0b	0b	1b
OTG settings									
OTG device peripheral chirp	00b	1b	10b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed	00b	0b	00b	0b	1b	0b	0b	1b	1b
OTG device peripheral full-speed	01b	1b	00b	0b	1b	1b	0b	1b	0b

Table 8. Operating states and corresponding resistor settings *…continued*

Signaling mode	Register settings					Internal resistor settings			
	XCVR SELECT [1:0]	TERM SELECT	OPMODE [1:0]	DP_ PULL DOWN	DM_ PULL DOWN	RPU_DP _EN	RPD_DP _EN	RPD_ DM_EN	HSTERM_ EN
OTG device peripheral high-speed and full-speed suspend	01b	1b	00b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed and full-speed resume	01b	1b	10b	0b	1b	1b	0b	1b	0b
OTG device peripheral Test J or Test K	00b	0b	10b	0b	1b	0b	0b	1b	1b

9. Protocol description

This following subsections describe the protocol for using the ISP1504x1.

9.1 ULPI references

The ISP1504x1 provides a 12-pin ULPI interface to communicate with the link. It is highly recommended that you read *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1* and *UTMI+ Specification Rev. 1.0*.

9.2 Power-On Reset (POR)

An internal POR is generated when REG1V8 rises above $V_{POR(trip)}$ for at least $t_{w(REG1V8\_H)}$. The internal POR pulse will also be generated whenever REG1V8 drops below $V_{POR(trip)}$ for more than $t_{w(REG1V8\_L)}$, and then rises above $V_{POR(trip)}$ again. The voltage on REG1V8 is generated from V_{CC}.

To give a better view of the functionality, Figure 5 shows a possible curve of REG1V8. The internal POR starts with logic 0 at t0. At t1, the detector will see the passing of the trip level so that POR turns to logic 1 and a delay element will add another t_{PORP} before it drops to logic 0. If REG1V8 dips from t2 to t3 for > $t_{w(REG1V8\_L)}$, another POR pulse is generated. If the dip at t4 to t5 is too short, that is, < $t_{w(REG1V8\_L)}$, the internal POR pulse will not react and will remain LOW.

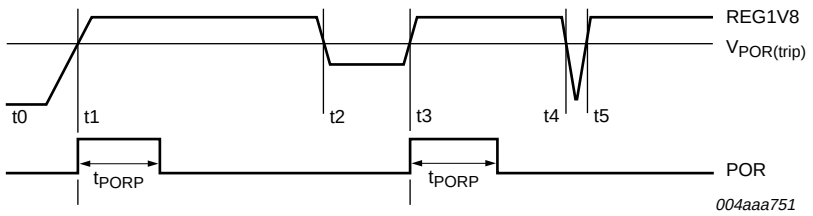


Fig 5. Internal power-on reset timing

9.3 Power-up, reset and bus idle sequence

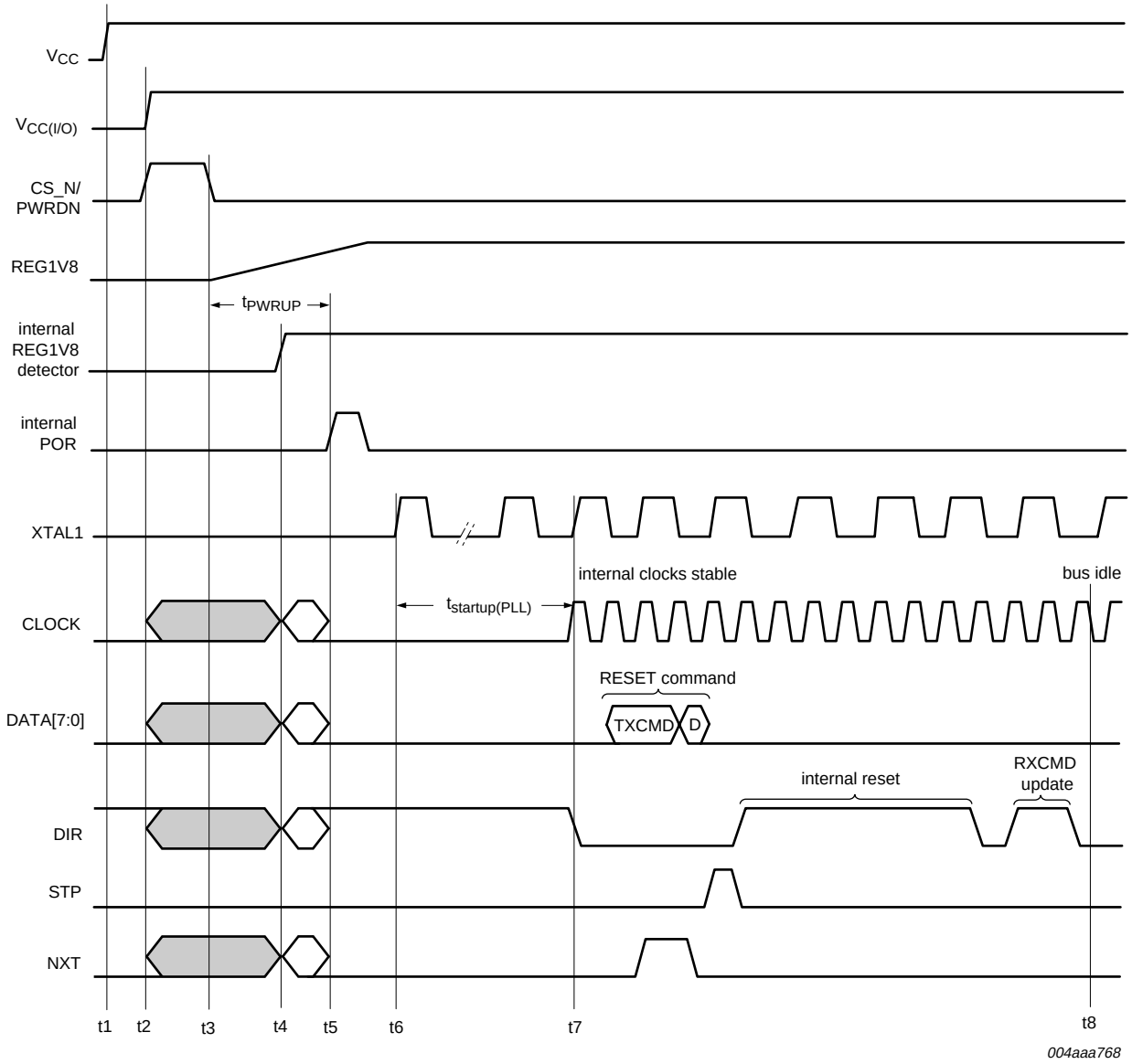
Figure 6 shows a typical start-up sequence.

On power-up, the ISP1504x1 performs an internal power-on reset and asserts DIR to indicate to the link that the ULPI bus cannot be used. When the internal PLL is stable, the ISP1504x1 de-asserts DIR and outputs 60 MHz on the CLOCK pin. The power-up time depends on the V_{CC} supply rise time, the crystal start-up time, and the PLL start-up time ($t_{startup(o)(CLOCK)}$). Whenever DIR is asserted, the ISP1504x1 drives the NXT pin to LOW and drives DATA[7:0] with RXCMD values. When DIR is de-asserted, the link must drive the data bus to a valid level. By default, the link must drive data to LOW. When the ISP1504x1 initially de-asserts DIR on power-up, the link must ignore all RXCMDs until it resets the ISP1504x1. Before beginning USB packets, the link must set the RESET bit in the Function Control register to reset the ISP1504x1. After the RESET bit is set, the ISP1504x1 will assert DIR until the internal reset completes. The ISP1504x1 will automatically de-assert DIR and clear the RESET bit when reset has completed. After every reset, an RXCMD is sent to the link to update USB status information. After this sequence, the ULPI bus is ready for use and the link can start USB operations.

The recommended power-up sequence for the link is:

1. The CS_N/PWRDN pin transitions from HIGH to LOW.
2. The link waits for 1 ms, ignoring all the ULPI pin status.
3. The link may start to detect DIR status level. If DIR is detected LOW for three clock cycles, the link may send a RESET command.
4. The ULPI interface is ready for use.

For details on power-up sequence, see Figure 6.



t1 = V_{CC} is applied to the ISP1504x1.

t2 = $V_{CC(I/O)}$ is turned on. ULPI interface pins (CLOCK, DATA[7:0], DIR and NXT) are in 3-state as long as CS_N/PWRDN is HIGH.

t3 = CS_N/PWRDN turns from HIGH to LOW. The ISP1504x1 regulator starts to turn on.

t4 = ULPI pads detect REG1V8 rising above the REG1V8 regulator threshold and are not in 3-state. These pads may drive either LOW or HIGH. It is recommended that the link ignores the ULPI pins status during t_{PWRUP}.

t5 = The POR threshold is reached and a POR pulse is generated. After the POR pulse, ULPI pins are driven to a defined level. DIR is driven to HIGH and the other pins are driven to LOW.

t6 = The 19.2 MHz or 26 MHz input clock starts. This clock may be started any time.

t7 = The internal PLL is stabilized after $t_{startup(PLL)}$. If the 19.2 MHz or 26 MHz clock is started before POR, the internal PLL will be stabilized after $t_{startup(PLL)}$ from POR. The CLOCK pin starts to output 60 MHz. The DIR pin will transition from HIGH to LOW. The link is expected to issue a RESET command to initialize the ISP1504x1.

t8 = The power-up sequence is completed and the ULPI bus interface is ready for use.

Fig 6. Power-up and reset sequence required before the ULPI bus is ready for use

9.3.1 Interface protection

By default, the ISP1504x1 enables a weak pull-up resistor on STP. If the STP pin is unexpectedly HIGH at any time, the ISP1504x1 will protect the ULPI interface by enabling weak pull-down resistors on DATA[7:0].

The interface protect feature prevents unwanted activity of the ISP1504x1 whenever the ULPI interface is not correctly driven by the link. For example, when the link powers up more slowly than the ISP1504x1.

The interface protect feature can be disabled by setting the INTF_PROT_DIS bit to logic 1. If the interface protect feature is not needed, it must be disabled to reduce power consumption.

9.3.2 Interface behavior with respect to RESET_N

The use of the RESET_N pin is optional. When RESET_N is asserted (LOW), the ISP1504x1 will assert DIR. All logic in the ISP1504x1 will be reset, including the analog circuitry and ULPI registers. During reset, the link must drive DATA[7:0] and STP to LOW; otherwise undefined behavior may result. When RESET_N is de-asserted (HIGH), the DIR output will de-assert (LOW) four or five clock cycles later. Figure 7 shows the ULPI interface behavior when RESET_N is asserted (LOW), and when RESET_N is subsequently de-asserted (HIGH). The behavior of Figure 7 applies only when CS_N/PWRDN is asserted (LOW). If RESET_N is not used, it must be tied to $V_{CC(I/O)}$.

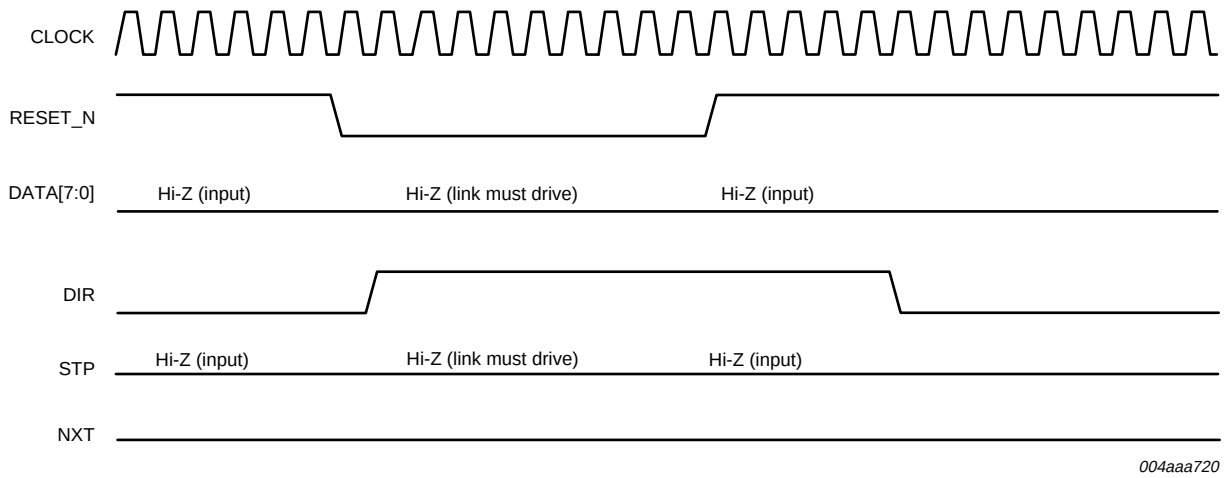


Fig 7. Interface behavior with respect to RESET_N

9.3.3 Interface behavior with respect to CS_N/PWRDN

The use of the CS_N/PWRDN pin is optional. When de-asserted (HIGH), the CS_N/PWRDN pin will 3-state ULPI pins and power down internal circuitry. If CS_N/PWRDN is not used, it must be tied to LOW. Figure 8 shows the ULPI interface behavior when CS_N/PWRDN is asserted (LOW) and when CS_N/PWRDN is subsequently de-asserted (HIGH). The behavior of Figure 8 assumes that RESET_N is de-asserted (HIGH).

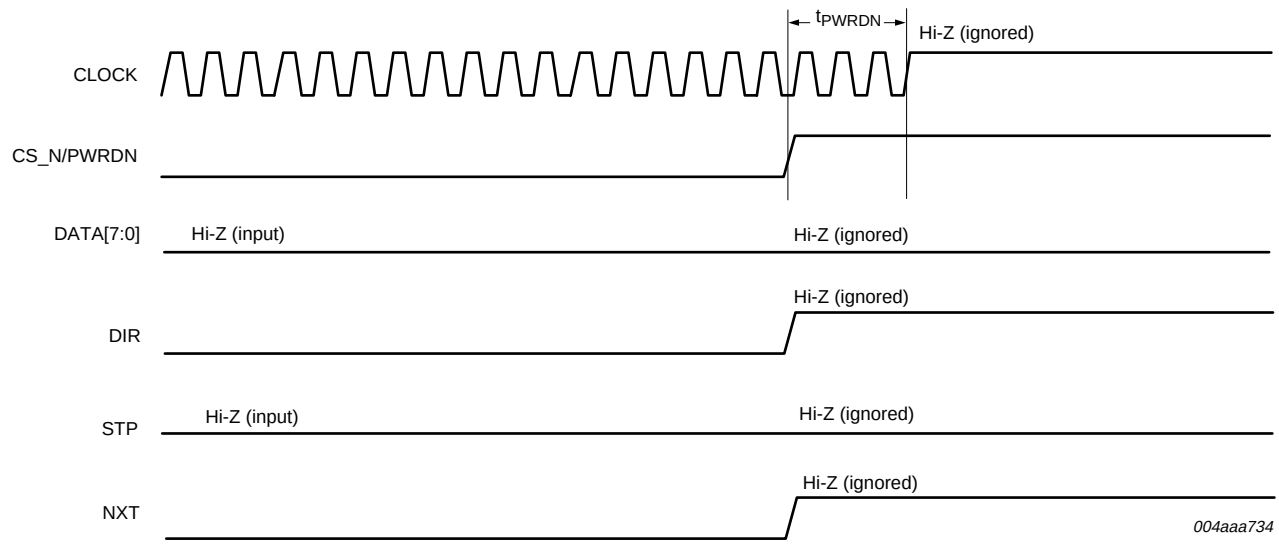


Fig 8. Interface behavior with respect to CS_N/PWRDN

9.4 V_{BUS} power and overcurrent detection

9.4.1 Driving 5 V on V_{BUS}

The ISP1504x1 supports external 5 V supplies. The ISP1504x1 can control the external supply using the active-LOW PSW_N open-drain output pin. To enable the external supply by driving PSW_N to LOW, the link must set the DRV_VBUS_EXT bit in the OTG Control register to logic 1.

Table 9 summarizes settings to drive 5 V on V_{BUS}.

Table 9. OTG Control register power control bits

DRV_VBUS_EXT	Power source used
0	external 5 V V_{BUS} power source disabled (PSW_N = HIGH)
1	external 5 V V_{BUS} power source enabled (PSW_N = LOW)

9.4.2 Fault detection

The ISP1504x1 supports external V_{BUS} fault detector circuits that output a digital fault indicator signal. The indicator signal must be connected to the FAULT pin. To enable the ISP1504x1 to monitor the digital fault input, the link must set the USE_EXT_VBUS_IND bit in the OTG Control register and the IND_PASSTHRU bit in the Interface Control register to logic 1. For details, see Figure 10.

The FAULT input pin is mapped to the A_VBUS_VLD bit in RXCMD. Any changes for the FAULT input will trigger RXCMD carrying the FAULT condition with A_VBUS_VLD.

9.5 TXCMD and RXCMD

Commands between the ISP1504x1 and the link are described in the following subsections.

9.5.1 TXCMD

By default, the link must drive the ULPI bus to its idle state of 00h. To send commands and USB packets, the link drives a nonzero value on DATA[7:0] to the ISP1504x1 by sending a byte called TXCMD. Commands include USB packet transmissions, and register reads and writes. Once the TXCMD is interpreted and accepted by the ISP1504x1, the NXT signal is asserted and the link can follow up with the required number of data bytes. The TXCMD byte format is given in Table 10. Any values other than those in Table 10 are illegal and will result in undefined behavior.

Various TXCMD packet and register sequences are shown in later sections.

Table 10. TXCMD byte format

Command type name	Command code DATA[7:6]	Command payload DATA[5:0]	Command name	Command description
Idle	00b	00 0000b	NOOP	No operation. 00h is the idle value of the data bus. The link must drive NOOP by default.
Packet transmit	01b	00 0000b	NOPID	Transmit USB data that does not have a PID, such as chirp and resume signaling. The ISP1504x1 starts transmitting only after accepting the next data byte.
		00 XXXXb	PID	Transmit USB packet. DATA[3:0] indicates USB packet identifier PID[3:0].
Register write	10b	10 1111b	EXTW	Extended register write command (optional). The 8-bit address must be provided after the command is accepted.
		XX XXXXb	REGW	Register write command with 6-bit immediate address.
Register read	11b	10 1111b	EXTR	Extended register read command (optional). The 8-bit address must be provided after the command is accepted.
		XX XXXXb	REGR	Register read command with 6-bit immediate address.

9.5.2 RXCMD

The ISP1504x1 communicates status information to the link by asserting DIR and sending an RXCMD byte on the DATA bus. The RXCMD data byte format follows *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1* and is given in Table 11.

The ISP1504x1 will automatically send an RXCMD whenever there is a change in any of the RXCMD data fields. The link must be able to accept an RXCMD at any time; including single RXCMDs, back-to-back RXCMDs, and RXCMDs at any time during USB receive packets when NXT is LOW. An example is shown in Figure 9. For details and diagrams, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

An RXCMD may not be sent when exiting low-power mode or serial mode, if the interrupt condition is removed before exiting.

Table 11. RXCMD byte format

DATA	Name	Description and value
1 to 0	LINESTATE	**LINESTATE signals**: For a definition of LINESTATE, see Section 9.5.2.1. **DATA0 —** LINESTATE[0] **DATA1 —** LINESTATE[1]
3 to 2	V_{BUS} state	**Encoded V_{BUS} voltage state**: For an explanation of the V_{BUS} state, see Section 9.5.2.2.
5 to 4	RxEvent	**Encoded USB event signals**: For an explanation of RxEvent, see Section 9.5.2.4.
6	ID	Set to the value of the ID pin.
7	ALT_INT	By default, this signal is not used and is not needed in typical designs. Optionally, the link can enable the BVALID_RISE and/or BVALID_FALL bits in the Power Control register. Corresponding changes in BVALID will cause an RXCMD to be sent to the link with the ALT_INT bit asserted.

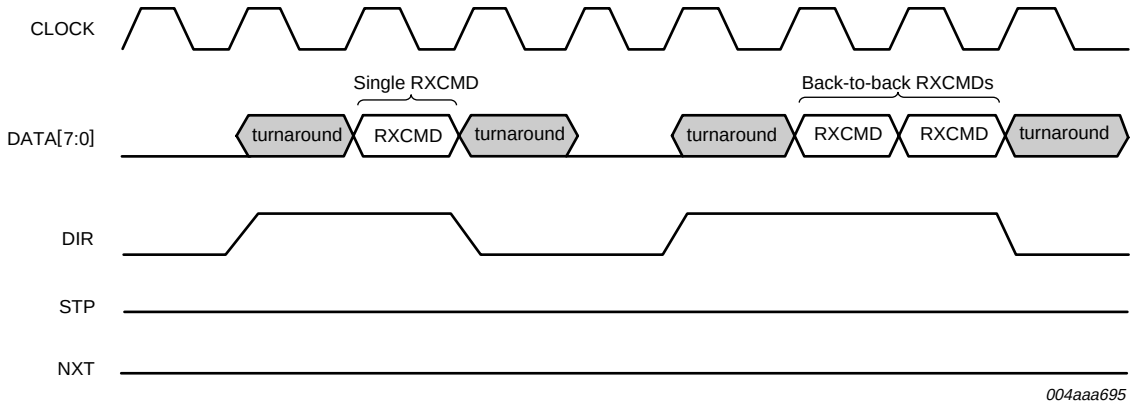


Fig 9. Single and back-to-back RXCMDs from the ISP1504x1 to the link

9.5.2.1 Linestate encoding

LINESTATE[1:0] reflects the current state of DP and DM. Whenever the ISP1504x1 detects a change in DP or DM, an RXCMD will be sent to the link with the new LINESTATE[1:0] value. The value given on LINESTATE[1:0] depends on the setting of various registers. Table 12 shows the LINESTATE[1:0] encoding for upstream facing ports, which applies to peripherals. Table 13 shows the LINESTATE[1:0] encoding for downstream facing ports, which applies to Host Controllers. Dual-role devices must choose the correct table, depending on whether it is in peripheral or host mode.

Table 12. LINESTATE[1:0] encoding for upstream facing ports: peripheral
DP_PULLDOWN = 0.[1]

Mode		Full-speed	High-speed	Chirp
XCVRSELECT[1:0]		01, 11	00	00
TERMSELECT		1	0	1
LINESTATE[1:0]	00	SE0	squelch	squelch
	01	FS-J	!squelch	!squelch and HS_Differential_Receiver_Output
	10	FS-K	invalid	!squelch and !HS_Differential_Receiver_Output
	11	SE1	invalid	invalid

[1] !squelch indicates inactive squelch. !HS_Differential_Receiver_Output indicates inactive HS_Differential_Receiver_Output.

Table 13. LINESTATE[1:0] encoding for downstream facing ports: host
DP_PULLDOWN and DM_PULLDOWN = 1.[1]

Mode		Low-speed	Full-speed	High-speed	Chirp
XCVRSELECT[1:0]		10	01, 11	00	00
TERMSELECT		1	1	0	0
OPMODE[1:0]		X	X	00, 01 or 11	10
LINESTATE[1:0]	00	SE0	SE0	squelch	squelch
	01	LS-K	FS-J	!squelch	!squelch and HS_Differential_Receiver_Output
	10	LS-J	FS-K	invalid	!squelch and !HS_Differential_Receiver_Output
	11	SE1	SE1	invalid	invalid

[1] !squelch indicates inactive squelch. !HS_Differential_Receiver_Output indicates inactive HS_Differential_Receiver_Output.

9.5.2.2 V_{BUS} state encoding

USB devices must monitor the V_{BUS} voltage for purposes such as overcurrent detection, starting a session and SRP. The V_{BUS} state field in the RXCMD is an encoding of the voltage level on V_{BUS}.

The SESS_END and SESS_VLD indicators in the V_{BUS} state are directly taken from internal comparators built-in to the ISP1504x1, and encoded as shown in Table 11 and Table 14.

Table 14. Encoded V_{BUS} voltage state

Value	V_{BUS} voltage	SESS_END	SESS_VLD	A_VBUS_VLD
00	$V_{BUS} < V_{B\_SESS\_END}$	1	0	0
01	$V_{B\_SESS\_END} \leq V_{BUS} < V_{A\_SESS\_VLD}$	0	0	0
10	$V_{A\_SESS\_VLD} \leq V_{BUS} < V_{A\_VBUS\_VLD}$	X	1	0
11	$V_{BUS} \geq V_{A\_VBUS\_VLD}$	X	X	1

The A_VBUS_VLD indicator in the V_{BUS} state provides several options and must be configured based on current draw requirements. A_VBUS_VLD can input from one or more V_{BUS} voltage indicators, as shown in Figure 10.

A description on how to use and select the V_{BUS} state encoding is given in Section 9.5.2.3.

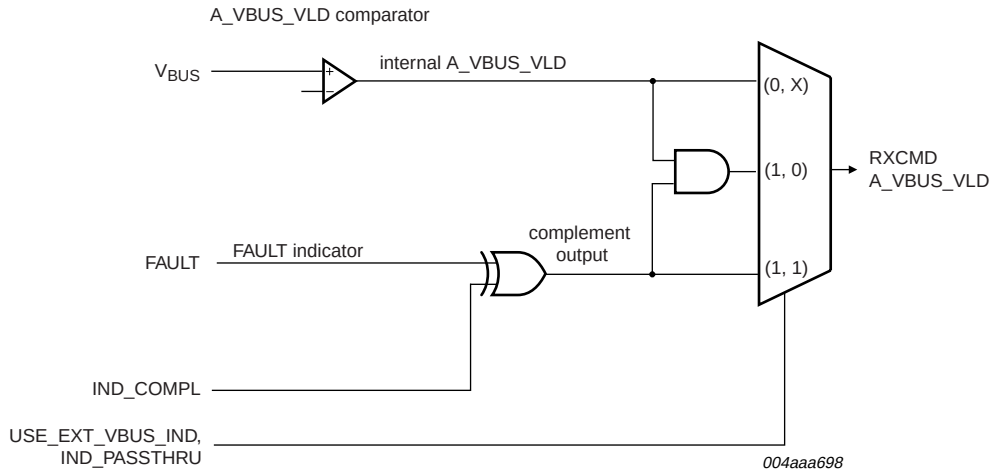


Fig 10. RXCMD A_VBUS_VLD indicator source

9.5.2.3 Using and selecting the V_{BUS} state encoding

The V_{BUS} state encoding is shown in Table 11. The ISP1504x1 will send an RXCMD to the link whenever there is a change in the V_{BUS} state. To receive V_{BUS} state updates, the link must first enable corresponding interrupts in the USB Interrupt Enable Rising Edge and USB Interrupt Enable Falling Edge registers.

The link can use the V_{BUS} state to monitor V_{BUS} and take appropriate action. Table 15 shows the recommended usage for typical applications.

Table 15. V_{BUS} indicators in RXCMD required for typical applications

Application	A_VBUS_VLD	SESS_VLD	SESS_END
Standard host	yes	no	no
Standard peripheral	no	yes	no
OTG A-device	yes	yes	no
OTG B-device	no	yes	yes

Standard USB Host Controllers: For standard hosts, the system must be able to provide 500 mA on V_{BUS} in the range of 4.75 V to 5.25 V. An external circuit must be used to detect overcurrent conditions. If the external overcurrent detector provides a digital fault signal, then the fault signal must be connected to the ISP1504x1 FAULT input pin, and the link must do the following:

1. Set the IND_COMPL bit in the Interface Control register to logic 0 or logic 1, depending on the polarity of the external fault signal.
2. Set the USE_EXT_VBUS_IND bit in the OTG Control register to logic 1.
3. If it is not necessary to qualify the fault indicator with the internal A_VBUS_VLD comparator, set the IND_PASSTHRU bit in the Interface Control register to logic 1.

Standard USB Peripheral Controllers: Standard peripherals must be able to detect when V_{BUS} is at a sufficient level for operation. SESS_VLD must be enabled to detect the start and end of USB peripheral operations. Detection of A_VBUS_VLD and SESS_END thresholds is not needed for standard peripherals.

OTG devices: When an OTG device is configured as an OTG A-device, it must be able to provide a minimum of 8 mA on V_{BUS}. If the OTG A-device provides less than 100 mA, then there is no need for an overcurrent detection circuit because the internal A_VBUS_VLD comparator is sufficient. If the OTG A-device provides more than 100 mA on V_{BUS}, an overcurrent detector must be used and Section "Standard USB Host Controllers" applies. The OTG A-device also uses SESS_VLD to detect when an OTG A-device is initiating V_{BUS} pulsing SRP.

When an OTG device is configured as an OTG B-device, SESS_VLD must be used to detect when V_{BUS} is at a sufficient level for operation. SESS_END must be used to detect when V_{BUS} has dropped to a LOW level, allowing the B-device to safely initiate V_{BUS} pulsing SRP.

9.5.2.4 RxEvent encoding

The RxEvent field (see Table 16) of the RXCMD informs the link of information related packets received on the USB bus. RxActive and RxError are defined in *USB 2.0 Transceiver Macrocell Interface (UTMI) Specification Ver. 1.05*. HostDisconnect is defined in *UTMI+ Specification Rev. 1.0*. A short definition is also given in the following subsections.

Table 16. Encoded USB event signals

Value	RxActive	RxError	HostDisconnect
00	0	0	0
01	1	0	0
11	1	1	0
10	X	X	1

RxActive: When the ISP1504x1 has detected a SYNC pattern on the USB bus, it signals an RxActive event to the link. An RxActive event can be communicated using two methods. The first method is for the ISP1504x1 to simultaneously assert DIR and NXT. The second method is for the ISP1504x1 to send an RXCMD to the link with the RxActive field in RxEvent bits set to logic 1. The link must be able to detect both methods. RxActive frames the receive packet from the first byte to the last byte.

The link must assume that RxActive is set to logic 0 when indicated in an RXCMD or when DIR is de-asserted, whichever occurs first.

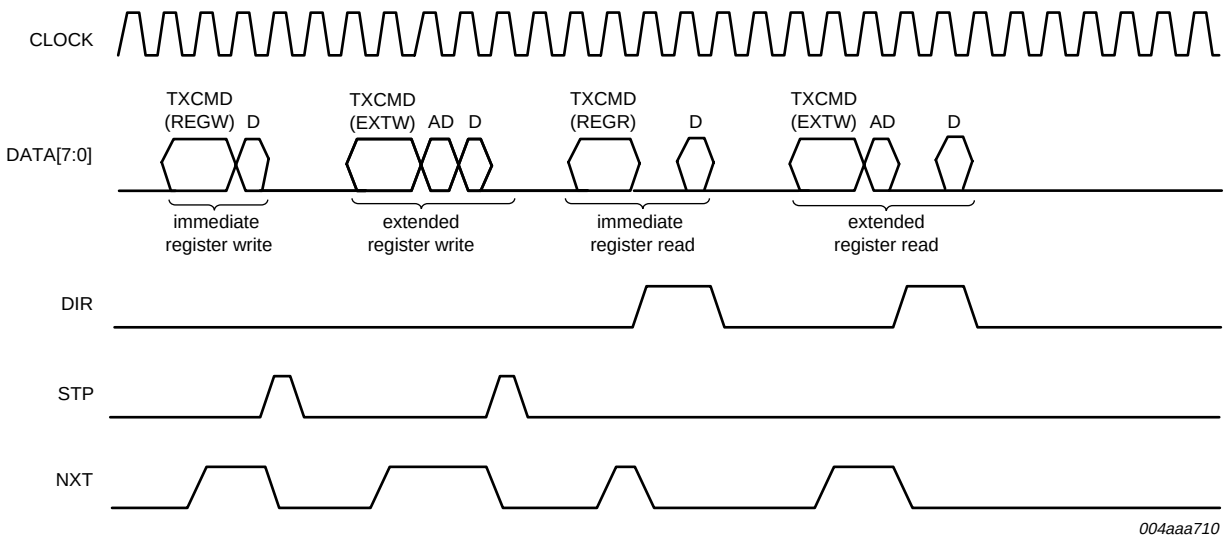
The link uses RxActive to time high-speed packets and ensure that bus turnaround times are met. For more information on the USB packet timing, see Section 9.8.1.

RxError: When the ISP1504x1 has detected an error while receiving a USB packet, it de-asserts NXT and sends an RXCMD with the RxError field set to logic 1. The received packet is no longer valid and must be dropped by the link.

HostDisconnect: HostDisconnect is encoded into the RxEvent field of the RXCMD. HostDisconnect is valid only when the ISP1504x1 is configured as a host (both DP_PULLDOWN and DM_PULLDOWN are set to logic 1), and indicates to the Host Controller when a peripheral is connected or disconnected. The Host Controller must enable HostDisconnect by setting the HOST_DISCON_R and HOST_DISCON_F bits in the USB Interrupt Enable Rising Edge and USB Interrupt Enable Falling Edge registers, respectively. Changes in HostDisconnect will cause the PHY to send an RXCMD to the link with the updated value.

9.6 Register read and write operations

Figure 11 shows register read and write sequences. The ISP1504x1 supports immediate addressing and extended addressing register operations. Extended register addressing is optional for links. Note that register operations will be aborted if the ISP1504x1 asserts DIR during the operation. When a register operation is aborted, the link must retry until successful. For more information on register operations, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.



AD indicates the address byte, and D indicates the data byte.

Fig 11. Example of register write, register read, extended register write and extended register read

9.7 USB reset and high-speed detection handshake (chirp)

Figure 12 shows the sequence of events for USB reset and high-speed detection handshake (chirp). The sequence is shown for hosts and peripherals. Figure 12 does not show all RXCMD updates, and timing is not to scale. The sequence is as follows:

1. USB reset: The host detects a peripheral attachment as low-speed if DM is HIGH and as full-speed if DP is HIGH. If a host detects a low-speed peripheral, it does not follow the remainder of this protocol. If a host detects a full-speed peripheral, it resets the peripheral by writing to the Function Control register and setting XCVRSELECT[1:0] = 00b (high-speed) and TERMSELECT = 0b, which drives SE0 on the bus (DP and DM are connected to ground through 45 Ω). The host also sets OPMODE[1:0] = 10b for correct chirp transmit and receive. The start of SE0 is labeled T_0.

   Remark: To receive chirp signaling, the host must also consider the high-speed differential receiver output. The Host Controller must interpret LINESTATE as shown in Table 13.

2. High-speed detection handshake (chirp)

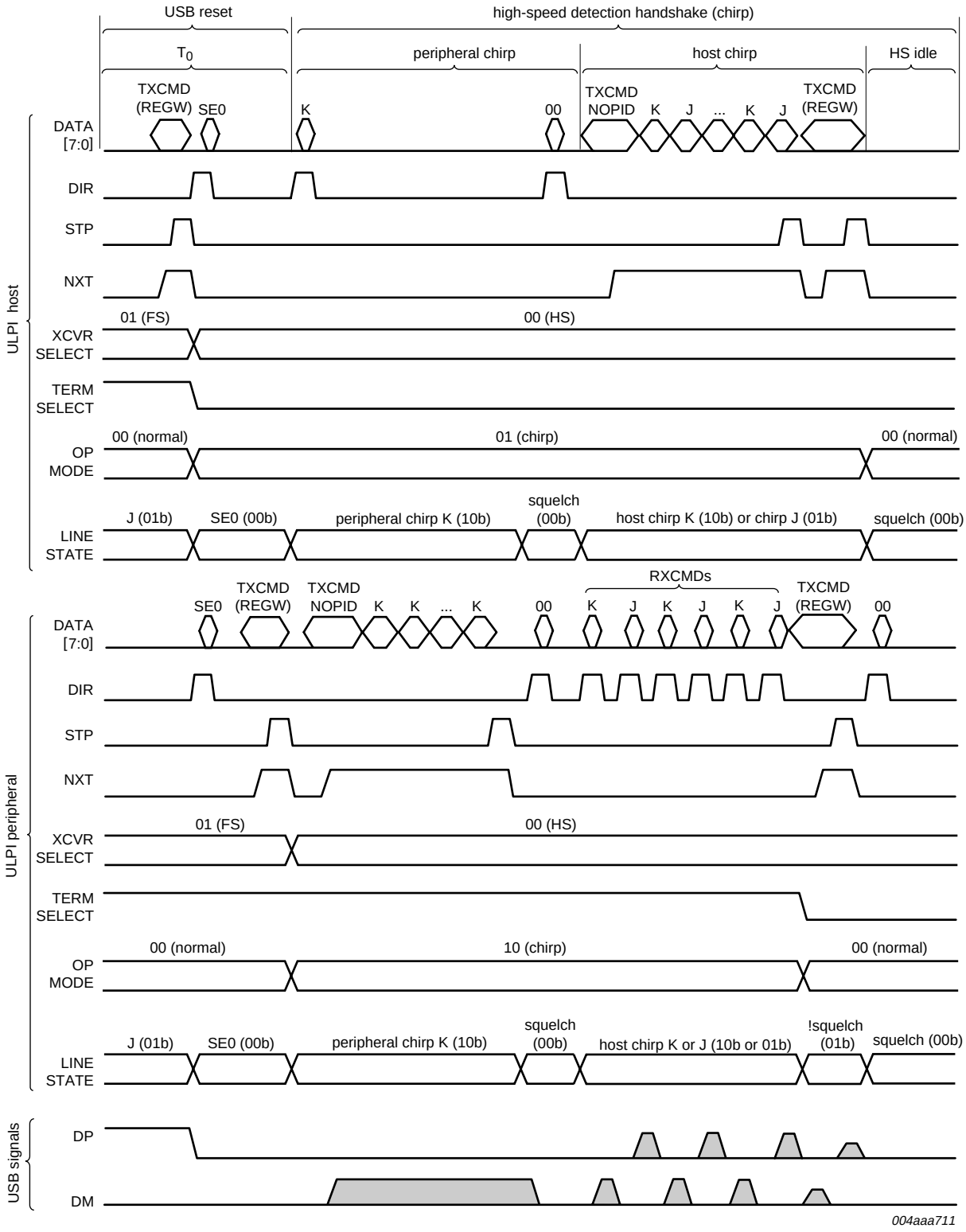
   a. Peripheral chirp: After detecting SE0 for no less than 2.5 μs, if the peripheral is capable of high-speed, it sets XCVRSELECT[1:0] to 00b (high-speed) and OPMODE[1:0] to 10b (chirp). The peripheral immediately follows this with a TXCMD (NOPID), transmitting a Chirp K for no less than 1 ms and ending no more

than 7 ms after reset time T_0. If the peripheral is in low-power mode, it must wake up its clock within 5.6 ms, leaving 200 µs for the link to start transmitting the Chirp K, and 1.2 ms for the Chirp K to complete (worst case with 10 % slow clock).

b. Host chirp: If the host does not detect the peripheral chirp, it must continue asserting SE0 until the end of reset. If the host detects the peripheral Chirp K for no less than 2.5 µs, then no more than 100 µs after the bus leaves the Chirp K state, the host sends a TXCMD (NOPID) with an alternating sequence of Chirp Ks and Js. Each Chirp K or Chirp J must last no less than 40 µs and no longer than 60 µs.

c. High-speed idle: The peripheral must detect a minimum of Chirp K-J-K-J-K-J. Each Chirp K and Chirp J must be detected for at least 2.5 µs. After seeing that minimum sequence, the peripheral sets TERMSELECT = 0b and OPMODE[1:0] = 00b. The peripheral is now in high-speed mode and sees !squelch (01b on LINESTATE). When the peripheral sees squelch (10b on LINESTATE), it knows that the host has completed chirp and waits for high-speed USB traffic to begin. After transmitting the chirp sequence, the host changes OPMODE[1:0] to 00b and begins sending USB packets.

For more information, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.



Timing is not to scale.

Fig 12. USB reset and high-speed detection handshake (chirp) sequence

9.8 USB packet transmit and receive

An example of a packet transmit and receive is shown in Figure 13. For details on USB packets, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

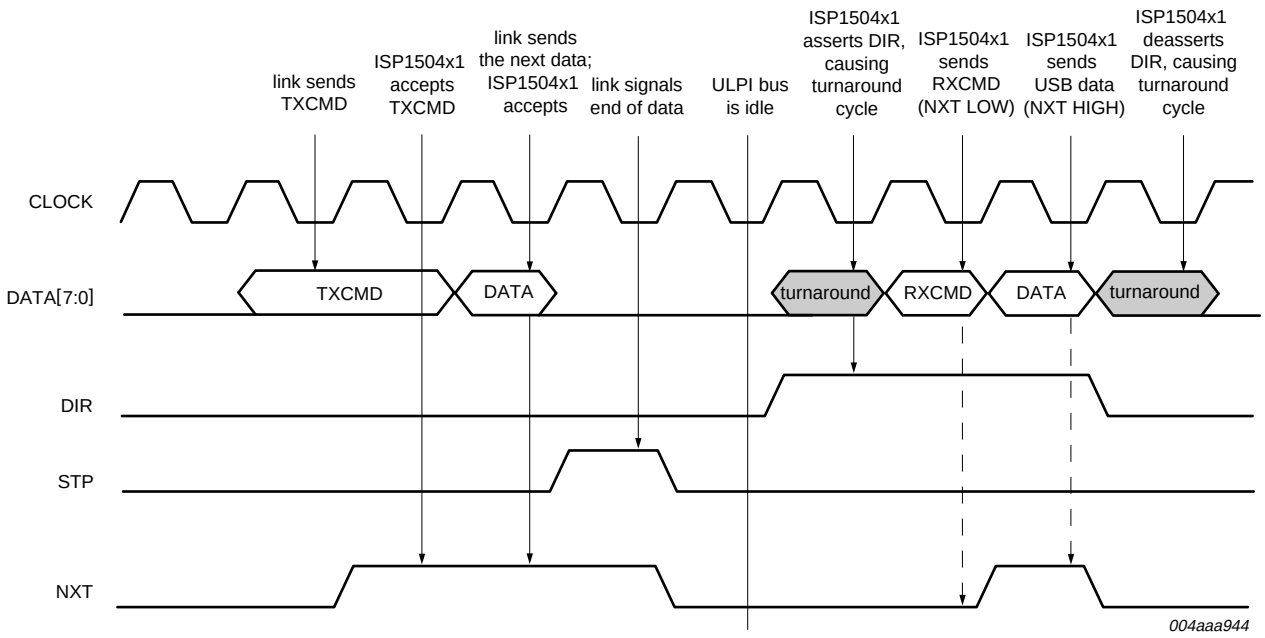


Fig 13. Example of using the ISP1504x1 to transmit and receive USB data

9.8.1 USB packet timing

9.8.1.1 ISP1504x1 pipeline delays

The ISP1504x1 delays are shown in Table 17. For detailed description, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.8.2.6.2*.

Table 17. PHY pipeline delays

Parameter name	High-speed PHY delay	Full-speed PHY delay	Low-speed PHY delay
RXCMD delay (J and K)	4	4	4
RXCMD delay (SE0)	4	4 to 6	16 to 18
TX start delay	1 to 2	6 to 10	74 to 75
TX end delay (packets)	3 to 4	not applicable	not applicable
TX end delay (SOF)	6 to 9	not applicable	not applicable
RX start delay	5 to 6	not applicable	not applicable
RX end delay	5 to 6	17 to 18	122 to 123

9.8.1.2 Allowed link decision time

The amount of clock cycles allocated to the link to respond to a received packet and correctly receive back-to-back packets is given in Table 18. Link designs must follow values given in Table 18 for correct USB system operation. Examples of high-speed packet sequences and timing are shown in Figure 14 and Figure 15. For details, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.8.2.6.3*.

Table 18. Link decision times

Packet sequence	High-speed link delay	Full-speed link delay	Low-speed link delay	Definition
Transmit-Transmit (host only)	15 to 24	7 to 18	77 to 247	Number of clocks a host link must wait before driving the TXCMD for the second packet. In high-speed, the link starts counting from the assertion of STP for the first packet. In full-speed, the link starts counting from the RXCMD, indicating LINESTATE has changed from SE0 to J for the first packet. The timing given ensures inter-packet delays of 2 bit times to 6.5 bit times.
Receive-Transmit (host or peripheral)	1 to 14	7 to 18	77 to 247	Number of clocks the link must wait before driving the TXCMD for the transmit packet. In high-speed, the link starts counting from the end of the receive packet; de-assertion of DIR or an RXCMD indicating RxActive is LOW. In full-speed or low-speed, the link starts counting from the RXCMD, indicating LINESTATE has changed from SE0 to J for the receive packet. The timing given ensures inter-packet delays of 2 bit times to 6.5 bit times.
Receive-Receive (peripheral only)	1	1	1	Minimum number of clocks between consecutive receive packets. The link must be capable of receiving both packets.
Transmit-Receive (host or peripheral)	92	80	718	Host or peripheral transmits a packet and will time-out after this amount of clock cycles if a response is not received. Any subsequent transmission can occur after this time.

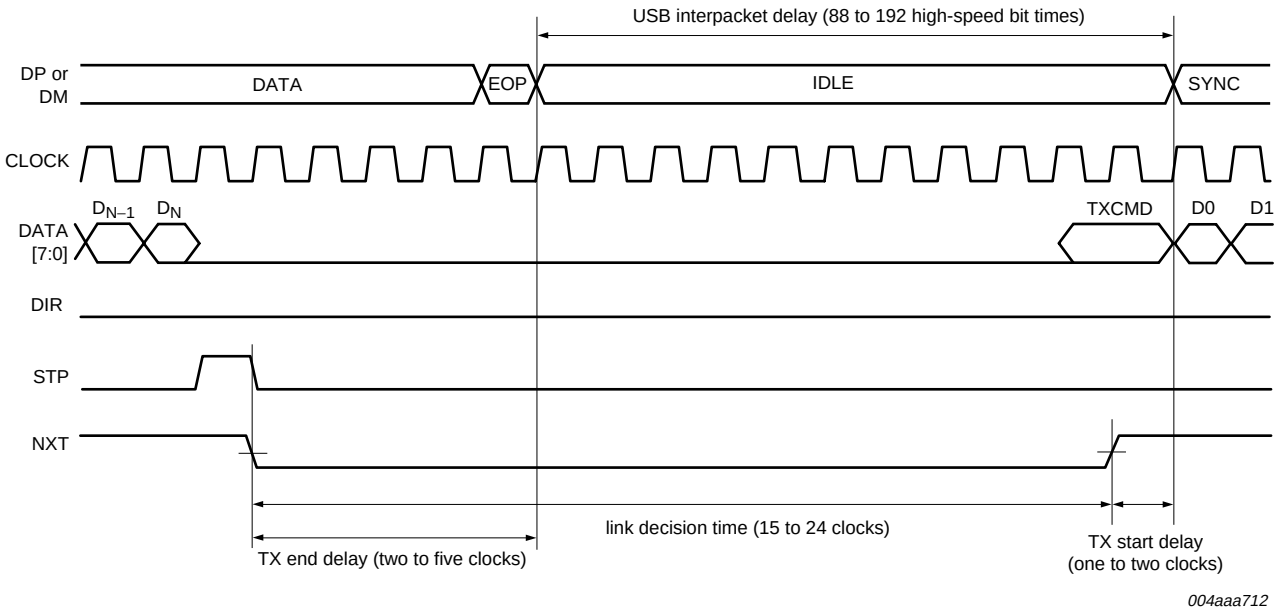


Fig 14. High-speed transmit-to-transmit packet timing

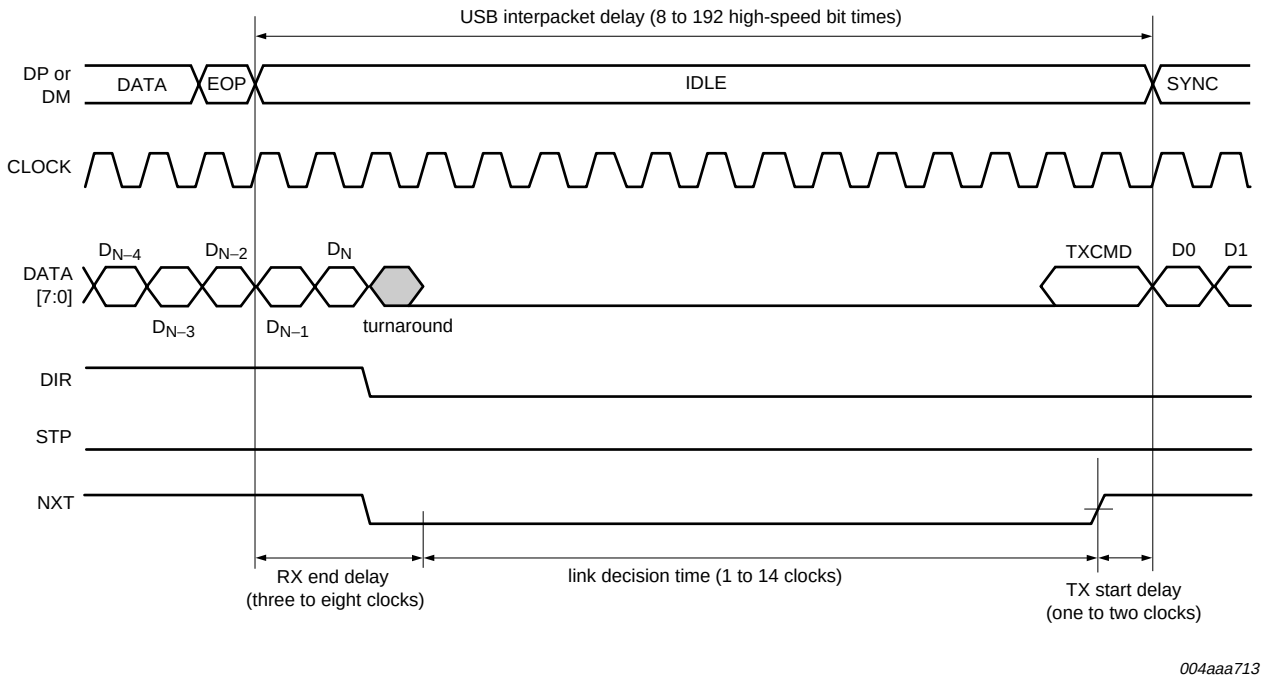
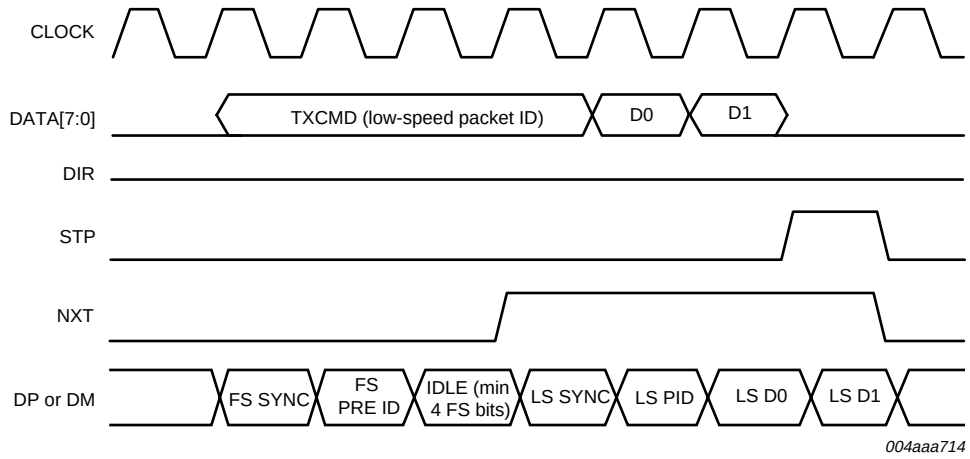


Fig 15. High-speed receive-to-transmit packet timing

9.9 Preamble

Preamble packets are headers to low-speed packets that must travel over a full-speed bus, between a host and a hub. To enter preamble mode, the link sets XCVRSELECT[1:0] = 11b in the Function Control register. When in preamble mode, the ISP1504x1 operates just as in full-speed mode, and sends all data with full-speed rise and fall times. Whenever the link transmits a USB packet in preamble mode, the ISP1504x1 will automatically send a preamble header at full-speed bit rate before sending the link packet at low-speed bit rate. The ISP1504x1 will ensure a minimum gap of four full-speed bit times between the last bit of the full-speed PRE PID and the first bit of the low-speed packet SYNC. The ISP1504x1 will drive a J for at least one full-speed bit time after sending the PRE PID, after which the pull-up resistor can hold the J state on the bus. An example transmit packet is shown in Figure 16.

In preamble mode, the ISP1504x1 can also receive low-speed packets from the full-speed bus.



DP and DM timing is not to scale.

Fig 16. Preamble sequence

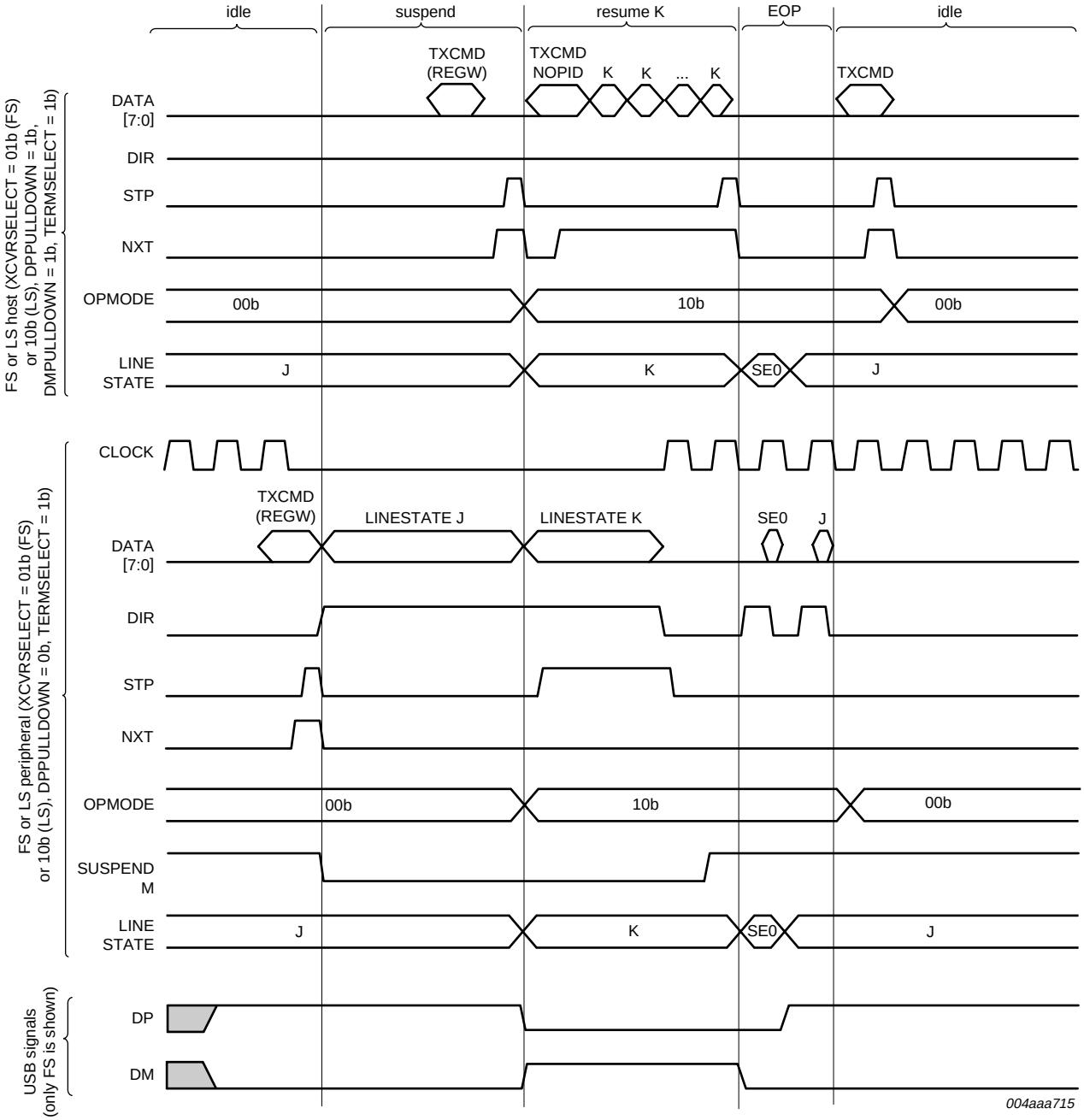
9.10 USB suspend and resume

9.10.1 Full-speed or low-speed host-initiated suspend and resume

Figure 17 illustrates how a host or a hub places a full-speed or low-speed peripheral into suspend and sometime later initiates resume signaling to wake up the downstream peripheral. Note that Figure 17 timing is not to scale, and does not show all RXCMD LINESTATE updates.

The sequence of events for a host and a peripheral, both with ISP1504x1, is as follows:

1. Idle: Initially, the host and the peripheral are idle. The host has its 15 kΩ pull-down resistors enabled (DP_PULLDOWN and DM_PULLDOWN are set to 1b) and 45 Ω terminations disabled (TERMSELECT is set to 1b). The peripheral has the 1.5 kΩ pull-up resistor connected to DP for full-speed or DM for low-speed (TERMSELECT is set to 1b).
2. Suspend: When the peripheral sees no bus activity for 3 ms, it enters the suspend state. The peripheral link places the PHY into low-power mode by setting the SUSPENDM bit in the Function Control register, causing the PHY to draw only suspend current. The host may or may not be powered down.
3. Resume K: When the host wants to wake up the peripheral, it sets OPMODE[1:0] to 10b and transmits a K for at least 20 ms. The peripheral link sees the resume K on LINESTATE, and asserts STP to wake up the PHY.
4. EOP: When STP is asserted, the ISP1504x1 on the host side automatically appends an EOP of two bits of SE0 at low-speed bit rate, followed by one bit of J. The ISP1504x1 on the host side knows to add the EOP because DP_PULLDOWN and DM_PULLDOWN are set to 1b for a host. After the EOP is completed, the host link sets OPMODE[1:0] to 00b for normal operation. The peripheral link sees the EOP and also resumes normal operation.



Timing is not to scale.

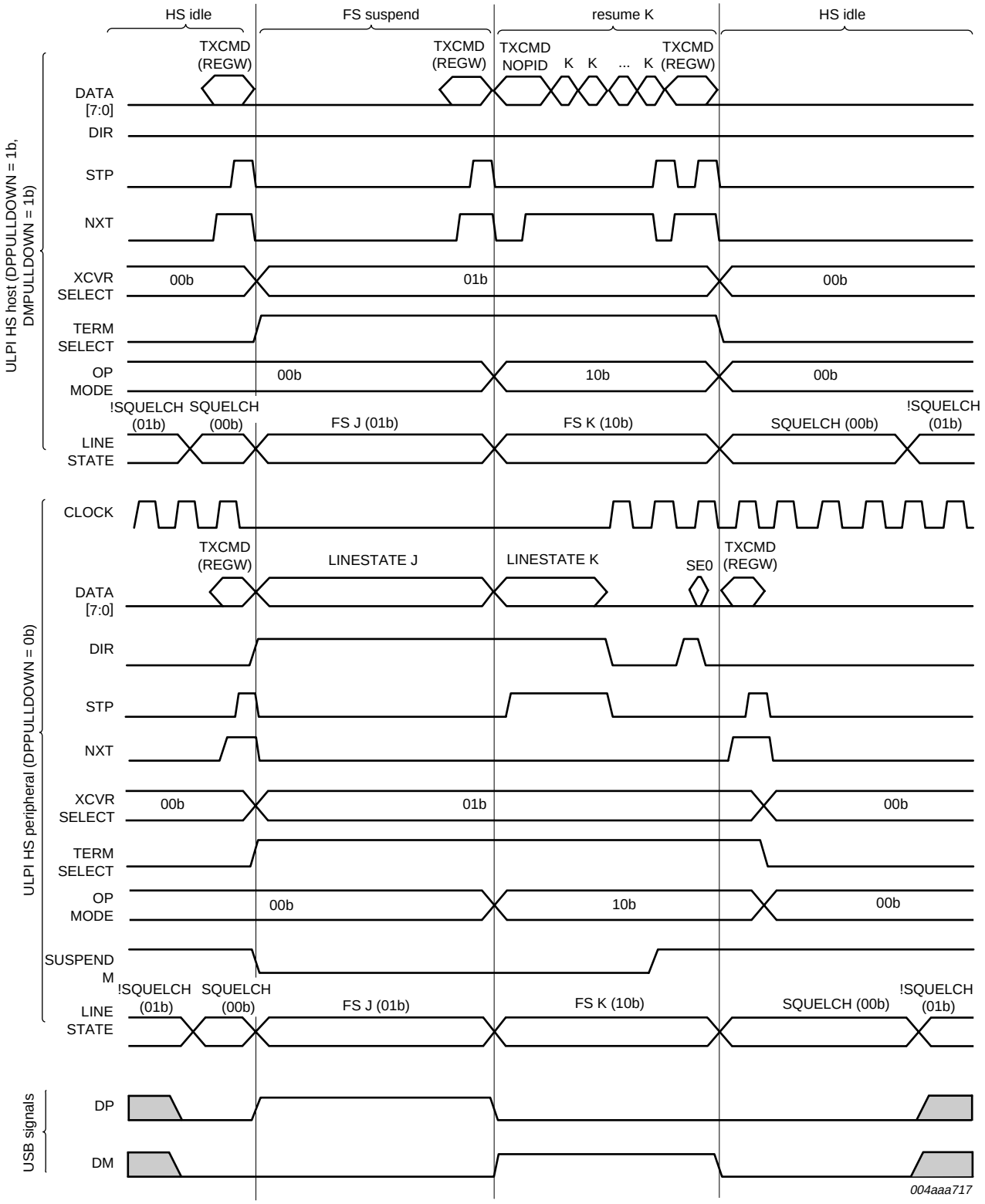
Fig 17. Full-speed suspend and resume

9.10.2 High-speed suspend and resume

Figure 18 illustrates how a host or a hub places a high-speed enabled peripheral into suspend and then initiates resume signaling. The high-speed peripheral will wake up and return to high-speed operations. Note that Figure 18 timing is not to scale, and does not show all RXCMD LINESTATE updates.

The sequence of events related to a host and a peripheral, both with ISP1504x1, is as follows.

1. High-speed idle: Initially, the host and the peripheral are idle. The host has its 15 kΩ pull-down resistors enabled (DP_PULLDOWN and DM_PULLDOWN are set to 1b) and 45 Ω terminations enabled (TERMSELECT is set to 0b). The peripheral has its 45 Ω terminations enabled (TERMSELECT is set to 0b).
2. Full-speed suspend: When the peripheral sees no bus activity for 3 ms, it enters the suspend state. The peripheral link places the ISP1504x1 into full-speed mode (XCVRSELECT is set to 01b), removes 45 Ω terminations, and enables the 1.5 kΩ pull-up resistor on DP (TERMSELECT is set to 1b). The peripheral link then places the ISP1504x1 into low-power mode by setting SUSPENDM, causing the ISP1504x1 to draw only suspend current. The host also changes the ISP1504x1 to full-speed (XCVRSELECT is set to 01b), removes 45 Ω terminations (TERMSELECT is set to 1b), and then may or may not be powered down.
3. Resume K: When the host wants to wake up the peripheral, it sets OPMODE to 10b and transmits a full-speed K for at least 20 ms. The peripheral link sees the resume K (10b) on LINESTATE, and asserts STP to wake up the ISP1504x1.
4. High-speed traffic: The host link sets high-speed (XCVRSELECT is set to 00b) and enables its 45 Ω terminations (TERMSELECT is set to 0b). The peripheral link sees SE0 on LINESTATE and also sets high-speed (XCVRSELECT is set to 00b), and enables its 45 Ω terminations (TERMSELECT is set to 0b). The host link sets OPMODE to 00b for normal high-speed operation.



Timing is not to scale.

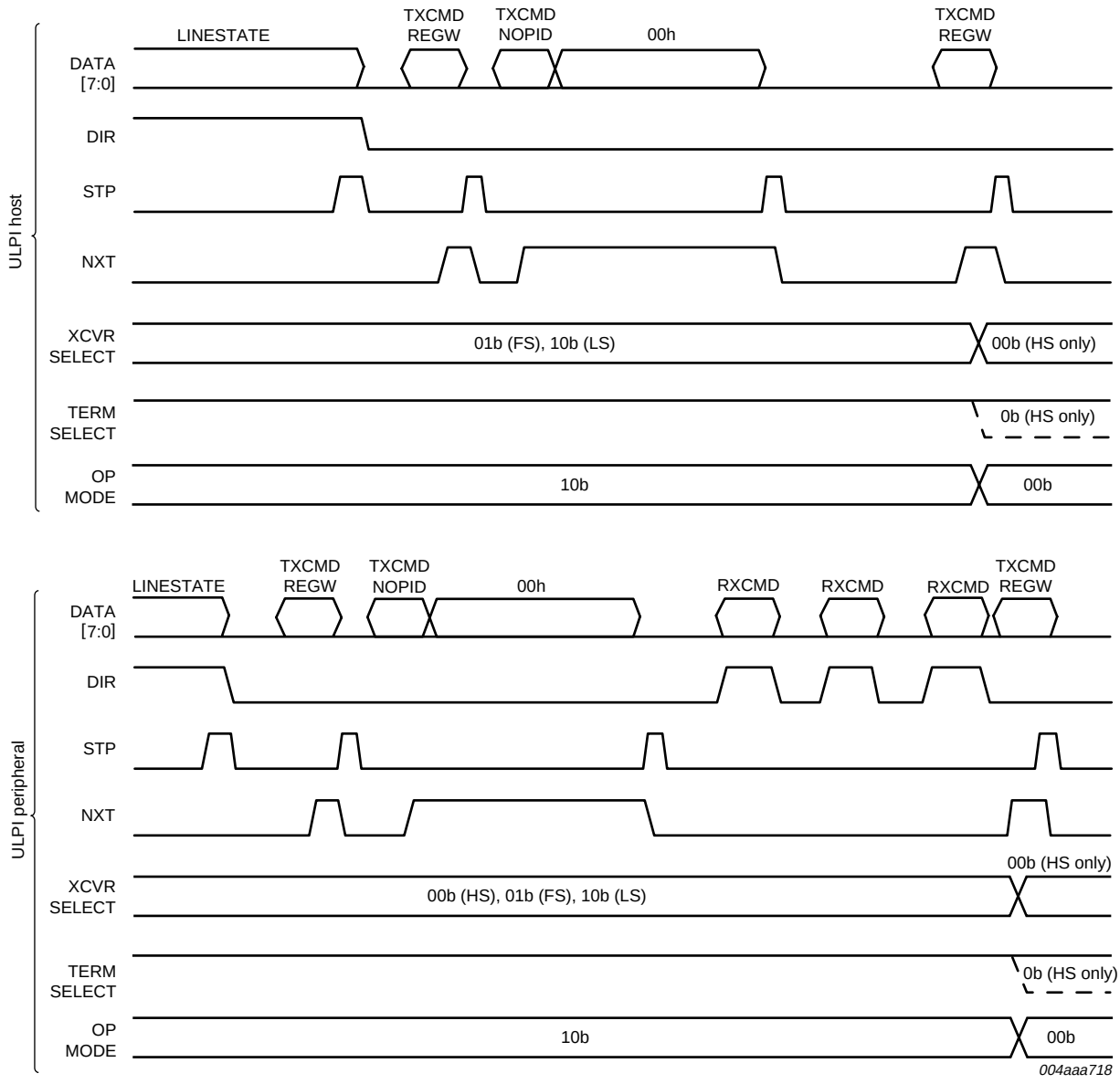
Fig 18. High-speed suspend and resume

9.10.3 Remote wake-up

The ISP1504x1 supports peripherals that initiate remote wake-up resume. When placed into USB suspend, the peripheral link remembers what speed it was originally operating. Depending on the original speed, the link follows one of the protocols detailed here. In Figure 19, timing is not to scale, and not all RXCMD LINESTATE updates are shown.

The sequence of events related to a host and a peripheral, both with ISP1504x1, is as follows.

1. Both the host and the peripheral are assumed to be in low-power mode.
2. The peripheral begins remote wake-up by re-enabling its clock and setting its SUSPENDM bit to 1b.
3. The peripheral begins driving K on the bus to signal resume. Note that the peripheral link must assume that LINESTATE is K (01b) while transmitting because it will not receive any RXCMDs.
4. The host recognizes the resume, re-enables its clock and sets its SUSPENDM bit.
5. The host takes over resume driving within 1 ms of detecting the remote wake-up.
6. The peripheral stops driving resume.
7. The peripheral sees the host continuing to drive the resume.
8. The host stops driving resume and the ISP1504x1 automatically adds the EOP to the end of the resume. The peripheral recognizes the EOP as the end of resume.
9. Both the host and the peripheral revert to normal operation by writing 00b to OPMODE. If the host or the peripheral was previously in high-speed mode, it must revert to high-speed before the SE0 of the EOP is completed. This can be achieved by writing XCVRSELECT = 00b and TERMSELECT = 0b after LINESTATE indicates SE0.



Timing is not to scale.

Fig 19. Remote wake-up from low-power mode

9.11 No automatic SYNC and EOP generation (optional)

This setting allows the link to turn off the automatic SYNC and EOP generation, and must be used for high-speed packets only. It is provided for backwards compatibility with legacy controllers that include SYNC and EOP bytes in the data payload when transmitting packets. The ISP1504x1 will not automatically generate the SYNC and EOP patterns when OPMODE[1:0] is set to 11b. The ISP1504x1 will still NRZI encode data and perform bit stuffing. An example of a sequence is shown in Figure 20. The link must always send packets using the TXCMD (NOPID) type. The ISP1504x1 does not provide a mechanism to control bit stuffing in individual bytes, but will automatically turn off bit stuffing for EOP when STP is asserted with data set to FEh. If data is set to 00h when STP is asserted, the

PHY will not transmit any EOP. The ISP1504x1 will also detect if the PID byte is A5h, indicating an SOF packet and automatically send a long EOP when STP is asserted. To transmit chirp and resume signaling, the link must set OPMODE to 10b.

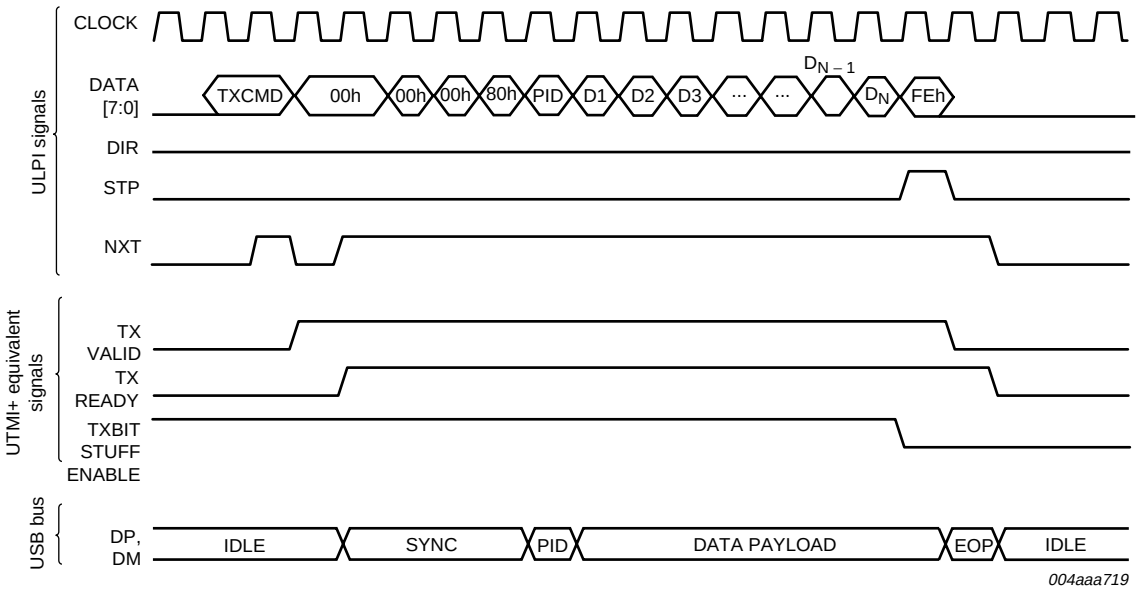


Fig 20. Transmitting USB packets without automatic SYNC and EOP generation

9.12 On-The-Go operations

On-The-Go (OTG) is a supplement to *Universal Serial Bus Specification Rev. 2.0* that allows a portable USB device to assume the role of a limited USB host by defining improvements, such as a small connector and low power. Non-portable devices, such as standard hosts and embedded hosts, can also benefit from OTG features.

The ISP1504x1 OTG PHY is designed to support all the tasks specified in the OTG supplement. The ISP1504x1 provides the front-end analog support for Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for dual-role devices. The supporting components include:

- Voltage comparators
  - A_VBUS_VLD
  - SESS_VLD (session valid, can be used for both A-session and B-session valid)
  - SESS_END (session end)
- Pull-up and pull-down resistors on DP and DM
- ID detector indicates if micro-A or micro-B plug is inserted
- Charge and discharge resistors on V_{BUS}

The following subsections describe how to use the ISP1504x1 OTG components.

9.12.1 OTG comparators

The ISP1504x1 provides comparators that conform to *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.2* requirements of $V_{A\_VBUS\_VLD}$, $V_{A\_SESS\_VLD}$, $V_{B\_SESS\_VLD}$ and $V_{B\_SESS\_END}$. In this data sheet, $V_{A\_SESS\_VLD}$ and $V_{B\_SESS\_VLD}$ are combined into $V_{A\_SESS\_VLD}$. Comparators are described in Section 7.6.2. Changes in comparator values are communicated to the link by RXCMDs as described in Section 9.5.2.2. Control over comparators is described in Section 10.1.5 to Section 10.1.8.

9.12.2 Pull-up and pull-down resistors

The USB resistors on DP and DM can be used to initiate data-line pulsing SRP. The link must set the required bus state using mode settings in Table 8.

9.12.3 ID detection

The ISP1504x1 provides an internal pull-up resistor to sense the value of the ID pin. The pull-up resistor must first be enabled by setting the ID_PULLUP register bit to logic 1. If the value on ID has changed, the ISP1504x1 will send an RXCMD or interrupt to the link by time t_{ID}. If the link does not receive any RXCMD or interrupt by t_{ID}, then the ID value has not changed.

9.12.4 V_{BUS} charge and discharge resistors

A pull-up resistor, $R_{UP(VBUS)}$, is provided to perform V_{BUS} pulsing SRP. A B-device is allowed to charge V_{BUS} above the session valid threshold to request the host to turn on the V_{BUS} power.

A pull-down resistor, $R_{DN(VBUS)}$, is provided for a B-device to discharge V_{BUS}. This is done whenever the A-device turns off the V_{BUS} power; the B-device can use the pull-down resistor to ensure V_{BUS} is below $V_{B\_SESS\_END}$ before starting a session.

For details, refer to *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.2*.

9.13 Serial modes

The ISP1504x1 supports both 6-pin serial mode and 3-pin serial mode, controlled by bits 6PIN_FSLS_SERIAL and 3PIN_FSLS_SERIAL of the Interface Control register. For details, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.10*.

Figure 21 and Figure 22 provide example of 6-pin serial mode and 3-pin serial mode, respectively.

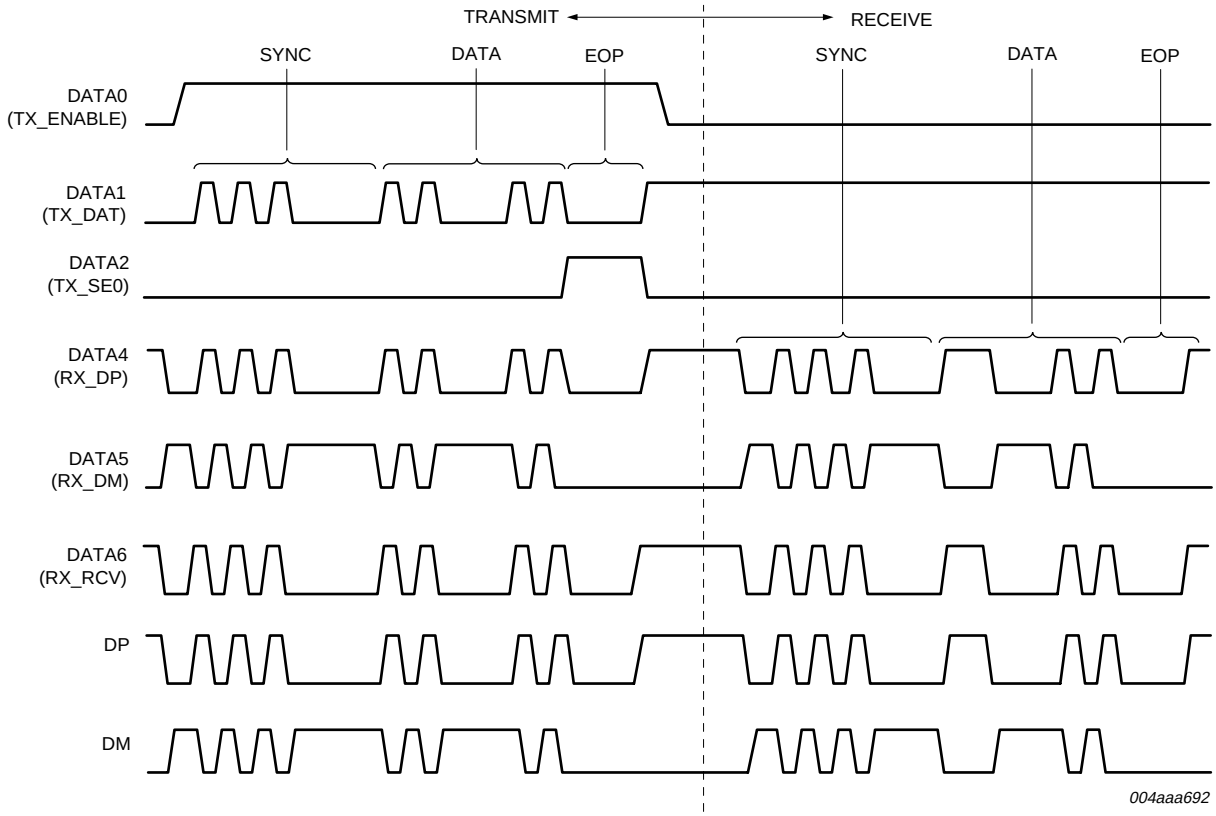


Fig 21. Example of transmit followed by receive in 6-pin serial mode

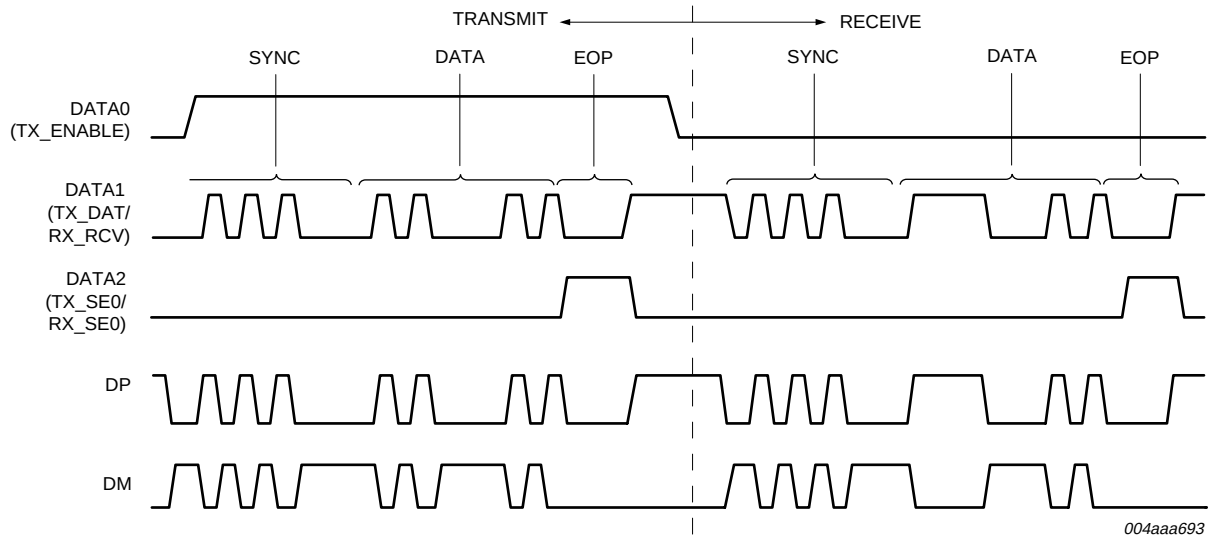


Fig 22. Example of transmit followed by receive in 3-pin serial mode

9.14 Aborting transfers

The ISP1504x1 supports aborting transfers on the ULPI bus. For details, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.8.4*.

9.15 Avoiding contention on the ULPI data bus

Because the ULPI data bus is bidirectional, avoid situations in which both the link and the PHY simultaneously drive the data bus.

The following points must be considered while implementing the data bus drive control on the link.

After power-up and clock stabilization, default states are as follows:

- The ISP1504x1 drives DIR to LOW.
- The data bus is input to the ISP1504x1.
- The ULPI link data bus is output, with all data bus lines driven to LOW.

When the ISP1504x1 wants to take control of data bus to initiate a data transfer, it changes the DIR value from LOW to HIGH.

At this point, the link must disable its output buffers. This must be as fast as possible so the link must use a combinational path from DIR.

The ISP1504x1 will not immediately enable its output buffers, but will delay the enabling of its buffers until the next clock edge, avoiding bus contention.

When the data transfer is no longer required by the ISP1504x1, it changes DIR from HIGH to LOW and starts to immediately turn off its output drivers. The link senses the change of DIR from HIGH to LOW, but delays enabling its output buffers for one CLOCK cycle, avoiding data bus contention.

10. Register map

Table 19. Immediate register set overview

Field name	Size (bits)	Address (6 bits)				References
		R[1]	W[2]	S[3]	C[4]	
Vendor ID Low register	8	00h	-	-	-	Section 10.1.1 on page 48
Vendor ID High register	8	01h	-	-	-	
Product ID Low register	8	02h	-	-	-	
Product ID High register	8	03h	-	-	-	
Function Control register	8	04h to 06h	04h	05h	06h	Section 10.1.2 on page 48
Interface Control register	8	07h to 09h	07h	08h	09h	Section 10.1.3 on page 49
OTG Control register	8	0Ah to 0Ch	0Ah	0Bh	0Ch	Section 10.1.4 on page 50
USB Interrupt Enable Rising register	8	0Dh to 0Fh	0Dh	0Eh	0Fh	Section 10.1.5 on page 51
USB Interrupt Enable Falling register	8	10h to 12h	10h	11h	12h	Section 10.1.6 on page 52
USB Interrupt Status register	8	13h	-	-	-	Section 10.1.7 on page 52
USB Interrupt Latch register	8	14h	-	-	-	Section 10.1.8 on page 53
Debug register	8	15h	-	-	-	Section 10.1.9 on page 54
Scratch register	8	16h to 18h	16h	17h	18h	Section 10.1.10 on page 54
Reserved (not used, not available)	-	19h to 2Eh				Section 10.1.11 on page 54
Access extended register set	8	-	2Fh	-	-	Section 10.1.12 on page 54
Vendor-specific registers	8	30h to 3Ch				Section 10.1.13 on page 54
Power Control register	8	3D to 3Fh				Section 10.1.14 on page 54

[1] Read (R): A register can be read. Read-only if this is the only mode given.

[2] Write (W): The pattern on the data bus will be written over all bits of a register.

[3] Set (S): The pattern on the data bus is OR-ed with and written to a register.

[4] Clear (C): The pattern on the data bus is a mask. If a bit in the mask is set, then the corresponding register bit will be set to zero (cleared).

Table 20. Extended register set overview

Field name	Size (bits)	Address (6 bits)				References
		R[1]	W[2]	S[3]	C[4]	
Maps to immediate register set above	8	00h to 3Fh				Section 10.2 on page 55
Reserved (do not use)	8	40h to FFh				

[1] Read (R): A register can be read. Read-only if this is the only mode given.

[2] Write (W): The pattern on the data bus will be written over all bits of a register.

[3] Set (S): The pattern on the data bus is OR-ed with and written to a register.

[4] Clear (C): The pattern on the data bus is a mask. If a bit in the mask is set, then the corresponding register bit will be set to zero (cleared).

10.1 Immediate register set

10.1.1 Vendor ID and Product ID registers

10.1.1.1 Vendor ID Low register

Table 21 shows the bit description of the register.

Table 21. Vendor ID Low register (address R = 00h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	VENDOR_ID_LOW[7:0]	R	CCh	**Vendor ID Low**: Lower byte of the NXP vendor ID supplied by USB-IF; has a fixed value of CCh

10.1.1.2 Vendor ID High register

The bit description of the register is given in Table 22.

Table 22. Vendor ID High register (address R = 01h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	VENDOR_ID_HIGH[7:0]	R	04h	**Vendor ID High**: Upper byte of the NXP vendor ID supplied by USB-IF; has a fixed value of 04h

10.1.1.3 Product ID Low register

The bit description of the Product ID Low register is given in Table 23.

Table 23. Product ID Low register (address R = 02h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	PRODUCT_ID_LOW[7:0]	R	04h	**Product ID Low**: Lower byte of the NXP product ID number; has a fixed value of 04h

10.1.1.4 Product ID High register

The bit description of the register is given in Table 24.

Table 24. Product ID High register (address R = 03h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	PRODUCT_ID_HIGH[7:0]	R	15h	**Product ID High**: Upper byte of the NXP product ID number; has a fixed value of 15h

10.1.2 Function Control register

This register controls UTMI function settings of the PHY. The bit allocation of the register is given in Table 25.

Table 25. Function Control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	SUSPENDM	RESET	OPMODE[1:0]		TERM SELECT	XCVRSELECT[1:0]	
Reset	0	1	0	0	0	0	0	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 26. Function Control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit description

Bit	Symbol	Description
7	-	reserved
6	SUSPENDM	**Suspend LOW**: Active LOW PHY suspend. Sets the PHY into low-power mode. The PHY will power down all blocks, except the full-speed receiver, OTG comparators and ULPI interface pins. To come out of low-power mode, the link must assert STP. The PHY will automatically clear this bit when it exits low-power mode. **0b —** Low-power mode **1b —** Powered
5	RESET	**Reset**: Active HIGH transceiver reset. After the link sets this bit, the PHY will assert DIR and reset the digital core. This does not reset the ULPI interface or the ULPI register set. When the reset is completed, the PHY will de-assert DIR and automatically clear this bit, followed by an RXCMD update to the link. The link must wait for DIR to de-assert before using the ULPI bus. **0b —** Do not reset **1b —** Reset
4 to 3	OPMODE[1:0]	**Operation Mode**: Selects the required bit-encoding style during transmit. **00b —** Normal operation **01b —** Non-driving **10b —** Disable bit-stuffing and NRZI encoding **11b —** Do not automatically add SYNC and EOP when transmitting; must be used only for high-speed packets
2	TERMSELECT	**Termination Select**: Controls the internal 1.5 kΩ full-speed pull-up resistor and 45 Ω high-speed terminations. Control over bus resistors changes, depending on XCVRSELECT[1:0], OPMODE[1:0], DP_PULLDOWN and DM_PULLDOWN, as shown in Table 8.
1 to 0	XCVRSELECT [1:0]	**Transceiver Select**: Selects the required transceiver speed. **00b —** Enable the high-speed transceiver **01b —** Enable the full-speed transceiver **10b —** Enable the low-speed transceiver **11b —** Enable the full-speed transceiver for low-speed packets (full-speed preamble is automatically prefixed)

10.1.3 Interface Control register

The Interface Control register enables alternative interfaces. All of these modes are optional features provided for legacy link cores. Setting more than one of these fields results in undefined behavior. Table 27 provides the bit allocation of the register.

Table 27. Interface Control register (address R = 07h to 09h, W = 07h, S = 08h, C = 09h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	INTF_ PROT_DIS	IND_PASS THRU	IND_ COMPL	reserved	CLOCK_ SUSPENDM	reserved	3PIN_ FSLS_ SERIAL	6PIN_ FSLS_ SERIAL
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 28. Interface Control register (address R = 07h to 09h, W = 07h, S = 08h, C = 09h) bit description

Bit	Symbol	Description
7	INTF_PROT_DIS	**Interface Protect Disable**: Controls circuitry built into the ISP1504x1 to protect the ULPI interface when the link 3-states STP and DATA[7:0]. When this bit is enabled, the ISP1504x1 will automatically detect when the link stops driving STP. **0b —** Enables the interface protect circuit (default). The ISP1504x1 attaches a weak pull-up resistor on STP. If STP is unexpectedly HIGH, the ISP1504x1 attaches weak pull-down resistors on DATA[7:0], protecting data inputs. **1b —** Disables the interface protect circuit, detaches weak pull-down resistors on DATA[7:0], and a weak pull-up resistor on STP.
6	IND_PASSTHRU	**Indicator Pass-through**: Controls whether the complement output is qualified with the internal A_VBUS_VLD comparator before being used in the V_{BUS} state in RXCMD. For details, see Section 9.5.2.2. **0b —** The complement output signal is qualified with the internal A_VBUS_VLD comparator. **1b —** The complement output signal is not qualified with the internal A_VBUS_VLD comparator.
5	IND_COMPL	**Indicator Complement**: Informs the PHY to invert the FAULT input signal, generating the complement output. For details, see Section 9.5.2.2. **0b —** The ISP1504x1 will not invert the FAULT signal (default). **1b —** The ISP1504x1 will invert the FAULT signal.
4	-	reserved
3	CLOCK_ SUSPENDM	**Clock Suspend LOW**: Active LOW clock suspend. Powers down the internal clock circuitry only. By default, the clock will not be powered in 6-pin serial mode or 3-pin serial mode. Valid only in 6-pin serial mode and 3-pin serial mode. Valid only when SUSPENDM is set to logic 1, otherwise this bit is ignored. **0b —** Clock will not be powered in 3-pin or 6-pin serial mode. **1b —** Clock will be powered in 3-pin and 6-pin serial modes.
2	-	reserved
1	3PIN_FSLS_ SERIAL	**3-Pin Full-Speed Low-Speed Serial Mode**: Changes the ULPI interface to a 3-bit serial interface. The PHY will automatically clear this bit when 3-pin serial mode is exited. **0b —** Full-speed or low-speed packets are sent using the parallel interface. **1b —** Full-speed or low-speed packets are sent using the 3-pin serial interface.
0	6PIN_FSLS_ SERIAL	**6-Pin Full-Speed Low-Speed Serial Mode**: Changes the ULPI interface to a 6-bit serial interface. The PHY will automatically clear this bit when 6-pin serial mode is exited. **0b —** Full-speed or low-speed packets are sent using the parallel interface. **1b —** Full-speed or low-speed packets are sent using the 6-pin serial interface.

10.1.4 OTG Control register

This register controls various OTG functions of the ISP1504x1. The bit allocation of the OTG Control register is given in Table 29.

Table 29. OTG Control register (address R = 0Ah to 0Ch, W = 0Ah, S = 0Bh, C = 0Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	USE_EXT_ VBUS_IND	DRV_ VBUS_EXT	reserved	CHRG_ VBUS	DISCHRG_ VBUS	DM_PULL DOWN	DP_PULL DOWN	ID_PULL UP
Reset	0	0	0	0	0	1	1	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 30. OTG Control register (address R = 0Ah to 0Ch, W = 0Ah, S = 0Bh, C = 0Ch) bit description

Bit	Symbol	Description
7	USE_EXT_VBUS_IND	**Use External V_{BUS} Indicator**: Informs the PHY to use an external V_{BUS} overcurrent indicator. **0b —** Use the internal OTG comparator. **1b —** Use the external V_{BUS} valid indicator signal input from the FAULT pin.
6	DRV_VBUS_EXT	**Drive V_{BUS} External**: Controls external charge pump or 5 V supply by the PSW_N pin. **0b —** PSW_N is HIGH. **1b —** PSW_N to LOW.
5	-	reserved
4	CHRG_VBUS	**Charge V_{BUS}**: Charges V_{BUS} through a resistor. Used for the V_{BUS} pulsing of SRP. The link must first check that V_{BUS} is discharged (see bit DISCHRG_VBUS), and that both the DP and DM data lines have been LOW (SE0) for 2 ms. **0b —** Do not charge V_{BUS}. **1b —** Charge V_{BUS}.
3	DISCHRG_VBUS	**Discharge V_{BUS}**: Discharges V_{BUS} through a resistor. If the link sets this bit to logic 1, it waits for an RXCMD indicating that SESS_END has changed from 0 to 1, and then resets this bit to 0 to stop the discharge. **0b —** Do not discharge V_{BUS}. **1b —** Discharge V_{BUS}.
2	DM_PULLDOWN	**DM Pull Down**: Enables the 15 kΩ pull-down resistor on DM. **0b —** Pull-down resistor is not connected to DM. **1b —** Pull-down resistor is connected to DM.
1	DP_PULLDOWN	**DP Pull Down**: Enables the 15 kΩ pull-down resistor on DP. **0b —** Pull-down resistor is not connected to DP. **1b —** Pull-down resistor is connected to DP.
0	ID_PULLUP	**ID Pull Up**: Connects a pull-up to the ID line and enables sampling of the ID level. Disabling the ID line sampler will reduce PHY power consumption. **0b —** Disable sampling of the ID line. **1b —** Enable sampling of the ID line.

10.1.5 USB Interrupt Enable Rising Edge register

The bits in this register enable interrupts and RXCMDs to be sent when the corresponding bits in the USB Interrupt Status register change from logic 0 to logic 1. By default, all transitions are enabled. Table 31 shows the bit allocation of the register.

Table 31. USB Interrupt Enable Rising Edge register (address R = 0Dh to 0Fh, W = 0Dh, S = 0Eh, C = 0Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND_R	SESS_END_R	SESS_VALID_R	VBUS_VALID_R	HOST_DISCON_R
Reset	0	0	0	1	1	1	1	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 32. USB Interrupt Enable Rising Edge register (address R = 0Dh to 0Fh, W = 0Dh, S = 0Eh, C = 0Fh) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND_R	**ID Ground Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on ID_GND.
3	SESS_END_R	**Session End Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on SESS_END.
2	SESS_VALID_R	**Session Valid Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on SESS_VLD.
1	VBUS_VALID_R	**V_{BUS} Valid Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on A_VBUS_VLD.
0	HOST_DISCON_R	**Host Disconnect Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on HOST_DISCON.

10.1.6 USB Interrupt Enable Falling Edge register

The bits in this register enable interrupts and RXCMDs to be sent when the corresponding bits in the USB Interrupt Status register change from logic 1 to logic 0. By default, all transitions are enabled. See Table 33.

Table 33. USB Interrupt Enable Falling Edge register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND_F	SESS_END_F	SESS_VALID_F	VBUS_VALID_F	HOST_DISCON_F
Reset	0	0	0	1	1	1	1	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 34. USB Interrupt Enable Falling Edge register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND_F	**ID Ground Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on ID_GND.
3	SESS_END_F	**Session End Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on SESS_END.
2	SESS_VALID_F	**Session Valid Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on SESS_VLD.
1	VBUS_VALID_F	**V_{BUS} Valid Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on A_VBUS_VLD.
0	HOST_DISCON_F	**Host Disconnect Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on HOST_DISCON.

10.1.7 USB Interrupt Status register

This register (see Table 35) indicates the current value of the interrupt source signal.

Table 35. USB Interrupt Status register (address R = 13h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND	SESS_END	SESS_VALID	VBUS_VALID	HOST_DISCON
Reset	X	X	X	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 36. USB Interrupt Status register (address R = 13h) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND	**ID Ground**: Reflects the current value of the ID detector circuit.
3	SESS_END	**Session End**: Reflects the current value of the session end voltage comparator.
2	SESS_VALID	**Session Valid**: Reflects the current value of the session valid voltage comparator.
1	VBUS_VALID	**V_{BUS} Valid**: Reflects the current value of the V_{BUS} valid voltage comparator.
0	HOST_DISCON	**Host Disconnect**: Reflects the current value of the host disconnect detector.

10.1.8 USB Interrupt Latch register

The bits of the USB Interrupt Latch register are automatically set by the ISP1504x1 when an unmasked change occurs on the corresponding interrupt source signal. The ISP1504x1 will automatically clear all bits when the link reads this register, or when the PHY enters low-power mode.

Remark: It is optional for the link to read this register when the clock is running because all signal information will automatically be sent to the link through the RXCMD byte.

The bit allocation of this register is given in Table 37.

Table 37. USB Interrupt Latch register (address R = 14h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND_L	SESS_END_L	SESS_VALID_L	VBUS_VALID_L	HOST_DISCON_L
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 38. USB Interrupt Latch register (address R = 14h) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND_L	**ID Ground Latch**: Automatically set when an unmasked event occurs on ID_GND. Cleared when this register is read.
3	SESS_END_L	**Session End Latch**: Automatically set when an unmasked event occurs on SESS_END. Cleared when this register is read.
2	SESS_VALID_L	**Session Valid Latch**: Automatically set when an unmasked event occurs on SESS_VLD. Cleared when this register is read.
1	VBUS_VALID_L	**V_{BUS} Valid Latch**: Automatically set when an unmasked event occurs on A_VBUS_VLD. Cleared when this register is read.
0	HOST_DISCON_L	**Host Disconnect Latch**: Automatically set when an unmasked event occurs on HOST_DISCON. Cleared when this register is read.

10.1.9 Debug register

The bit allocation of the Debug register is given in Table 39. This register indicates the current value of signals useful for debugging.

Table 39. Debug register (address R = 15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						LINE STATE1	LINE STATE0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 40. Debug register (address R = 15h) bit description

Bit	Symbol	Description
7 to 2	-	reserved
1	LINESTATE1	**Line State 1**: Contains the current value of LINESTATE 1
0	LINESTATE0	**Line State 0**: Contains the current value of LINESTATE 0

10.1.10 Scratch register

This is an empty register for testing purposes, see Table 41.

Table 41. Scratch register (address R = 16h to 18h, W = 16h, S = 17h, C = 18h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	SCRATCH[7:0]	R/W/S/C	00h	**Scratch**: This is an empty register byte for testing purposes. Software can read, write, set and clear this register, and the functionality of the PHY will not be affected.

10.1.11 Reserved

Registers 19h to 2Eh are not implemented. Operating on these addresses will have no effect on the PHY.

10.1.12 Access extended register set

Address 2Fh does not contain register data. Instead it links to the extended register set. The immediate register set maps to the lower end of the extended register set.

10.1.13 Vendor-specific registers

Address 30h to 3Fh contains vendor-specific registers.

10.1.14 Power Control register

This register controls various aspects of the ISP1504x1. Table 42 shows the bit allocation of the register.

Table 42. Power Control register (address R = 3Dh to 3Fh, W = 3Dh, S = 3Eh, C = 3Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				BVALID_ FALL	BVALID_ RISE	reserved	
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 43. Power Control register (address R = 3Dh to 3Fh, W = 3Dh, S = 3Eh, C = 3Fh) bit description

Bit	Symbol	Description
7 to 4	-	reserved; the link must never write logic 1 to these bits.
3	BVALID_FALL	**BValid Fall**: Enables RXCMDs for HIGH-to-LOW transitions on BVALID. When BVALID changes from HIGH to LOW, the ISP1504x1 will send an RXCMD to the link with the ALT_INT bit set to logic 1. This bit is optional and is not necessary for OTG devices. The session valid comparator must be used instead.
2	BVALID_RISE	**BValid Rise**: Enables RXCMDs for LOW-to-HIGH transitions on BVALID. When BVALID changes from LOW to HIGH, the ISP1504x1 will send an RXCMD to the link with the ALT_INT bit set to logic 1. This bit is optional and is not necessary for OTG devices. The session valid comparator must be used instead.
1 to 0	-	reserved; the link must never write logic 1 to this bit.

10.2 Extended register set

Addresses 00h to 3Fh of the extended register set directly map to the immediate set. This means a read, write, set or clear operation to these extended addresses will operate on the immediate register set.

Addresses 40h to FFh are not implemented. Operating on these addresses may result in undefined behavior of the PHY.

11. Limiting values

Table 44. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+5.5	V
$V_{CC(I/O)}$	input/output supply voltage			–0.5	+4.6	V
V_I	input voltage	on pins CLOCK, STP, DATA[7:0], RESET_N and CS_N/PWRDN		–0.5	$V_{CC(I/O)}$ + 0.5	V
		on pins V_{BUS}, FAULT and PSW_N		–0.5	+5.5	V
		on pin XTAL1		–0.5	+2.5	V
		on pin ID		–0.5	+4.6	V
		on pins DP and DM	[1]	–0.5	+4.6	V
V_{ESD}	electrostatic discharge voltage	I_{LI} < 1 µA; Human Body Model (JESD22-A114D)	[2]	–2000	+2000	V
		I_{LI} < 1 µA; Machine Model (JESD22-A115-A)		–200	+200	V
		I_{LI} < 1 µA; Charge Device Model (JESD22-C101-C)		–500	+500	V
I_{lu}	latch-up current	$-0.5 \times V_{CC} < V < +1.5 \times V_{CC}$		-	100	mA
T_{stg}	storage temperature			–40	+125	°C
T_j	junction temperature			–40	+125	°C

[1] The ISP1504x1 has been tested according to the additional requirements listed in *Universal Serial Bus Specification Rev. 2.0, Section 7.1.1*. The short circuit withstand test and the AC stress test were performed for 24 hours, and the ISP1504x1 was found to be fully operational after the test completed.

[2] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor (Human Body Model).

12. Recommended operating conditions

Table 45. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			3.0	3.6	4.5	V
$V_{CC(I/O)}$	input/output supply voltage		[1]	1.65	1.8	3.6	V
V_I	input voltage	on pins CLOCK, STP, DATA[7:0], RESET_N and CS_N/PWRDN		0	-	$V_{CC(I/O)}$	V
		on pins V_{BUS}, FAULT and PSW_N		0	-	5.25	V
		on pins DP, DM and ID		0	-	3.6	V
		on pin XTAL1		0	-	1.95	V
T_{amb}	ambient temperature			–40	+25	+85	°C

[1] $V_{CC(I/O)}$ must not exceed V_{CC}.

13. Static characteristics

Table 46. Static characteristics: supply pins

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(REG3V3)}$	voltage on pin REG3V3			3.0	3.3	3.6	V
$V_{(REG1V8)}$	voltage on pin REG1V8			1.65	1.8	1.95	V
$V_{POR(trip)}$	power-on reset trip voltage			1.0	-	1.5	V
I_{CC}	supply current	power-down mode (pin CS_N/PWRDN = HIGH or $V_{CC(I/O)}$ is not present)		-	0.5	10	µA
		low-power mode; V_{BUS} valid detector disabled; 1.5 kΩ pull-up resistor on pin DP disconnected		-	50	120	µA
		low-power mode; V_{BUS} valid detector disabled; 1.5 kΩ pull-up resistor on pin DP connected		-	235	315	µA
		full-speed idle; no USB activity		-	11	-	mA
		high-speed idle; no USB activity		-	19	-	mA
		full-speed continuous data transmit; 50 pF load on pins DP and DM	[1]	-	15	-	mA
		full-speed continuous data receive	[1]	-	11	-	mA
		high-speed continuous data transmit; 45 Ω load on pins DP and DM to ground	[1]	-	48	-	mA
		high-speed continuous data receive	[1]	-	28	-	mA
$I_{CC(I/O)}$	supply current on pin $V_{CC(I/O)}$	static current; digital I/O pins are idle		-	-	10	µA

[1] A continuous stream of 1 kB packets with minimum inter-packet gap and all data bits set to logic 0 for continuous toggling.

Table 47. Static characteristics: digital pins CLOCK, DIR, STP, NXT, DATA[7:0], RESET_N, CS_N/PWRDN

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		-	-	$0.3 \times V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage		$0.7 \times V_{CC(I/O)}$	-	-	V
I_{LI}	input leakage current		−1	+0.1	+1	µA
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = −2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = +2 mA	$V_{CC(I/O)} - 0.4$	-	-	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{CC(I/O)} - 0.4$ V	−4.8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4.2	-	-	mA
I_{OZ}	off-state output current	$0 V < V_O < V_{CC(I/O)}$	-	-	1	µA
Impedance						
Z_L	load impedance		45	-	65	Ω

Table 47. Static characteristics: digital pins CLOCK, DIR, STP, NXT, DATA[7:0], RESET_N, CS_N/PWRDN *…continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pull-up and pull-down						
I_{pd}	pull-down current	interface protect enabled; DATA[7:0] pins only; V_I = $V_{CC(I/O)}$	25	50	90	µA
I_{pu}	pull-up current	interface protect enabled; STP pin only; V_I = 0 V	−30	−50	−80	µA
Capacitance						
C_{in}	input capacitance		-	-	3.5	pF

Table 48. Static characteristics: digital pin FAULT

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
I_{IL}	LOW-level input current	V_I = 0 V	-	-	1	µA
I_{IH}	HIGH-level input current	V_I = $V_{CC(I/O)}$	-	-	1	µA

Table 49. Static characteristics: digital pin PSW_N

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output levels						
V_{OH}	HIGH-level output voltage	external pull-up resistor connected	3.0[1]	-	5.25	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	external pull-up resistor connected	-	-	1	µA
I_{OL}	LOW-level output current	V_O = 0.4 V	4.0	-	-	mA

[1] When V_{OH} is less than 3.0 V, I_{CC} may increase because of the cross current.

Table 50. Static characteristics: analog I/O pins DP, DM

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Original USB transceiver (low-speed and full-speed)						
Input levels (differential receiver)						
V_{DI}	differential input sensitivity	$\lvert V_{DP} - V_{DM} \rvert$	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	0.8	-	2.5	V
Input levels (single-ended receivers)						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V

Table 50. Static characteristics: analog I/O pins DP, DM *...continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output levels							
V_{OL}	LOW-level output voltage	pull-up on pin DP; R_L = 1.5 kΩ to 3.6 V		0.0	0.18	0.3	V
V_{OH}	HIGH-level output voltage	pull-down on pins DP and DM; R_L = 15 kΩ to GND		2.8	3.2	3.6	V
V_{CRS}	output signal crossover voltage	excluding the first transition from the idle state		1.3	-	2.0	V
Termination							
V_{TERM}	termination voltage for upstream facing port pull-up			3.0	-	3.6	V
Resistance							
$R_{UP(DP)}$	pull-up resistance on pin DP			1425	1500	1575	Ω
High-speed USB transceiver (HS)							
Input levels (differential receiver)							
V_{HSSQ}	high-speed squelch detection threshold voltage (differential signal amplitude)			100	-	150	mV
V_{HSDSC}	high-speed disconnect detection threshold voltage (differential signal amplitude)			525	-	625	mV
V_{HSDI}	high-speed differential input sensitivity	$\lvert V_{DP} - V_{DM} \rvert$		300	-	-	mV
V_{HSCM}	high-speed data signaling common mode voltage range	includes V_{DI} range		−50	-	+500	mV
Output levels							
V_{HSOI}	high-speed idle level			−10	-	+10	mV
V_{HSOL}	high-speed data signaling LOW-level voltage			−10	-	+10	mV
V_{HSOH}	high-speed data signaling HIGH-level voltage			360	-	440	mV
V_{CHIRPJ}	Chirp J level (differential voltage)			700	-	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)			−900	-	−500	mV
Leakage current							
I_{LZ}	off-state leakage current			−1	-	+1	µA
Capacitance							
C_{in}	input capacitance	pin to GND		-	-	5	pF
Resistance							
$R_{DN(DP)}$	pull-down resistance on pin DP			14.25	15	15.75	kΩ
$R_{DN(DM)}$	pull-down resistance on pin DM			14.25	15	15.75	kΩ
Termination							
$Z_{O(drv)(DP)}$	driver output impedance on pin DP	steady-state drive	[1]	40.5	45	49.5	Ω
$Z_{O(drv)(DM)}$	driver output impedance on pin DM	steady-state drive	[1]	40.5	45	49.5	Ω
Z_{INP}	input impedance			1	-	-	MΩ

[1] For high-speed USB and full-speed USB.

Table 51. Static characteristics: analog pin V_{BUS}

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Comparators						
$V_{A\_VBUS\_VLD}$	A-device V_{BUS} valid voltage		4.4	-	4.75	V
$V_{A\_SESS\_VLD}$	A-device session valid voltage	for A-device and B-device	0.8	1.6	2.0	V
$V_{hys(A\_SESS\_VLD)}$	A-device session valid hysteresis voltage	for A-device and B-device	70	90	110	mV
$V_{B\_SESS\_END}$	B-device session end voltage		0.2	0.5	0.8	V
Resistance						
$R_{UP(VBUS)}$	pull-up resistance on pin V_{BUS}	connect to pin REG3V3 when CHRG_VBUS is logic 1	281	680	-	Ω
$R_{DN(VBUS)}$	pull-down resistance on pin V_{BUS}	connect to GND when DISCHRG_VBUS is logic 1	656	1200	-	Ω
$R_{I(idle)(VBUS)}$	idle input resistance on pin V_{BUS}		40	70	100	kΩ

Table 52. Static characteristics: ID detection circuit

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ID}	ID detection time		50	-	-	ms
$V_{th(ID)}$	ID detector threshold voltage		0.8	1.2	2.0	V
$R_{UP(ID)}$	ID pull-up resistance	connect to pin REG3V3 ID_PULLUP is logic 1	40	50	60	kΩ

Table 53. Static characteristics: resistor reference

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(RREF)}$	output voltage on pin RREF	SUSPENDM is logic 1	-	1.22	-	V

14. Dynamic characteristics

Table 54. Dynamic characteristics: reset and clock

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reset							
$t_{W(POR)}$	internal power-on reset pulse width			0.2	-	-	µs
$t_{w(REG1V8\_H)}$	REG1V8 HIGH pulse width			2	-	-	µs
$t_{w(REG1V8\_L)}$	REG1V8 LOW pulse width			11	-	-	µs
$t_{W(RESET\_N)}$	external RESET_N pulse width			200	-	-	ns
$t_{startup(PLL)}$	PLL startup time			-	650	-	µs
t_{PWRUP}	regulator start-up time	4.7 µF ± 20 % capacitor each on pins REG1V8 and REG3V3		-	-	1	ms
t_{PWRDN}	regulator power-down time	4.7 µF ± 20 % capacitor each on pins REG1V8 and REG3V3		-	-	100	ms
Crystal or clock applied to XTAL1							
$f_{i(XTAL1)}$	input frequency on pin XTAL1	ISP1504A1ET		-	19.2000	-	MHz
		ISP1504C1ET		-	26.0000	-	MHz
$t_{jit(i)(XTAL1)RMS}$	RMS input jitter on pin XTAL1	$f_{i(XTAL1)}$ = 19.2 MHz		-	-	200	ps
		$f_{i(XTAL1)}$ = 26 MHz		-	-	300	ps
$\Delta f_{i(XTAL1)}$	input frequency tolerance on pin XTAL1			-	50	200	ppm
$\delta_{i(XTAL1)}$	input duty cycle on pin XTAL1		[1]	-	50	-	%
$t_{r(XTAL1)}$	rise time on pin XTAL1	only for square wave input		-	-	5	ns
$t_{f(XTAL1)}$	fall time on pin XTAL1	only for square wave input		-	-	5	ns
$V_{(XTAL1)(p-p)}$	peak-to-peak voltage on pin XTAL1	only for square wave input		0.566	-	1.95	V
Output CLOCK characteristics							
$f_{o(CLOCK)}$	output frequency on pin CLOCK			59.97	60.00	60.03	MHz
$t_{jit(o)(CLOCK)RMS}$	RMS output jitter on pin CLOCK			-	-	500	ps
$\delta_{o(CLOCK)}$	output clock duty cycle on pin CLOCK			45	50	55	%

[1] The internal PLL is triggered only on the positive edge from the crystal oscillator. Therefore, the duty cycle is not critical.

Table 55. Dynamic characteristics: digital I/O pins

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(I/O)}$ = 1.65 V to 1.95 V						
$t_{su(DATA)}$	DATA set-up time with respect to the rising edge of pin CLOCK	20 pF total external load per pin	5.7	-	-	ns
$t_{h(DATA)}$	DATA hold time with respect to the rising edge of pin CLOCK	20 pF total external load per pin	0	-	-	ns
$t_{d(DATA)}$	DATA output delay with respect to the rising edge of pin CLOCK	20 pF total external load per pin	-	-	7.8	ns
$t_{su(STP)}$	STP set-up time with respect to the rising edge of pin CLOCK	20 pF total external load per pin	4.5	-	-	ns
$t_{h(STP)}$	STP hold time with respect to the rising edge of pin CLOCK	20 pF total external load per pin	0	-	-	ns
$t_{d(DIR)}$	DIR output delay with respect to the rising edge of pin CLOCK	20 pF total external load per pin	-	-	8.9	ns
$t_{d(NXT)}$	NXT output delay with respect to the rising edge of pin CLOCK	20 pF total external load per pin	-	-	8.9	ns
$V_{CC(I/O)}$ = 3.0 V to 3.6 V						
$t_{su(DATA)}$	DATA set-up time with respect to the rising edge of pin CLOCK	30 pF total external load per pin	3.3	-	-	ns
$t_{h(DATA)}$	DATA hold time with respect to the rising edge of pin CLOCK	30 pF total external load per pin	0.8	-	-	ns
$t_{d(DATA)}$	DATA output delay with respect to the rising edge of pin CLOCK	30 pF total external load per pin	-	-	5.5	ns
$t_{su(STP)}$	STP set-up time with respect to the rising edge of pin CLOCK	30 pF total external load per pin	3.4	-	-	ns
$t_{h(STP)}$	STP hold time with respect to the rising edge of pin CLOCK	30 pF total external load per pin	0.8	-	-	ns
$t_{d(DIR)}$	DIR output delay with respect to the rising edge of pin CLOCK	30 pF total external load per pin	-	-	6.6	ns
$t_{d(NXT)}$	NXT output delay with respect to the rising edge of pin CLOCK	30 pF total external load per pin	-	-	6.6	ns

Table 56. Dynamic characteristics: other characteristics

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(busturn-DV)}$	data valid after bus turnaround delay time	30 pF load; see Figure 28	1.9	-	-	ns
$t_{O(THL)}$	high-to-low output transition time	line impedance 50 Ω	1.2	-	3.1	µs
$t_{O(TLH)}$	low-to-high output transition time	line impedance 50 Ω	1.2	-	3.1	µs

Table 57. Dynamic characteristics: analog I/O pins DP and DM

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High-speed driver						
t_{HSR}	rise time (10 % to 90 %)	drive 45 Ω to GND on pins DP and DM	500	-	-	ps
t_{HSF}	fall time (10 % to 90 %)	drive 45 Ω to GND on pins DP and DM	500	-	-	ps
Full-speed driver						
t_{FR}	rise time	C_L = 50 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 90 % to 10 % of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
FRFM	differential rise time/fall time matching	excluding the first transition from the idle state	90	-	111.1	%
USB low-speed driver characteristics						
t_{LR}	transition time: rise time	C_L = 200 pF to 600 pF; 1.5 kΩ pull-up on pin DM enabled; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LF}	transition time: fall time	C_L = 200 pF to 600 pF; 1.5 kΩ pull-up on pin DM enabled; 90 % to 10 % of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LRFM}	rise and fall time matching	t_{LR}/t_{LF}; excluding the first transition from the idle state	80	-	125	%
Driver timing (valid only for serial mode)						
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	TX_DAT, TX_SE0 to DP, DM; see Figure 24	-	-	11	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	TX_DAT, TX_SE0 to DP, DM; see Figure 24	-	-	11	ns
t_{PHZ}	driver disable delay from HIGH level	TX_ENABLE to DP, DM; see Figure 25	-	-	12	ns
t_{PLZ}	driver disable delay from LOW level	TX_ENABLE to DP, DM; see Figure 25	-	-	12	ns
t_{PZH}	driver enable delay to HIGH level	TX_ENABLE to DP, DM; see Figure 25	-	-	20	ns
t_{PZL}	driver enable delay to LOW level	TX_ENABLE to DP, DM; see Figure 25	-	-	20	ns
Receiver timing (valid only for serial mode)						
Differential receiver						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 26	-	-	17	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 26	-	-	17	ns

Table 57. Dynamic characteristics: analog I/O pins DP and DM *...continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Single-ended receiver						
$t_{PLH(se)}$	single-ended propagation delay (LOW to HIGH)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 26	-	-	17	ns
$t_{PHL(se)}$	single-ended propagation delay (HIGH to LOW)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 26	-	-	17	ns

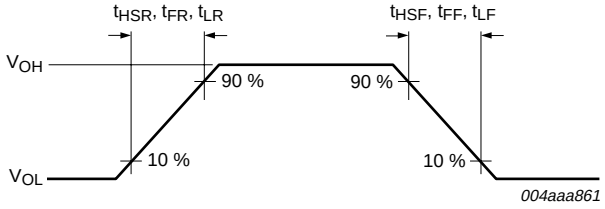


Fig 23. Rise time and fall time

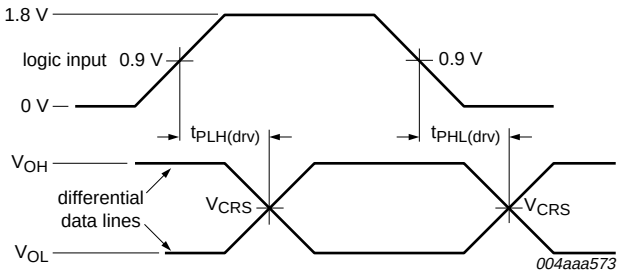


Fig 24. Timing of TX_DAT and TX_SE0 to DP and DM

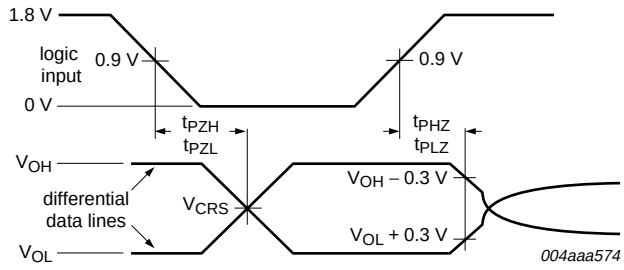


Fig 25. Timing of TX_ENABLE to DP and DM

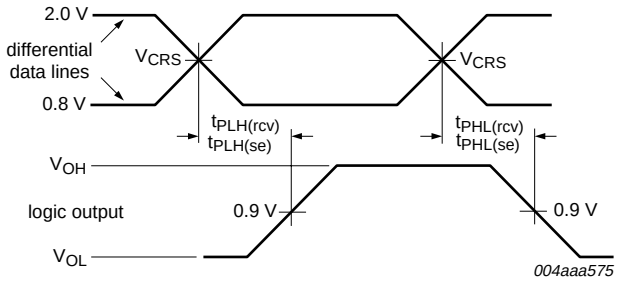


Fig 26. Timing of DP and DM to RX_RCV, RX_DP and RX_DM

14.1 Timing characteristics

ULPI interface timing requirements are given in Figure 27. This timing apply to synchronous mode only. All timing is measured with respect to the ISP1504x1 CLOCK pin. All signals are clocked on the rising edge of CLOCK.

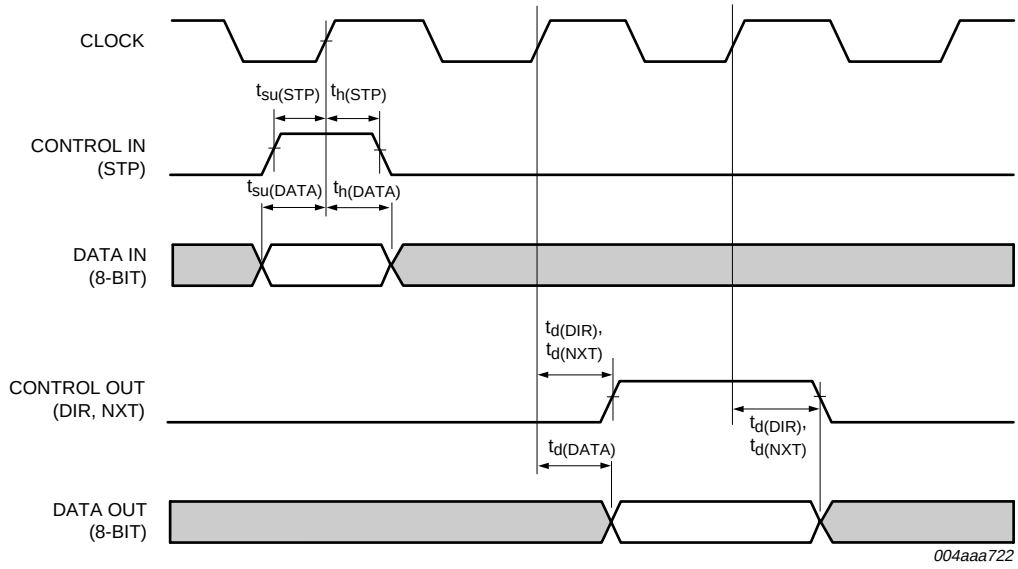


Fig 27. ULPI timing interface

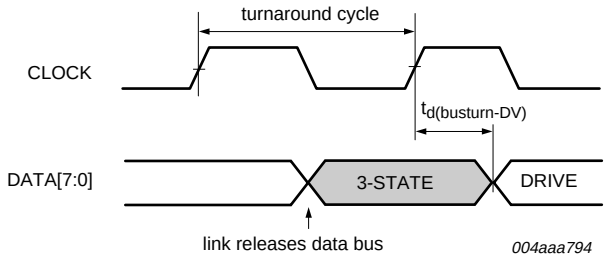


Fig 28. Bus turnaround timing

15. Application information

Table 58. Recommended bill of materials

Designator	Application	Part type	Comment
C_{bypass}	highly recommended for all applications	0.1 µF	-
C_{filter}	highly recommended for all applications	4.7 µF ± 20 %; use a LOW ESR capacitor (0.2 Ω to 2 Ω) for best performance	-
C_{VBUS}	mandatory for peripherals	0.1 µF and 1 µF to 10 µF in parallel	-
	mandatory for host	0.1 µF and 120 µF ± 20 % (min) in parallel	-
	mandatory for OTG	0.1 µF and 1 µF to 6.5 µF in parallel	-
D_{ESD}	recommended for all ESD-sensitive applications	IP4359CX4/LF	Wafer-Level Chip-Scale Package (WLCSP); ESD IEC 61000-4-2 level 4; ±15 kV contact; ±15 kV air discharge compliant protection
R_{pullup}	recommended; for applications with an external V_{BUS} supply controlled by PSW_N	4.7 kΩ (recommended)	-
R_{RREF}	mandatory in all applications	12 kΩ ± 1 %	-
$R_{S(VBUS)}$	strongly recommended for peripheral or external 5 V applications only	1 kΩ ± 5 %	-
R_{XTAL}	required only for applications driving a square wave into the XTAL1 pin	47 kΩ ± 5 %	used to avoid floating input on the XTAL1 pin
XTAL	crystal is used	19.2 MHz	C_L = 10 pF; R_S < 220 Ω; C_{XTAL} = 18 pF[1]
		26 MHz	C_L = 10 pF; R_S < 130 Ω; C_{XTAL} = 18 pF[1]
$C_{(XTAL)SQ}$	required only for applications driving a square wave into the XTAL1 pin that has a DC offset	100 pF	used to AC couple the input square wave to the XTAL1 pin

[1] Recommended crystal specification: 500 µW (max) drive level, ESR 100 Ω (max) and shunt capacitance 7 pF (max).

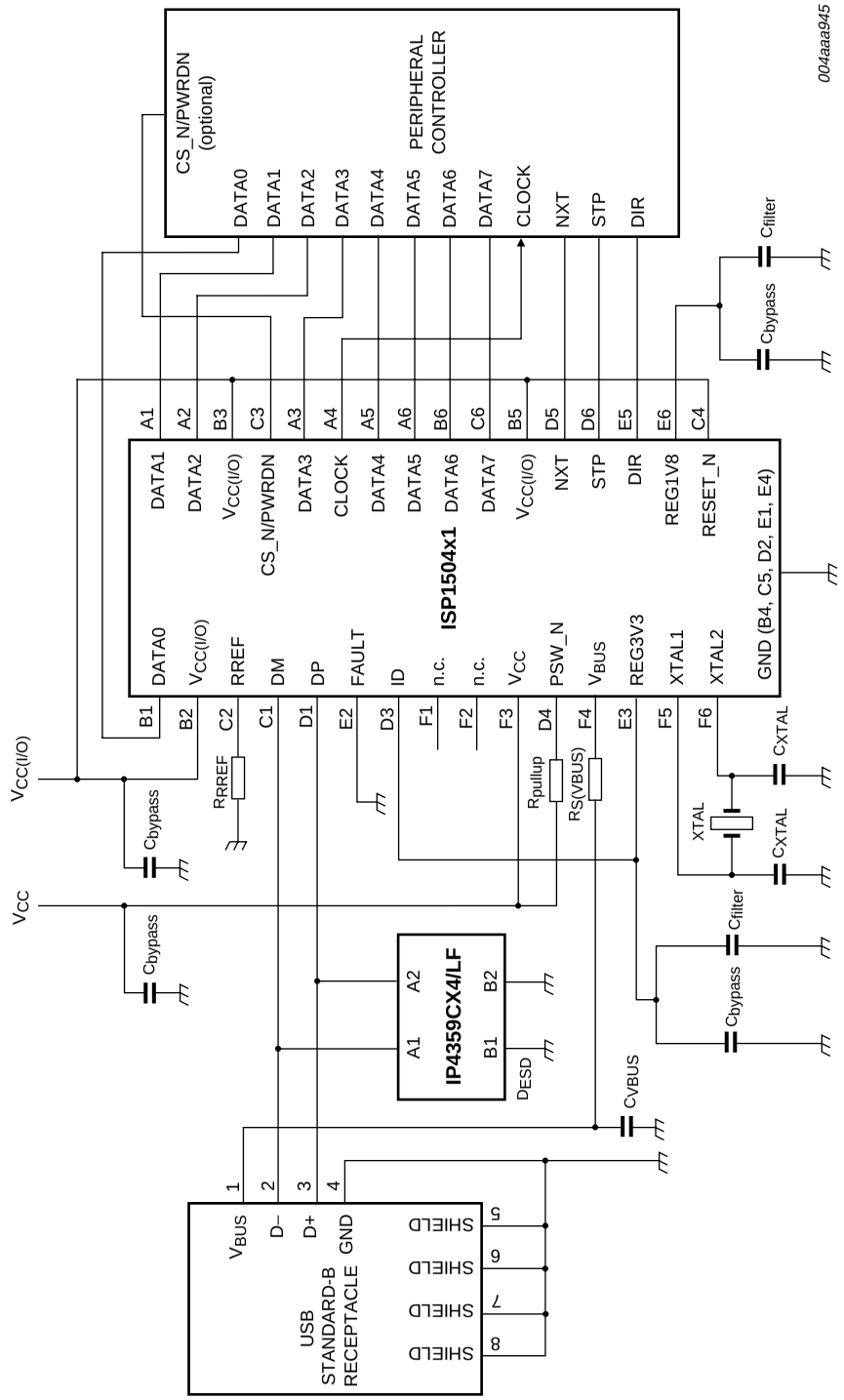
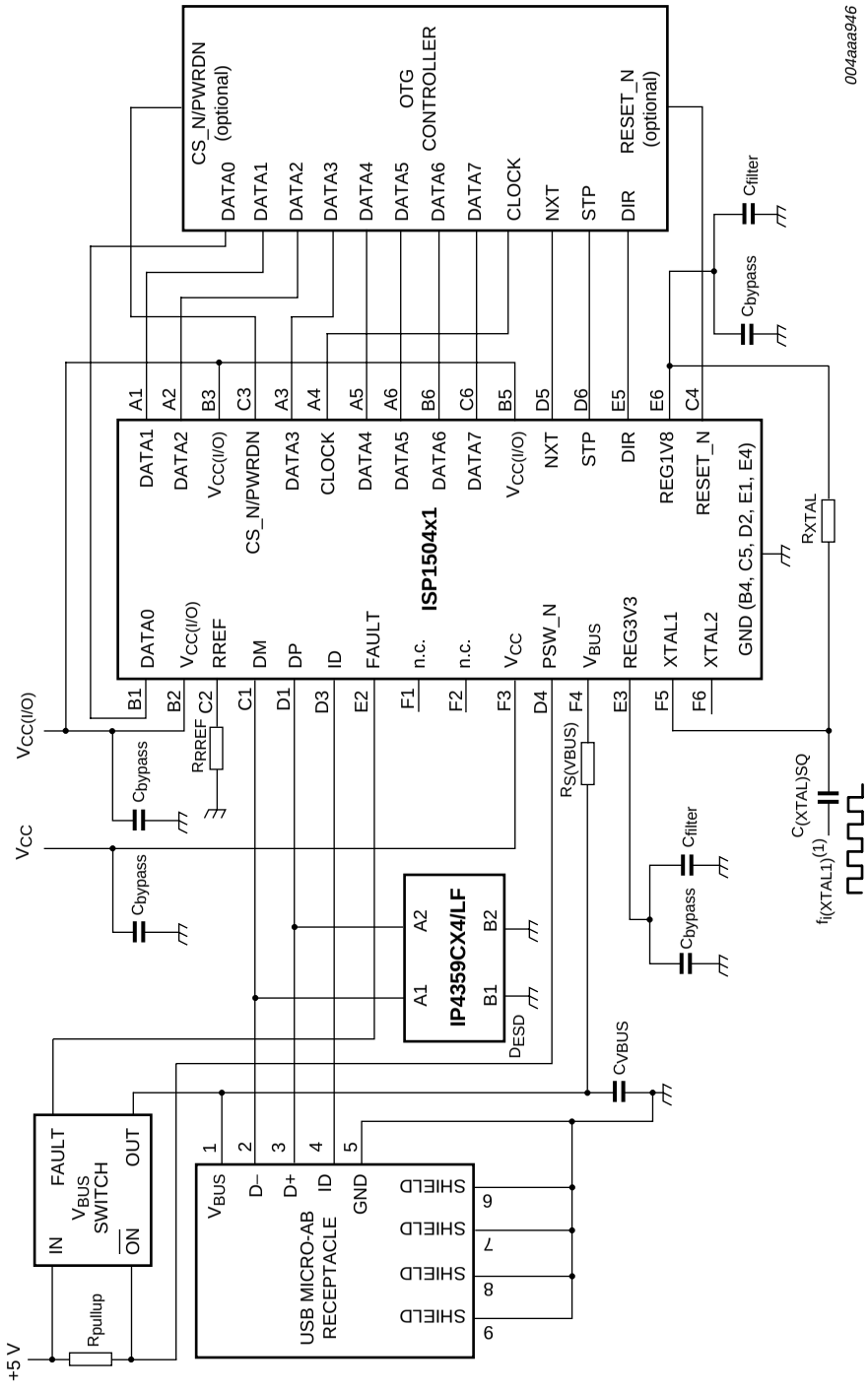


Fig 29. Using the ISP1504x1 with a standard USB Peripheral Controller; external crystal



(1) Can be a square wave clock of 19.2 MHz or 26 MHz.

Fig 30. Using the ISP1504x1 with an OTG Controller; external 5 V source with built-in FAULT and external square wave input on pin XTAL1

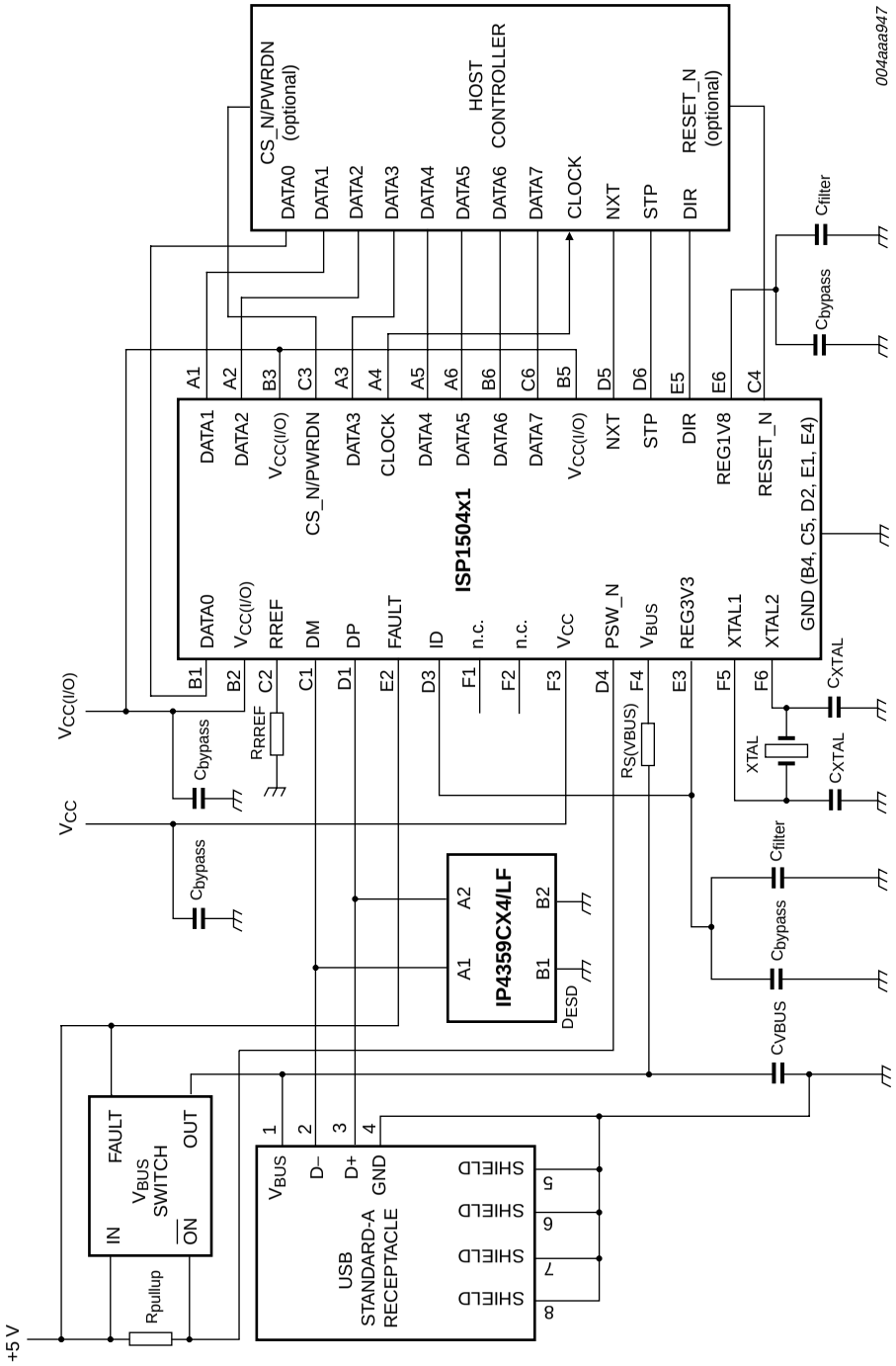
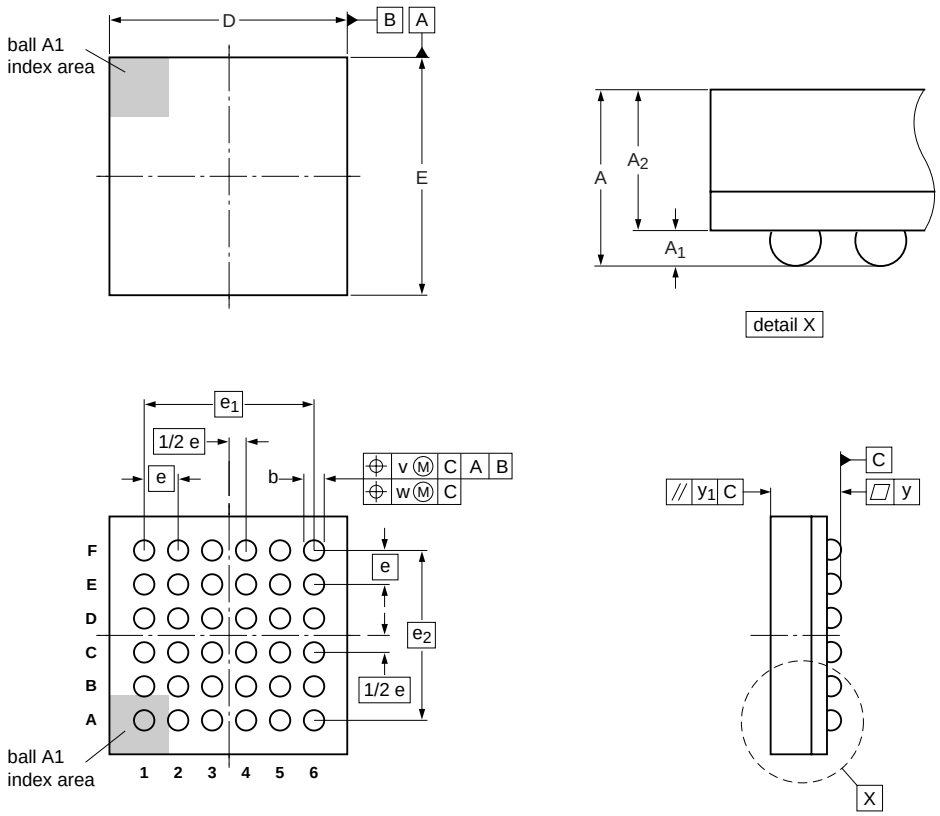


Fig 31. Using the ISP1504x1 with a standard USB Host Controller; external 5 V source with built-in FAULT and external crystal

16. Package outline

TFBGA36: plastic thin fine-pitch ball grid array package; 36 balls; body 3.5 x 3.5 x 0.8 mm **SOT912-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.15	0.25 0.15	0.90 0.75	0.35 0.25	3.6 3.4	3.6 3.4	0.5	2.5	2.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT912-1	- - -	- - -	- - -			~~05-08-09~~ 05-09-01

Fig 32. Package outline SOT912-1 (TFBGA36)

17. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 33) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 59 and 60

Table 59. SnPb eutectic process (from J-STD-020C)

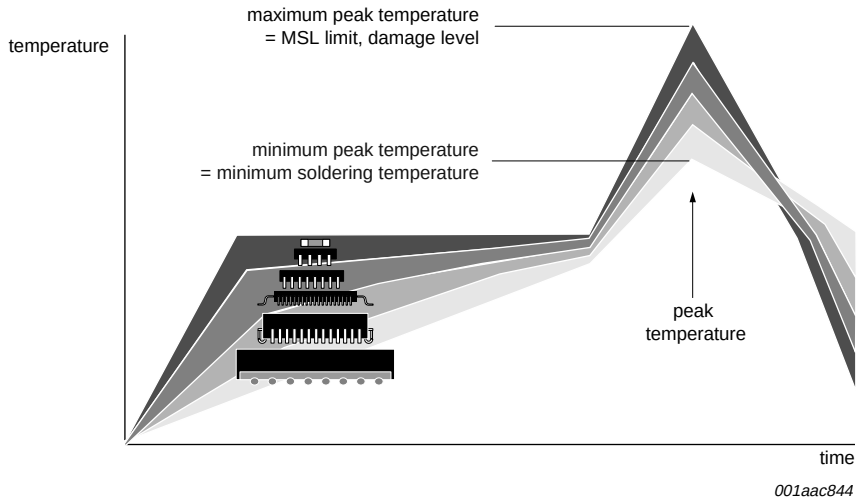
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 60. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 33.



MSL: Moisture Sensitivity Level

Fig 33. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18. Abbreviations

Table 61. Abbreviations

Acronym	Description
ASIC	Application-Specific Integrated Circuit
ATX	Analog USB Transceiver
EOP	End-Of-Packet
ESR	Effective Series Resistance
FS	Full-Speed
HBM	Human Body Model
HNP	Host Negotiation Protocol
HS	High-Speed
ID	Identification
LS	Low-Speed
MM	Machine Model
NRZI	Non-Return-to-Zero Inverted
OTG	On-The-Go
PHY	Physical Layer[1]
PID	Packet Identifier
PLL	Phase-Locked Loop
POR	Power-On Reset
RXCMD	Receive Command
SE0	Single-Ended Zero

Table 61. Abbreviations *...continued*

Acronym	Description
SOF	Start-Of-Frame
SRP	Session Request Protocol
SYNC	Synchronous
TTL	Transistor-Transistor Logic
TXCMD	Transmit Command
USB	Universal Serial Bus
USB-IF	USB Implementers Forum
ULPI	UTMI+ Low Pin Interface
UTMI	USB 2.0 Transceiver Macrocell Interface
UTMI+	USB 2.0 Transceiver Macrocell Interface Plus

[1] Physical layer containing the USB transceiver. The ISP1504x1 is a PHY.

19. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] On-The-Go Supplement to the USB 2.0 Specification Rev. 1.2

[3] UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1

[4] UTMI+ Specification Rev. 1.0

[5] USB 2.0 Transceiver Macrocell Interface (UTMI) Specification Ver. 1.05

[6] Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) (JESD22-A114D)

[7] Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM) (JESD22-A115-A)

[8] Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components (JESD22-C101-C)

20. Revision history

Table 62. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ISP1504A1_ISP1504C1_1	20070806	Product data sheet	-	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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23. Tables

continued >>

continued >>

24. Figures

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