



# High-Performance **Mixed-Signal Microcontrollers**

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Part No.	Flash Memory (bytes)	MIPS (peak)	RAM (bytes)	Digital Port I/O Pins	Serial Buses	Timers (16-bit) PWM/PCA	Internal Oscillator	ADC	DAC	Temp Sensor	VREF	Comparators	Other	Package	EPROM Version	Evaluation Kit	
<b>Automotive MCUs</b>																	
New	C8051F500	64 kB	50	4 kB	40	CAN 2.0, LIN 2.0, SPI, UART, I <sup>2</sup> C	4 6	0.5%	12-bit, 32-ch., 200 ksps	—	Y	Y	2	Volt Reg., -40 to 125 °C	QFP48	—	C8051F500DK
New	C8051F501	64 kB	50	4 kB	40	SPI, UART, I <sup>2</sup> C	4 6	1.0%	12-bit, 32-ch., 200 ksps	—	Y	Y	2	Volt Reg., -40 to 125 °C	QFP48	—	C8051F500DK
New	C8051F502	64 kB	50	4 kB	25	CAN 2.0, LIN 2.0, SPI, UART, I <sup>2</sup> C	4 6	0.5%	12-bit, 25-ch., 200 ksps	—	Y	Y	2	Volt Reg., -40 to 125 °C	QFP32	—	C8051F500DK
New	C8051F503	64 kB	50	4 kB	25	SPI, UART, I <sup>2</sup> C	4 6	1.0%	12-bit, 25-ch., 200 ksps	—	Y	Y	2	Volt Reg., -40 to 125 °C	QFP32	—	C8051F500DK
New	C8051F504	32 kB	50	4 kB	40	CAN 2.0, LIN 2.0, SPI, UART, I <sup>2</sup> C	4 6	0.5%	12-bit, 32-ch., 200 ksps	—	Y	Y	2	Volt Reg., -40 to 125 °C	QFP48	—	C8051F500DK
New	C8051F505	32 kB	50	4 kB	40	SPI, UART, I <sup>2</sup> C	4 6	1.0%	12-bit, 32-ch., 200 ksps	—	Y	Y	2	Volt Reg., -40 to 125 °C	QFP48	—	C8051F500DK
New	C8051F506	32 kB	50	4 kB	25	CAN 2.0, LIN 2.0, SPI, UART, I <sup>2</sup> C	4 6	0.5%	12-bit, 25-ch., 200 ksps	—	Y	Y	2	Volt Reg., -40 to 125 °C	QFP32	—	C8051F500DK
New	C8051F507	32 kB	50	4 kB	25	SPI, UART, I <sup>2</sup> C	4 6	1.0%	12-bit, 25-ch., 200 ksps	—	Y	Y	2	Volt Reg., -40 to 125 °C	QFP32	—	C8051F500DK
New	C8051F520A	8 kB	25	256	6	LIN 2.1, SPI, UART	3 3	0.5%	12-bit, 6ch., 200ksps	—	Y	Y	1	Volt Reg., -40 to 125 °C	DFN10	—	C8051F530DK
New	C8051F521A	8 kB	25	256	6	SPI, UART	3 3	0.5%	12-bit, 6ch., 200ksps	—	Y	Y	1	Volt Reg., -40 to 125 °C	DFN10	—	C8051F530DK
New	C8051F523A	4 kB	25	256	6	LIN 2.1, SPI, UART	3 3	0.5%	12-bit, 6ch., 200ksps	—	Y	Y	1	Volt Reg., -40 to 125 °C	DFN10	—	C8051F530DK
New	C8051F524A	4 kB	25	256	6	SPI, UART	3 3	0.5%	12-bit, 6ch., 200ksps	—	Y	Y	1	Volt Reg., -40 to 125 °C	DFN10	—	C8051F530DK
New	C8051F526A	2 kB	25	256	6	LIN 2.1, SPI, UART	3 3	0.5%	12-bit, 6ch., 200ksps	—	Y	Y	1	Volt Reg., -40 to 125 °C	DFN10	—	C8051F530DK
New	C8051F527A	2 kB	25	256	6	SPI, UART	3 3	0.5%	12-bit, 6ch., 200ksps	—	Y	Y	1	Volt Reg., -40 to 125 °C	DFN10	—	C8051F530DK
New	C8051F530A	8 kB	25	256	16	LIN 2.1, SPI, UART	3 3	0.5%	12-bit, 16ch., 200ksps	—	Y	Y	1	Volt Reg., -40 to 125 °C	TSSOP20	—	C8051F530DK
New	C8051F531A	8 kB	25	256	16	SPI, UART	3 3	0.5%	12-bit, 16ch., 200ksps	—	Y	Y	1	Volt Reg., -40 to 125 °C	QFN20	—	C8051F530DK
New	C8051F533A	4 kB	25	256	16	LIN 2.1, SPI, UART	3 3	0.5%	12-bit, 16ch., 200ksps	—	Y	Y	1	Volt Reg., -40 to 125 °C	QFN20	—	C8051F530DK
New	C8051F534A	4 kB	25	256	16	SPI, UART	3 3	0.5%	12-bit, 16ch., 200ksps	—	Y	Y	1	Volt Reg., -40 to 125 °C	QFN20	—	C8051F530DK
New	C8051F536A	2 kB	25	256	16	LIN 2.1, SPI, UART	3 3	0.5%	12-bit, 16ch., 200ksps	—	Y	Y	1	Volt Reg., -40 to 125 °C	QFN20	—	C8051F530DK
New	C8051F537A	2 kB	25	256	16	SPI, UART	3 3	0.5%	12-bit, 16ch., 200ksps	—	Y	Y	1	Volt Reg., -40 to 125 °C	QFN20	—	C8051F530DK
<b>Interface MCUs</b>																	
	CP2102	1 kB	—	1 kB	—	UART to USB Bridge	— —	Y	—	—	—	—	—	Voltage Reg.	QFN28	—	CP2102EK
	CP2103	1 kB	—	1 kB	4	UART to USB Bridge	— —	Y	—	—	—	—	—	Voltage Reg., RS485, Split V <sub>DDIO</sub>	QFN28	—	CP2103EK
<b>Low-Voltage/Low-Power MCUs</b>																	
	C8051F920	64 kB	25	4 kB	24	UART, EMIS, I <sup>2</sup> C, 2 SPI	4 6	±2%	10-bit, 23ch., 300 ksps	—	Y	Y	2	smaRTClock; up to 23 touch sense inputs	QFN32/ LQFP32	—	C8051F930DK
	C8051F921	64 kB	25	4 kB	16	UART, EMIS, I <sup>2</sup> C, 2 SPI	4 6	±2%	10-bit, 15ch., 300 ksps	—	Y	Y	2	smaRTClock; up to 23 touch sense inputs	QFN24	—	C8051F930DK
	C8051F930	32 kB	25	4 kB	24	UART, EMIS, I <sup>2</sup> C, 2 SPI	4 6	±2%	10-bit, 23ch., 300 ksps	—	Y	Y	2	smaRTClock; up to 23 touch sense inputs	QFN32/ LQFP32	—	C8051F930DK

Part No.	Flash Memory (bytes)		MIPS (peak)	RAM (bytes)	Digital Port I/O Pins	Serial Buses	Timers (16-bit)		PWM/PCA	Internal Oscillator	ADC	DAC	Temp Sensor	VREF	Comparators	Other	Package	Flash Version	Evaluation Kit
C8051F931	32 kB	25	4 kB	16	UART, EMIS, I <sup>2</sup> C, 2 SPI	4 6	±2%	10-bit, 15ch., 300 ksps	—	—	—	Y	Y	2	smaRTClock; up to 23 touch sense inputs	QFN24	—	C8051F930DK	
<b>One Time Programmable EPROM-Based MCUs</b>																			
C8051T600	8 kB	25	256	8	UART, I <sup>2</sup> C	3 3	±2%	10-bit, 8ch., 500 ksps	—	—	—	Y	—	1	VREG	QFN11/SOIC14	F300	C8051T600DK	
C8051T601	8 kB	25	256	8	UART, I <sup>2</sup> C	3 3	±2%	—	—	—	—	—	—	1	VREG	QFN11/SOIC14	F301	C8051T600DK	
C8051T602	4 kB	25	256	8	UART, I <sup>2</sup> C	3 3	±2%	10-bit, 8ch., 500 ksps	—	—	—	Y	—	1	VREG	QFN11/SOIC14	F302	C8051T600DK	
C8051T603	4 kB	25	256	8	UART, I <sup>2</sup> C	3 3	±2%	—	—	—	—	—	—	1	VREG	QFN11/SOIC14	F303	C8051T600DK	
C8051T604	2 kB	25	256	8	UART, I <sup>2</sup> C	3 3	±2%	10-bit, 8ch., 500 ksps	—	—	—	Y	—	1	VREG	QFN11/SOIC14	F304	C8051T600DK	
C8051T605	2 kB	25	256	8	UART, I <sup>2</sup> C	3 3	±2%	—	—	—	—	—	—	1	VREG	QFN11/SOIC14	F305	C8051T600DK	
C8051T610	16 kB	25	1280	29	I <sup>2</sup> C, SPI, UART	4 5	±2%	10-bit, 21ch., 500 ksps	—	—	—	Y	Y	2	VREG	LQFP32	F310	C8051T610DK	
C8051T611	16 kB	25	1280	25	I <sup>2</sup> C, SPI, UART	4 5	±2%	10-bit, 21ch., 500 ksps	—	—	—	Y	—	2	VREG	QFN28	F311	C8051T610DK	
C8051T612	8 kB	25	1280	29	I <sup>2</sup> C, SPI, UART	4 5	±2%	10-bit, 21ch., 500 ksps	—	—	—	Y	—	2	VREG	LQFP32	F312	C8051T610DK	
C8051T613	8 kB	25	1280	25	I <sup>2</sup> C, SPI, UART	4 5	±2%	10-bit, 21ch., 500 ksps	—	—	—	Y	—	2	VREG	QFN28	F313	C8051T610DK	
C8051T614	8 kB	25	1280	29	I <sup>2</sup> C, SPI, UART	4 5	±2%	—	—	—	—	—	—	2	VREG	LQFP32	F314	C8051T610DK	
C8051T615	8 kB	25	1280	25	I <sup>2</sup> C, SPI, UART	4 5	±2%	—	—	—	—	—	—	2	VREG	QFN28	F315	C8051T610DK	
C8051T616	16 kB	25	1280	21	I <sup>2</sup> C, SPI, UART	4 5	±2%	10-bit, 17ch., 500 ksps	—	—	—	Y	—	2	VREG	QFN24	F316	C8051T610DK	
C8051T617	16 kB	25	1280	21	I <sup>2</sup> C, SPI, UART	4 5	±2%	—	—	—	—	—	—	2	VREG	QFN24	F317	C8051T610DK	
C8051T630	8 kB	25	768	17	I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 6ch., 500 ksps	10-bit, 1ch	Y	Y	1	—	—	VREG, LFO	QFN20	F330	C8051T630DK	
C8051T631	8 kB	25	768	17	I <sup>2</sup> C, SPI, UART	4 3	±2%	—	—	—	—	—	—	1	VREG, LFO	QFN20	F331	C8051T630DK	
C8051T632	4 kB	25	768	17	I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 500 ksps	10-bit, 1ch	Y	Y	1	—	—	VREG, LFO	QFN20	F332	C8051T630DK	
C8051T633	4 kB	25	768	17	I <sup>2</sup> C, SPI, UART	4 3	±2%	—	—	—	—	—	—	1	VREG, LFO	QFN20	F333	C8051T630DK	
C8051T634	2 kB	25	768	17	I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 500 ksps	10-bit, 1ch	Y	T	1	—	—	VREG, LFO	QFN20	F334	C8051T630DK	
C8051T635	2 kB	25	768	17	I <sup>2</sup> C, SPI, UART	4 3	±2%	—	—	—	—	—	—	1	VREG, LFO	QFN20	F335	C8051T630DK	
<b>Precision Mixed-Signal MCUs</b>																			
C8051F000	32 kB	20	256	32	UART, I <sup>2</sup> C, SPI	4 5	±20%	12-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	—	TQFP64	—	C8051F005DK	
C8051F001	32 kB	20	256	16	UART, I <sup>2</sup> C, SPI	4 5	±20%	12-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	—	TQFP48	—	C8051F005DK	
C8051F002	32 kB	20	256	8	UART, I <sup>2</sup> C, SPI	4 5	±20%	12-bit, 4ch., 100 ksps	12-bit, 2ch.	Y	Y	1	—	—	—	LQFP32	—	C8051F005DK	
C8051F005	32 kB	25	2304	32	UART, I <sup>2</sup> C, SPI	4 5	±20%	12-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	—	TQFP64	—	C8051F005DK	
C8051F006	32 kB	25	2304	16	UART, I <sup>2</sup> C, SPI	4 5	±20%	12-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	—	TQFP48	—	C8051F005DK	
C8051F007	32 kB	25	2304	8	UART, I <sup>2</sup> C, SPI	4 5	±20%	12-bit, 4ch., 100 ksps	12-bit, 2ch.	Y	Y	1	—	—	—	LQFP32	—	C8051F005DK	
C8051F010	32 kB	20	256	32	UART, I <sup>2</sup> C, SPI	4 5	±20%	10-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	—	TQFP64	—	C8051F005DK	
C8051F011	32 kB	20	256	16	UART, I <sup>2</sup> C, SPI	4 5	±20%	10-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	—	TQFP48	—	C8051F005DK	
C8051F012	32 kB	20	256	8	UART, I <sup>2</sup> C, SPI	4 5	±20%	10-bit, 4ch., 100 ksps	12-bit, 2ch.	Y	Y	1	—	—	—	LQFP32	—	C8051F005DK	
C8051F015	32 kB	25	2304	32	UART, I <sup>2</sup> C, SPI	4 5	±20%	10-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	—	TQFP64	—	C8051F005DK	
C8051F016	32 kB	25	2304	16	UART, I <sup>2</sup> C, SPI	4 5	±20%	10-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	—	TQFP48	—	C8051F005DK	
C8051F017	32 kB	25	2304	8	UART, I <sup>2</sup> C, SPI	4 5	±20%	10-bit, 4ch., 100 ksps	12-bit, 2ch.	Y	Y	1	—	—	—	LQFP32	—	C8051F005DK	
C8051F018	16 kB	25	1280	32	UART, I <sup>2</sup> C, SPI	4 5	±20%	10-bit, 8ch., 100 ksps	—	—	—	Y	Y	2	—	TQFP64	—	C8051F005DK	
C8051F019	16 kB	25	1280	16	UART, I <sup>2</sup> C, SPI	4 5	±20%	10-bit, 8ch., 100 ksps	—	—	—	Y	Y	2	—	TQFP48	—	C8051F005DK	

Part No.	Flash Memory (bytes)	MIPS (peak)	RAM (bytes)	Digital Port I/O Pins	Serial Buses	Timers (16-bit)	PWM/PCA	Internal Oscillator	ADC	DAC	Temp Sensor	VREF	Comparators	Other	Package	EPROM Version	Evaluation Kit
C8051F020	64 kB	25	4352	64	2 UARTs, I <sup>2</sup> C, SPI	5	5 ±20%	12-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	TQFP100	—	C8051F020DK
C8051F021	64 kB	25	4352	32	2 UARTs, I <sup>2</sup> C, SPI	5	5 ±20%	12-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	TQFP64	—	C8051F020DK
C8051F022	64 kB	25	4352	64	2 UARTs, I <sup>2</sup> C, SPI	5	5 ±20%	10-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	TQFP100	—	C8051F020DK
C8051F023	64 kB	25	4352	32	2 UARTs, I <sup>2</sup> C, SPI	5	5 ±20%	10-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	TQFP64	—	C8051F020DK
C8051F040	64 kB	25	4352	64	CAN2.0B, 2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	12-bit, 13ch., 100 ksps	12-bit, 2ch.	Y	Y	3	±60 V PGA	—	TQFP100	—	C8051F040DK
C8051F041	64 kB	25	4352	32	CAN2.0B, 2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	12-bit, 13ch., 100 ksps	12-bit, 2ch.	Y	Y	3	±60 V PGA	—	TQFP64	—	C8051F040DK
C8051F042	64 kB	25	4352	64	CAN2.0B, 2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 13ch., 100 ksps	12-bit, 2ch.	Y	Y	3	±60 V PGA	—	TQFP100	—	C8051F040DK
C8051F043	64 kB	25	4352	32	CAN2.0B, 2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 13ch., 100 ksps	12-bit, 2ch.	Y	Y	3	±60 V PGA	—	TQFP64	—	C8051F040DK
C8051F044	64 kB	25	4352	64	CAN2.0B, 2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 13ch., 100 ksps	—	Y	Y	3	±60 V PGA	—	TQFP100	—	C8051F040DK
C8051F045	64 kB	25	4352	32	CAN2.0B, 2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 13ch., 100 ksps	—	Y	Y	3	±60 V PGA	—	TQFP64	—	C8051F040DK
C8051F046	32 kB	25	4352	64	CAN2.0B, 2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 13ch., 100 ksps	—	Y	Y	3	±60 V PGA	—	TQFP100	—	C8051F040DK
C8051F047	32 kB	25	4352	32	CAN2.0B, 2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 13ch., 100 ksps	—	Y	Y	3	±60 V PGA	—	TQFP64	—	C8051F040DK
C8051F060	64 kB	25	4352	59	CAN2.0B, 2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	16-bit, 2ch., 1 Msps	12-bit, 2ch.	Y	Y	3	DMA	—	TQFP100	—	C8051F060DK
C8051F061	64 kB	25	4352	24	CAN2.0B, 2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	16-bit, 2ch., 1 Msps	12-bit, 2ch.	Y	Y	3	DMA	—	TQFP64	—	C8051F060DK
C8051F062	64 kB	25	4352	59	CAN2.0B, 2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	16-bit, 2ch., 1 Msps	12-bit, 2ch.	Y	Y	3	DMA	—	TQFP100	—	C8051F060DK
C8051F063	64 kB	25	4352	24	CAN2.0B, 2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	16-bit, 2ch., 1 Msps	12-bit, 2ch.	Y	Y	3	DMA	—	TQFP64	—	C8051F060DK
C8051F064	64 kB	25	4352	59	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	16-bit, 2ch., 1 Msps	—	—	Y	3	DMA	—	TQFP100	—	C8051F060DK
C8051F065	64 kB	25	4352	24	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	16-bit, 2ch., 1 Msps	—	—	Y	3	DMA	—	TQFP64	—	C8051F060DK
C8051F066	32 kB	25	4352	59	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	16-bit, 2ch., 1 Msps	—	—	Y	3	DMA	—	TQFP100	—	C8051F060DK
C8051F067	32 kB	25	4352	24	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	16-bit, 2ch., 1 Msps	—	—	Y	3	DMA	—	TQFP64	—	C8051F060DK
C8051F120	128 kB	100	8448	64	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	12-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	16x16 MAC	—	TQFP100	—	C8051F120DK
C8051F121	128 kB	100	8448	32	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	12-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	16x16 MAC	—	TQFP64	—	C8051F120DK
C8051F122	128 kB	100	8448	64	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	16x16 MAC	—	TQFP100	—	C8051F120DK
C8051F123	128 kB	100	8448	32	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	16x16 MAC	—	TQFP64	—	C8051F120DK
C8051F124	128 kB	50	8448	64	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	12-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	TQFP100	—	C8051F120DK
C8051F125	128 kB	50	8448	32	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	12-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	TQFP64	—	C8051F120DK
C8051F126	128 kB	50	8448	64	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	TQFP100	—	C8051F120DK
C8051F127	128 kB	50	8448	32	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 8ch., 100 ksps	12-bit, 2ch.	Y	Y	2	—	—	TQFP64	—	C8051F120DK
C8051F130	128 kB	100	8448	64	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 8ch., 100 ksps	—	Y	Y	2	16x16 MAC	—	TQFP100	—	C8051F120DK
C8051F131	128 kB	100	8448	32	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 8ch., 100 ksps	—	Y	Y	2	16x16 MAC	—	TQFP64	—	C8051F120DK
C8051F132	64 kB	100	8448	64	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 8ch., 100 ksps	—	Y	Y	2	16x16 MAC	—	TQFP100	—	C8051F120DK
C8051F133	64 kB	100	8448	32	2 UARTs, I <sup>2</sup> C, SPI	5	6 ±2%	10-bit, 8ch., 100 ksps	—	Y	Y	2	16x16 MAC	—	TQFP64	—	C8051F120DK
C8051F350	8 kB	50	768	17	UART, I <sup>2</sup> C, SPI	4	3 ±2%	24-bit, 8ch., 1 ksps	8-bit, 2ch.	Y	—	1	—	—	LQFP32	—	C8051F350DK
C8051F351	8 kB	50	768	17	UART, I <sup>2</sup> C, SPI	4	3 ±2%	24-bit, 8ch., 1 ksps	8-bit, 2ch.	Y	—	1	—	—	QFN28	—	C8051F350DK
C8051F352	8 kB	50	768	17	UART, I <sup>2</sup> C, SPI	4	3 ±2%	16-bit, 8ch., 1 ksps	8-bit, 2ch.	Y	—	1	—	—	LQFP32	—	C8051F350DK
C8051F353	8 kB	50	768	17	UART, I <sup>2</sup> C, SPI	4	3 ±2%	16-bit, 8ch., 1 ksps	8-bit, 2ch.	Y	—	1	—	—	QFN28	—	C8051F350DK
<b>Small Form Factor MCUs</b>																	
C8051F206	8 kB	25	1280	32	UART, SPI	3	— ±20%	12-bit, 32ch., 100 ksps	—	—	—	2	—	—	TQFP48	—	C8051F206DK
C8051F220	8 kB	25	256	32	UART, SPI	3	— ±20%	8-bit, 32ch., 100 ksps	—	—	—	2	—	—	TQFP48	—	C8051F226DK
C8051F221	8 kB	25	256	22	UART, SPI	3	— ±20%	8-bit, 32ch., 100 ksps	—	—	—	2	—	—	LQFP32	—	C8051F226DK
C8051F226	8 kB	25	1280	32	UART, SPI	3	— ±20%	8-bit, 32ch., 100 ksps	—	—	—	2	—	—	TQFP48	—	C8051F226DK
C8051F230	8 kB	25	256	32	UART, SPI	3	— ±20%	—	—	—	—	2	—	—	TQFP48	—	C8051F226DK
C8051F231	8 kB	25	256	22	UART, SPI	3	— ±20%	—	—	—	—	2	—	—	LQFP32	—	C8051F226DK
C8051F236	8 kB	25	1280	32	UART, SPI	3	— ±20%	—	—	—	—	2	—	—	TQFP48	—	C8051F226DK
C8051F300	8 kB	25	256	8	UART, I <sup>2</sup> C	3	3 ±2%	8-bit, 8ch., 500 ksps	—	Y	—	1	—	—	QFN11	T600	C8051F300DK



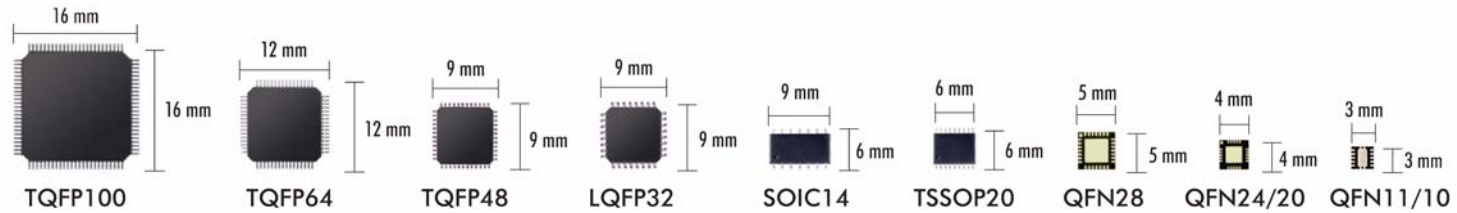
Part No.	Flash Memory (bytes)			MIPS (peak)	RAM (bytes)	Digital Port I/O Pins	Serial Buses	Timers (16-bit)	PWM/PCA	Internal Oscillator	ADC	DAC	Temp Sensor	VREF	Comparators	Other	Package	EPROM Version	Evaluation Kit
C8051F301	8 kB	25	256	8		UART, I <sup>2</sup> C	3 3	±2%	—	—	—	—	—	—	1	—	QFN11	T601	C8051F300DK
C8051F302	8 kB	25	256	8		UART, I <sup>2</sup> C	3 3	±20%	8-bit, 8ch., 500 ksps	—	—	—	Y	—	1	—	QFN11	T602	C8051F300DK
C8051F303	8 kB	25	256	8		UART, I <sup>2</sup> C	3 3	±20%	—	—	—	—	—	—	1	—	QFN11	T603	C8051F300DK
C8051F304	4 kB	25	256	8		UART, I <sup>2</sup> C	3 3	±20%	—	—	—	—	—	—	1	—	QFN11	T604	C8051F300DK
C8051F305	2 kB	25	256	8		UART, I <sup>2</sup> C	3 3	±20%	—	—	—	—	—	—	1	—	QFN11	T605	C8051F300DK
C8051F310	16 kB	25	1280	29		I <sup>2</sup> C, SPI, UART	4 5	±2%	10-bit, 21ch., 200 ksps	—	—	—	Y	—	2	—	LQFP32	T610	C8051F310DK
C8051F311	16 kB	25	1280	25		I <sup>2</sup> C, SPI, UART	4 5	±2%	10-bit, 17ch., 200 ksps	—	—	—	Y	—	2	—	QFN28	T611	C8051F310DK
C8051F312	8 kB	25	1280	29		I <sup>2</sup> C, SPI, UART	4 5	±2%	10-bit, 21ch., 200 ksps	—	—	—	Y	—	2	—	LQFP32	T612	C8051F310DK
C8051F313	8 kB	25	1280	25		I <sup>2</sup> C, SPI, UART	4 5	±2%	10-bit, 17ch., 200 ksps	—	—	—	Y	—	2	—	QFN28	T613	C8051F310DK
C8051F314	8 kB	25	1280	29		I <sup>2</sup> C, SPI, UART	4 5	±2%	—	—	—	—	Y	—	2	—	LQFP32	T614	C8051F310DK
C8051F315	8 kB	25	1280	25		I <sup>2</sup> C, SPI, UART	4 5	±2%	—	—	—	—	Y	—	2	—	QFN28	T615	C8051F310DK
C8051F316	16 kB	25	1280	32		I <sup>2</sup> C, SPI, UART	4 5	±2%	10-bit, 16ch., 200 ksps	—	—	—	Y	—	2	—	QFN24	T616	C8051F310DK
C8051F317	16 kB	25	1280	21		I <sup>2</sup> C, SPI, UART	4 5	±2%	—	—	—	—	Y	—	2	—	QFN24	T617	C8051F310DK
C8051F330	8 kB	25	768	17		I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 200 ksps	10-bit, 1ch.	Y	Y	1	—	—	—	QFN20	T630	C8051F330DK
C8051F330D	8 kB	25	768	17		I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 200 ksps	10-bit, 1ch.	Y	Y	1	—	—	—	PDIP20	—	C8051F330DK
C8051F331	8 kB	25	768	17		I <sup>2</sup> C, SPI, UART	4 3	±2%	—	—	—	—	—	—	1	—	QFN20	T631	C8051F330DK
C8051F332	4 kB	25	768	17		I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 200 ksps	—	—	—	Y	Y	1	—	QFN20	T632	C8051F330DK
C8051F333	4 kB	25	768	17		I <sup>2</sup> C, SPI, UART	4 3	±2%	—	—	—	—	—	—	1	—	QFN20	T633	C8051F330DK
C8051F334	2 kB	25	768	17		I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 200 ksps	—	—	—	Y	Y	1	—	QFN20	T634	C8051F330DK
C8051F335	2 kB	25	768	17		I <sup>2</sup> C, SPI, UART	4 3	±2%	—	—	—	—	—	—	1	—	QFN20	T635	C8051F330DK
C8051F336	16 kB	25	768	17		I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 200 ksps	10-bit, 1ch.	—	—	—	—	1	LFO	QFN20	—	C8051F336DK
C8051F337	16 kB	25	768	17		I <sup>2</sup> C, SPI, UART	4 3	±2%	—	—	—	—	—	—	1	LFO	QFN20	—	C8051F336DK
C8051F338	16 kB	25	768	21		I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 200 ksps	10-bit, 1ch.	—	—	—	—	1	LFO	QFN24	—	C8051F336DK
C8051F339	16 kB	25	768	21		I <sup>2</sup> C, SPI, UART	4 3	±2%	—	—	—	—	—	—	1	LFO	QFN24	—	C8051F336DK
C8051F360	32 kB	100	1 kB	39		I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 200 ksps	10-bit, 2ch.	Y	Y	2	16x16 MAC	—	—	TQFP48	—	C8051F360DK
C8051F361	32 kB	100	1 kB	27		I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 200 ksps	10-bit, 2ch.	Y	Y	2	16x16 MAC	—	—	LQFP32	—	C8051F360DK
C8051F362	32 kB	100	1 kB	24		I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 200 ksps	10-bit, 2ch.	Y	Y	2	16x16 MAC	—	—	QFN28	—	C8051F360DK
C8051F363	32 kB	100	1 kB	39		I <sup>2</sup> C, SPI, UART	4 3	±2%	—	—	—	—	—	—	2	16x16 MAC	TQFP48	—	C8051F360DK
C8051F364	32 kB	100	1 kB	27		I <sup>2</sup> C, SPI, UART	4 3	±2%	—	—	—	—	—	—	2	16x16 MAC	LQFP32	—	C8051F360DK
C8051F365	32 kB	100	1 kB	24		I <sup>2</sup> C, SPI, UART	4 3	±2%	—	—	—	—	—	—	2	16x16 MAC	QFN28	—	C8051F360DK
C8051F366	32 kB	50	1 kB	29		I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 200 ksps	—	—	—	Y	Y	2	16x16 MAC	LQFP32	—	C8051F360DK
C8051F367	32 kB	50	1 kB	25		I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 200 ksps	—	—	—	Y	Y	2	16x16 MAC	QFN28	—	C8051F360DK
C8051F368	16 kB	50	1 kB	29		I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 200 ksps	—	—	—	Y	Y	2	16x16 MAC	LQFP32	—	C8051F360DK
C8051F369	16 kB	50	1 kB	25		I <sup>2</sup> C, SPI, UART	4 3	±2%	10-bit, 16ch., 200 ksps	—	—	—	Y	Y	2	16x16 MAC	QFN28	—	C8051F360DK
C8051F410	32 kB	50	2304	24		I <sup>2</sup> C, SPI, UART	4 6	±2%	12-bit, 24ch., 200 ksps	12-bit, 2ch.	Y	Y	2	VREG, RTC	—	—	LQFP32	—	C8051F410DK
C8051F411	32 kB	50	2304	20		I <sup>2</sup> C, SPI, UART	4 6	±2%	12-bit, 20ch., 200 ksps	12-bit, 2ch.	Y	Y	2	VREG, RTC	—	—	QFN28	—	C8051F410DK
C8051F412	16 kB	50	1280	24		I <sup>2</sup> C, SPI, UART	4 6	±2%	12-bit, 24ch., 200 ksps	12-bit, 2ch.	Y	Y	2	VREG, RTC	—	—	LQFP32	—	C8051F410DK
C8051F413	16 kB	50	1280	20		I <sup>2</sup> C, SPI, UART	4 6	±2%	12-bit, 20ch., 200 ksps	12-bit, 2ch.	Y	Y	2	VREG, RTC	—	—	QFN28	—	C8051F410DK
<b>USB MCUs</b>																			
C8051F320	16 kB	25	2304	25		USB 2.0, UART, I <sup>2</sup> C, SPI	4 5	±1.5%	10-bit, 17ch., 200 ksps	—	—	—	Y	Y	2	—	LQFP32	—	C8051F320DK
C8051F321	16 kB	25	2304	21		USB 2.0, UART, I <sup>2</sup> C, SPI	4 5	±1.5%	10-bit, 13ch., 200 ksps	—	—	—	Y	Y	2	—	QFN28	—	C8051F320DK

Part No.	Flash Memory (bytes)	MIPS (peak)	RAM (bytes)	Digital Port I/O Pins	Serial Buses	Timers (16-bit) PWM/PCA	Internal Oscillator	ADC	DAC	Temp Sensor	VREF	Comparators	Other	Package	EPROM Version	Evaluation Kit
C8051F326	16 kB	25	1536	15	USB 2.0, UART	2	— ±1.5%	—	—	—	—	—	Separate I/O Supply Pin	QFN28	—	C8051F326DK
C8051F327	16 kB	25	1536	15	USB 2.0, UART	2	— ±1.5%	—	—	—	—	—	—	QFN28	—	C8051F326DK
C8051F340	64 kB	48	5376	40	USB 2.0, 2 x UART, I <sup>2</sup> C, SPI	4	5 ±1.5%	10-bit, 17ch., 200 ksps	—	Y	Y	2	—	TQFP48	—	C8051F340DK
C8051F341	32 kB	48	3328	40	USB 2.0, 2 x UART, I <sup>2</sup> C, SPI	4	5 ±1.5%	10-bit, 17ch., 200 ksps	—	Y	Y	2	—	TQFP48	—	C8051F340DK
C8051F342	64 kB	48	5376	25	USB 2.0, UART, I <sup>2</sup> C, SPI	4	5 ±1.5%	10-bit, 17ch., 200 ksps	—	Y	Y	2	—	LQFP32	—	C8051F340DK
C8051F343	32 kB	48	3328	25	USB 2.0, UART, I <sup>2</sup> C, SPI	4	5 ±1.5%	10-bit, 17ch., 200 ksps	—	Y	Y	2	—	LQFP32	—	C8051F340DK
C8051F344	64 kB	25	5376	40	USB 2.0, 2 x UART, I <sup>2</sup> C, SPI	4	5 ±1.5%	10-bit, 17ch., 200 ksps	—	Y	Y	2	—	TQFP48	—	C8051F340DK
C8051F345	32 kB	25	3328	40	USB 2.0, 2 x UART, I <sup>2</sup> C, SPI	4	5 ±1.5%	10-bit, 17ch., 200 ksps	—	Y	Y	2	—	TQFP48	—	C8051F340DK
C8051F346	64 kB	25	5376	25	USB 2.0, UART, I <sup>2</sup> C, SPI	4	5 ±1.5%	10-bit, 17ch., 200 ksps	—	Y	Y	2	—	LQFP32	—	C8051F340DK
C8051F347	32 kB	25	3328	25	USB 2.0, UART, I <sup>2</sup> C, SPI	4	5 ±1.5%	10-bit, 17ch., 200 ksps	—	Y	Y	2	—	LQFP32	—	C8051F340DK
<b>New</b> C8051F348	32 kB	25	256	40	SMBus, SPI, UART0, UART1	4	5 ±1.5%	—	—	—	—	2	Volt. Reg. EMIF	QFP48	—	C8051F340DK
<b>New</b> C8051F349	32 kB	25	256	25	SMBus, SPI, UART0	4	5 ±1.5%	—	—	—	—	2	Volt. Reg.	QFP32	—	C8051F340DK
<b>New</b> C8051F34A	64 kB	48	5376	25	USB 2.0, 2x UART, I <sup>2</sup> C, SPI	4	5 ±1.5%	10-bit, 17ch., 200 ksps	—	1	1	2	—	LQFP32	—	C8051F340DK
<b>New</b> C8051F34B	32 kB	48	3328	25	USB 2.0, 2x UART, I <sup>2</sup> C, SPI	4	5 ±1.5%	10-bit, 17ch., 200 ksps	—	1	1	2	—	LQFP32	—	C8051F340DK

Interface MCUs (Ethernet)

Part Number	Flash	Parallel Host Interface	Parallel Host Interface Speed	Auto-Negotiation	Pre-Programmed MAC Address	RAM Size	LEDs	Temp. Range	Transceiver	Package	Eval Kit	Dev Kit
CP2200	8 kB	8-bit non-multiplexed EMIF	30 Mbps	Y	Y	2 kB TX & 4 kB RX buffer	Separate link and activity	-40 to +85	Included	TQFP48	CP2201EK	ETHERNETDK
CP2201	8 kB	8-bit multiplexed EMIF	25 Mbps	Y	Y	2 kB TX & 4 kB RX buffer	Combined link and activity	-40 to +85	Included	QFN28	CP2201EK	ETHERNETDK

Package Sizes





# Automotive MCUs

### Analog Peripherals

12-Bit ADC, 5 V input signal; up to 32 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

Built-in Temperature Sensor ( $\pm 3$  °C)

Two Comparators

Precision Internal Voltage Reference

V<sub>DD</sub> Monitor/Brown-out Detector

On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Multiple power saving sleep and shutdown modes

**Temperature Range: -40 to +125 °C**

**Operating Voltage: 1.8 to 5.25 V**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput

### Memory

- 64 kB Flash; in-system programmable; flexible security features
- 4352 bytes data RAM (256 + 4 kB)

### CAN 2.0B

- 32 message objects

### LIN 2.1

- Master or slave operation using dedicated hardware

### Digital Peripherals

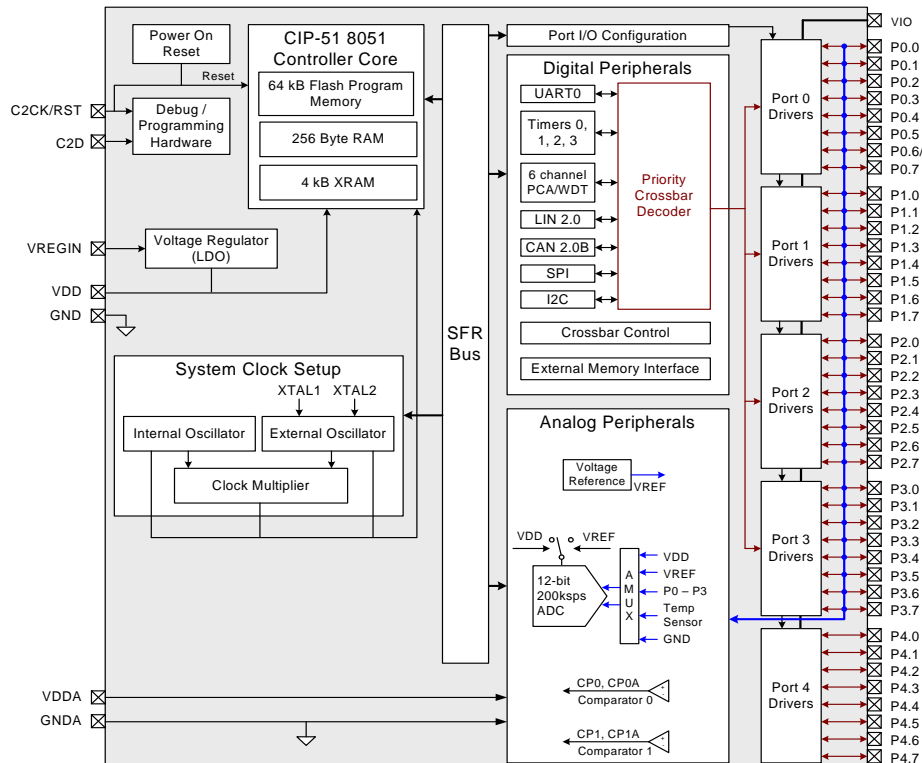
- Up to 40 digital I/O; all are 5 V push-pull
- Hardware I<sup>2</sup>C, SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 4 general-purpose 16-bit counter/timers
- External Memory Interface (EMIF)

### Clock Sources

- Internal programmable 0.5% oscillator: up to 50 MHz
- External oscillator: Crystal, RC, C, or CMOS Clock

### Ordering Part Numbers

- C8051F500-IM, 48-Pin QFN (RoHS-compliant), 7x7 mm<sup>2</sup>
- C8051F500-IQ, 48-Pin QFP (RoHS-compliant), 9x9 mm<sup>2</sup>



### Analog Peripherals

**12-Bit ADC, 5 V input signal; up to 32 external inputs**

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

**Built-in Temperature Sensor ( $\pm 3$  °C)**

**Two Comparators**

**Precision Internal Voltage Reference**

**V<sub>DD</sub> Monitor/Brown-out Detector**

**On-Chip Debug**

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Multiple power saving sleep and shutdown modes

**Temperature Range: -40 to +125 °C**

**Operating Voltage: 1.8 to 5.25 V**

**Development Kit: C8051F500DK**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput

### Memory

- 64 kB Flash; in-system programmable; flexible security features
- 4352 bytes data RAM (256 + 4 kB)

### Digital Peripherals

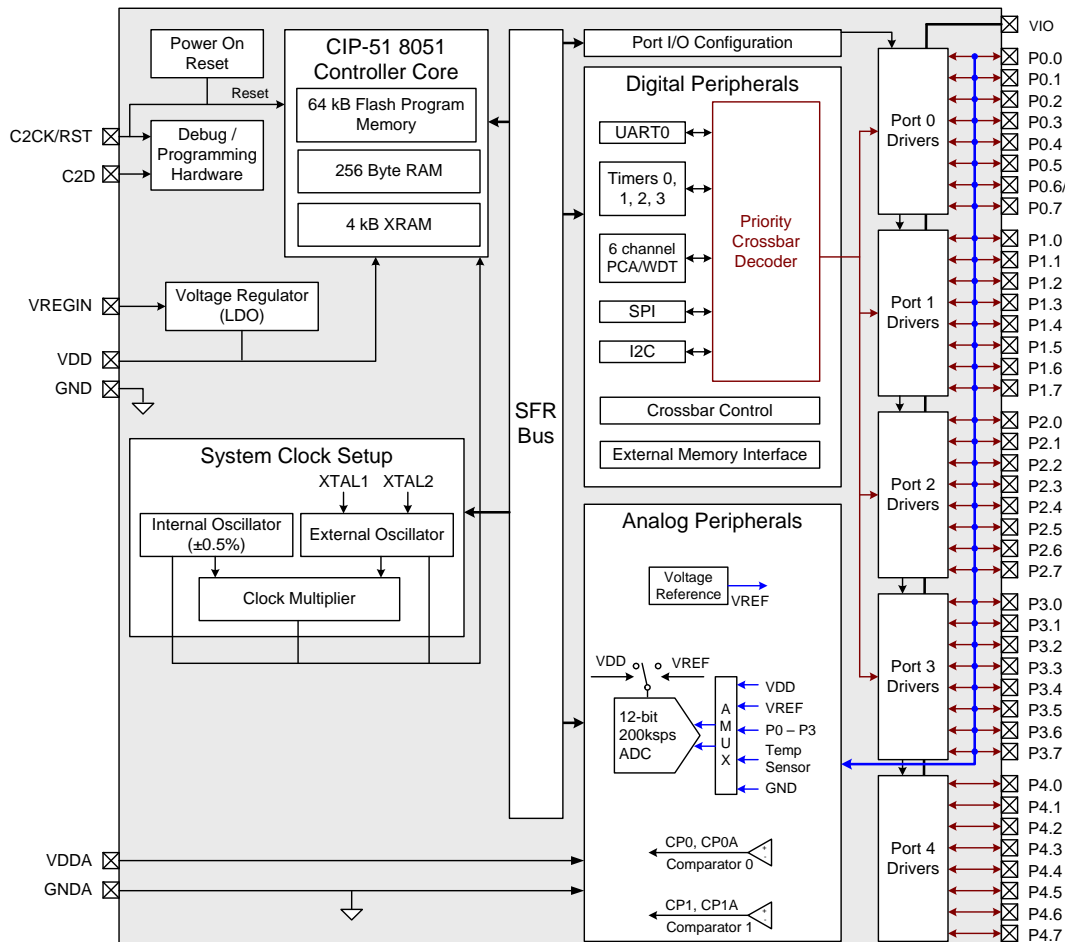
- Up to 40 digital I/O; all are 5 V push-pull
- Hardware I<sup>2</sup>C, SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 4 general-purpose 16-bit counter/timers
- External Memory Interface (EMIF)

### Clock Sources

- Internal programmable  $\pm 0.5\%$  oscillator: up to 50 MHz
- External oscillator: Crystal, RC, C, or CMOS Clock

### Ordering Part Numbers

- C8051F501-IM, 48-Pin QFN (RoHS-compliant), 7x7 mm<sup>2</sup>
- C8051F501-IQ, 48-Pin QFP (RoHS-compliant), 9x9 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 24 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Two Comparators

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
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#### Temperature Range: -40 to +125 °C

#### Operating Voltage: 1.8 to 5.25 V

#### Development Kit: C8051F500DK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput

### Memory

- 64 kB Flash; in-system programmable; flexible security features
- 4352 bytes data RAM (256 + 4 kB)

### CAN 2.0B

- 32 message objects

### LIN 2.1

- Master or slave operation using dedicated hardware

### Digital Peripherals

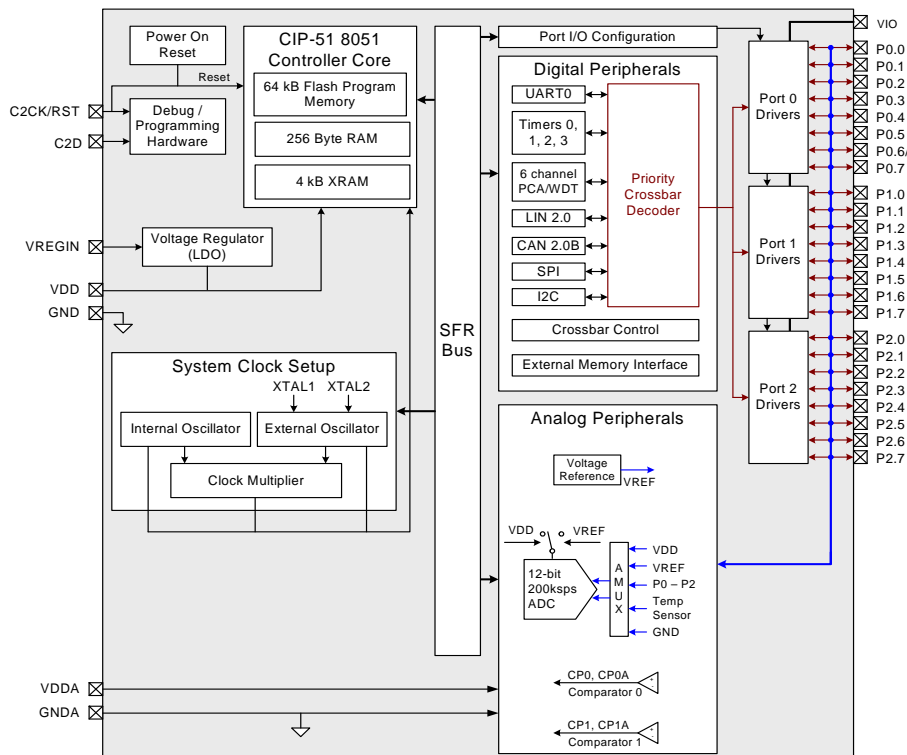
- Up to 24 digital I/O; all are 5 V push-pull
- Hardware I<sup>2</sup>C, SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 4 general-purpose 16-bit counter/timers
- External Memory Interface (EMIF)

### Clock Sources

- Internal programmable  $\pm 0.5\%$  oscillator: up to 50 MHz
- External oscillator: Crystal, RC, C, or CMOS Clock

### Ordering Part Numbers

- C8051F502-IM, 32-Pin QFN (RoHS-compliant), 5x5 mm<sup>2</sup>
- C8051F502-IQ, 32-Pin QFP (RoHS-compliant), 9x9 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 24 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksp/s
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Two Comparators

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Multiple power saving sleep and shutdown modes

### Temperature Range: -40 to +125 °C

### Operating Voltage: 1.8 to 5.25 V

### Development Kit: C8051F500DK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput

### Memory

- 64 kB Flash; in-system programmable; flexible security features
- 4352 bytes data RAM (256 + 4 kB)

### Digital Peripherals

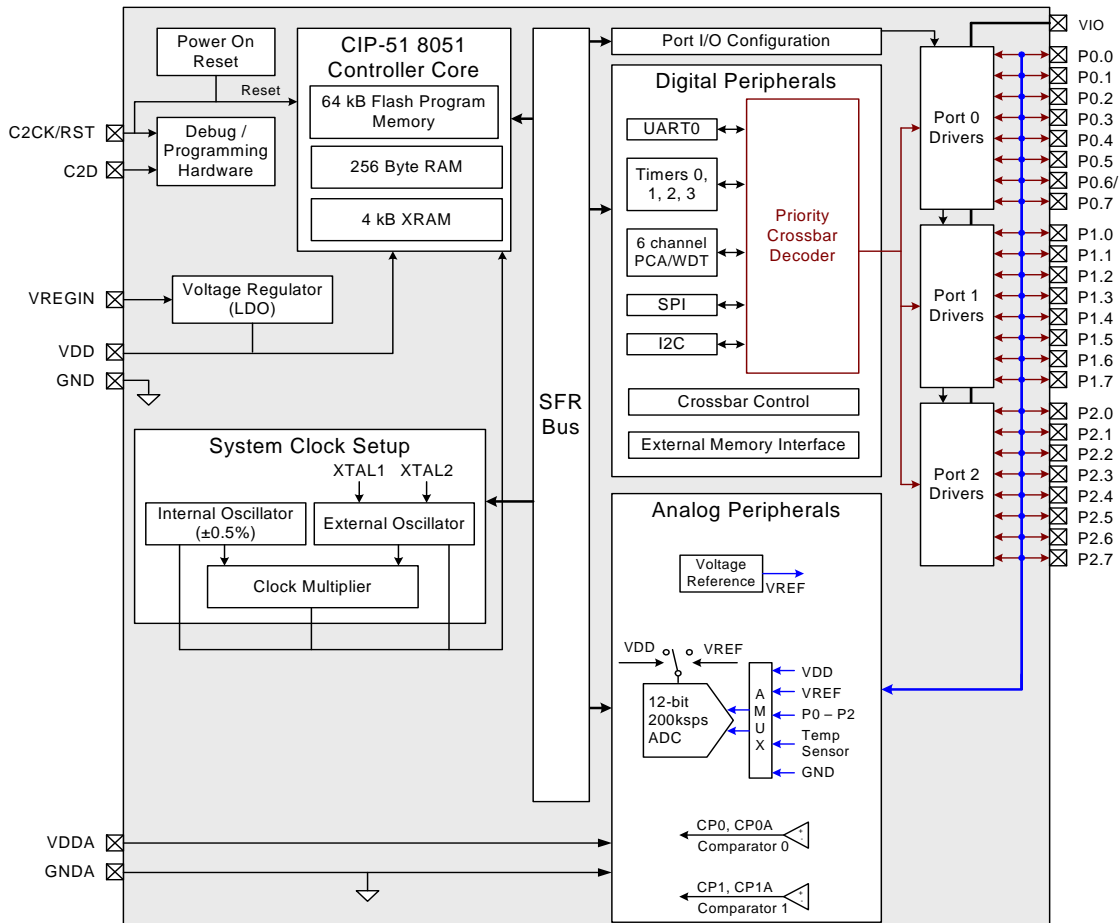
- Up to 24 digital I/O; all are 5 V push-pull
- Hardware I<sup>2</sup>C, SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 4 general-purpose 16-bit counter/timers
- External Memory Interface (EMIF)

### Clock Sources

- Internal programmable  $\pm 0.5\%$  oscillator: up to 50 MHz
- External oscillator: Crystal, RC, C, or CMOS Clock

### Ordering Part Numbers

- C8051F503-IM, 32-Pin QFN (RoHS-compliant), 5x5 mm<sup>2</sup>
- C8051F503-IQ, 32-Pin QFP (RoHS-compliant), 9x9 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 32 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Two Comparators

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Multiple power saving sleep and shutdown modes

**Temperature Range: -40 to +125 °C**

**Operating Voltage: 1.8 to 5.25 V**

**Development Kit: C8051F500DK**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput

### Memory

- 32 kB Flash; in-system programmable; flexible security features
- 4352 bytes data RAM (256 + 4 kB)

### CAN 2.0B

- 32 message objects

### LIN 2.1

- Master or slave operation using dedicated hardware

### Digital Peripherals

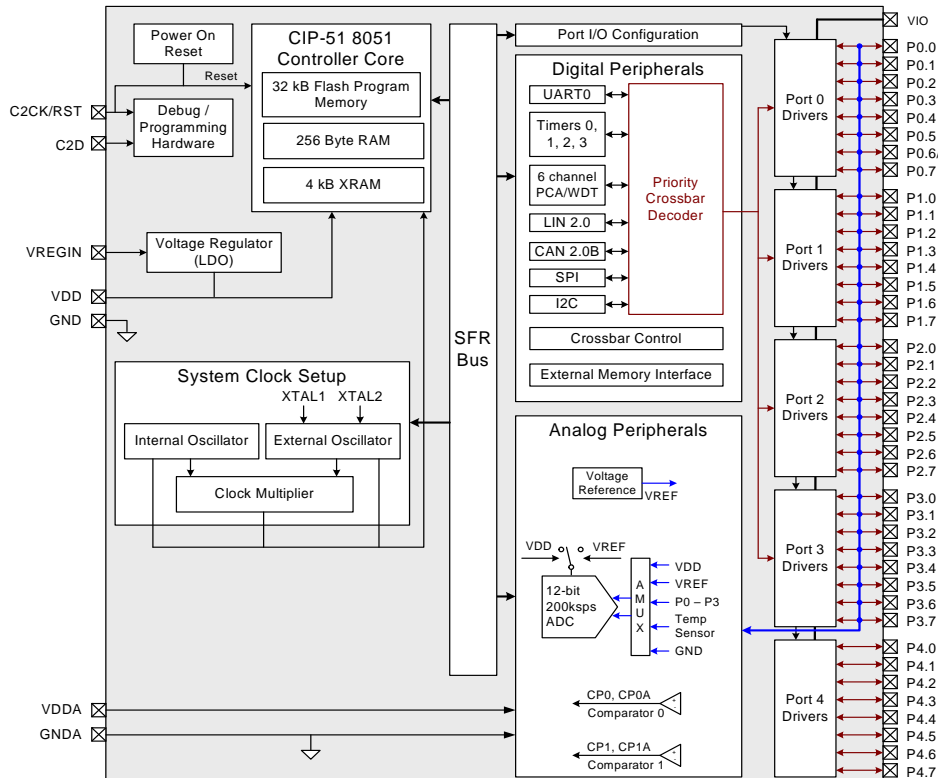
- Up to 40 digital I/O; all are 5 V push-pull
- Hardware I<sup>2</sup>C, SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 4 general-purpose 16-bit counter/timers
- External Memory Interface (EMIF)

### Clock Sources

- Internal programmable  $\pm 0.5\%$  oscillator: up to 50 MHz
- External oscillator: Crystal, RC, C, or CMOS Clock

### Ordering Part Numbers

- C8051F504-IM, 48-Pin QFN (RoHS-compliant), 7x7 mm<sup>2</sup>
- C8051F504-IQ, 48-Pin QFP (RoHS-compliant), 9x9 mm<sup>2</sup>





### Analog Peripherals

**12-Bit ADC, 5 V input signal; up to 32 external inputs**

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

**Built-in Temperature Sensor ( $\pm 3$  °C)**

**Two Comparators**

**Precision Internal Voltage Reference**

**V<sub>DD</sub> Monitor/Brown-out Detector**

**On-Chip Debug**

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
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- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Multiple power saving sleep and shutdown modes

**Temperature Range: -40 to +125 °C**

**Operating Voltage: 1.8 to 5.25 V**

**Development Kit: C8051F500DK**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput

### Memory

- 32 kB Flash; in-system programmable; flexible security features
- 4352 bytes data RAM (256 + 4 kB)

### Digital Peripherals

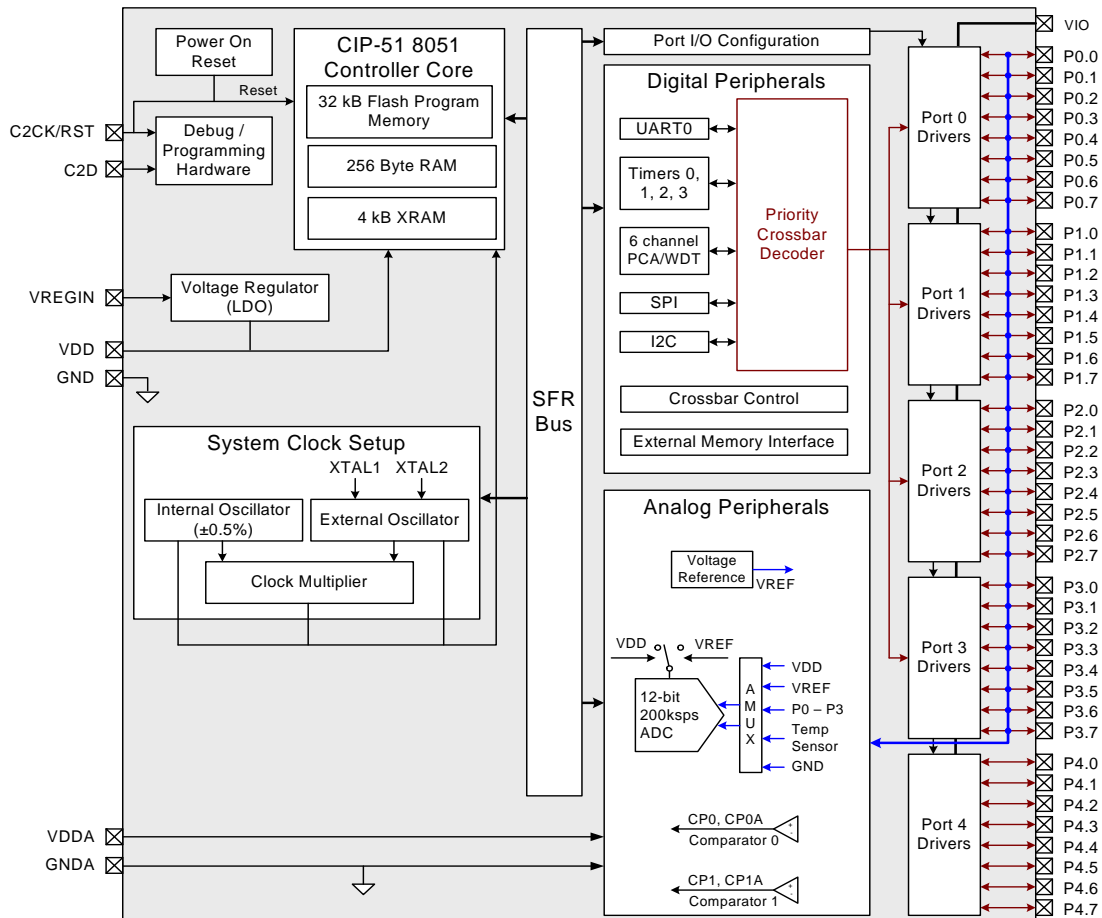
- Up to 40 digital I/O; all are 5 V push-pull
- Hardware I<sup>2</sup>C, SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 4 general-purpose 16-bit counter/timers
- External Memory Interface (EMIF)

### Clock Sources

- Internal programmable  $\pm 0.5\%$  oscillator: up to 50 MHz
- External oscillator: Crystal, RC, C, or CMOS Clock

### Ordering Part Numbers

- C8051F505-IM, 48-Pin QFN (RoHS-compliant), 7x7 mm<sup>2</sup>
- C8051F505-IQ, 48-Pin QFP (RoHS-compliant), 9x9 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 24 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Two Comparators

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Multiple power saving sleep and shutdown modes

**Temperature Range: -40 to +125 °C**

**Operating Voltage: 1.8 to 5.25 V**

**Development Kit: C8051F500DK**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput

### Memory

- 32 kB Flash; in-system programmable; flexible security features
- 4352 bytes data RAM (256 + 4 kB)

### CAN 2.0B

- 32 message objects

### LIN 2.1

- Master or slave operation using dedicated hardware

### Digital Peripherals

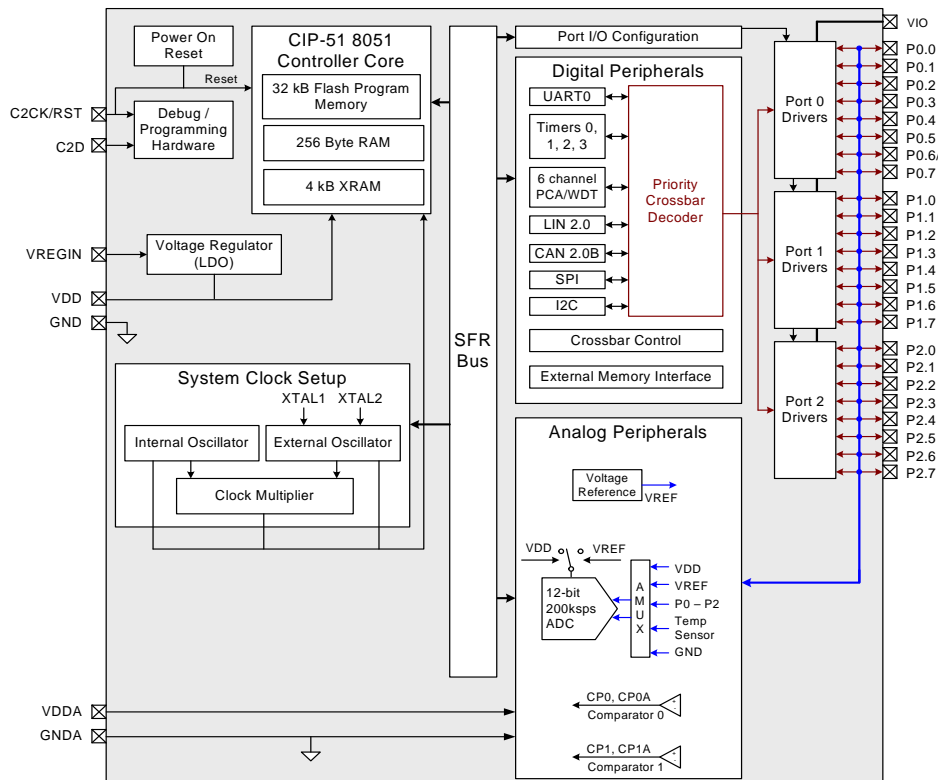
- Up to 24 digital I/O; all are 5 V push-pull
- Hardware I<sup>2</sup>C, SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 4 general-purpose 16-bit counter/timers
- External Memory Interface (EMIF)

### Clock Sources

- Internal programmable  $\pm 0.5\%$  oscillator: up to 50 MHz
- External oscillator: Crystal, RC, C, or CMOS Clock

### Ordering Part Numbers

- C8051F506-IM, 32-Pin QFN (RoHS-compliant), 5x5 mm<sup>2</sup>
- C8051F506-IQ, 32-Pin QFP (RoHS-compliant), 9x9 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 24 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Two Comparators

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Multiple power saving sleep and shutdown modes

#### Temperature Range: -40 to +125 °C

#### Operating Voltage: 1.8 to 5.25 V

#### Development Kit: C8051F500DK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput

### Memory

- 32 kB Flash; in-system programmable; flexible security features
- 4352 bytes data RAM (256 + 4 kB)

### Digital Peripherals

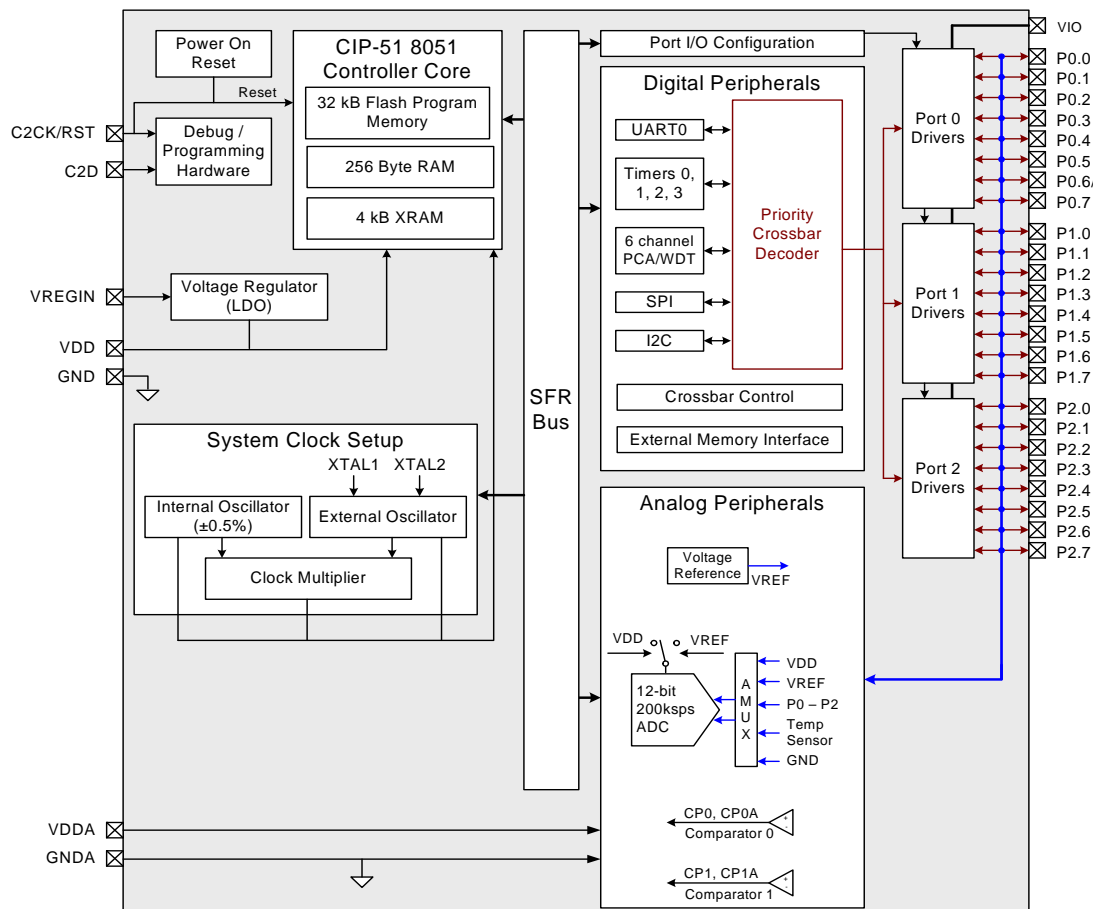
- Up to 24 digital I/O; all are 5 V push-pull
- Hardware I<sup>2</sup>C, SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 4 general-purpose 16-bit counter/timers
- External Memory Interface (EMIF)

### Clock Sources

- Internal programmable  $\pm 0.5\%$  oscillator: up to 50 MHz
- External oscillator: Crystal, RC, C, or CMOS Clock

### Ordering Part Numbers

- C8051F507-IM, 32-Pin QFN (RoHS-compliant), 5x5 mm<sup>2</sup>
- C8051F507-IQ, 32-Pin QFP (RoHS-compliant), 9x9 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 6 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksp/s
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Programmable Comparator

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

### Temperature Range: -40 to +125 °C

### Supply Voltage: 1.8 to 5.25 V

- Typical operating current: 7 mA at 25 MHz at 5.0 V
- Multiple power saving sleep and shutdown modes

### Development Kit: C8051F530ADK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 8 kB Flash; in-system programmable; flexible security features
- 256 bytes data RAM

### LIN 2.1

- Master or slave operation using dedicated hardware (not software implementation with UART)

### Digital Peripherals

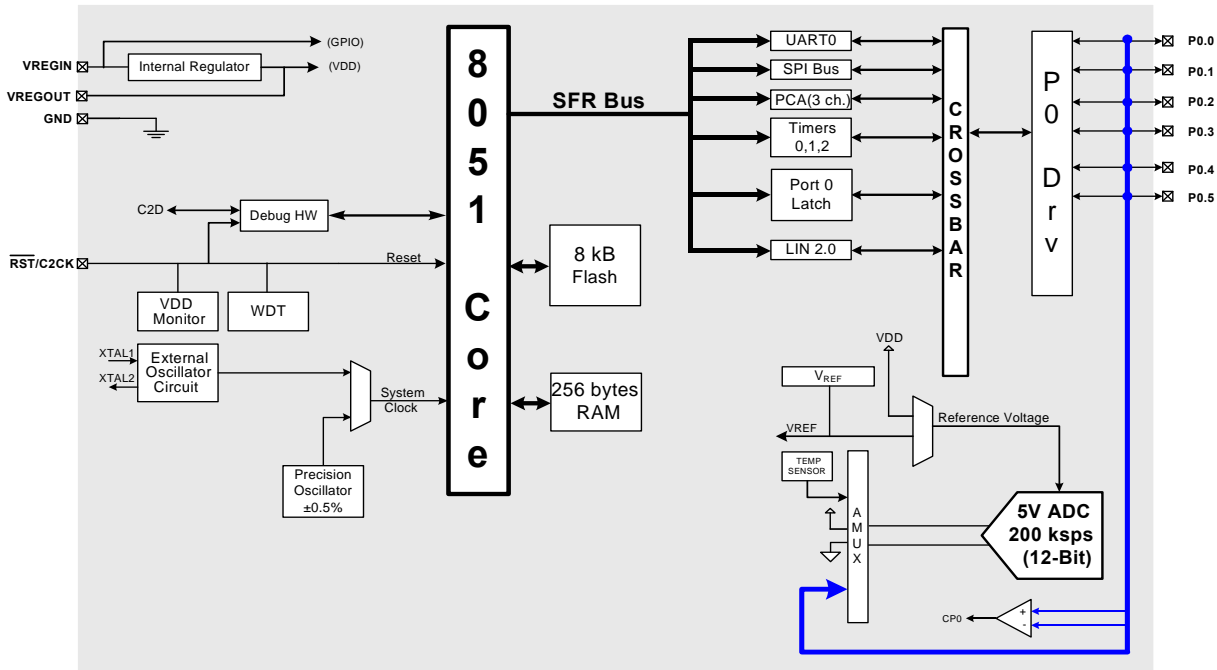
- Up to six digital I/O; all are 5 V push-pull
- Programmable 16-bit counter array with three capture/compare modules
- Three general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- High-precision internal programmable oscillator up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Ordering Part Number

- C8051F520A-IM, 10-Pin QFN (RoHS-compliant), 3x3 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 6 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Programmable Comparator

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

#### Temperature Range: -40 to +125 °C

#### Supply Voltage: 1.8 to 5.25 V

- Typical operating current: 7 mA at 25 MHz at 5.0 V
- Multiple power saving sleep and shutdown modes

#### Development Kit: C8051F530ADK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 8 kB Flash; in-system programmable; flexible security features
- 256 bytes data RAM

### Digital Peripherals

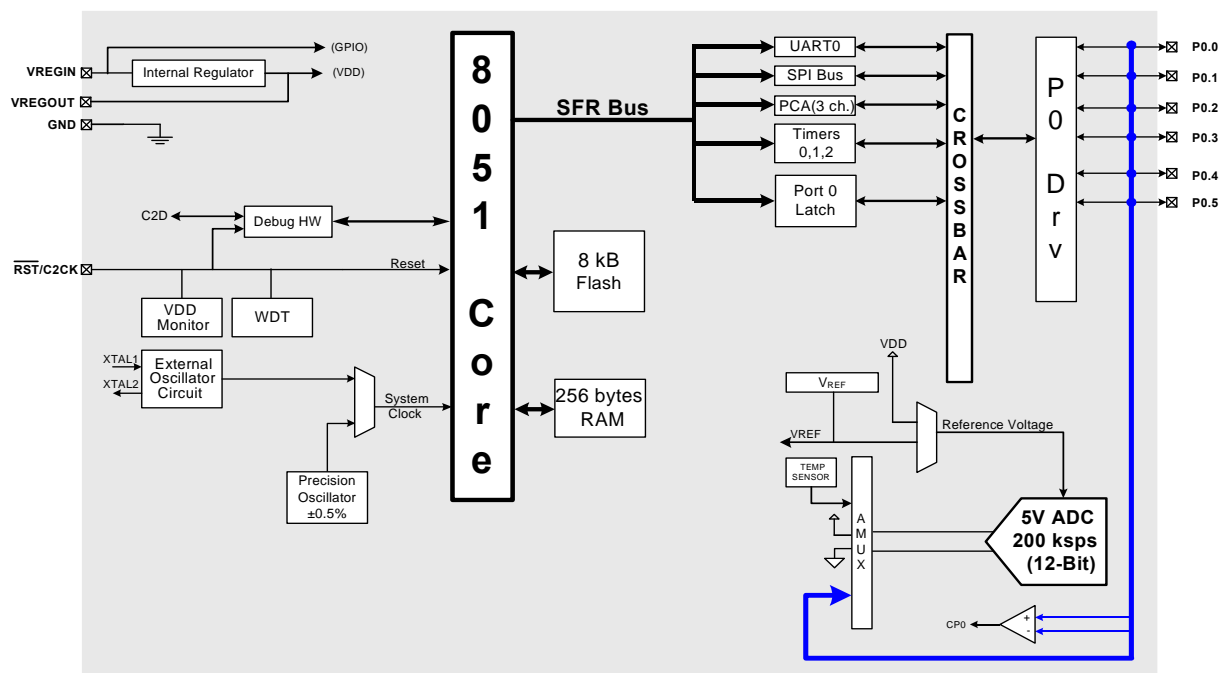
- Up to six digital I/O; all are 5 V push-pull
- Programmable 16-bit counter array with three capture/compare modules
- Three general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- High-precision internal programmable oscillator up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Ordering Part Number

- C8051F521A-IM, 10-Pin QFN (RoHS-compliant), 3x3 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 6 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksp/s
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Programmable Comparator

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

### Temperature Range: -40 to +125 °C

### Supply Voltage: 1.8 to 5.25 V

- Typical operating current: 7 mA at 25 MHz at 5.0 V
- Multiple power saving sleep and shutdown modes

### Development Kit: C8051F530ADK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4 kB Flash; in-system programmable; flexible security features
- 256 bytes data RAM

### LIN 2.1

- Master or slave operation using dedicated hardware (not software implementation with UART)

### Digital Peripherals

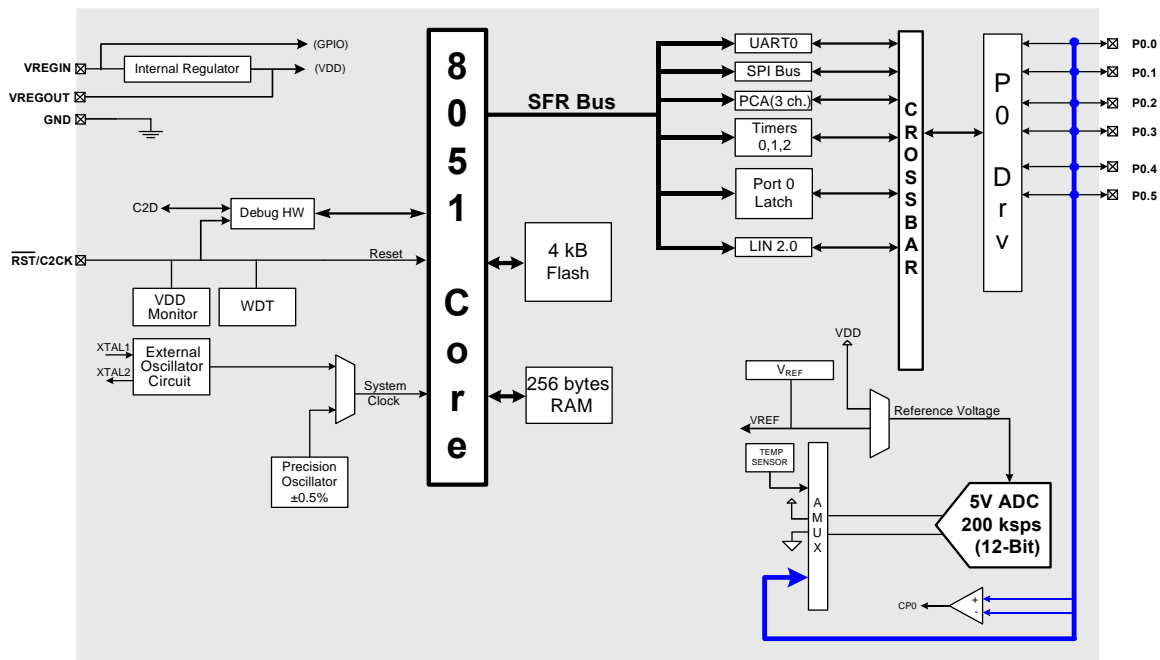
- Up to six digital I/O; all are 5 V push-pull
- Programmable 16-bit counter array with three capture/compare modules
- Three general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- High-precision internal programmable oscillator up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Ordering Part Number

- C8051F523A-IM, 10-Pin QFN (RoHS-compliant), 3x3 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 6 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Programmable Comparator

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

#### Temperature Range: $-40$ to $+125$ °C

#### Supply Voltage: 1.8 to 5.25 V

- Typical operating current: 7 mA at 25 MHz at 5.0 V
- Multiple power saving sleep and shutdown modes

#### Development Kit: C8051F530ADK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4 kB Flash; in-system programmable; flexible security features
- 256 bytes data RAM

### Digital Peripherals

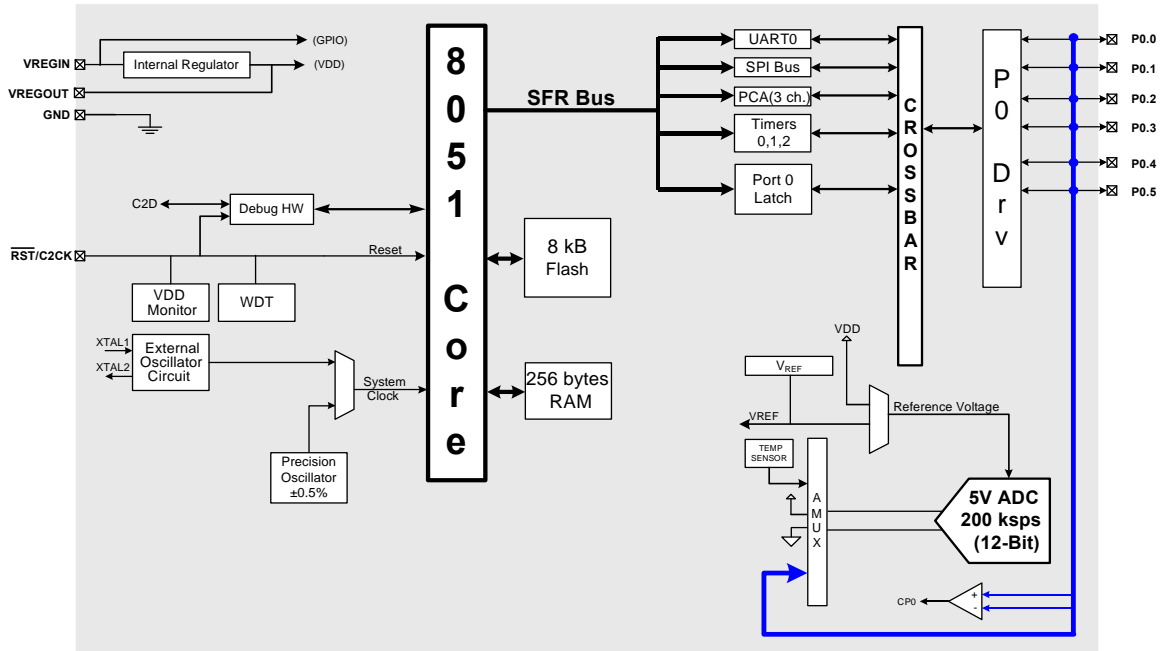
- Up to six digital I/O; all are 5 V push-pull
- Programmable 16-bit counter array with three capture/compare modules
- Three general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- High-precision internal programmable oscillator up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Ordering Part Number

- C8051F524A-IM, 10-Pin QFN (RoHS-compliant), 3x3 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 6 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Programmable Comparator

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

#### Temperature Range: -40 to +125 °C

#### Supply Voltage: 1.8 to 5.25 V

- Typical operating current: 7 mA at 25 MHz at 5.0 V
- Multiple power saving sleep and shutdown modes

#### Development Kit: C8051F530ADK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 2 kB Flash; in-system programmable; flexible security features
- 256 bytes data RAM

### LIN 2.1

- Master or slave operation using dedicated hardware (not software implementation with UART)

### Digital Peripherals

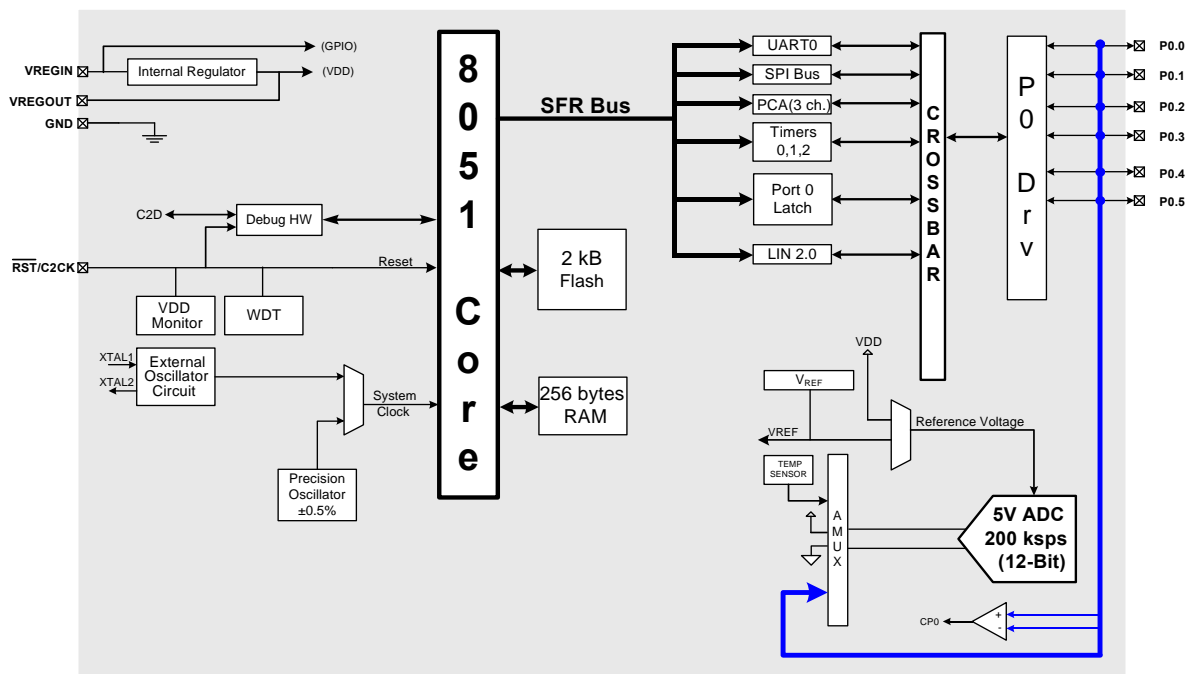
- Up to six digital I/O; all are 5 V push-pull
- Programmable 16-bit counter array with three capture/compare modules
- Three general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- High-precision internal programmable oscillator up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Ordering Part Number

- C8051F526A-IM, 10-Pin QFN (RoHS-compliant), 3x3 mm<sup>2</sup>





### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 6 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Programmable Comparator

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
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- Multiple power saving sleep and shutdown modes

#### Development Kit: C8051F530ADK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 2 kB Flash; in-system programmable; flexible security features
- 256 bytes data RAM

### Digital Peripherals

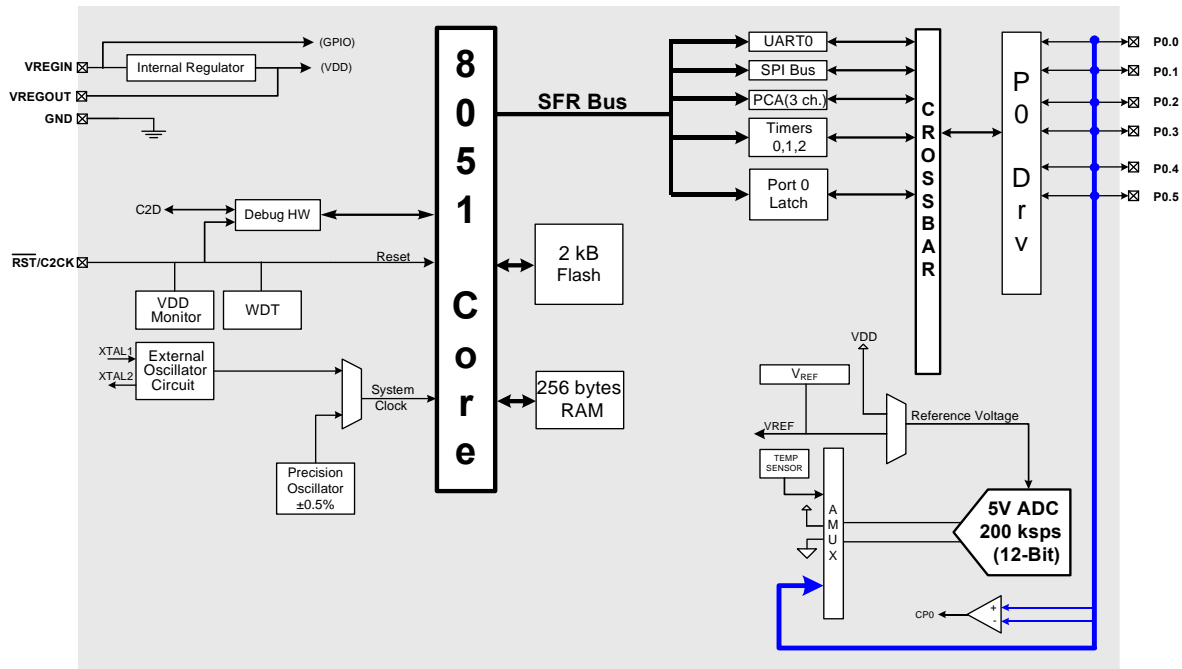
- Up to six digital I/O; all are 5 V push-pull
- Programmable 16-bit counter array with three capture/compare modules
- Three general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- High-precision internal programmable oscillator up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Ordering Part Number

- C8051F527A-IM, 10-Pin QFN (RoHS-compliant), 3x3 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 16 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksp/s
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Programmable Comparator

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

#### Temperature Range: -40 to +125 °C

#### Supply Voltage: 1.8 to 5.25 V

- Typical operating current: 7 mA at 25 MHz at 5.0 V
- Multiple power saving sleep and shutdown modes

#### Development Kit: C8051F530ADK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 8 kB Flash; in-system programmable; flexible security features
- 256 bytes data RAM

### LIN 2.1

- Master or slave operation using dedicated hardware (not software implementation with UART)

### Digital Peripherals

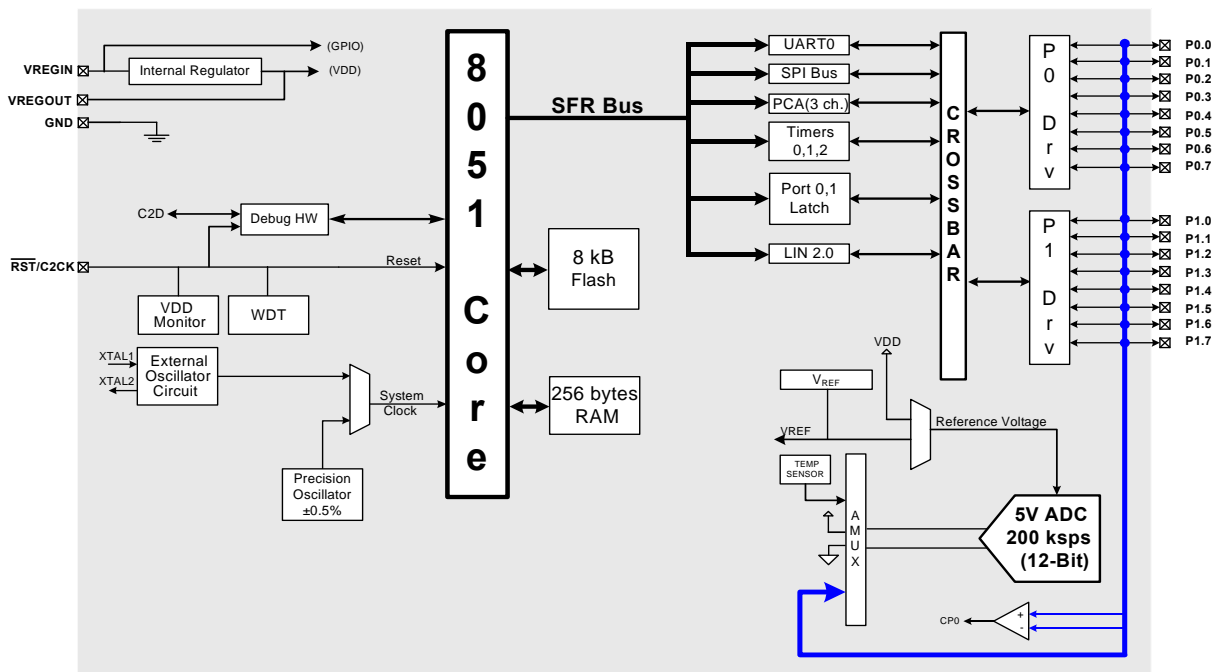
- Up to 16 digital I/O; all are 5 V push-pull
- Programmable 16-bit counter array with three capture/compare modules
- Three general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- High-precision internal programmable oscillator up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Ordering Part Numbers

- C8051F530A-IT, 20-Pin TSSOP (RoHS-compliant), 6x6 mm<sup>2</sup>
- C8051F530A-IM, 20-Pin QFN (RoHS-compliant), 4x4 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 16 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Programmable Comparator

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

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- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
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#### Development Kit: C8051F530ADK

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- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 8 kB Flash; in-system programmable; flexible security features
- 256 bytes data RAM

### Digital Peripherals

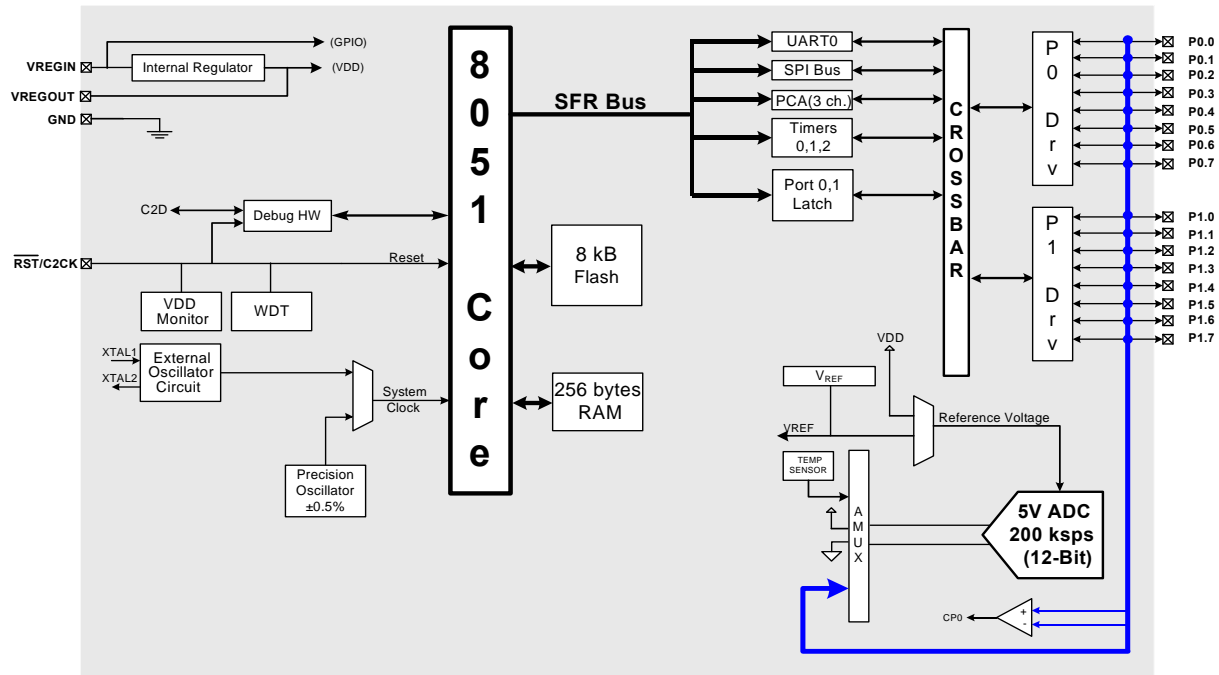
- Up to 16 digital I/O; all are 5 V push-pull
- Programmable 16-bit counter array with three capture/compare modules
- Three general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- High-precision internal programmable oscillator up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Ordering Part Numbers

- C8051F531A-IT, 20-Pin TSSOP (RoHS-compliant), 6x6 mm<sup>2</sup>
- C8051F531A-IM, 20-Pin QFN (RoHS-compliant), 4x4 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 16 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksp/s
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Programmable Comparator

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

#### Temperature Range: -40 to +125 °C

#### Supply Voltage: 1.8 to 5.25 V

- Typical operating current: 7 mA at 25 MHz at 5.0 V
- Multiple power saving sleep and shutdown modes

#### Development Kit: C8051F530ADK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4 kB Flash; in-system programmable; flexible security features
- 256 bytes data RAM

### LIN 2.1

- Master or slave operation using dedicated hardware (not software implementation with UART)

### Digital Peripherals

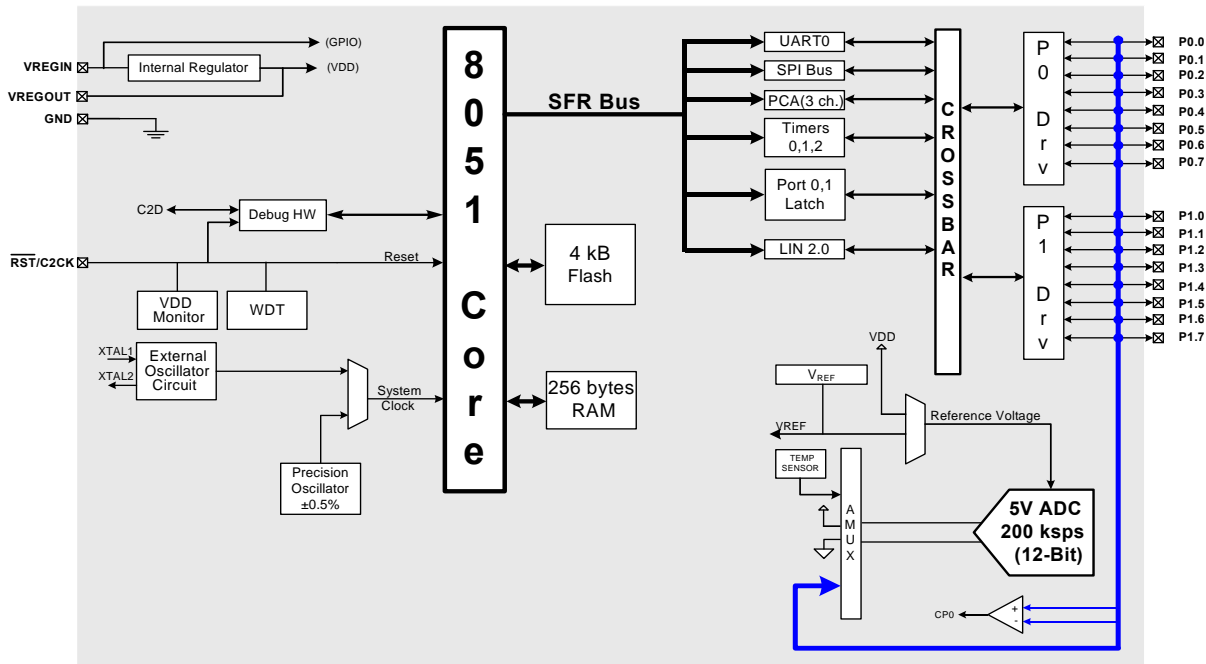
- Up to 16 digital I/O; all are 5 V push-pull
- Programmable 16-bit counter array with three capture/compare modules
- Three general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- High-precision internal programmable oscillator up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Ordering Part Numbers

- C8051F533A-IT, 20-Pin TSSOP (RoHS-compliant), 6x6 mm<sup>2</sup>
- C8051F533A-IM, 20-Pin QFN (RoHS-compliant), 4x4 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 16 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksp/s
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Programmable Comparator

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

#### Temperature Range: $-40$ to $+125$ °C

#### Supply Voltage: 1.8 to 5.25 V

- Typical operating current: 7 mA at 25 MHz at 5.0 V
- Multiple power saving sleep and shutdown modes

#### Development Kit: C8051F530ADK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4 kB Flash; in-system programmable; flexible security features
- 256 bytes data RAM

### Digital Peripherals

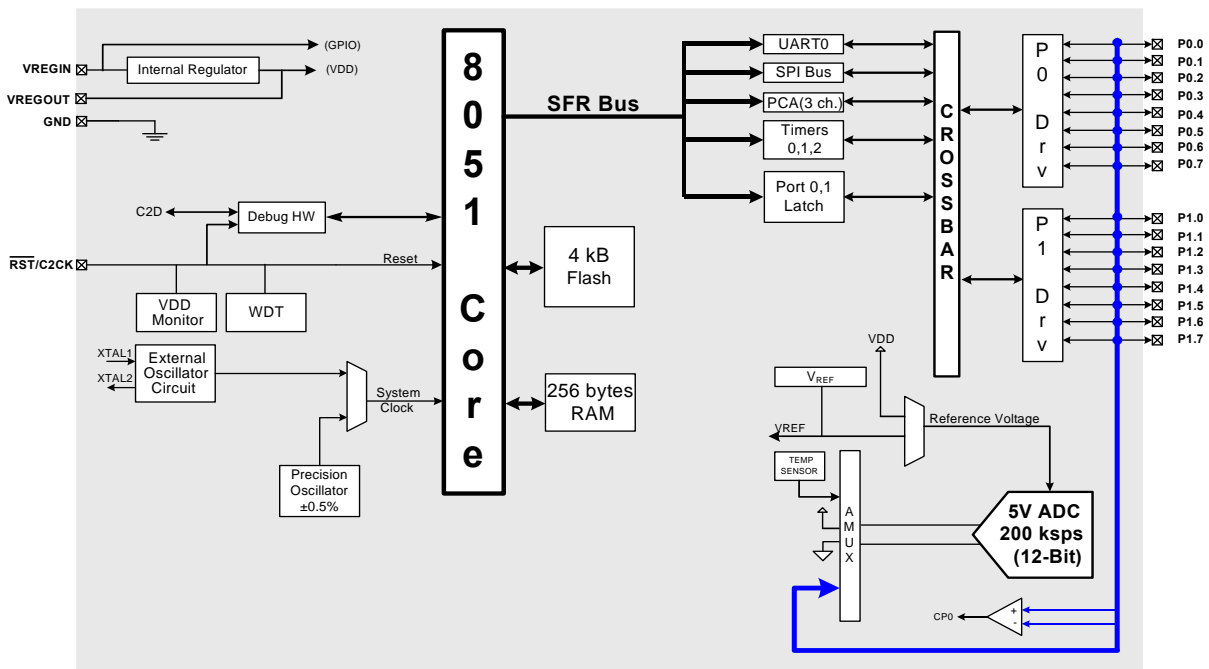
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- Programmable 16-bit counter array with three capture/compare modules
- Three general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- High-precision internal programmable oscillator up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Ordering Part Numbers

- C8051F534A-IT, 20-Pin TSSOP (RoHS-compliant), 6x6 mm<sup>2</sup>
- C8051F534A-IM, 20-Pin QFN (RoHS-compliant), 4x4 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 16 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksp/s
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Programmable Comparator

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
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- Superior performance to emulation systems using ICE-chips, target pods, and sockets

### Temperature Range: -40 to +125 °C

### Supply Voltage: 1.8 to 5.25 V

- Typical operating current: 7 mA at 25 MHz at 5.0 V
- Multiple power saving sleep and shutdown modes

### Development Kit: C8051F530ADK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 2 kB Flash; in-system programmable; flexible security features
- 256 bytes data RAM

### LIN 2.1

- Master or slave operation using dedicated hardware (not software implementation with UART)

### Digital Peripherals

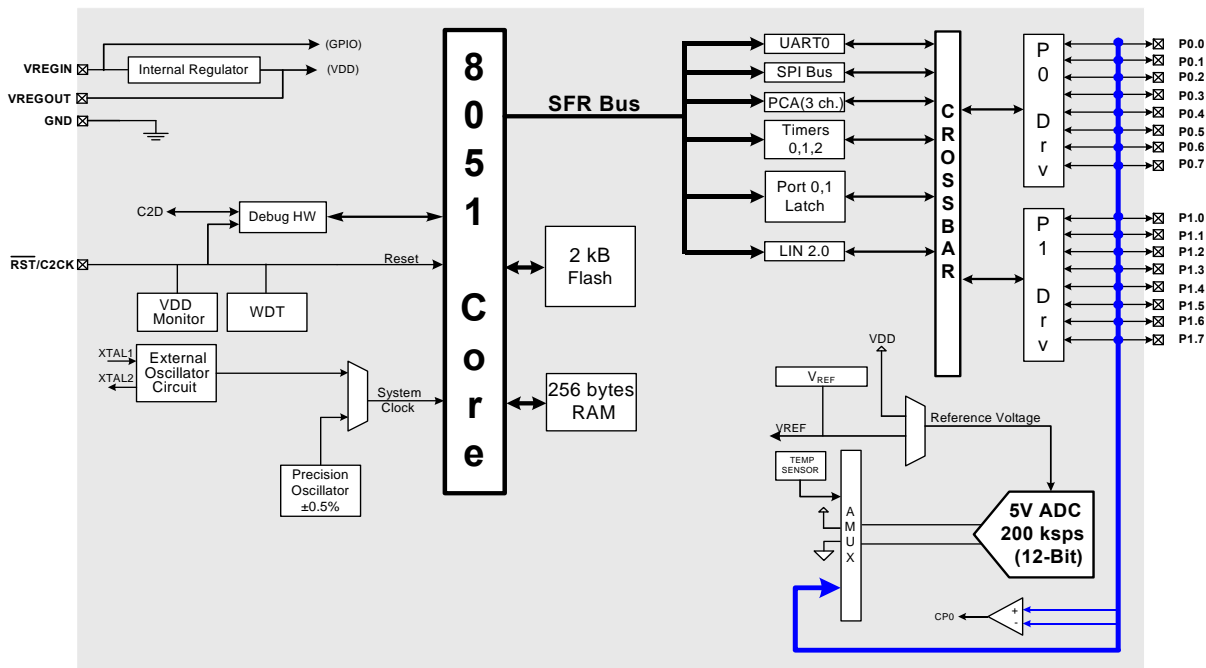
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- Real-time clock mode using timer 3 or PCA

### Clock Sources

- High-precision internal programmable oscillator up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Ordering Part Numbers

- C8051F536A-IT, 20-Pin TSSOP (RoHS-compliant), 6x6 mm<sup>2</sup>
- C8051F536A-IM, 20-Pin QFN (RoHS-compliant), 4x4 mm<sup>2</sup>



### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 16 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksp/s
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

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#### Programmable Comparator

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

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#### Temperature Range: $-40$ to $+125$ °C

#### Supply Voltage: 1.8 to 5.25 V

- Typical operating current: 7 mA at 25 MHz at 5.0 V
- Multiple power saving sleep and shutdown modes

#### Development Kit: C8051F530ADK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
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- Expanded interrupt handler

### Memory

- 2 kB Flash; in-system programmable; flexible security features
- 256 bytes data RAM

### Digital Peripherals

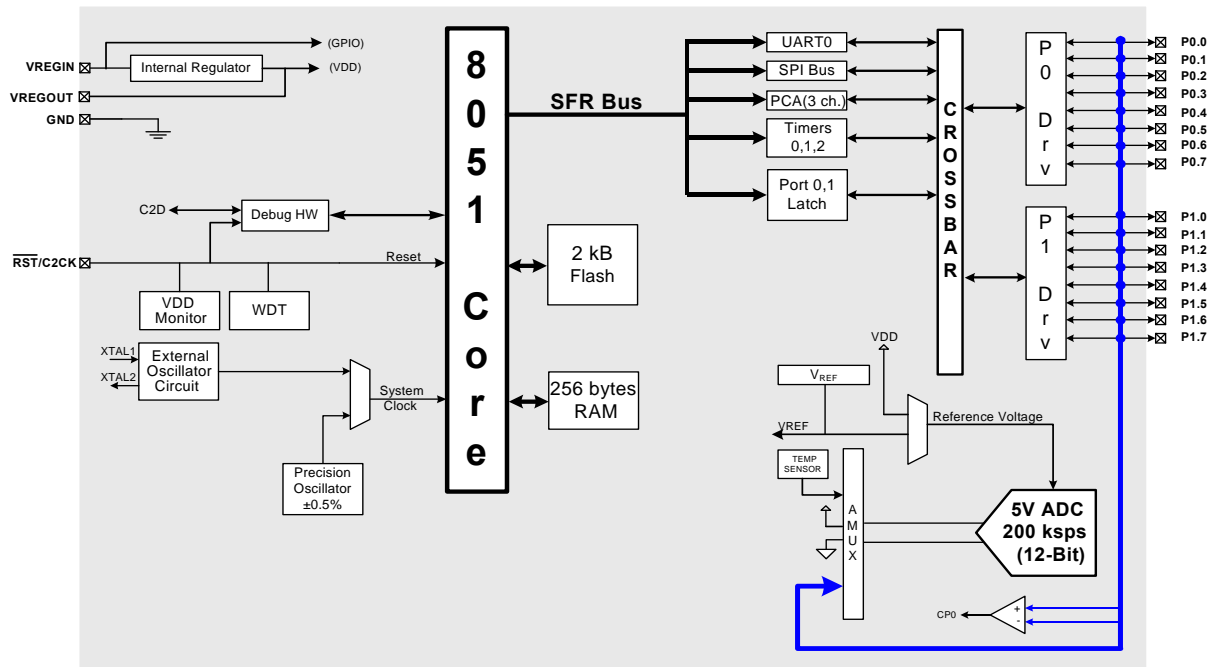
- Up to 16 digital I/O; all are 5 V push-pull
- Programmable 16-bit counter array with three capture/compare modules
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- High-precision internal programmable oscillator up to 25 MHz
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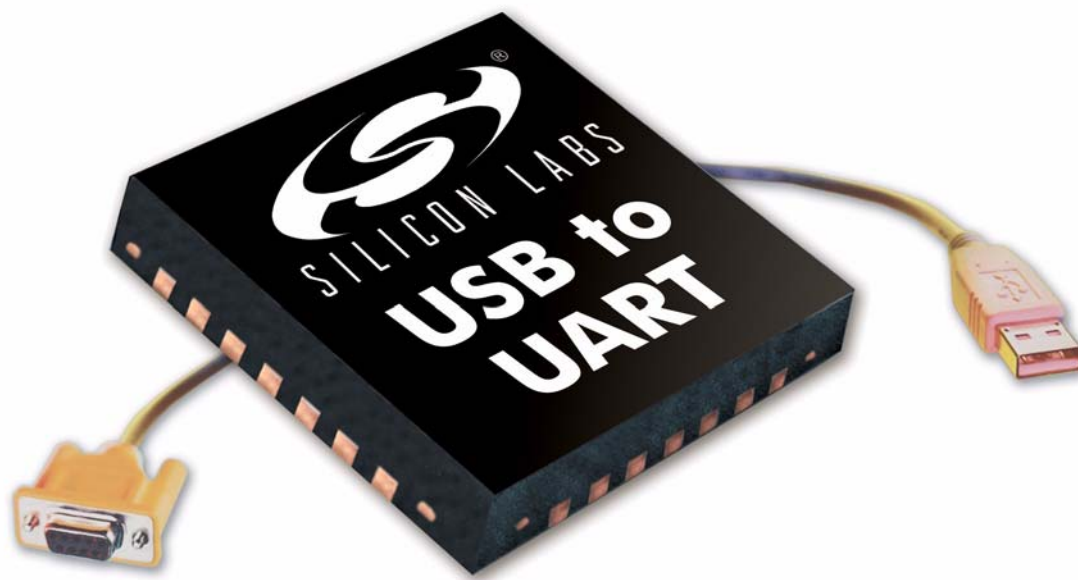
### Ordering Part Numbers

- C8051F537A-IT, 20-Pin TSSOP (RoHS-compliant), 6x6 mm<sup>2</sup>
- C8051F537A-IM, 20-Pin QFN (RoHS-compliant), 4x4 mm<sup>2</sup>









# Interface

### Description

- The CP2102 is a highly-integrated USB-to-UART bridge controller providing a simple solution for updating RS-232 designs to USB using a minimum of components and PCB space. Offering Baud rates aliasing and supporting additional data formats, the CP2102 is a pin-to-pin upgrade from CP2101. The CP2102 also includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, EEPROM and asynchronous serial data bus (UART) with full modem control signals in a compact 5 x 5 mm QFN-28. No other external USB components are required.

### Example Applications

- Upgrade of RS-232 legacy devices to USB
- Cellular phone USB interface cable
- PDA USB interface cable
- USB to RS-232 serial adapter

### Virtual Com Port Drivers

- Works with existing COM port applications
- Royalty-free distribution license
- Windows 98SE/2000/XP
- MAC OS-9
- MAC OS-X
- Linux 2.40

**Temperature Range: -40 to +85 °C**

### Features

#### USB Function Controller and Transceiver

- USB specification 2.0 compliant; full-speed (12 Mbps)
- Integrated 1024-byte EEPROM for custom Baud rates, vendor ID, etc.
- EEPROM security lock function
- User programmable custom Baud rates
- Integrated transceiver; no external resistors required
- Integrated clock; no external crystal required
- USB suspend states supported via SUSPEND pins

#### Asynchronous Serial Data Bus (UART)

- All handshaking and modem interface signals
- Data formats supported: 8, 7, 6, 5-bit; 1, 1.5, 2 Stop bits
- Parity: Odd, Even, Mark, Space, No Parity
- Baud rates: 300 bps to 1 Mbps
- 576-byte receive buffer; 640-byte transmit buffer
- Hardware and X-On/X-Off handshaking
- Event character support

#### Power-On Reset Circuit

#### Supply Voltage

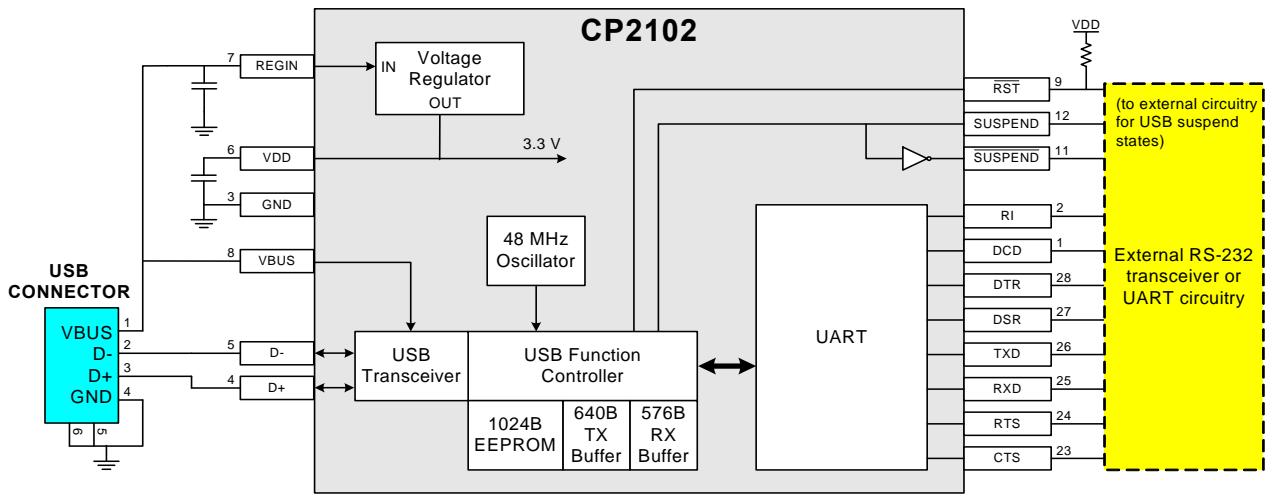
- Self-powered: 3.0–3.6 V
- USB bus powered: 4.0–5.25 V

#### Package

- 28-pin QFN (lead-free package)

#### Ordering Part Number

- CP2102-GM



**Note:** The CP2102 is both pin-compatible and software-compatible with the CP2101 and features enhanced functionality. Silicon Laboratories recommends the use of the CP2102 for new designs.

### Description

- The CP2103 is a highly-integrated USB-to-UART bridge controller providing a simple solution for updating RS-232 or RS-485 designs to USB using a minimum of components and PCB space. The CP2103 is a functional upgrade to CP2101/2 with new features such as configurable I/O levels (3.3 to 1.8 V) and four general purpose I/O signals for system status and control.

It includes the standard USB 2.0 full-speed function controller, USB transceiver, oscillator, EEPROM and asynchronous serial data bus (UART) with full modem control signals in a compact 5 x 5 mm MLP-28 package. No other external USB components are required.

### Example Applications

- Upgrade of RS-232 legacy devices to USB
- Upgrade of RS-485 legacy devices to USB
- USB to RS-232 serial adapter

### Virtual Com Port Drivers

- Works with existing COM port applications
- Royalty-free distribution license
- Windows 98SE/2000/XP
- MAC OS-9
- MAC OS-X
- Linux 2.40

### USBXpress™ Direct Driver Support

Temperature Range: **-40 to +85 °C**

### Features

#### USB Function Controller and Transceiver

- USB specification 2.0 compliant; full-speed (12 Mbps)
- Integrated 1024-byte EEPROM for custom Baud rates, vendor ID, etc.
- Integrated transceiver; no external resistors required
- Integrated clock; no external crystal required
- USB suspend states supported via SUSPEND pins

#### Asynchronous Serial Data Bus (UART)

- All handshaking and modem interface signals
- Data formats supported: 8, 7, 6, 5-bit; 1, 1.5, 2 Stop bits
- Parity: Odd, Even, Mark, Space, No Parity
- Baud rates: 300 bps to 1 Mbps
- 576-byte receive buffer; 640-byte transmit buffer
- Event character support; line break event support
- Four GPIO signals for status and control
- Configurable I/O (3.3 to 1.8 V  $V_{OH}$ ) using  $V_{IO}$  pin
- RS-485 mode with bus transceiver control

#### Power-On Reset Circuit

#### Supply Voltage

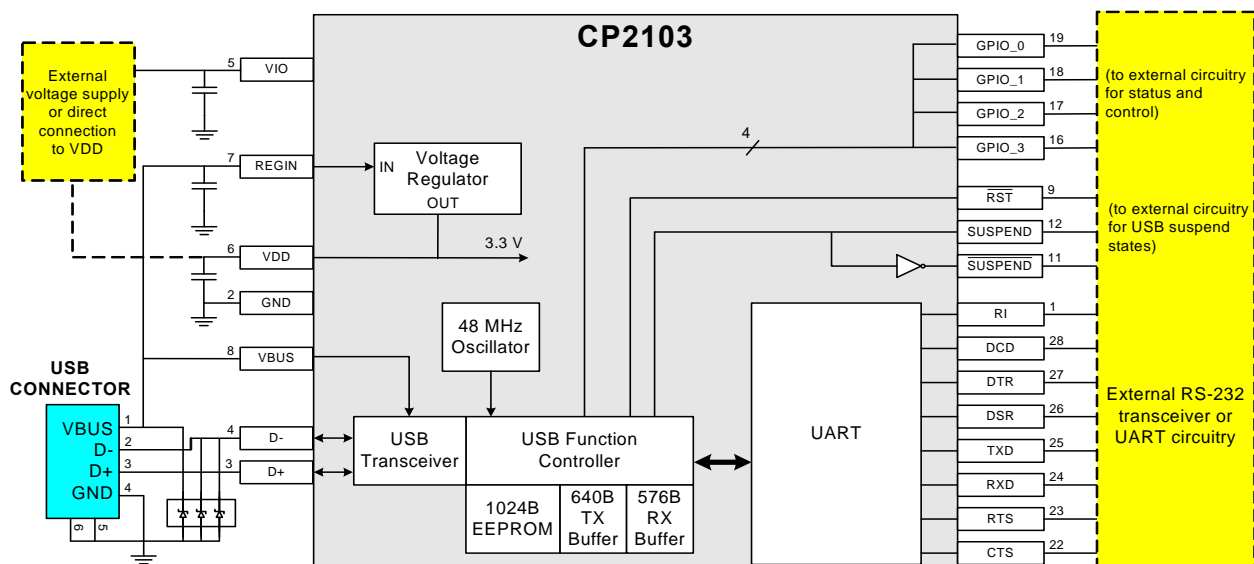
- Self-powered: 3.0–3.6 V
- USB bus powered: 4.0–5.25 V

#### Package

- 28-pin QFN (lead-free package)

#### Ordering Part Numbers

- CP2103-GM



### Description

The CP2200/1 is a single-chip Ethernet controller containing an integrated IEEE 802.3 Ethernet Media Access Controller (MAC), a 10 BASE-T Physical Layer (PHY), and 8 kB of Non-Volatile Flash Memory available in a 28-pin QFN (5x5 mm) or 48-pin TQFP package.

The CP2200/1 can add Ethernet connectivity to any micro-controller or host processor with 11 or more Port I/O pins. The 8-bit parallel interface bus supports both Intel and Motorola bus formats in multiplexed and non-multiplexed mode. The 28-pin QFN device supports multiplexed addressing only. Mode select pins are used to configure the bus interface mode.

The on-chip Flash memory may be used to store user constants, web server content, or can be used as general purpose non-volatile memory. The Flash is factory pre-programmed with a unique 48-bit MAC address stored in the last six memory locations. Having a unique MAC address stored in the CP2200/1 often removes the necessary serialization step from the product manufacturing process of most embedded systems.

### Firmware Features

#### Software Support

- Royalty-free TCP/IP stack with device drivers
- TCP/IP Configuration Wizard
- Hardware diagnostic software and example code

#### Example Applications

- Remote sensing and monitoring
- Inventory management
- VoIP phone adapters
- Point-of-sale devices
- Network clocks
- Embedded web server
- Remote Ethernet-to-UART bridge

**Temperature Range: -40 to +85 °C**

### Hardware Features

#### Ethernet Controller

- Integrated IEEE 802.3 MAC and 10 BASE-T PHY
- Fully compatible with 100/1000 BASE-T networks
- Full/Half duplex with auto-negotiation
- Automatic polarity detection and correction
- Automatic retransmission on collision
- Automatic padding and CRC generation
- Supports broadcast and multi-cast MAC addressing

#### Parallel Host Interface (30 Mbps Transfer Rate)

- 8-bit multiplexed or non-multiplexed mode
- Only 11 I/O pins required in multiplexed mode
- Intel or Motorola Bus Format
- Interrupt on received packets and Wake-on-LAN

#### 8 kB Flash Memory

- 8192 bytes of non-volatile user data storage
- Factory pre-programmed unique 48-bit MAC address
- No external EEPROM required

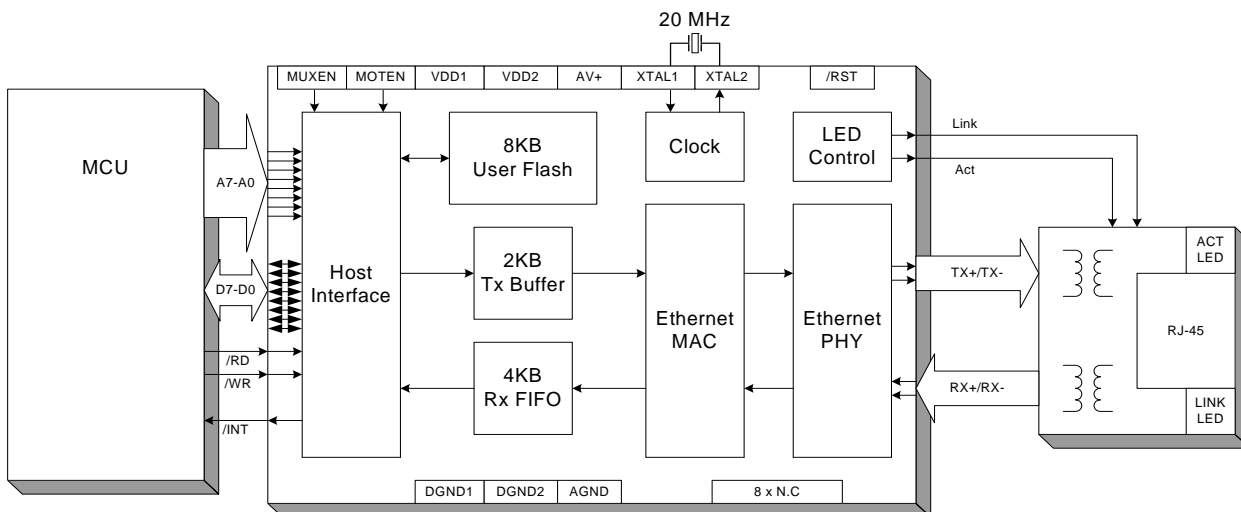
#### Other Features

- LED output drivers (Link/Activity)
- Dedicated 2 kB RAM transmit buffer and 4 kB RAM receive FIFO buffer
- Power-on Reset
- 5 V tolerant I/O

**Supply Voltage: 3.1 to 3.6 V**

#### Package Options

- Lead free 48-pin TQFP (9 x 9 mm footprint)
- Lead free 28-pin QFN (5 x 5 mm footprint)





# Low-Voltage/Low-Power MCUs

### Supply Voltage: 0.9 to 3.6 V

- One-cell mode supports 0.9–1.8 V operation
- Two-cell mode supports 1.8–3.6 V operation
- Built-in dc-dc converter with 1.8–3.3 V output (65 mW max) for use in one-cell mode; can supply external devices
- Typical sleep mode current < 0.1  $\mu$ A; retains state and RAM-contents over full supply range; fast wakeup
- 2 built-in brown-out detectors cover sleep and active modes

### 10-Bit Analog to Digital Converter

- Up to 300 ksp/s
- Up to 23 external inputs
- External pin or internal VREF (no external capacitor required)
- Built-in temperature sensor
- External conversion start input option
- Autonomous Burst Mode with 16-bit automatic averaging accumulator

### Two Comparators

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)
- Up to 23 Capacitive Touch Sense inputs

### Memory

- 4352 bytes internal data RAM (256 + 4K)
- 32 kB bytes Flash; In-system programmable in 1024-byte sectors; Full read/write/erase functionality over the entire supply range
- External memory interface (multiplexed address/data)

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)

### High-Speed 8051 $\mu$ C Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS peak throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

- 24 port I/O; All 5 V tolerant with programmable drive strength
- Hardware enhanced UART, SPI and SMBus™ serial ports available concurrently
- Low power 32-bit smaRTClock (0.5  $\mu$ A) operates down to 0.9V
- Four general purpose 16-bit counter/timers
- 16-bit programmable counter array (PCA) with six capture/compare modules and watchdog timer:
  - 8, 9, 10, 11, or 16-bit PWM
  - Rising/falling edge capture
  - Frequency output
  - Software timer

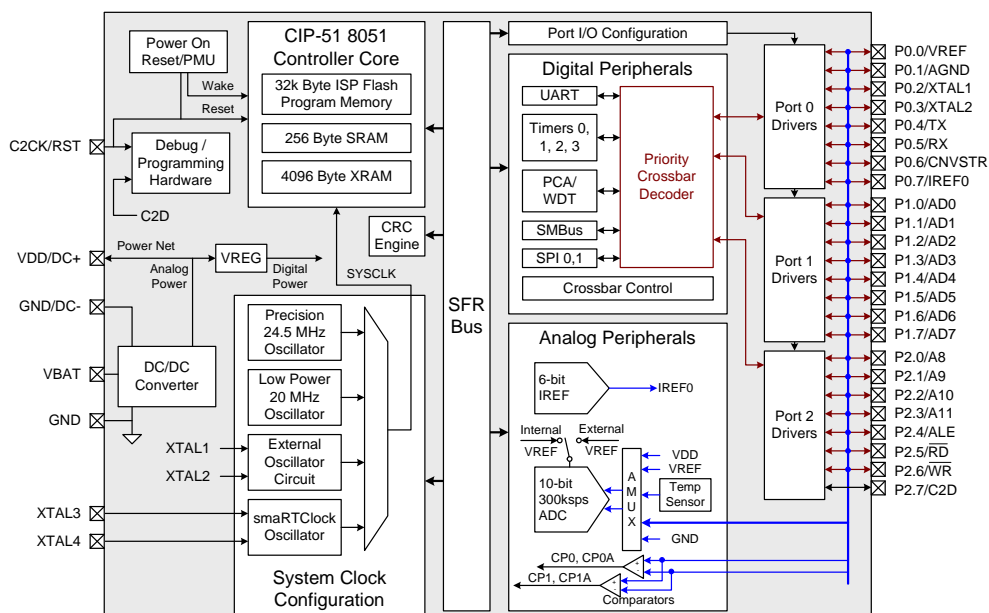
### Clock Sources

- Precision internal oscillators: 24.5 MHz with  $\pm$ 2% accuracy supports UART operation; spread-spectrum mode for reduced EMI
- Low power internal oscillator: 20 MHz
- External oscillator: Crystal, RC, C, CMOS clock
- smaRTClock oscillator: 32.768 kHz crystal or self-oscillate
- Can switch between clock sources on-the-fly; useful in power saving modes

### Ultra-Small Package Options

- 32-pin QFN (5x5 mm)
- 32-pin LQFP (7x7 mm)

### Temperature Range: -40 to +85 °C



### Supply Voltage: 0.9 to 3.6 V

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- Two-cell mode supports 1.8–3.6 V operation
- Built-in dc-dc converter with 1.8–3.3 V output (65 mW max) for use in one-cell mode; can supply external devices
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### 10-Bit Analog to Digital Converter

- Up to 300 kps
- Up to 15 external inputs
- External pin or internal VREF (no external capacitor required)
- Built-in temperature sensor
- External conversion start input option
- Autonomous Burst Mode with 16-bit automatic averaging accumulator

### Two Comparators

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)
- Up to 15 Capacitive Touch Sense inputs

### Memory

- 4352 bytes internal data RAM (256 + 4K)
- 32 kB bytes Flash; In-system programmable in 1024-byte sectors; Full read/write/erase functionality over the entire supply range

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)

### High-Speed 8051 $\mu$ C Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS peak throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

- 16 port I/O; All 5 V tolerant with programmable drive strength
- Hardware enhanced UART, SPI and SMBus™ serial ports available concurrently
- Low power 32-bit smaRTClock (0.5  $\mu$ A) operates down to 0.9V
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  - Frequency output
  - Software timer

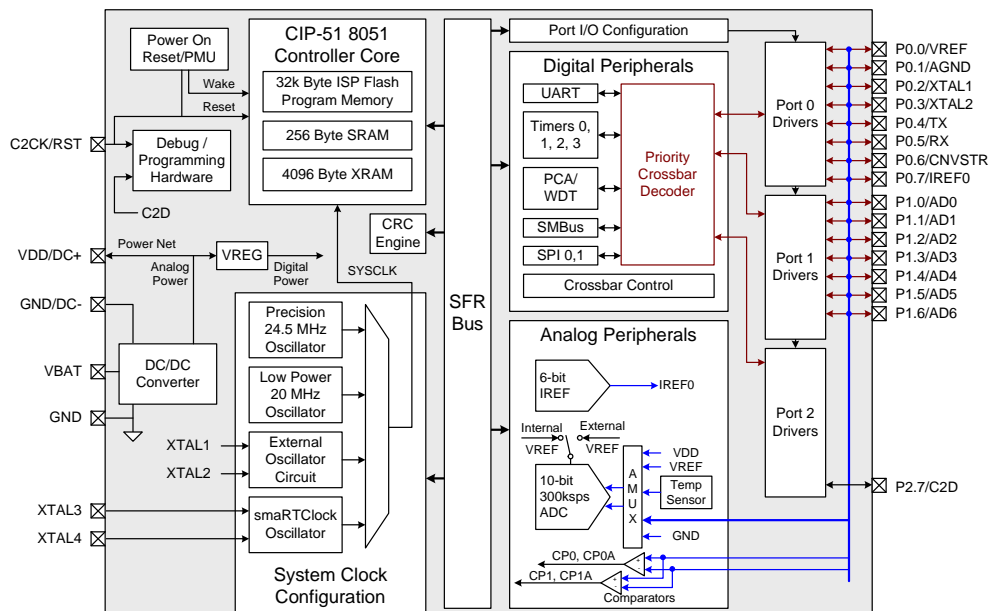
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- Low power internal oscillator: 20 MHz
- External oscillator: Crystal, RC, C, CMOS clock
- smaRTClock oscillator: 32.768 kHz crystal or self-oscillate
- Can switch between clock sources on-the-fly; useful in power saving modes

### Ultra-Small Package

- 24-pin QFN (4x4 mm)

### Temperature Range: –40 to +85 °C



### Supply Voltage: 0.9 to 3.6 V

- One-cell mode supports 0.9–1.8 V operation
- Two-cell mode supports 1.8–3.6 V operation
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- Up to 23 Capacitive Touch Sense inputs

### Memory

- 4352 bytes internal data RAM (256 + 4K)
- 64 kB bytes Flash; In-system programmable in 1024-byte sectors; Full read/write/erase functionality over the entire supply range
- External memory interface (multiplexed address/data)

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)

### High-Speed 8051 $\mu$ C Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS peak throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

- 24 port I/O; All 5 V tolerant with programmable drive strength
- Hardware enhanced UART, SPI and SMBus™ serial ports available concurrently
- Low power 32-bit smaRTClock (0.5 uA) operates down to 0.9V
- Four general purpose 16-bit counter/timers
- 16-bit programmable counter array (PCA) with six capture/compare modules and watchdog timer:
  - 8, 9, 10, 11, or 16-bit PWM
  - Rising/falling edge capture
  - Frequency output
  - Software timer

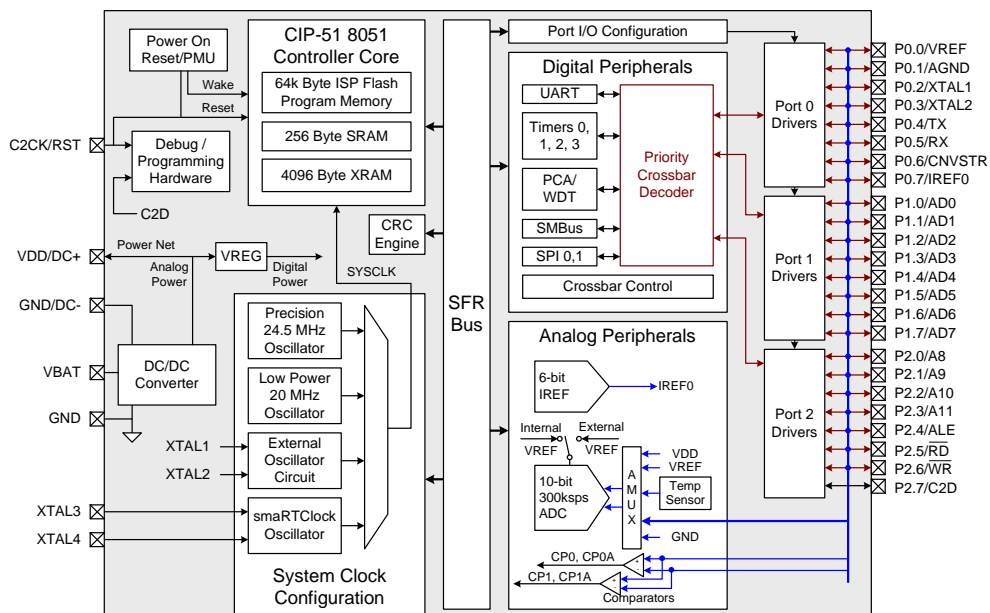
### Clock Sources

- Precision internal oscillators: 24.5 MHz with  $\pm$ 2% accuracy supports UART operation; spread-spectrum mode for reduced EMI
- Low power internal oscillator: 20 MHz
- External oscillator: Crystal, RC, C, CMOS clock
- smaRTClock oscillator: 32.768 kHz crystal or self-oscillate
- Can switch between clock sources on-the-fly; useful in power saving modes

### Ultra-Small Package Options

- 32-pin QFN (5x5 mm)
- 32-pin LQFP (7x7 mm)

### Temperature Range: –40 to +85 °C





### Supply Voltage: 0.9 to 3.6 V

- One-cell mode supports 0.9–1.8 V operation
- Two-cell mode supports 1.8–3.6 V operation
- Built-in dc-dc converter with 1.8–3.3 V output (65 mW max) for use in one-cell mode; can supply external devices
- Typical sleep mode current < 0.1  $\mu$ A; retains state and RAM-contents over full supply range; fast wakeup
- 2 built-in brown-out detectors cover sleep and active modes

### 10-Bit Analog to Digital Converter

- Up to 300 kpsps
- Up to 15 external inputs
- External pin or internal VREF (no external capacitor required)
- Built-in temperature sensor
- External conversion start input option
- Autonomous Burst Mode with 16-bit automatic averaging accumulator

### Two Comparators

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)
- Up to 15 Capacitive Touch Sense inputs

### Memory

- 4352 bytes internal data RAM (256 + 4K)
- 64 kB bytes Flash; In-system programmable in 1024-byte sectors; Full read/write/erase functionality over the entire supply range

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)

### High-Speed 8051 $\mu$ C Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS peak throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

- 16 port I/O; All 5 V tolerant with programmable drive strength
- Hardware enhanced UART, SPI and SMBus™ serial ports available concurrently
- Low power 32-bit smaRTClock (0.5  $\mu$ A) operates down to 0.9 V
- Four general purpose 16-bit counter/timers
- 16-bit programmable counter array (PCA) with six capture/compare modules and watchdog timer:
  - 8, 9, 10, 11, or 16-bit PWM
  - Rising/falling edge capture
  - Frequency output
  - Software timer

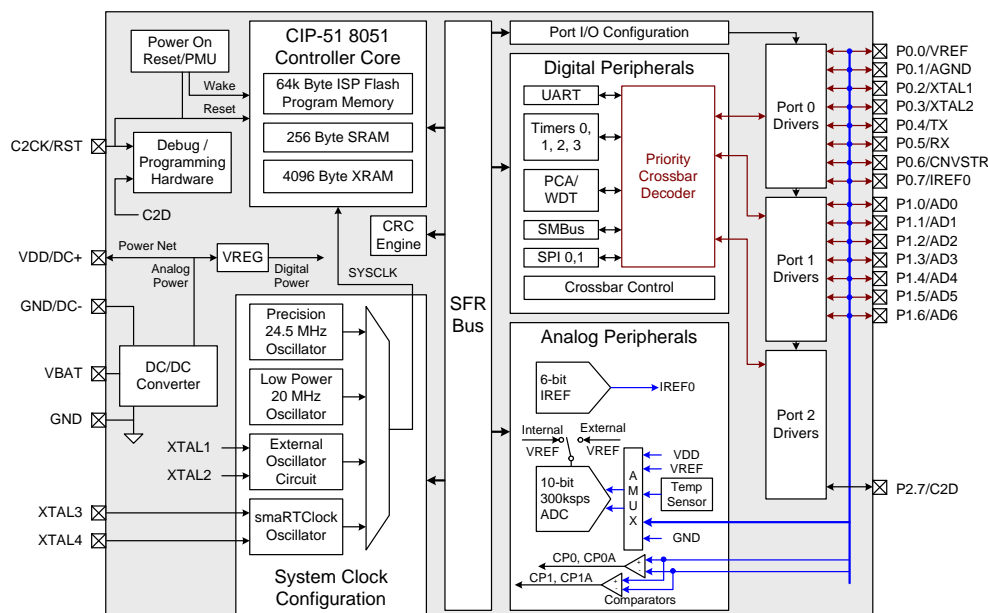
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- Precision internal oscillators: 24.5 MHz with  $\pm$ 2% accuracy supports UART operation; spread-spectrum mode for reduced EMI
- Low power internal oscillator: 20 MHz
- External oscillator: Crystal, RC, C, CMOS clock
- smaRTClock oscillator: 32.768 kHz crystal or self-oscillate
- Can switch between clock sources on-the-fly; useful in power saving modes

### Ultra-Small Package

- 24-pin QFN (4x4 mm)

### Temperature Range: –40 to +85 °C







# OTP EPROM-Based MCUs

### Analog Peripherals

#### 10-Bit Analog to Digital Converter

- Up to 500 ksps
- Up to 8 external inputs
- $V_{REF}$  from external pin,  $V_{DD}$ , or internal regulator
- Built-in temperature sensor
- External conversion start input option

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current ( $< 0.5 \mu A$ )

### Memory

- 256 bytes internal data RAM
- 8 kB one time programmable code memory

### On-Chip Debug

- C8051F300 can be used as in-system code development platform; complete development kit available
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug

**Temperature Range:  $-40$  to  $+85$  °C**

### High-Speed 8051 $\mu C$ Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS peak throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

- 8 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART and SMBus™ serial ports
- Three general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with three capture/compare modules
  - 8 or 16-bit PWM
  - Rising / falling edge capture
  - Frequency output
  - Software timer

### Clock Sources

- Internal oscillator: 24.5 MHz with  $\pm 2\%$  accuracy supports UART operation
- External oscillator: CMOS clock or external capacitor
- Can switch between clock sources on-the-fly; useful in power saving modes

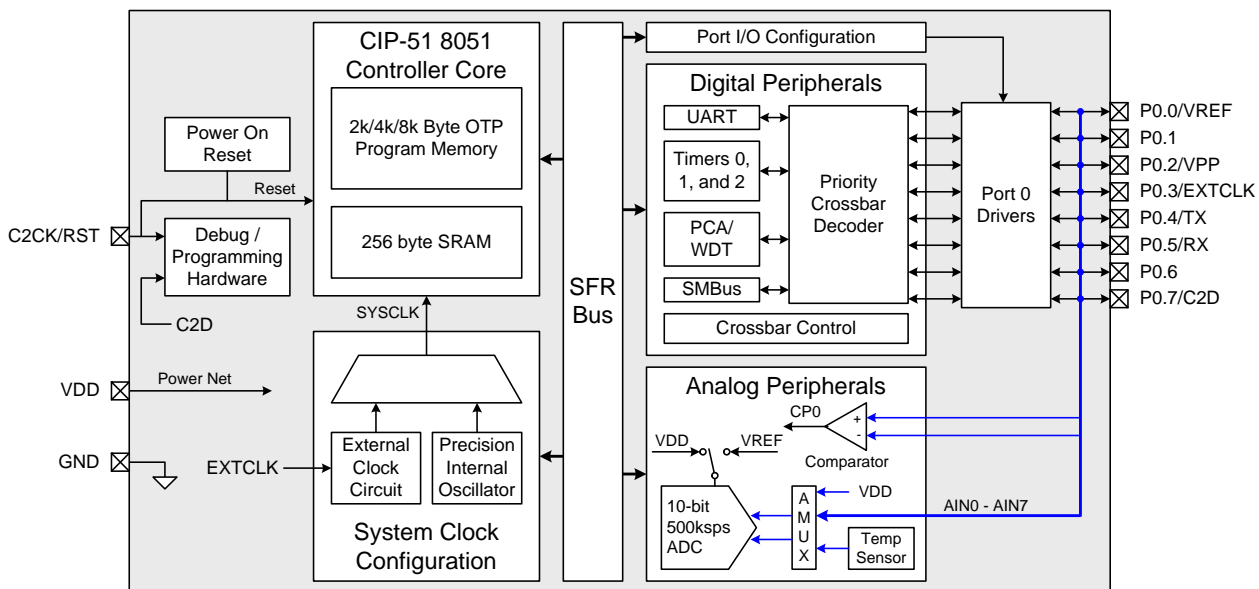
### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- Typical operating current: TBD mA @ TBD MHz:  
TBD  $\mu A$  @ TBD kHz
- Typical stop mode current (regulator off): TBD  $\mu A$

Built-in brown-out detector

### Package

- 11-pin QFN or 14-pin SOIC
- QFN size = 3x3 mm



### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

#### Memory

- 256 bytes internal data RAM
- 8 kB one time programmable code memory

#### On-Chip Debug

- C8051F300 can be used as in-system code development platform; complete development kit available
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- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
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### Digital Peripherals

- 8 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART and SMBus™ serial ports
- Three general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with three capture/compare modules
  - 8 or 16-bit PWM
  - Rising / falling edge capture
  - Frequency output
  - Software timer

### Clock Sources

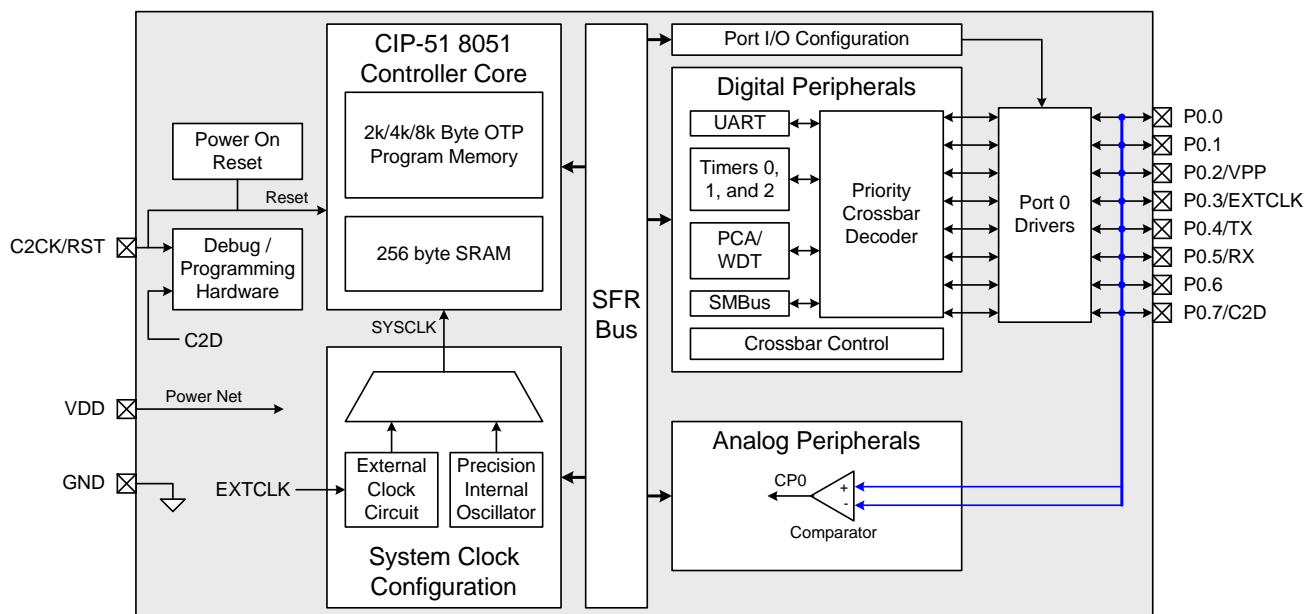
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- External oscillator: CMOS clock or external capacitor
- Can switch between clock sources on-the-fly; useful in power saving modes

### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- Typical operating current: TBD mA @ TBD MHz:  
TBD  $\mu$ A @ TBD kHz
- Typical stop mode current (regulator off): TBD  $\mu$ A
- Built-in brown-out detector

### Package

- 11-pin QFN or 14-pin SOIC
- QFN size = 3x3 mm



### Analog Peripherals

#### 10-Bit Analog to Digital Converter

- Up to 500 ksps
- Up to 8 external inputs
- $V_{REF}$  from external pin,  $V_{DD}$ , or internal regulator
- Built-in temperature sensor
- External conversion start input option

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current ( $< 0.5 \mu A$ )

### Memory

- 256 bytes internal data RAM
- 4 kB one time programmable code memory

### On-Chip Debug

- C8051F300 can be used as in-system code development platform; complete development kit available
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug

**Temperature Range:  $-40$  to  $+85$  °C**

### High-Speed 8051 $\mu C$ Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS peak throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

- 8 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART and SMBus™ serial ports
- Three general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with three capture/compare modules
  - 8 or 16-bit PWM
  - Rising / falling edge capture
  - Frequency output
  - Software timer

### Clock Sources

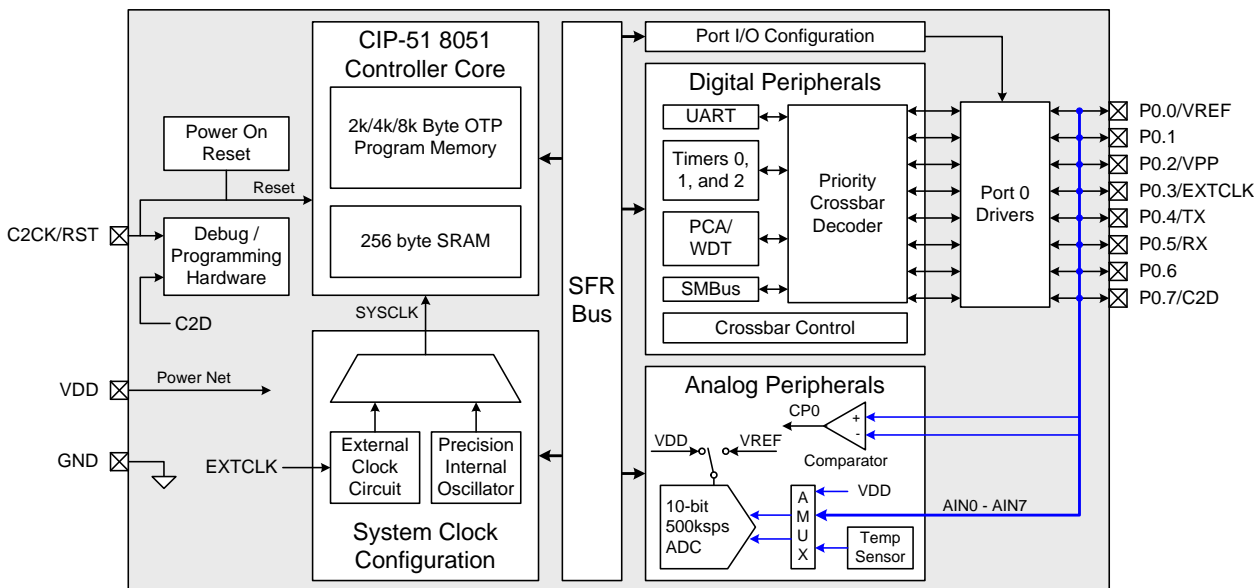
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- External oscillator: CMOS clock or external capacitor
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### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- Typical operating current: TBD mA @ TBD MHz:  
TBD  $\mu A$  @ TBD kHz
- Typical stop mode current (regulator off): TBD  $\mu A$
- Built-in brown-out detector

### Package

- 11-pin QFN or 14-pin SOIC
- QFN size = 3x3 mm



### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

#### Memory

- 256 bytes internal data RAM
- 4 kB one time programmable code memory

#### On-Chip Debug

- C8051F300 can be used as in-system code development platform; complete development kit available
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS peak throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

- 8 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART and SMBus™ serial ports
- Three general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with three capture/compare modules
  - 8 or 16-bit PWM
  - Rising / falling edge capture
  - Frequency output
  - Software timer

### Clock Sources

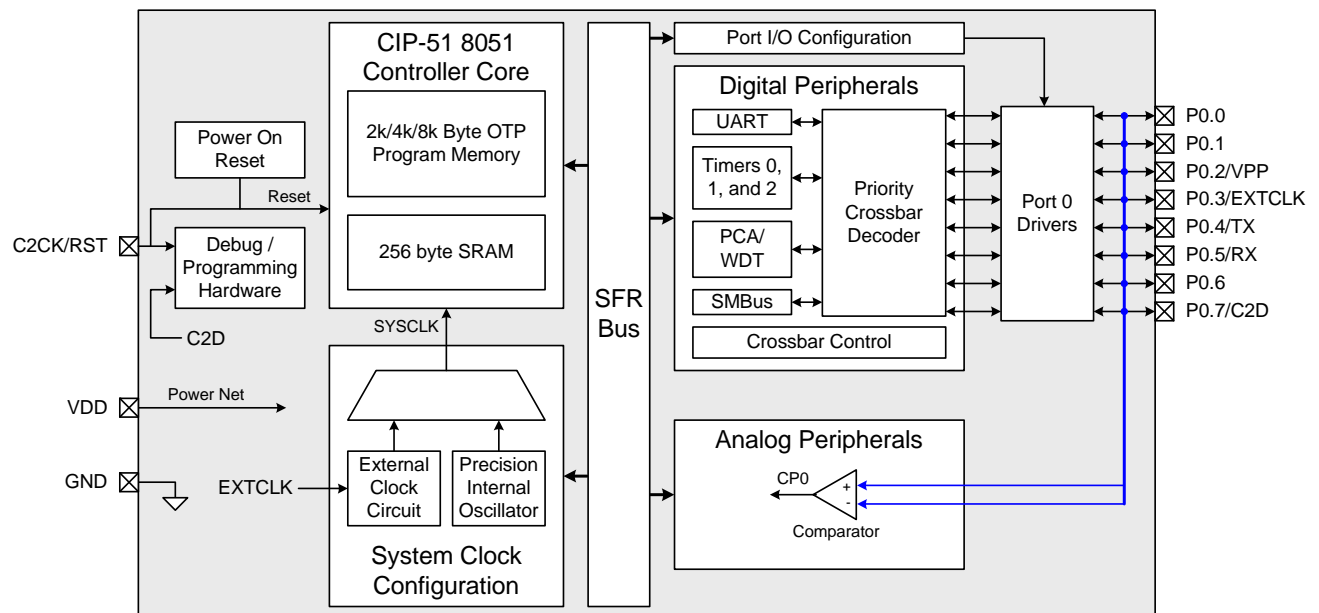
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- Typical stop mode current (regulator off): TBD  $\mu$ A
- Built-in brown-out detector

### Package

- 11-pin QFN or 14-pin SOIC
- QFN size = 3x3 mm



### Analog Peripherals

#### 10-Bit Analog to Digital Converter

- Up to 500 ksps
- Up to 8 external inputs
- $V_{REF}$  from external pin,  $V_{DD}$ , or internal regulator
- Built-in temperature sensor
- External conversion start input option

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current ( $< 0.5 \mu A$ )

### Memory

- 256 bytes internal data RAM
- 2 kB one time programmable code memory

### On-Chip Debug

- C8051F300 can be used as in-system code development platform; complete development kit available
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug

**Temperature Range:  $-40$  to  $+85$  °C**

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- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
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### Clock Sources

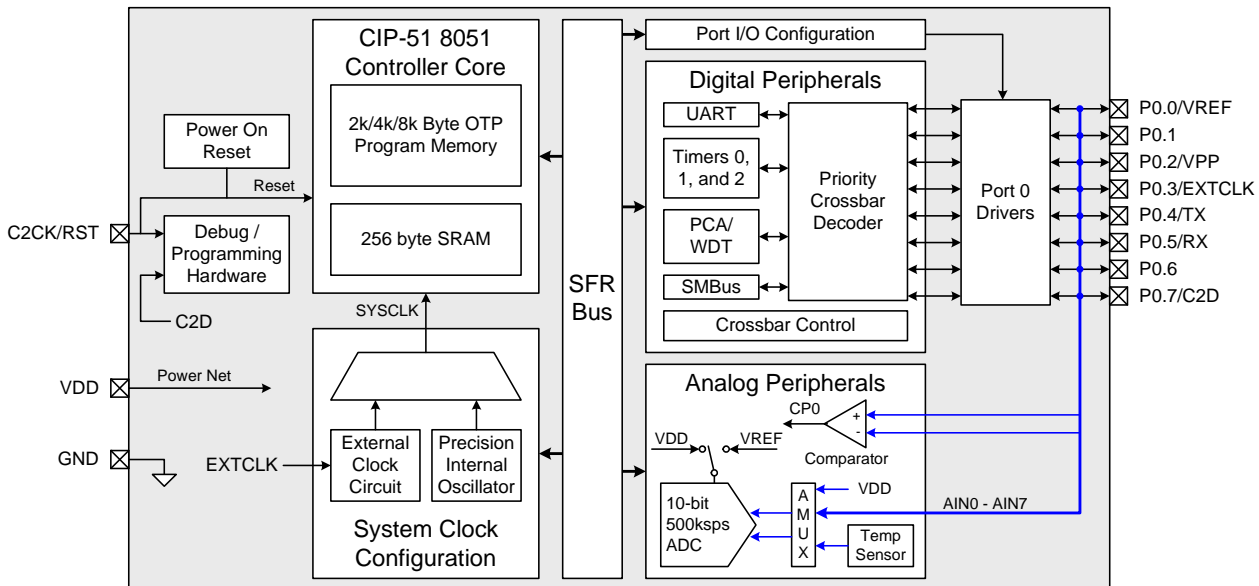
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- Built-in brown-out detector

### Package

- 11-pin QFN or 14-pin SOIC
- QFN size = 3x3 mm





### Analog Peripherals

#### Comparator

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- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

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### Clock Sources

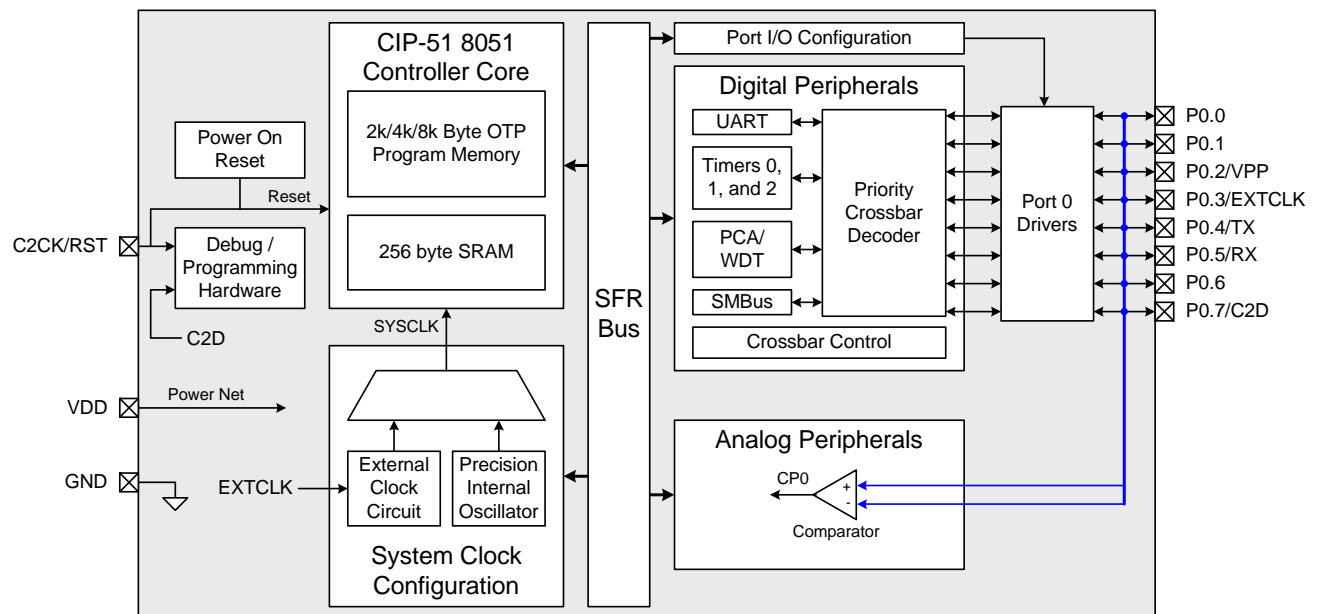
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### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
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TBD  $\mu$ A @ TBD kHz
- Typical stop mode current (regulator off): TBD  $\mu$ A
- Built-in brown-out detector

### Package

- 11-pin QFN or 14-pin SOIC
- QFN size = 3x3 mm



### Analog Peripherals

#### 10-Bit Analog to Digital Converter (C8051T610/1/2/3/6 only)

- Up to 500 ksps
- 21 external inputs
- $V_{REF}$  from external pin,  $V_{DD}$ , or internal regulator
- Built-in temperature sensor
- External conversion start input option

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current ( $< 0.5 \mu A$ )

### Memory

- 1280 bytes internal data RAM
- 16 kB byte-programmable EPROM code memory

### On-Chip Debug

- C8051F310 can be used as in-system code development platform; complete development kit available
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug

### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- On-chip voltage supply monitor

Temperature Range:  $-40$  to  $+85$  °C

### High-Speed 8051 $\mu C$ Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS peak throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

- 29 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SPI™, and SMBus™ serial ports
- Four general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with five capture/compare modules
  - PWM
  - Rising/falling edge capture
  - Frequency output
  - Software timer

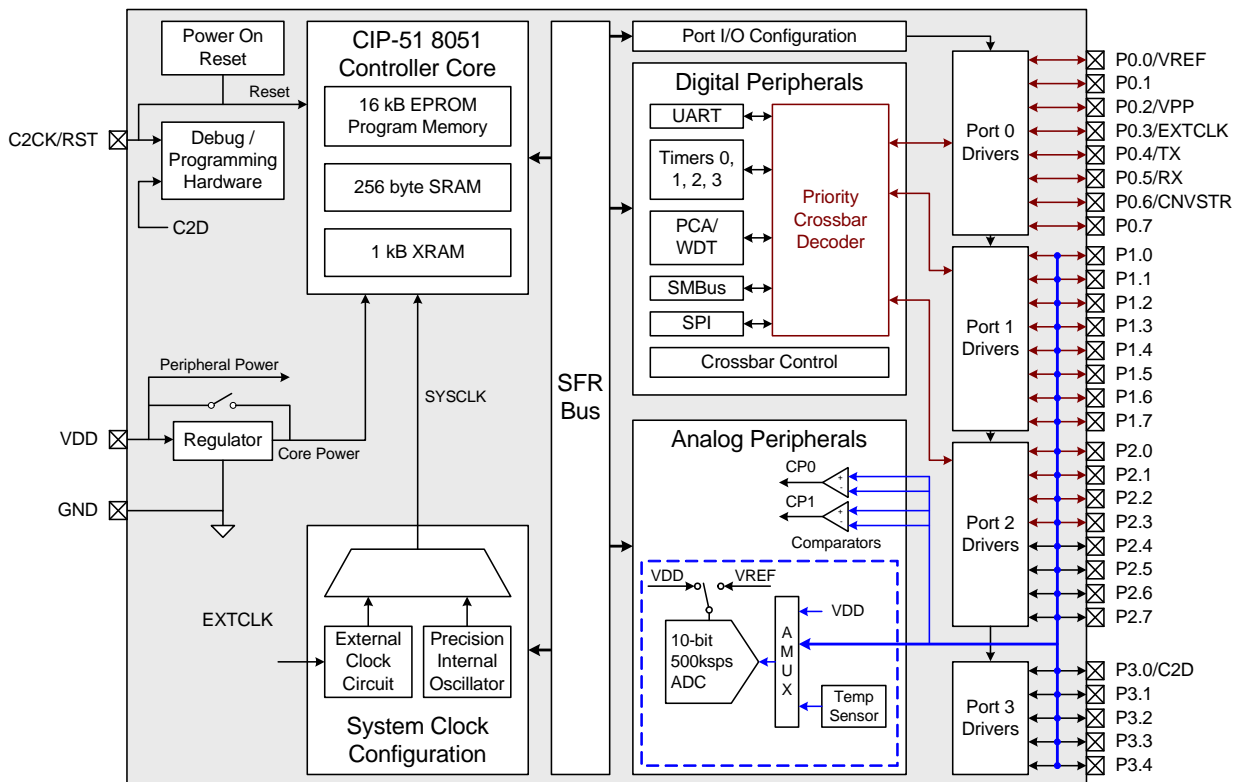
### Clock Sources

- Internal oscillator: 24.5 MHz with  $\pm 2\%$  accuracy supports UART operation
- External oscillator: CMOS clock or external capacitor
- Can switch between clock sources on-the-fly; useful in power saving modes

### Package

- 32-pin LQFP

Development Kit: C8051T610DK



### Analog Peripherals

#### 10-Bit Analog to Digital Converter

- Up to 500 ksps
- 17 external inputs
- $V_{REF}$  from external pin,  $V_{DD}$ , or internal regulator
- Built-in temperature sensor
- External conversion start input option

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current ( $< 0.5 \mu A$ )

#### Memory

- 1280 bytes internal data RAM
- 16 kB byte-programmable EPROM code memory

#### On-Chip Debug

- C8051F310 can be used as in-system code development platform; complete development kit available
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#### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- On-chip voltage supply monitor

#### Temperature Range: $-40$ to $+85$ °C

### High-Speed 8051 $\mu C$ Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS peak throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

- 25 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SPI™, and SMBus™ serial ports
- Four general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with five capture/compare modules
  - PWM
  - Rising / falling edge capture
  - Frequency output
  - Software timer

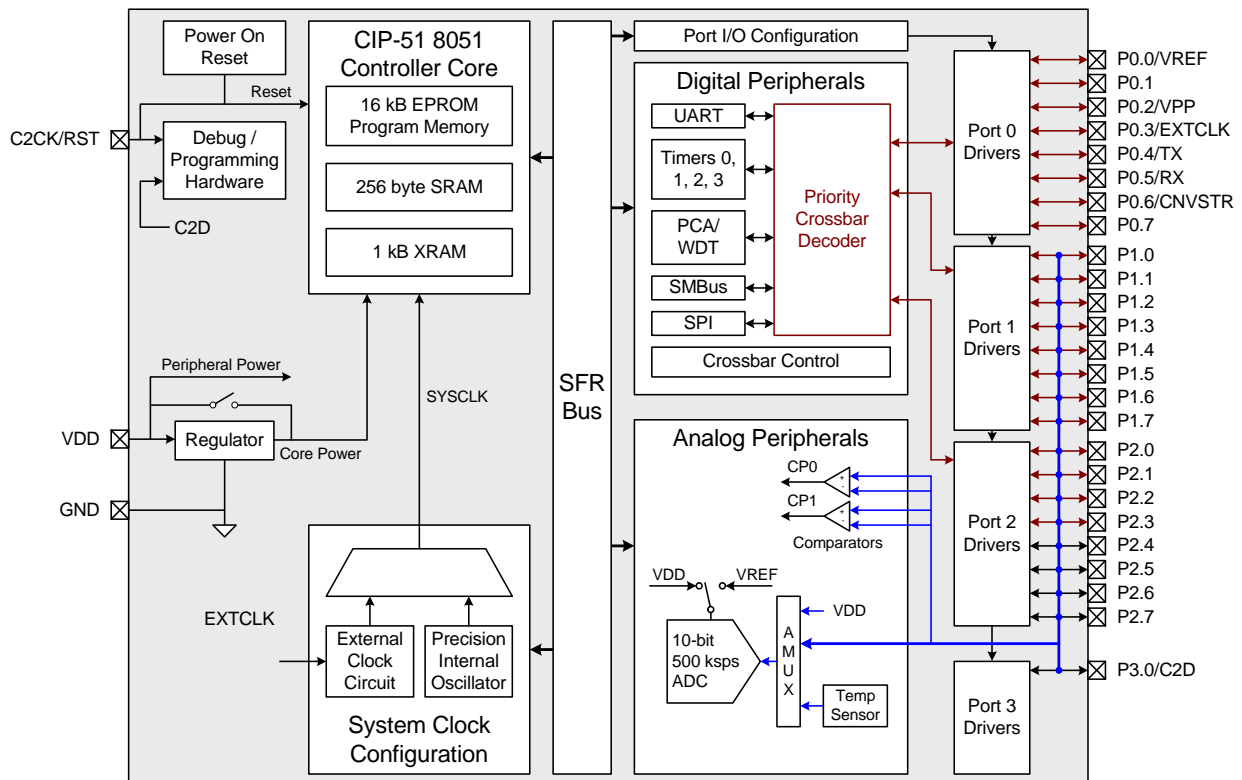
### Clock Sources

- Internal oscillator: 24.5 MHz with  $\pm 2\%$  accuracy supports UART operation
- External oscillator: CMOS clock or external capacitor
- Can switch between clock sources on-the-fly; useful in power saving modes

### Package

- 28-pin QFN

### Development Kit: C8051T610DK



### Analog Peripherals

#### 10-Bit Analog to Digital Converter

- Up to 500 ksp/s
- 21 external inputs
- $V_{REF}$  from external pin,  $V_{DD}$ , or internal regulator
- Built-in temperature sensor
- External conversion start input option

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

### Memory

- 1280 bytes internal data RAM
- 8kB byte-programmable EPROM code memory

### On-Chip Debug

- C8051F310 can be used as in-system code development platform; complete development kit available
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug

### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- On-chip voltage supply monitor

Temperature Range: -40 to +85 °C

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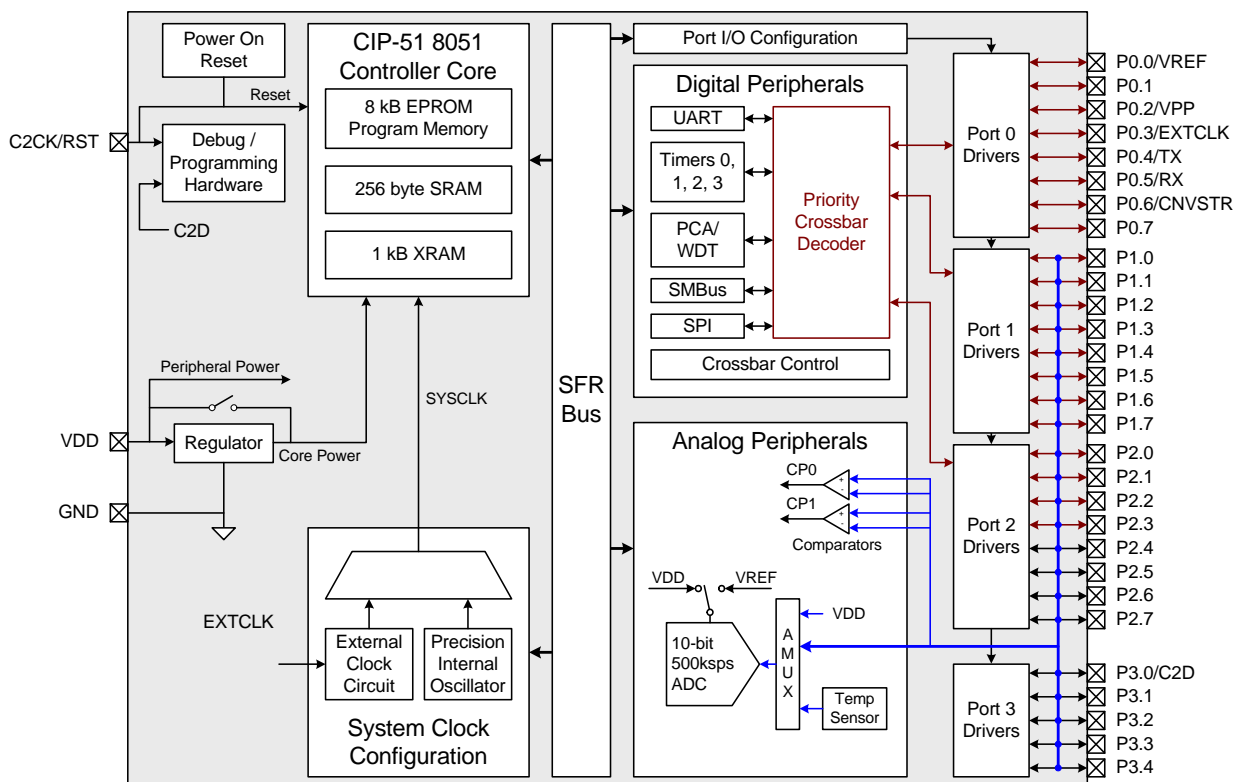
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- Internal oscillator: 24.5 MHz with  $\pm 2\%$  accuracy supports UART operation
- External oscillator: CMOS clock or external capacitor
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### Package

- 32-pin LQFP

Development Kit: C8051T610DK



### Analog Peripherals

#### 10-Bit Analog to Digital Converter

- Up to 500 ksps
- 17 external inputs
- $V_{REF}$  from external pin,  $V_{DD}$ , or internal regulator
- Built-in temperature sensor
- External conversion start input option

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current ( $< 0.5 \mu A$ )

#### Memory

- 1280 bytes internal data RAM
- 8 kB byte-programmable EPROM code memory

#### On-Chip Debug

- C8051F310 can be used as in-system code development platform; complete development kit available
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- On-chip LDO regulator for core supply
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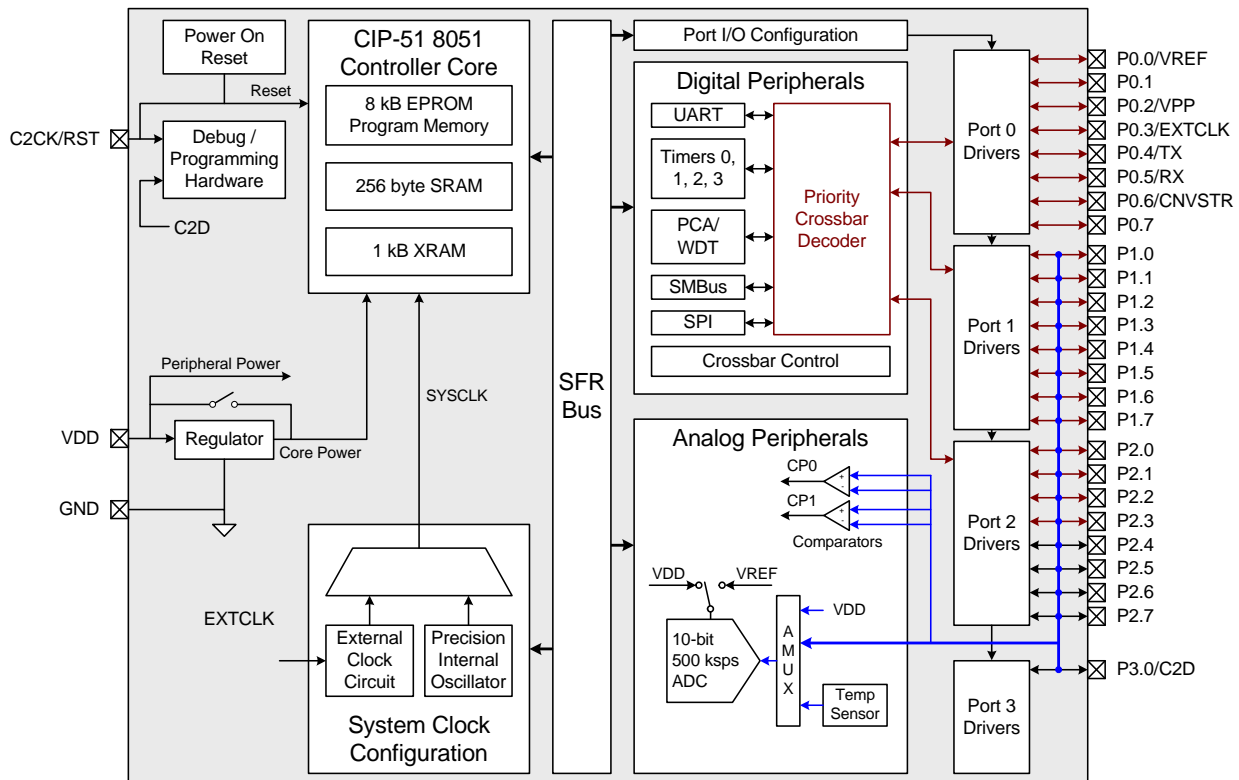
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- External oscillator: CMOS clock or external capacitor
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### Package

- 28-pin QFN

### Development Kit: C8051T610DK



### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

#### Memory

- 1280 bytes internal data RAM
- 8kB byte-programmable EPROM code memory

#### On-Chip Debug

- C8051F310 can be used as in-system code development platform; complete development kit available
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug

#### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- On-chip voltage supply monitor

#### Temperature Range: -40 to +85 °C

### High-Speed 8051 $\mu$ C Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
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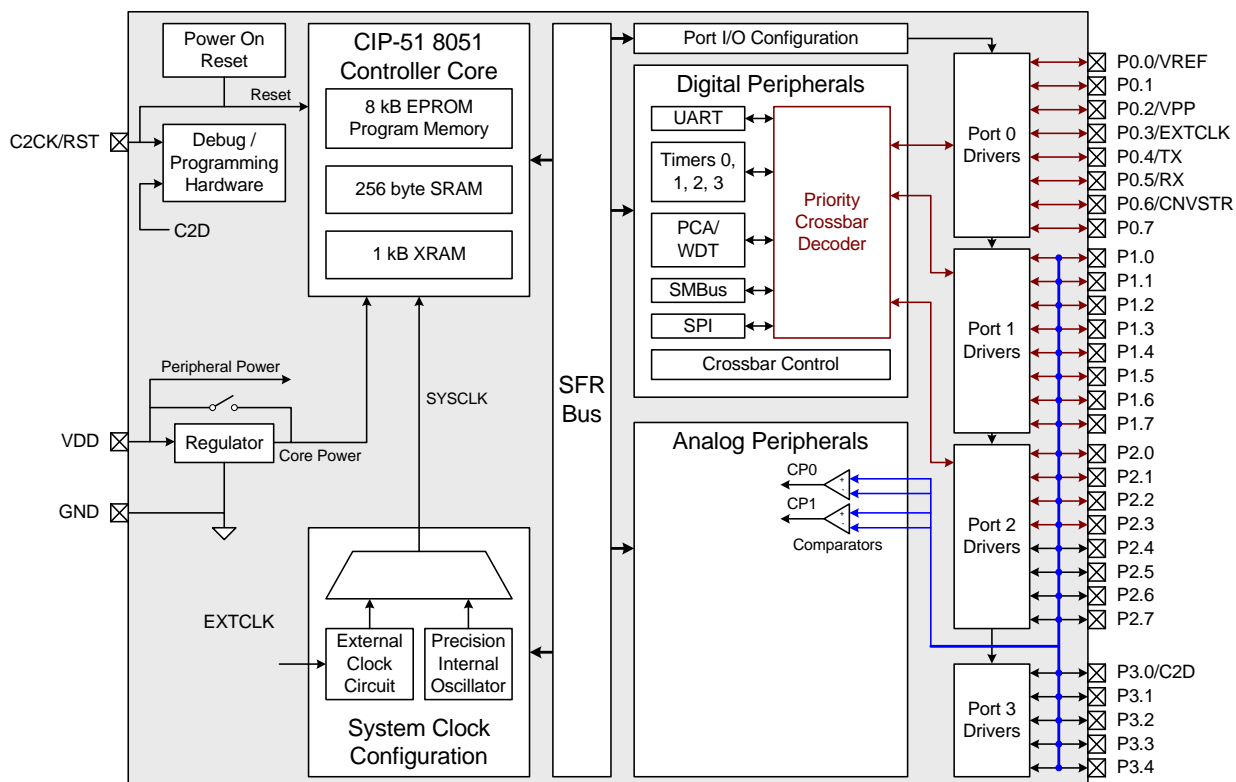
### Clock Sources

- Internal oscillator: 24.5 MHz with  $\pm 2\%$  accuracy supports UART operation
- External oscillator: CMOS clock or external capacitor
- Can switch between clock sources on-the-fly; useful in power saving modes

### Package

- 32-pin LQFP

### Development Kit: C8051T610DK



### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

#### Memory

- 1280 bytes internal data RAM
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### High-Speed 8051 $\mu$ C Core

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### Digital Peripherals

- 25 port I/O; All 5 V tolerant with high sink current
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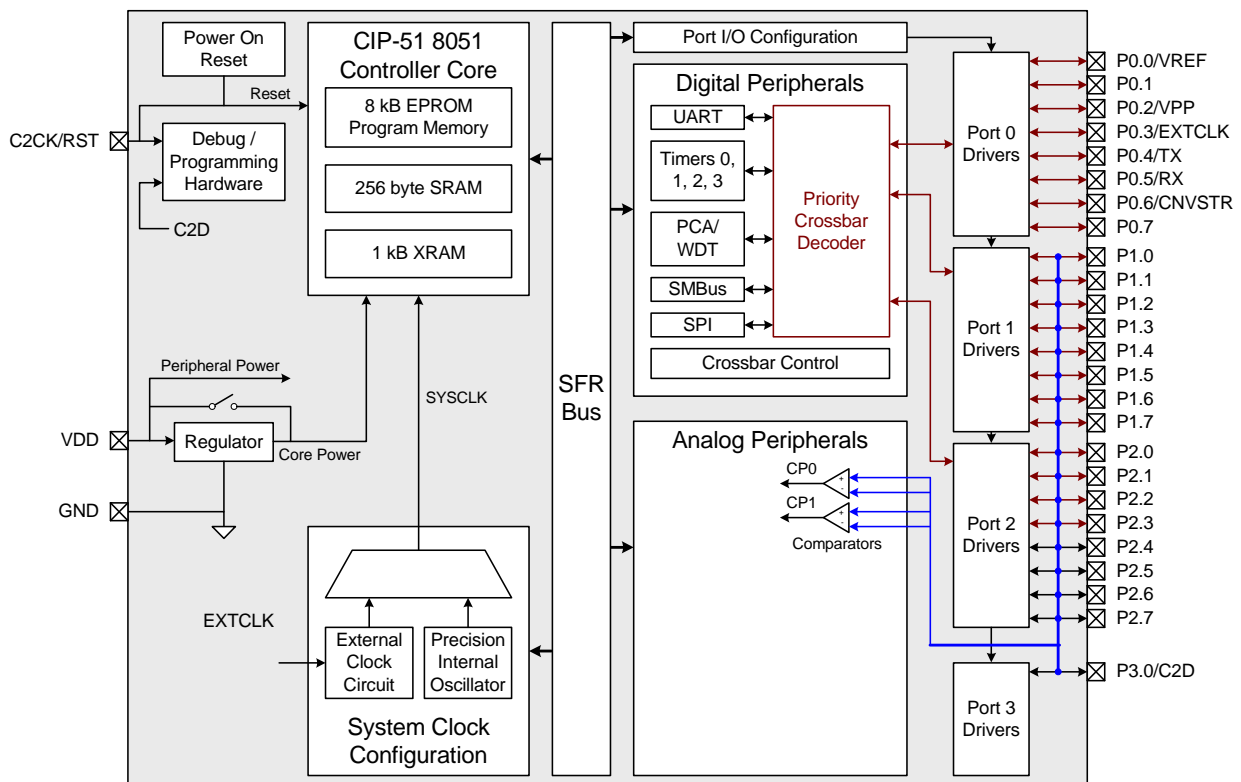
### Clock Sources

- Internal oscillator: 24.5 MHz with  $\pm$ 2% accuracy supports UART operation
- External oscillator: CMOS clock or external capacitor
- Can switch between clock sources on-the-fly; useful in power saving modes

### Package

- 28-pin QFN

### Development Kit: C8051T610DK



### Analog Peripherals

#### 10-Bit Analog to Digital Converter

- Up to 500 ksp/s
- 13 external inputs
- $V_{REF}$  from external pin,  $V_{DD}$ , or internal regulator
- Built-in temperature sensor
- External conversion start input option

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

### Memory

- 1280 bytes internal data RAM
- 16 kB byte-programmable EPROM code memory

### On-Chip Debug

- C8051F310 can be used as in-system code development platform; complete development kit available
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug

### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- On-chip voltage supply monitor

Temperature Range: -40 to +85 °C

### High-Speed 8051 $\mu$ C Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS peak throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

- 21 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SPI™, and SMBus™ serial ports
- Four general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with five capture/compare modules
  - PWM
  - Rising / falling edge capture
  - Frequency output
  - Software timer

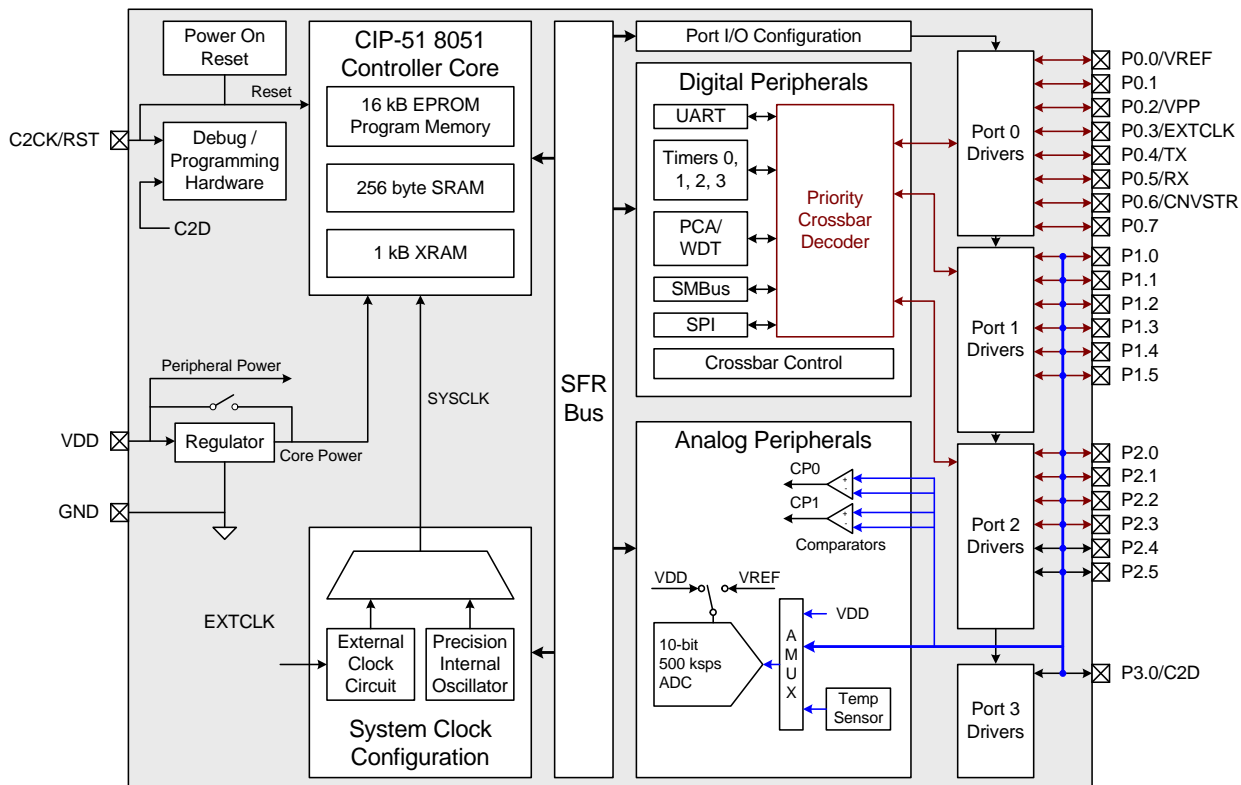
### Clock Sources

- Internal oscillator: 24.5 MHz with  $\pm 2\%$  accuracy supports UART operation
- External oscillator: CMOS clock or external capacitor
- Can switch between clock sources on-the-fly; useful in power saving modes

### Package

- 24-pin QFN

Development Kit: C8051T610DK





### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

#### Memory

- 1280 bytes internal data RAM
- 16 kB byte-programmable EPROM code memory

#### On-Chip Debug

- C8051F310 can be used as in-system code development platform; complete development kit available
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug

#### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- On-chip voltage supply monitor

#### Temperature Range: -40 to +85 °C

### High-Speed 8051 $\mu$ C Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS peak throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

- 21 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SPI™, and SMBus™ serial ports
- Four general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with five capture/compare modules
  - PWM
  - Rising/falling edge capture
  - Frequency output
  - Software timer

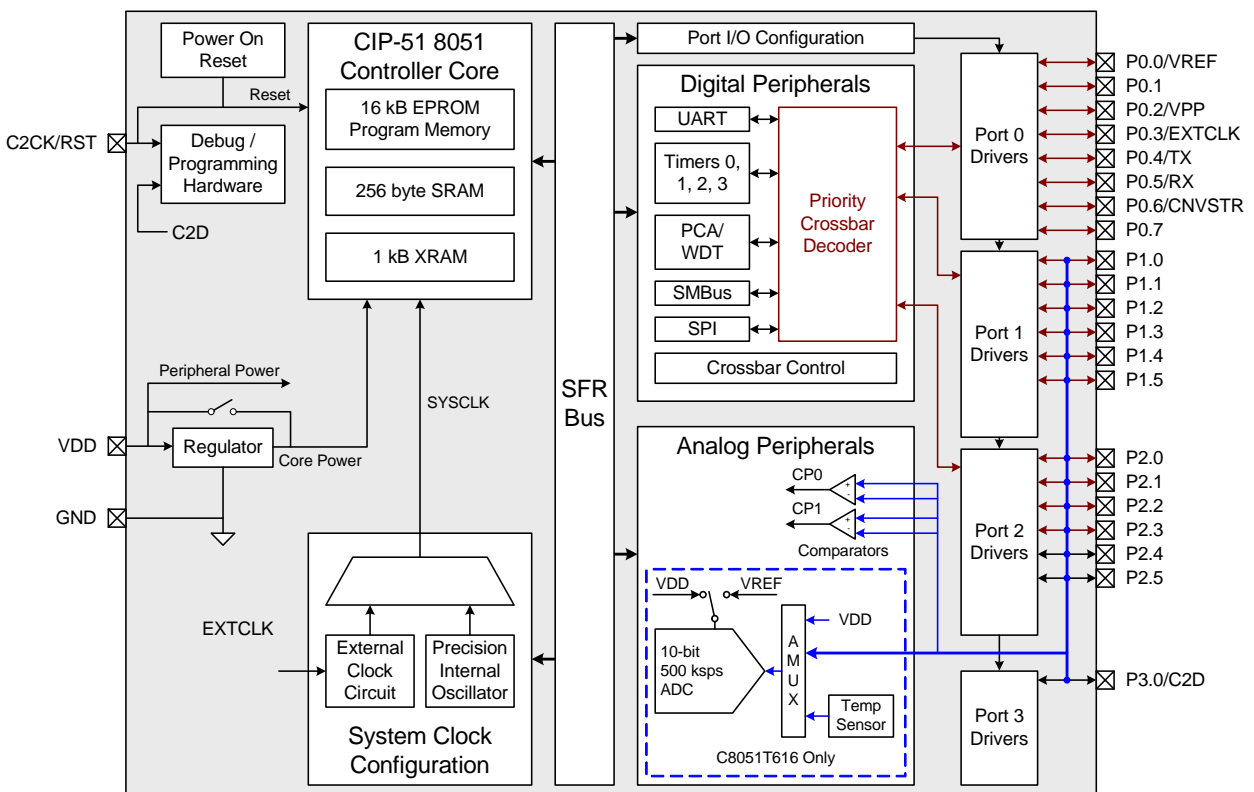
### Clock Sources

- Internal oscillator: 24.5 MHz with  $\pm$ 2% accuracy supports UART operation
- External oscillator: CMOS clock or external capacitor
- Can switch between clock sources on-the-fly; useful in power saving modes

### Package

- 24-pin QFN

### Development Kit: C8051T610DK



### Analog Peripherals

- 10-Bit ADC
- Up to 500 kbps
- Up to 16 external single-ended inputs
- VREF from external pin, VDD, or internal regulator
- Built-in temperature sensor
- External conversion start input

### 10-bit DAC (Current Mode)

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

### Memory

- 768 bytes data RAM
- 8 kB EPROM OTP code memory (byte programmable)

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- C8051F336 can be used as in-system code development platform; complete development kit available

### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- On-chip voltage supply monitor

### Temperature Range: -40 to +85 °C

### Development Kit: C8051T630DK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

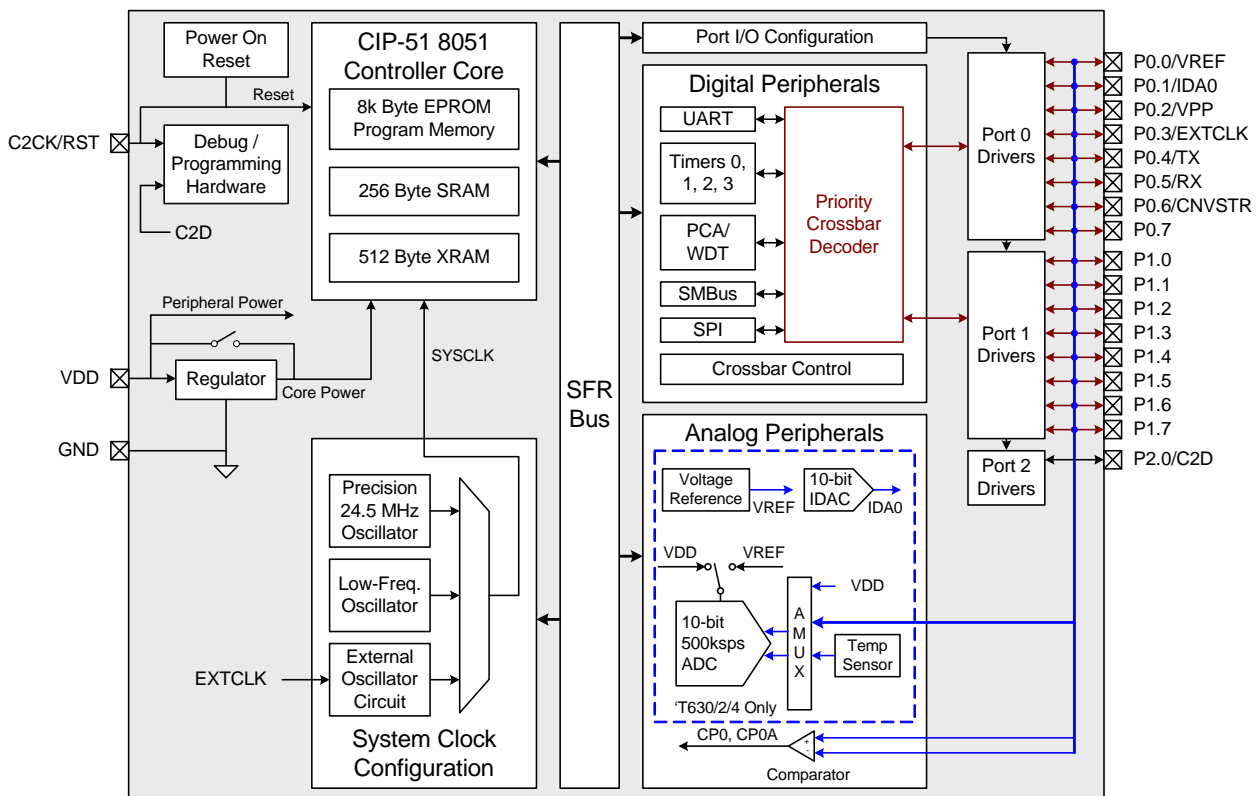
- 17 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SPI™, and SMBus™ serial ports
- Four general purpose 16-bit counter/timers
- Timer with Real-time clock capability
- 16-Bit programmable counter array (PCA) with five capture/compare modules
  - PWM
  - Rising/falling edge capture
  - Frequency output
- Software timer

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz with  $\pm$ 2% accuracy supports crystal-less UART operation
  - Low-power suspend mode with fast wake time
  - 80 kHz low frequency, low-power
- External oscillator: RC, C, or Clock
- Can switch between clock sources on-the-fly

### Package

- 20-pin QFN
- Pin Compatible with C8051F33x Family of Devices



### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

#### Memory

- 768 bytes data RAM
- 8 kB EPROM OTP code memory (byte programmable)

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- C8051F336 can be used as in-system code development platform; complete development kit available

#### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- On-chip voltage supply monitor

#### Temperature Range: -40 to +85 °C

#### Development Kit: C8051T630DK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

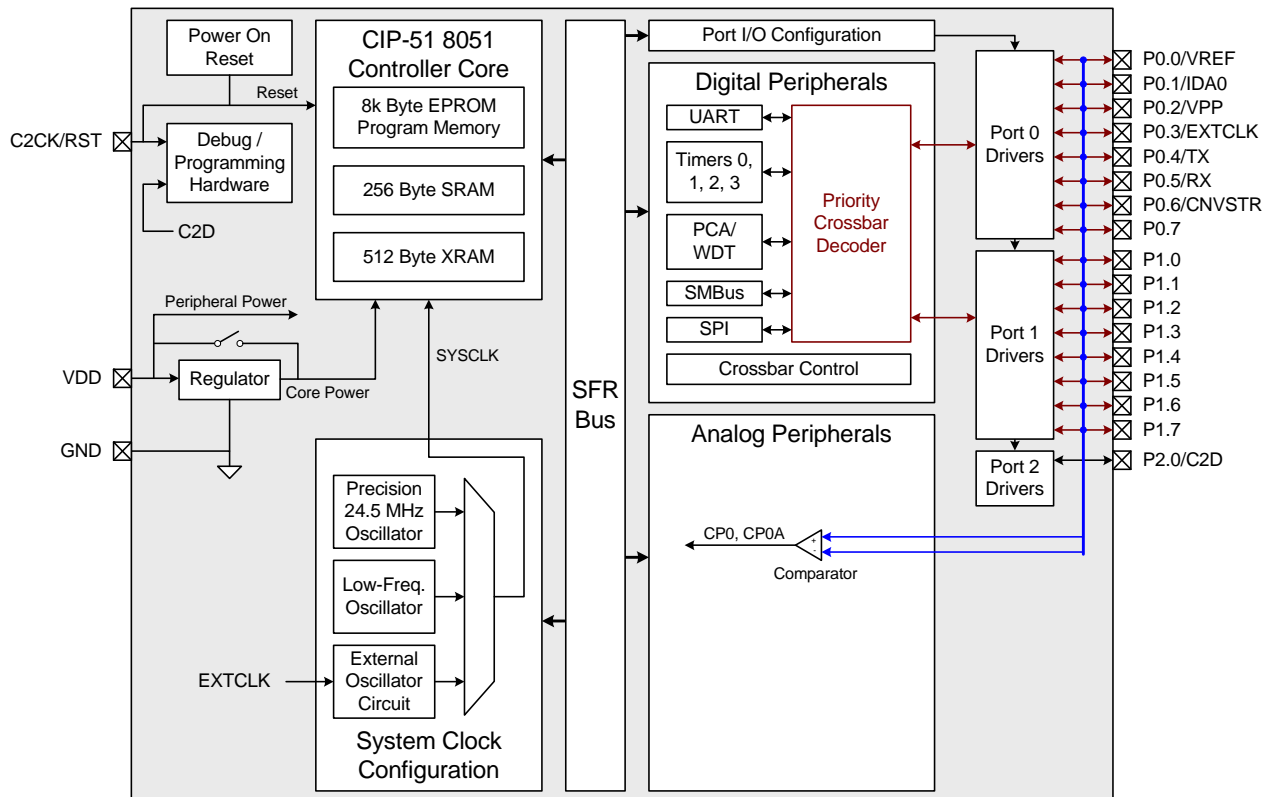
- 29/25/21 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SPI™, and SMBus™ serial ports
- Four general purpose 16-bit counter/timers
- Timer with Real-time clock capability
- 16-Bit programmable counter array (PCA) with five capture/compare modules
  - PWM
  - Rising / falling edge capture
  - Frequency output
- Software timer

### -Clock Sources

- Two internal oscillators:
  - 24.5 MHz with  $\pm$ 2% accuracy supports crystal-less UART operation
  - Low-power suspend mode with fast wake time
  - 80 kHz low frequency, low-power
- External oscillator: RC, C, or Clock
- Can switch between clock sources on-the-fly

### Package

- 20-pin QFN and 24-pin QFN
- Pin Compatible with C8051F33x Family of Devices



### Analog Peripherals

- 10-Bit ADC
- Up to 500 kbps
- Up to 16 external single-ended inputs
- VREF from external pin, VDD, or internal regulator
- Built-in temperature sensor
- External conversion start input

### 10-bit DAC (Current Mode)

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

### Memory

- 768 bytes data RAM
- 4 kB EPROM OTP memory (byte programmable)

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- C8051F336 can be used as in-system code development platform; complete development kit available

### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- On-chip voltage supply monitor

### Temperature Range: -40 to +85 °C

### Development Kit: C8051T630DK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

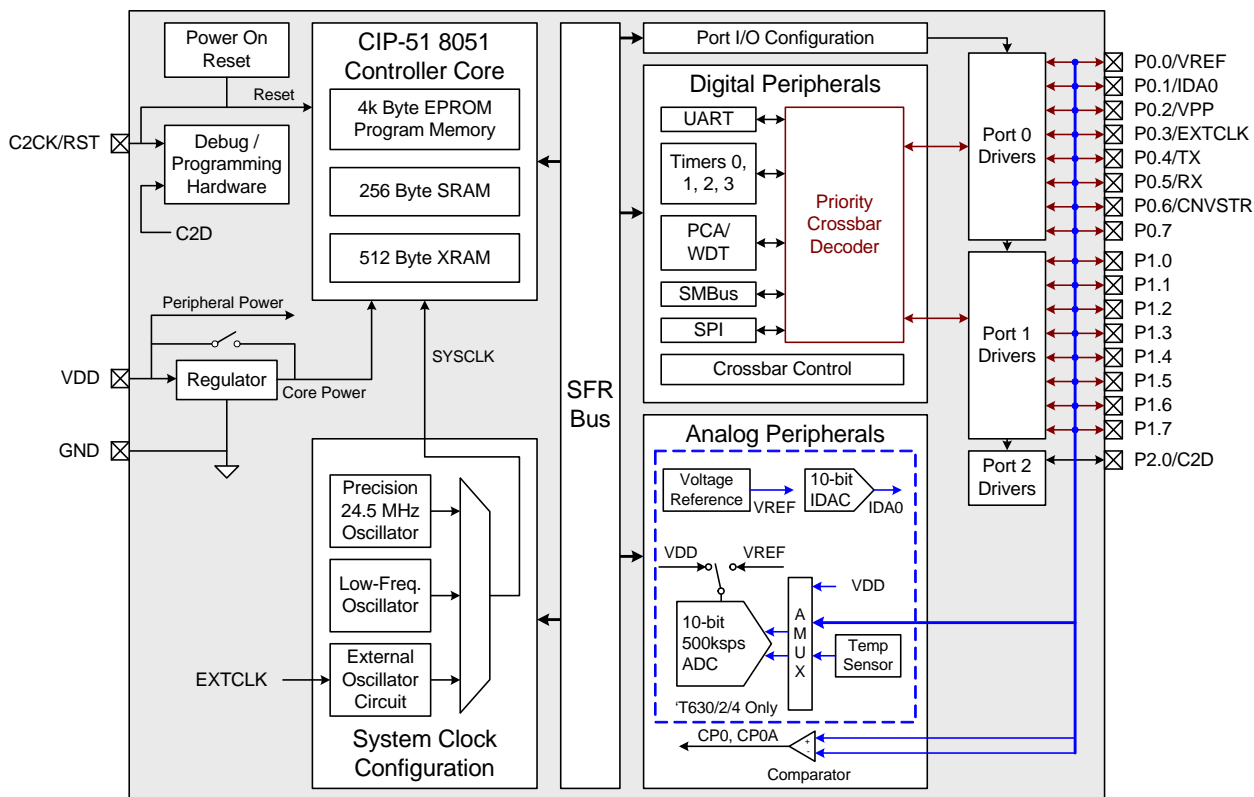
- 17 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SPI™, and SMBus™ serial ports
- Four general purpose 16-bit counter/timers
- Timer with Real-time clock capability
- 16-Bit programmable counter array (PCA) with five capture/compare modules
  - PWM
  - Rising / falling edge capture
  - Frequency output
- Software timer

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz with  $\pm$ 2% accuracy supports crystal-less UART operation
  - Low-power suspend mode with fast wake time
  - 80 kHz low frequency, low-power
- External oscillator: RC, C, or Clock
- Can switch between clock sources on-the-fly

### Package

- 20-pin QFN
- Pin Compatible with C8051F33x Family of Devices



### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

#### Memory

- 768 bytes data RAM
- 4 kB EPROM OTP code memory (byte programmable)

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- C8051F336 can be used as in-system code development platform; complete development kit available

#### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- On-chip voltage supply monitor

#### Temperature Range: -40 to +85 °C

#### Development Kit: C8051T630DK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

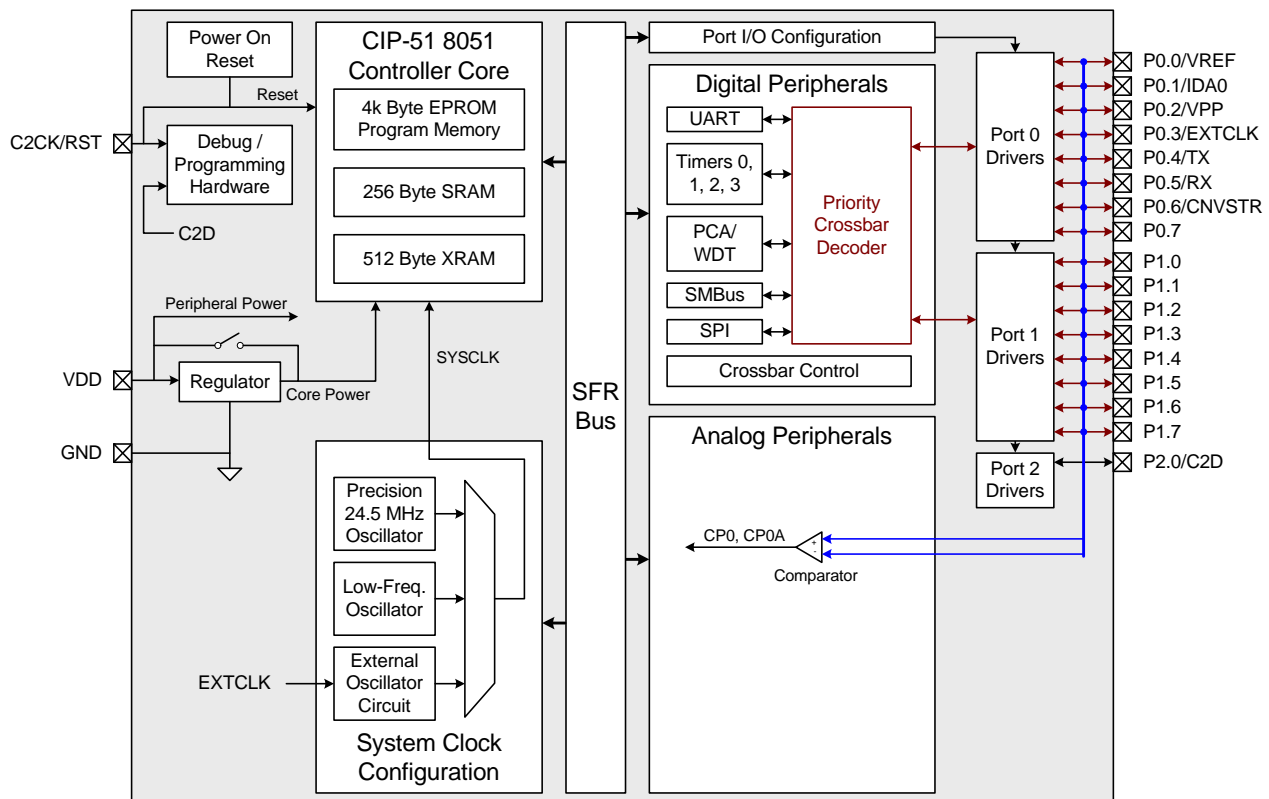
- 17 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SPI™, and SMBus™ serial ports
- Four general purpose 16-bit counter/timers
- Timer with Real-time clock capability
- 16-Bit programmable counter array (PCA) with five capture/compare modules
  - PWM
  - Rising / falling edge capture
  - Frequency output
- Software timer

### -Clock Sources

- Two internal oscillators:
  - 24.5 MHz with  $\pm$ 2% accuracy supports crystal-less UART operation
  - Low-power suspend mode with fast wake time
  - 80 kHz low frequency, low-power
- External oscillator: RC, C, or Clock
- Can switch between clock sources on-the-fly

### Package

- 20-pin QFN
- Pin Compatible with C8051F33x Family of Devices



### Analog Peripherals

- 10-Bit ADC
- Up to 500 kbps
- Up to 16 external single-ended inputs
- VREF from external pin, VDD, or internal regulator
- Built-in temperature sensor
- External conversion start input

### 10-bit DAC (Current Mode)

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

### Memory

- 768 bytes data RAM
- 2 kB EPROM OTP memory (byte programmable)

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- C8051F336 can be used as in-system code development platform; complete development kit available

### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- On-chip voltage supply monitor

### Temperature Range: -40 to +85 °C

### Development Kit: C8051T630DK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

- 17 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SPI™, and SMBus™ serial ports
- Four general purpose 16-bit counter/timers
- Timer with Real-time clock capability
- 16-Bit programmable counter array (PCA) with five capture/compare modules
  - PWM
  - Rising / falling edge capture
  - Frequency output

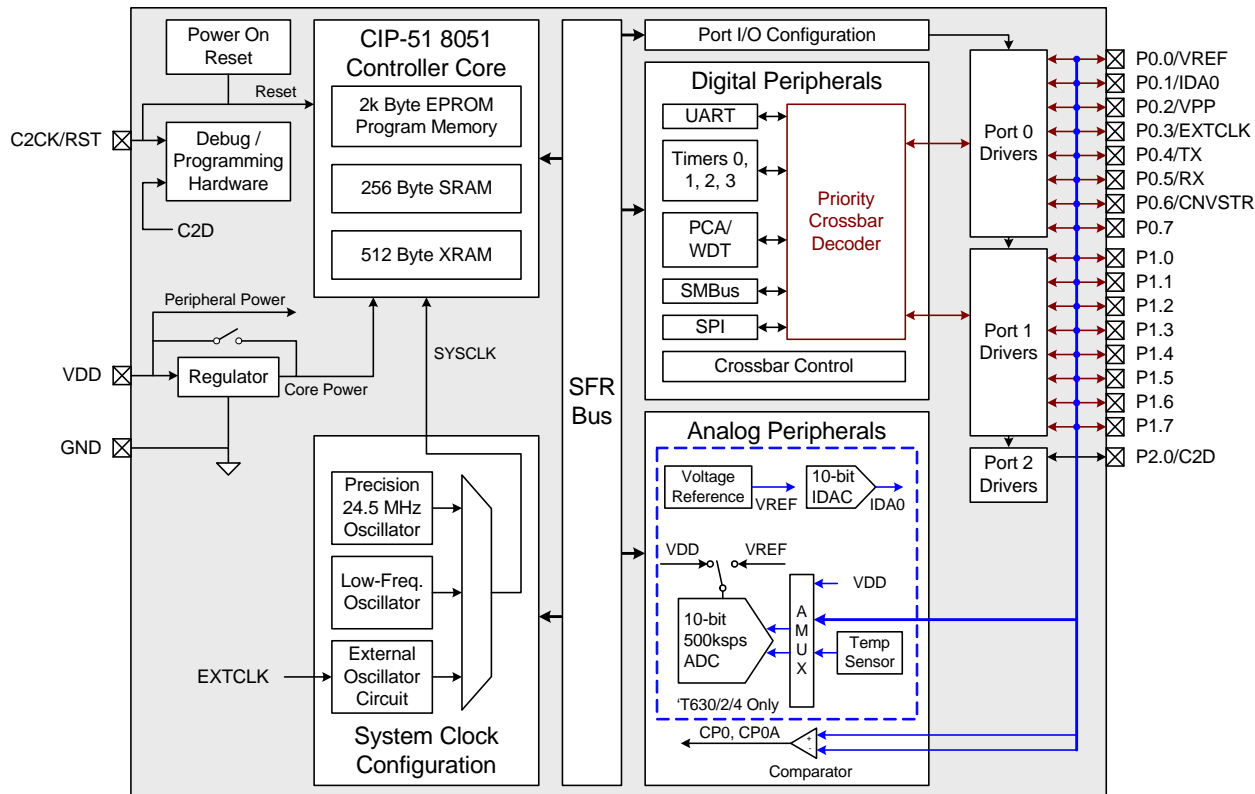
#### Software timer

### -Clock Sources

- Two internal oscillators:
  - 24.5 MHz with  $\pm$ 2% accuracy supports crystal-less UART operation
  - Low-power suspend mode with fast wake time
  - 80 kHz low frequency, low-power
- External oscillator: RC, C, or Clock
- Can switch between clock sources on-the-fly

### Package

- 20-pin QFN
- Pin Compatible with C8051F33x Family of Devices



### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5  $\mu$ A)

#### Memory

- 768 bytes data RAM
- 2 kB EPROM OTP code memory (byte programmable)

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- C8051F336 can be used as in-system code development platform; complete development kit available

#### Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- On-chip voltage supply monitor

#### Temperature Range: -40 to +85 °C

#### Development Kit: C8051T630DK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Digital Peripherals

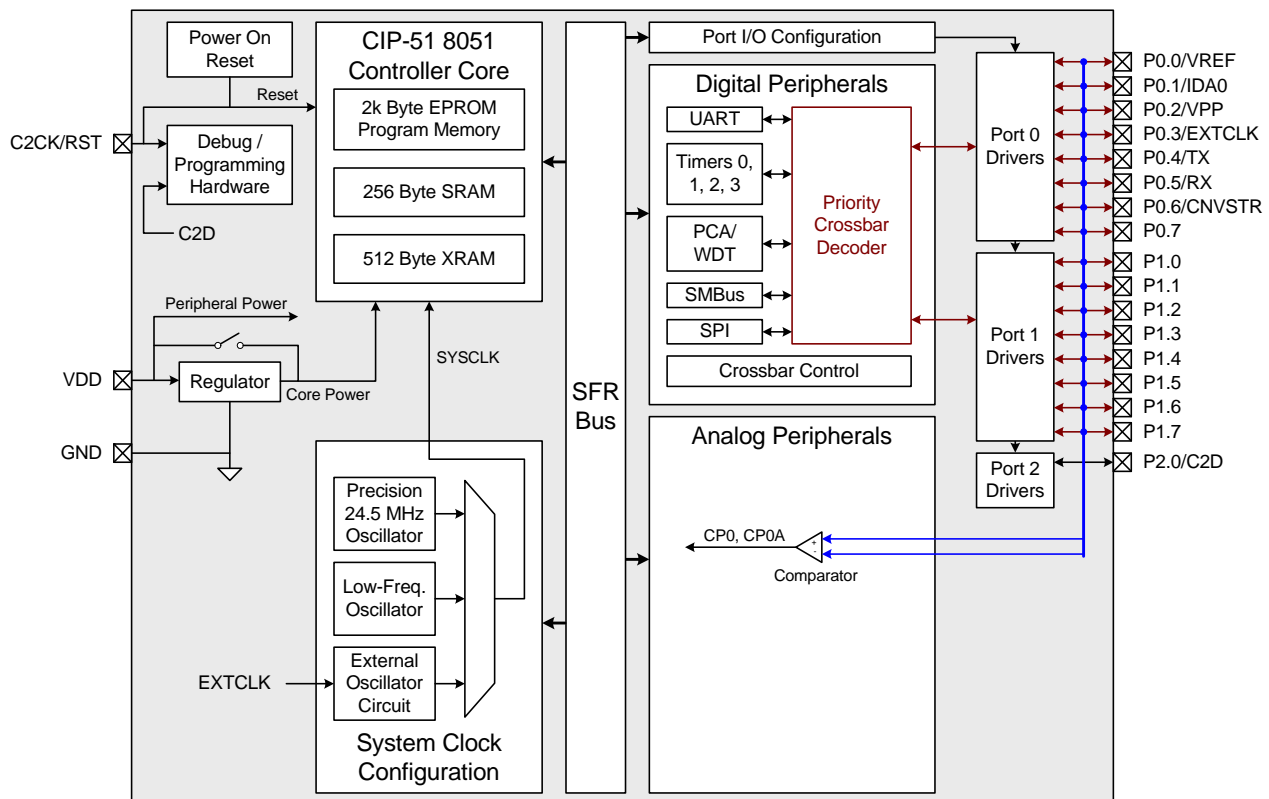
- 17 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SPI™, and SMBus™ serial ports
- Four general purpose 16-bit counter/timers
- Timer with Real-time clock capability
- 16-Bit programmable counter array (PCA) with five capture/compare modules
  - PWM
  - Rising / falling edge capture
  - Frequency output
- Software timer

### -Clock Sources

- Two internal oscillators:
  - 24.5 MHz with  $\pm$ 2% accuracy supports crystal-less UART operation
  - Low-power suspend mode with fast wake time
  - 80 kHz low frequency, low-power
- External oscillator: RC, C, or Clock
- Can switch between clock sources on-the-fly

### Package

- 20-pin QFN
- Pin Compatible with C8051F33x Family of Devices









# Precision Mixed-Signal MCUs

### Analog Peripherals

#### 12-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two 12-bit DACs

- Voltage output
- 10  $\mu$ sec settling time

#### Two Comparators

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 20 MIPS throughput with 20 MHz system clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 256 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

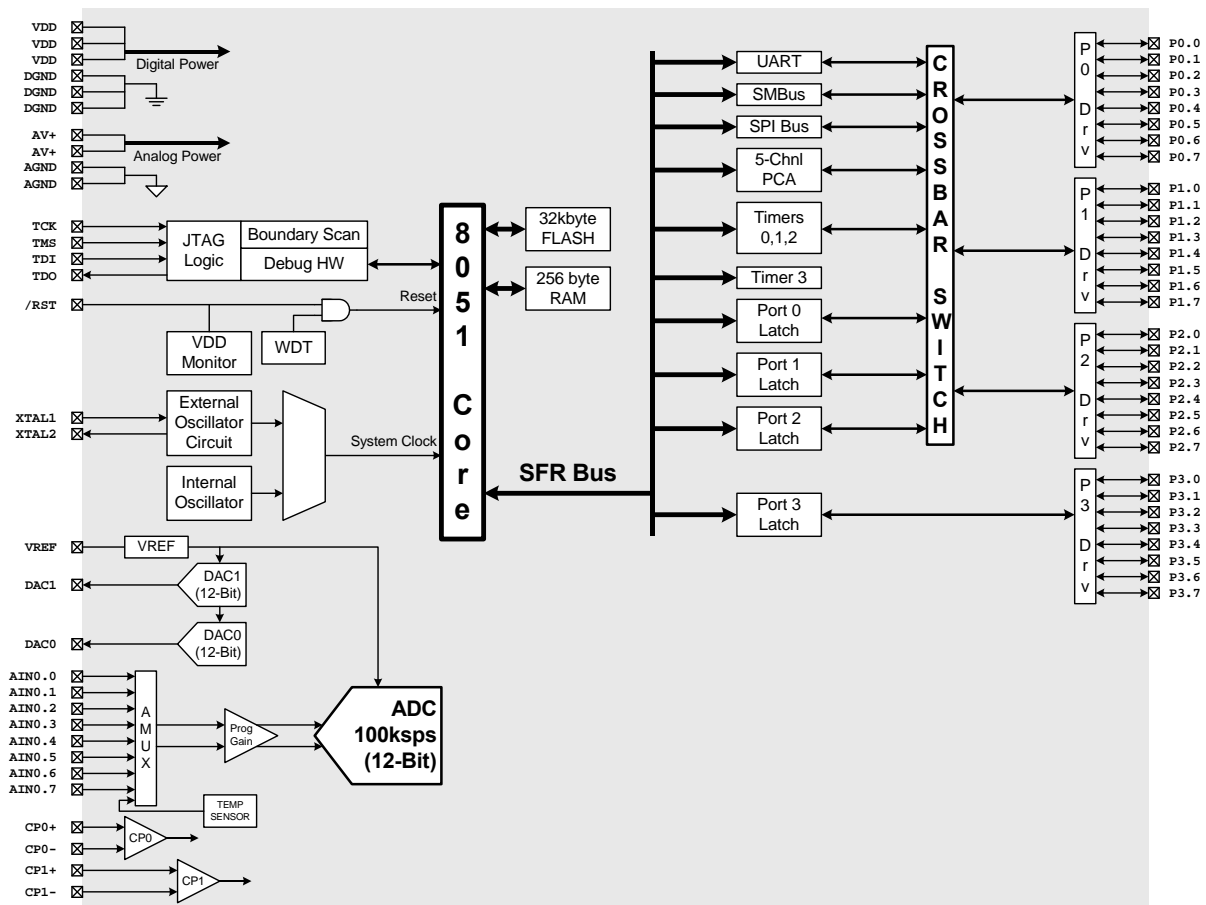
- Typical operating current: 10 mA at 20 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F000-GQ



**Analog Peripherals**

**12-Bit ADC**

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

**Two 12-Bit DACs**

- Voltage output
- 10  $\mu$ sec settling time

**Two Comparators**

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

**Internal Voltage Reference**

**V<sub>DD</sub> Monitor/Brown-out Detector**

**On-Chip JTAG Debug**

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

**High-Speed 8051  $\mu$ C Core**

- Pipelined instruction architecture; executes 70% of Instructions in 1 or 2 system clocks
- Up to 20 MIPS throughput with 20 MHz clock
- Expanded interrupt handler; up to 21 interrupt sources

**Memory**

- 256 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

**Digital Peripherals**

- 16 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

**Clock Sources**

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

**Supply Voltage: 2.7 to 3.6 V**

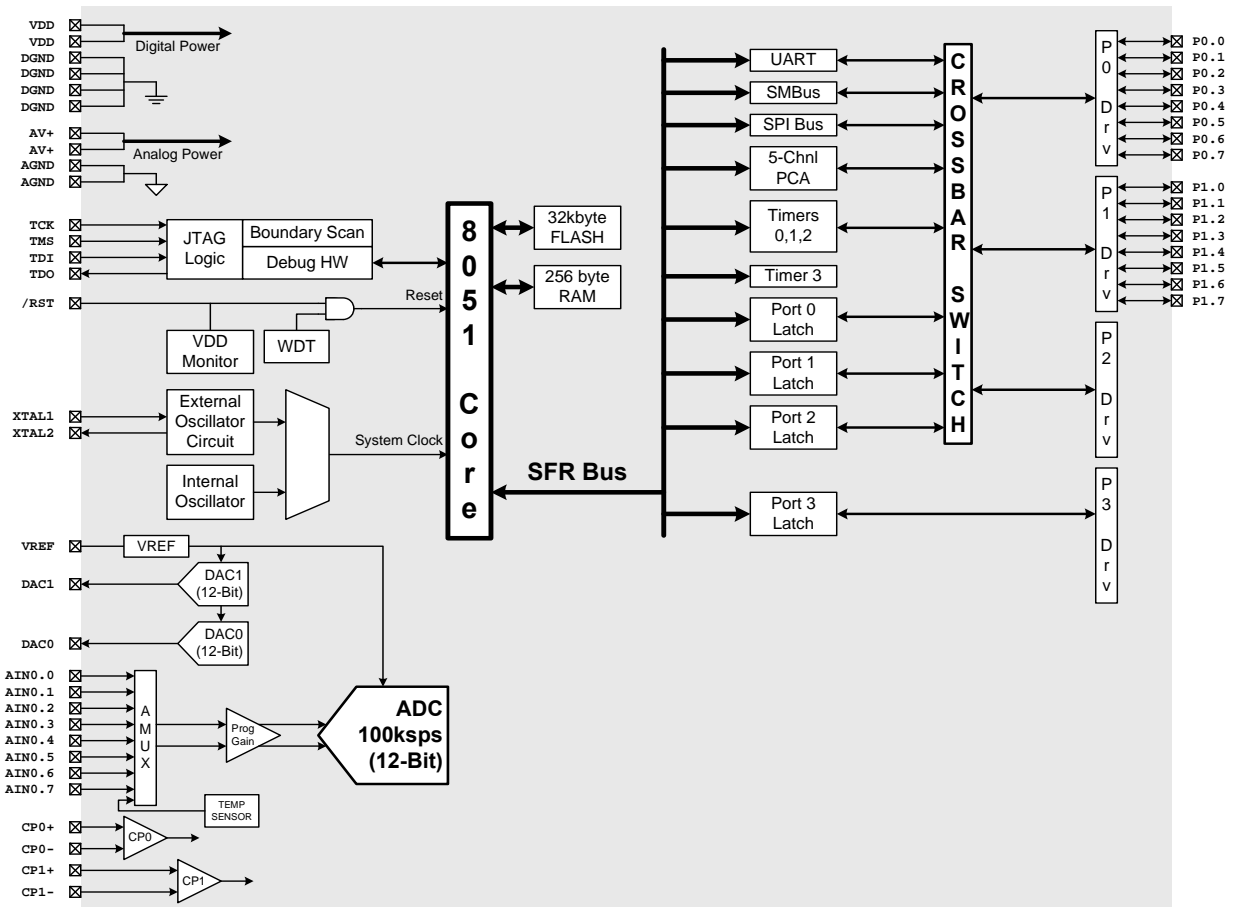
- Typical operating current: 10 mA at 20 MHz
- Multiple power saving sleep and shutdown modes

**Package**

- 48-pin TQFP (lead-free package)

**Ordering Part Number**

- C8051F001-GQ



### Analog Peripherals

#### 12-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 4 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two 12-Bit DACs

- Voltage output
- 10  $\mu$ sec settling time

#### Comparator

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of Instructions in 1 or 2 system clocks
- Up to 20 MIPS throughput with 20 MHz clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 256 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 8 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

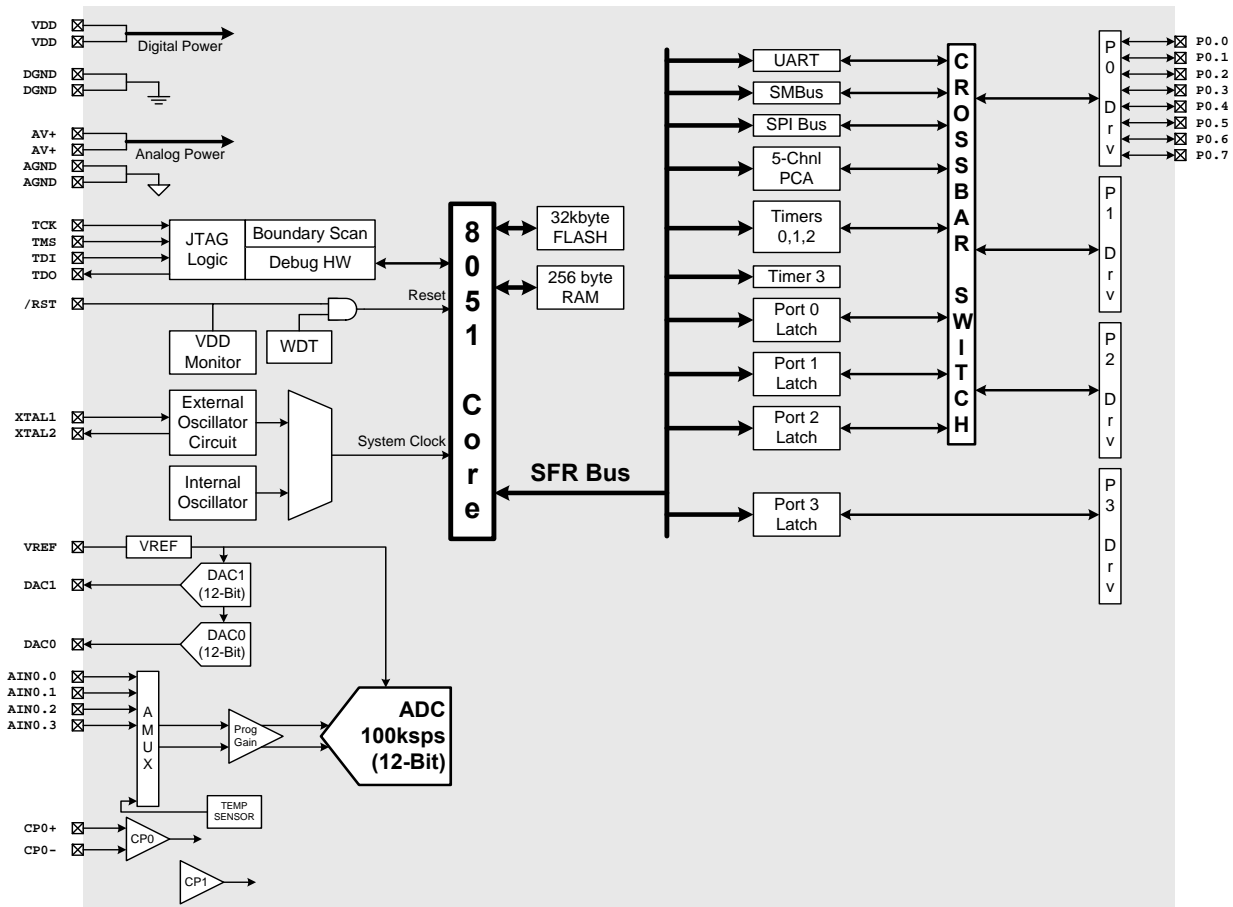
- Typical operating current: 10 mA at 20 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 32-pin LQFP (lead-free package)

### Ordering Part Number

- C8051F002-GQ



**Analog Peripherals**

**12-Bit ADC**

- ±1 LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor (±3 °C)

**Two 12-Bit DACs**

- Voltage output
- 10 µsec settling time

**Two Comparators**

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

**Internal Voltage Reference**

**V<sub>DD</sub> Monitor/Brown-out Detector**

**On-Chip JTAG Debug**

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

**High-Speed 8051 µC Core**

- Pipelined instruction architecture; executes 70% of Instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler; up to 21 interrupt sources

**Memory**

- 2304 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

**Digital Peripherals**

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

**Clock Sources**

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

**Supply Voltage: 2.7 to 3.6 V**

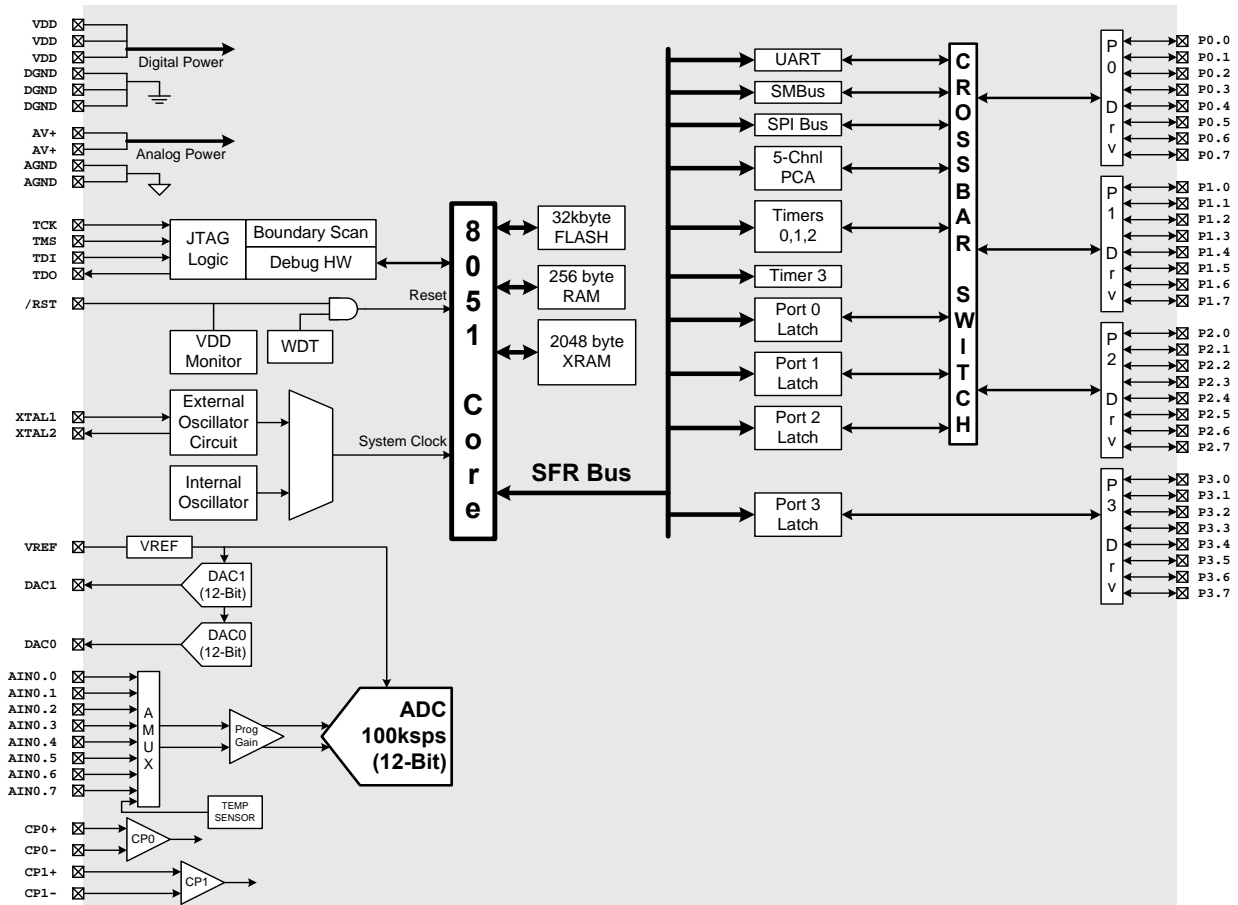
- Typical operating current: 12.5 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

**Package**

- 64-pin TQFP (lead-free package)

**Ordering Part Number**

- C8051F005-GQ



### Analog Peripherals

#### 12-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two 12-Bit DACs

- Voltage output
- 10  $\mu$ sec settling time

#### Two Comparators

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

#### Temperature Range: -40 to +85 °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of Instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 2304 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 16 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

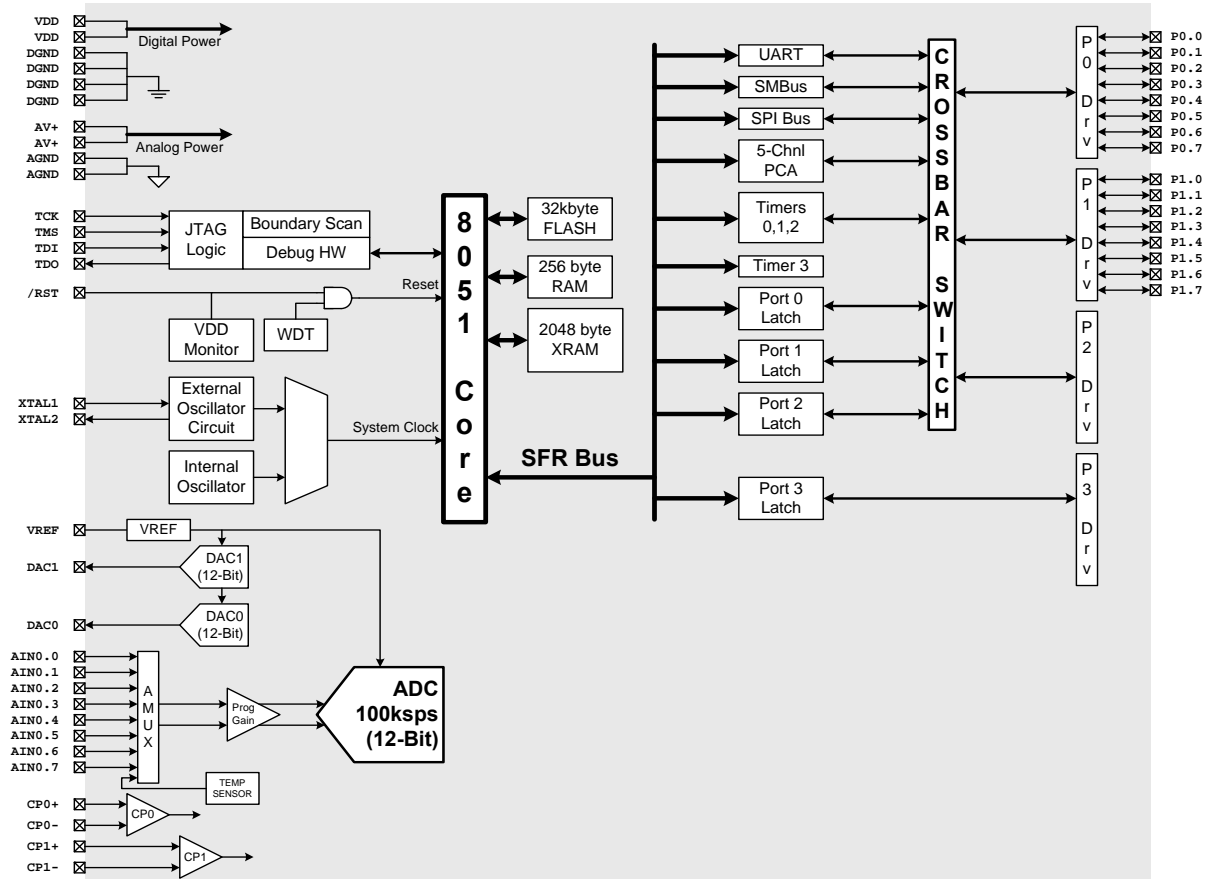
- Typical operating current: 12.5 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 48-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F006-GQ



**Analog Peripherals**

**12-Bit ADC**

- ±1 LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 4 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor (±3 °C)

**Two 12-Bit DACs**

- Voltage output
- 10 µsec settling time

**Comparator**

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

**Internal Voltage Reference**

**V<sub>DD</sub> Monitor/Brown-out Detector**

**On-Chip JTAG Debug**

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

**High-Speed 8051 µC Core**

- Pipelined instruction architecture; executes 70% of Instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler; up to 21 interrupt sources

**Memory**

- 2304 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

**Digital Peripherals**

- 8 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

**Clock Sources**

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

**Supply Voltage: 2.7 to 3.6 V**

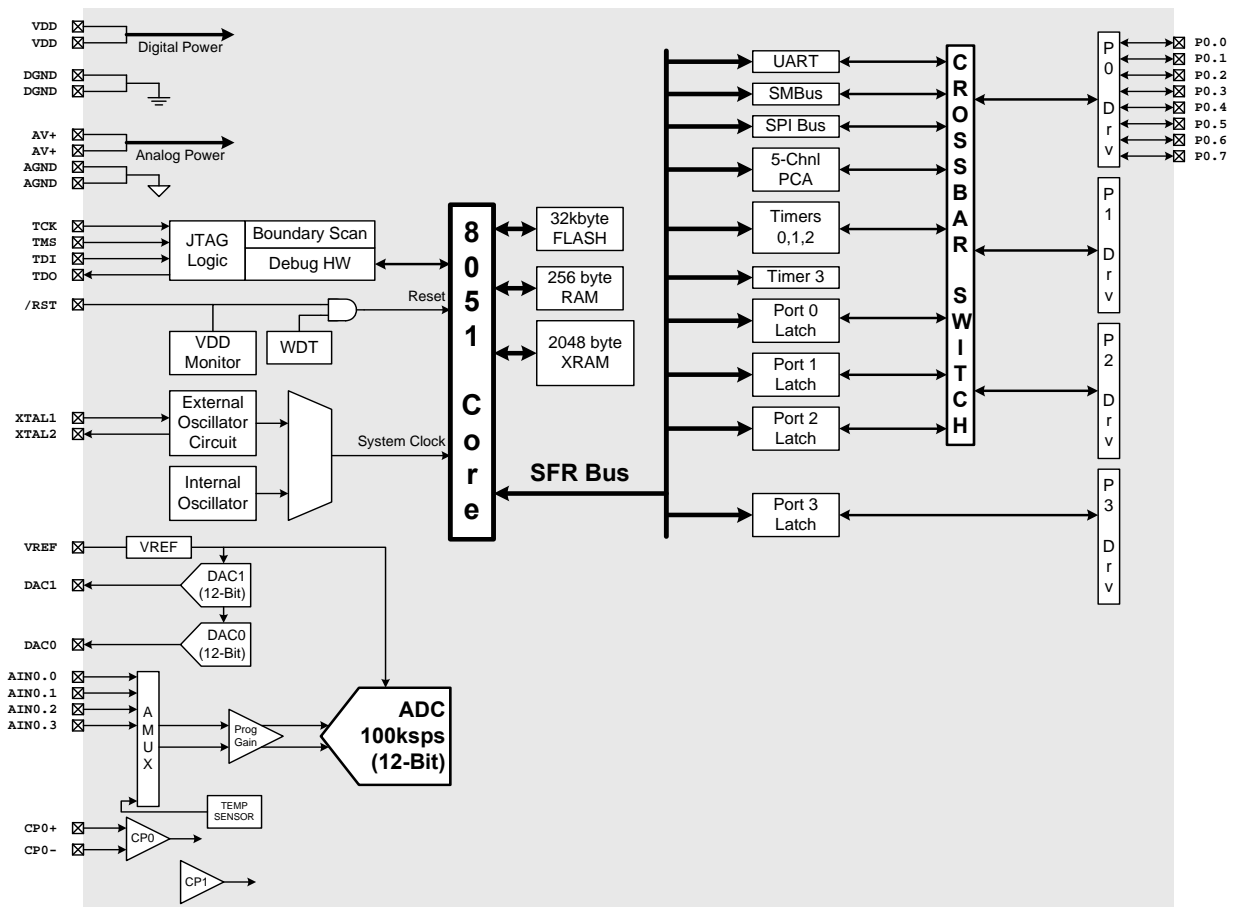
- Typical operating current: 12.5 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

**Package**

- 32-pin LQFP (lead-free package)

**Ordering Part Number**

- C8051F007-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two 12-Bit DACs

- Voltage output
- 10  $\mu$ sec settling time

#### Two Comparators

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of Instructions in 1 or 2 system clocks
- Up to 20 MIPS throughput with 20 MHz clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 256 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

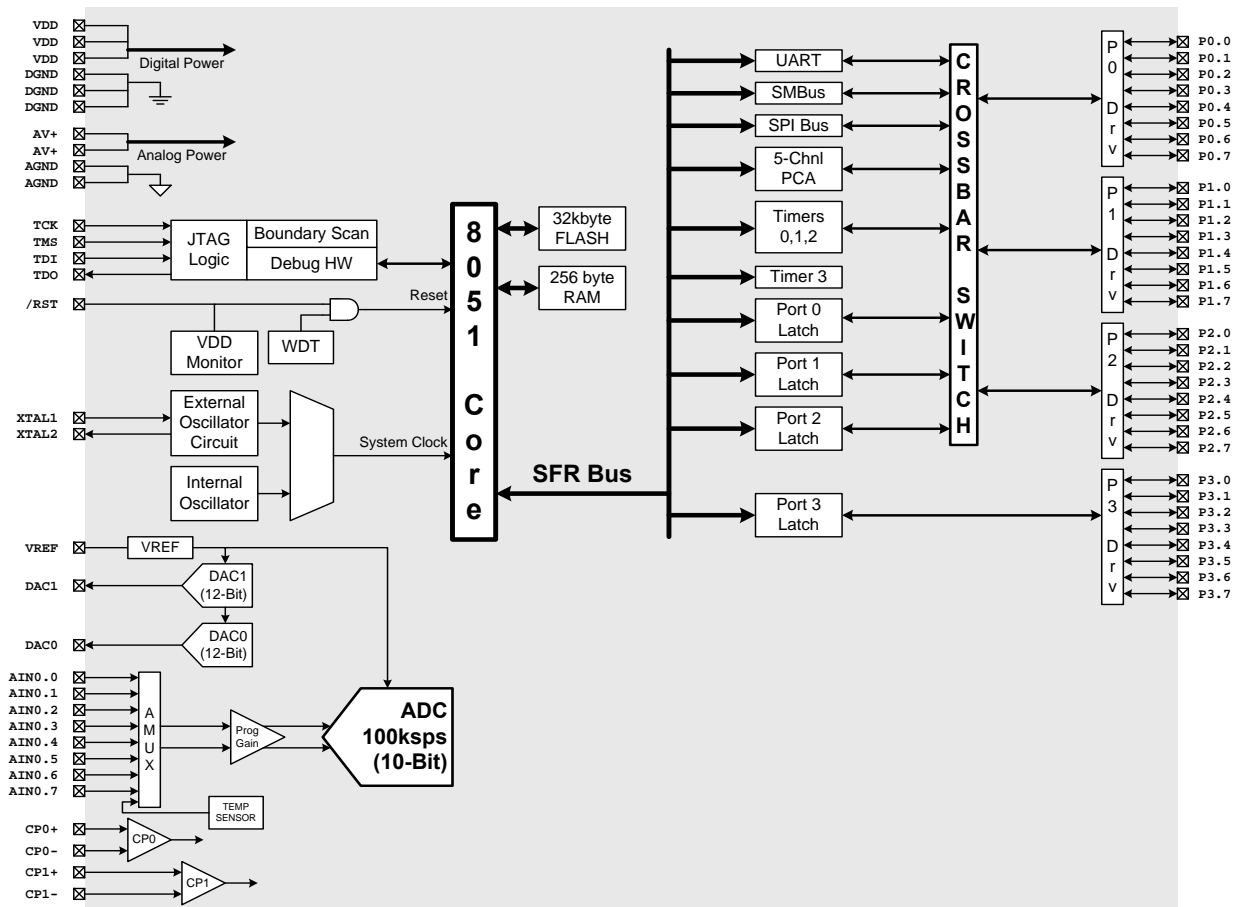
- Typical operating current: 10 mA at 20 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F010-GQ





### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two 12-Bit DACs

- Voltage output
- 10  $\mu$ sec settling time

#### Two Comparators

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of Instructions in 1 or 2 system clocks
- Up to 20 MIPS throughput with 20 MHz clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 256 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 16 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

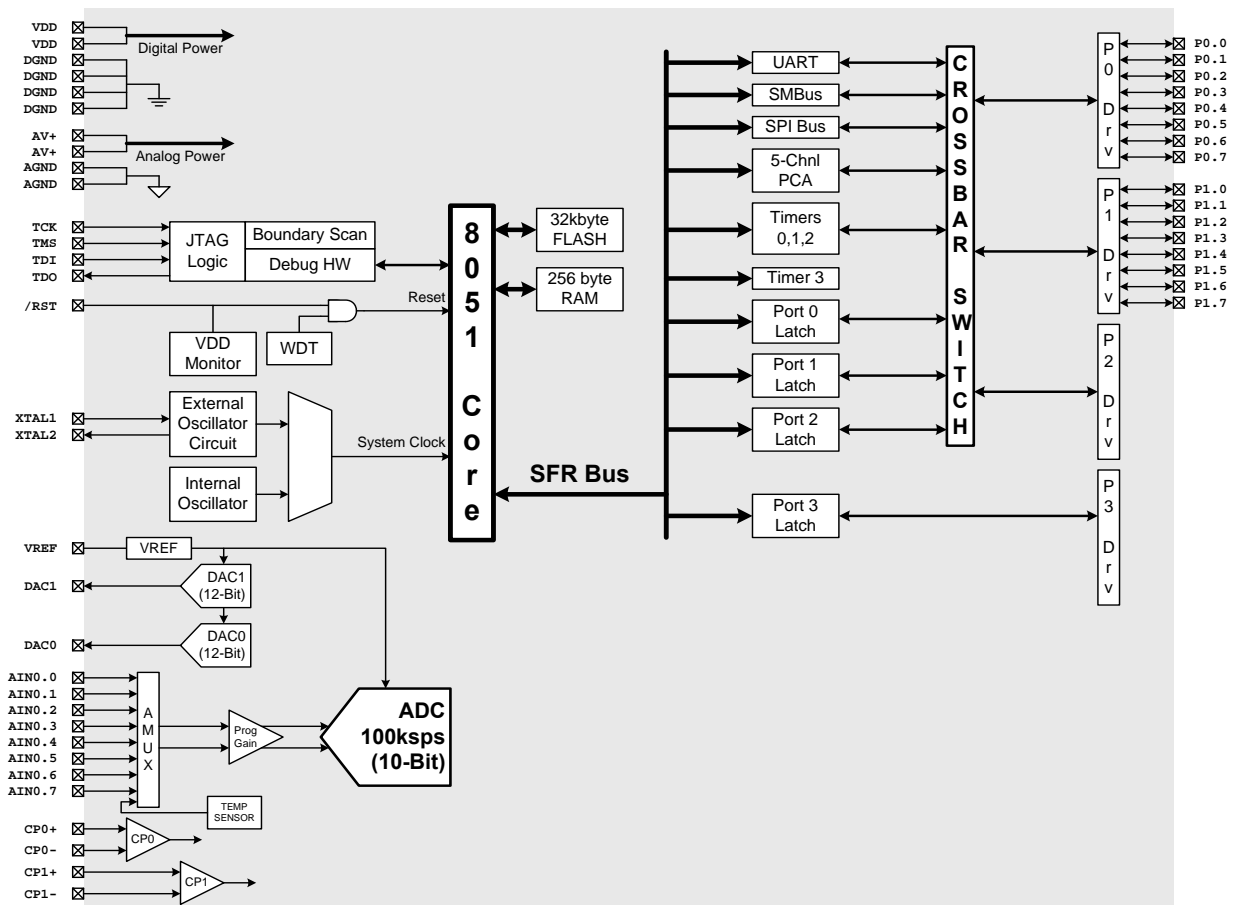
- Typical operating current: 10 mA at 20 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 48-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F011-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 4 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two 12-Bit DACs

- Voltage output
- 10  $\mu$ sec settling time

#### Comparator

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of Instructions in 1 or 2 system clocks
- Up to 20 MIPS throughput with 20 MHz clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 256 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 8 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

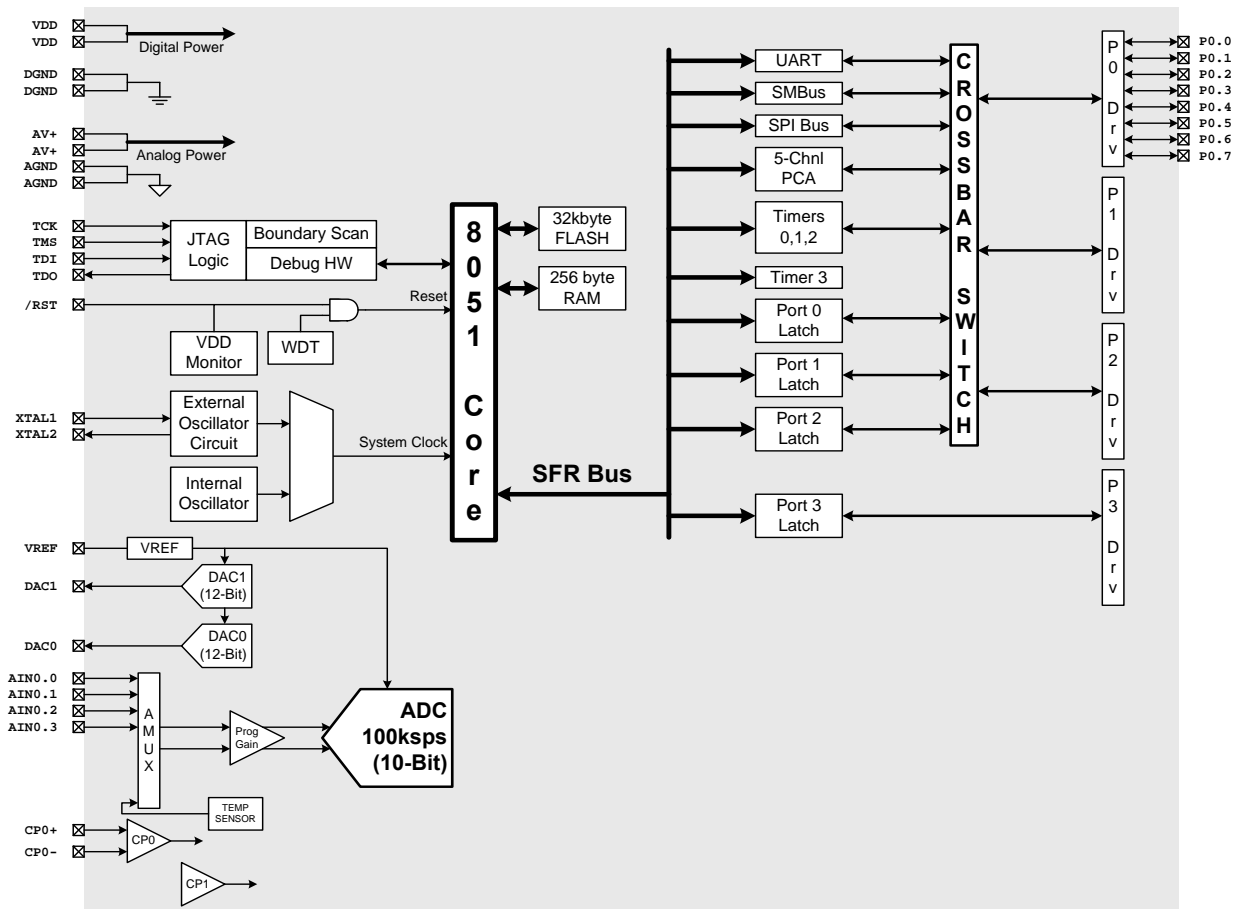
- Typical operating current: 10 mA at 20 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 32-pin LQFP (lead-free package)

### Ordering Part Number

- C8051F012-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two 12-Bit DACs

- Voltage output
- 10  $\mu$ sec settling time

#### Two Comparators

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of Instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 2304 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

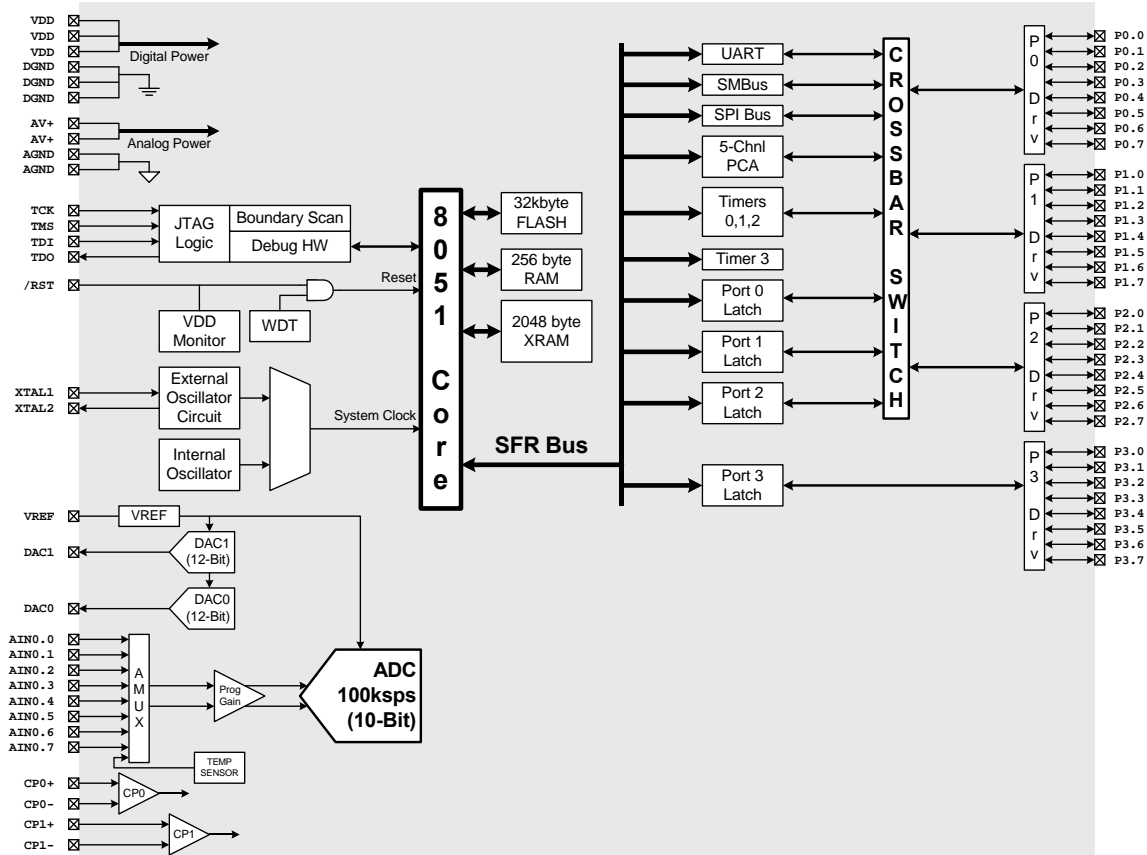
- Typical operating current: 12.5 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F015-GQ



### Analog Peripherals

#### 10-Bit ADC

- ±1 LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor (±3 °C)

#### Two 12-Bit DACs

- Voltage output
- 10 µsec settling time

#### Two Comparators

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of Instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 2304 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 16 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly
- Fully compliant with IEEE 1149.1 specification

### Supply Voltage: 2.7 to 3.6 V

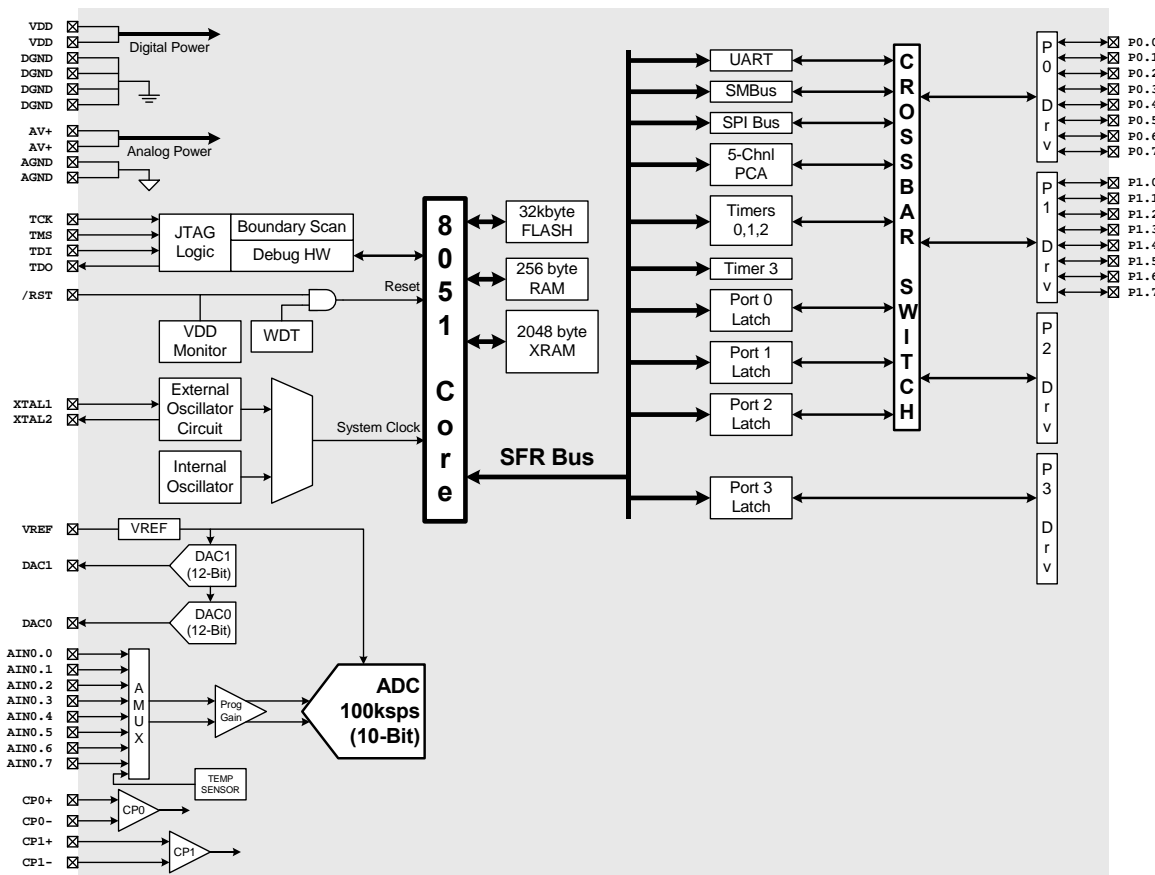
- Typical operating current: 12.5 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 48-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F016-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 4 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two 12-Bit DACs

- Voltage output
- 10  $\mu$ sec settling time

#### Comparator

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of Instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 2304 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 8 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

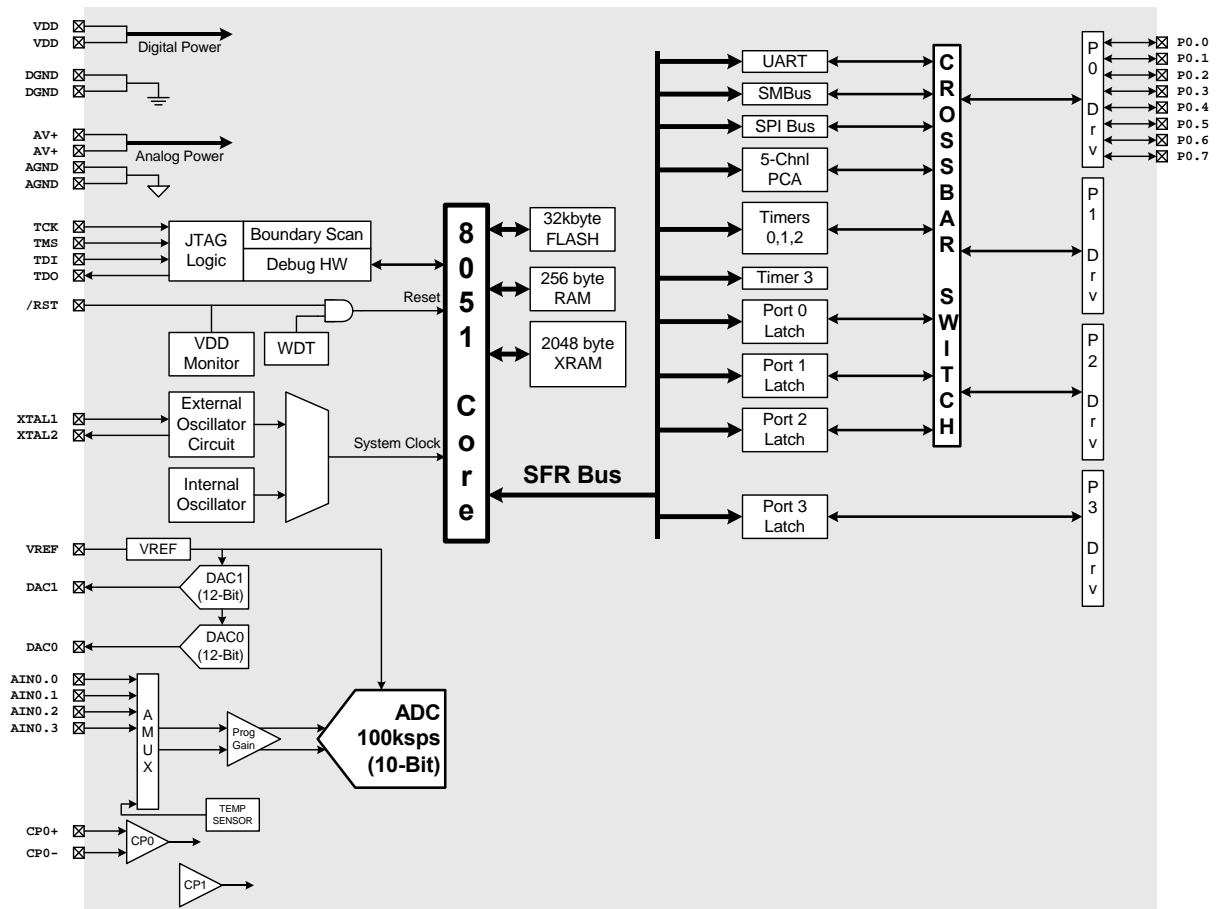
- Typical operating current: 12.5 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 32-pin LQFP (lead-free package)

### Ordering Part Number

- C8051F017-GQ



### Analog Peripherals

#### 10-Bit ADC

- ±1 LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- Data-dependent windowed interrupt generator
- Built-in temperature sensor (±3 °C)

#### Two Comparators

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 1280 bytes data RAM
- 16 kB Flash; in system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.8 to 3.6 V

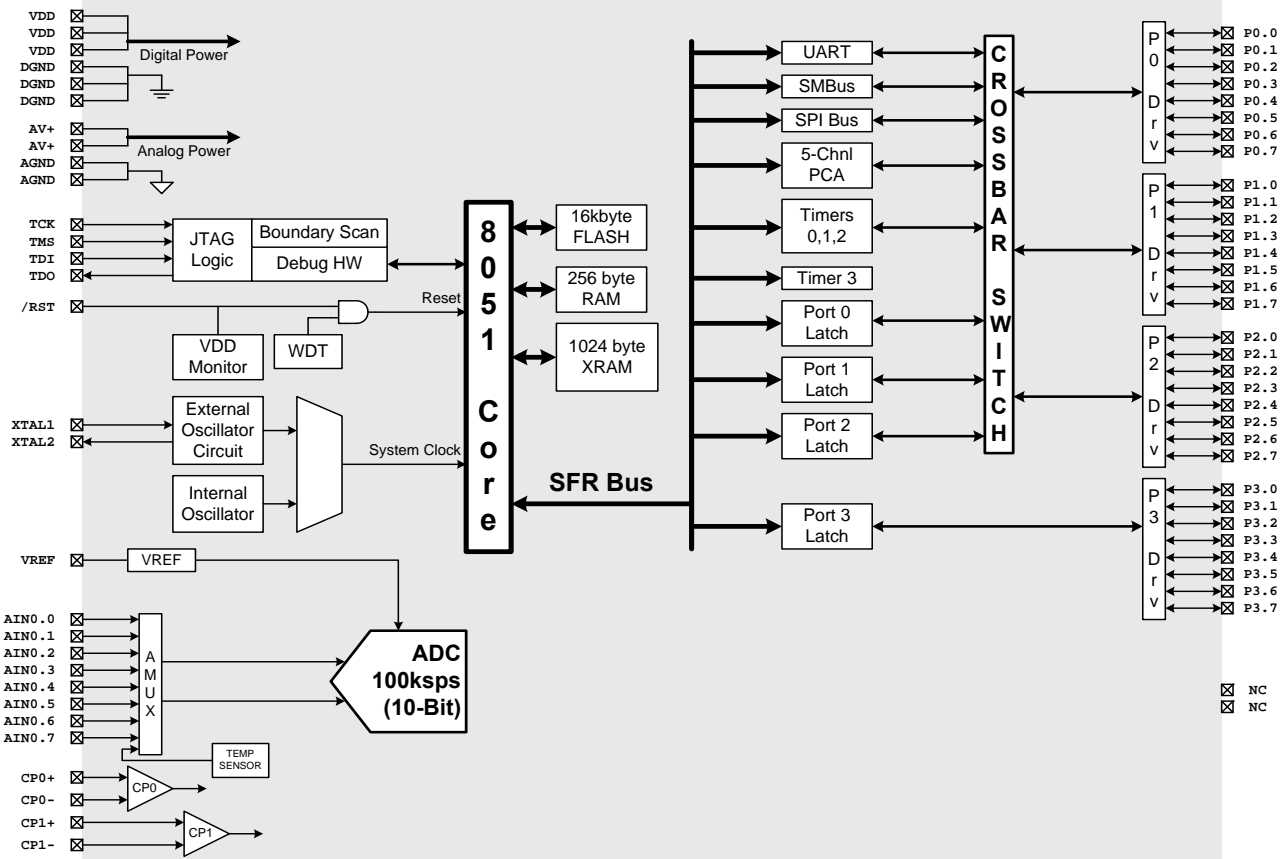
- Typical operating current: 12.5 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F018-GQ



**Analog Peripherals**

**10-Bit ADC**

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

**Two Comparators**

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

**Internal Voltage Reference**

**V<sub>DD</sub> Monitor/Brown-out Detector**

**On-Chip JTAG Debug & Boundary Scan**

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

**High-Speed 8051  $\mu$ C Core**

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

**Memory**

- 1280 bytes data RAM
- 16 kB Flash; in system programmable in 512-byte sectors (512 bytes are reserved)

**Digital Peripherals**

- 16 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

**Clock Sources**

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

**Supply Voltage: 2.8 to 3.6 V**

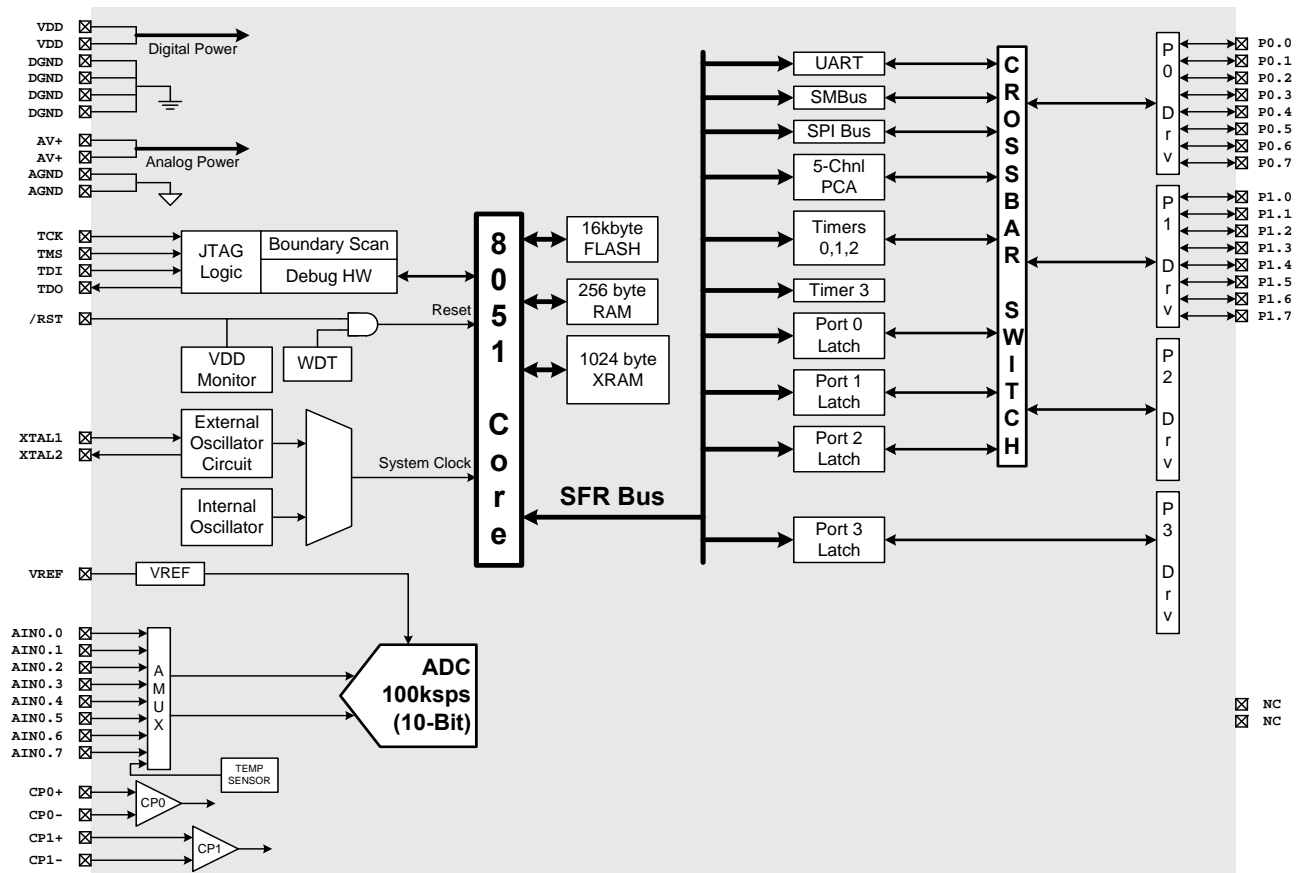
- Typical operating current: 12.5 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

**Package**

- 48-pin TQFP (lead-free package)

**Ordering Part Number**

- C8051F019-GQ



### Analog Peripherals

#### 12-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### 8-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksps
- 8 external inputs
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

Temperature Range: **-40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- 22 vectored interrupt sources

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 64 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with 5 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using Timer 3 or PCA

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

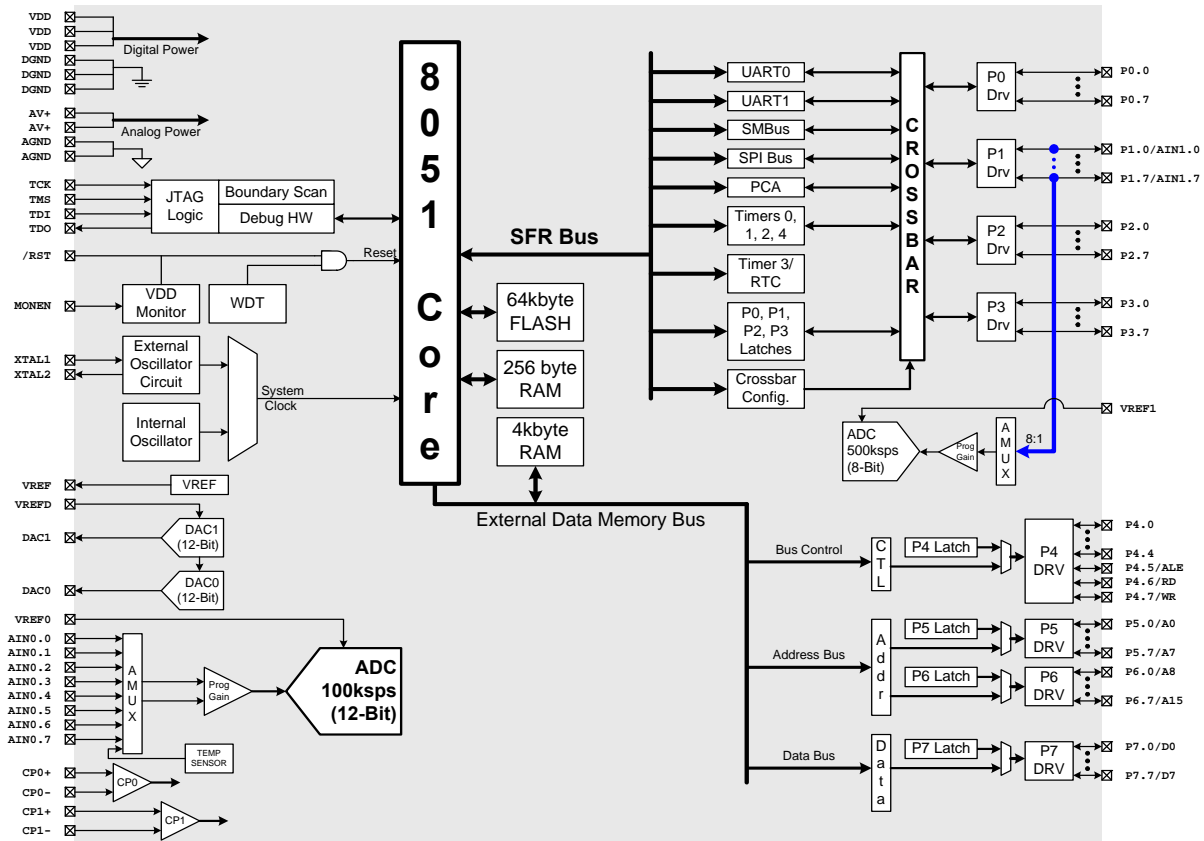
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F020-GQ





### Analog Peripherals

#### 12-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### 8-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksp/s
- 8 external inputs
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

Temperature Range: **-40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- 22 vectored interrupt sources

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with 5 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using Timer 3 or PCA

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

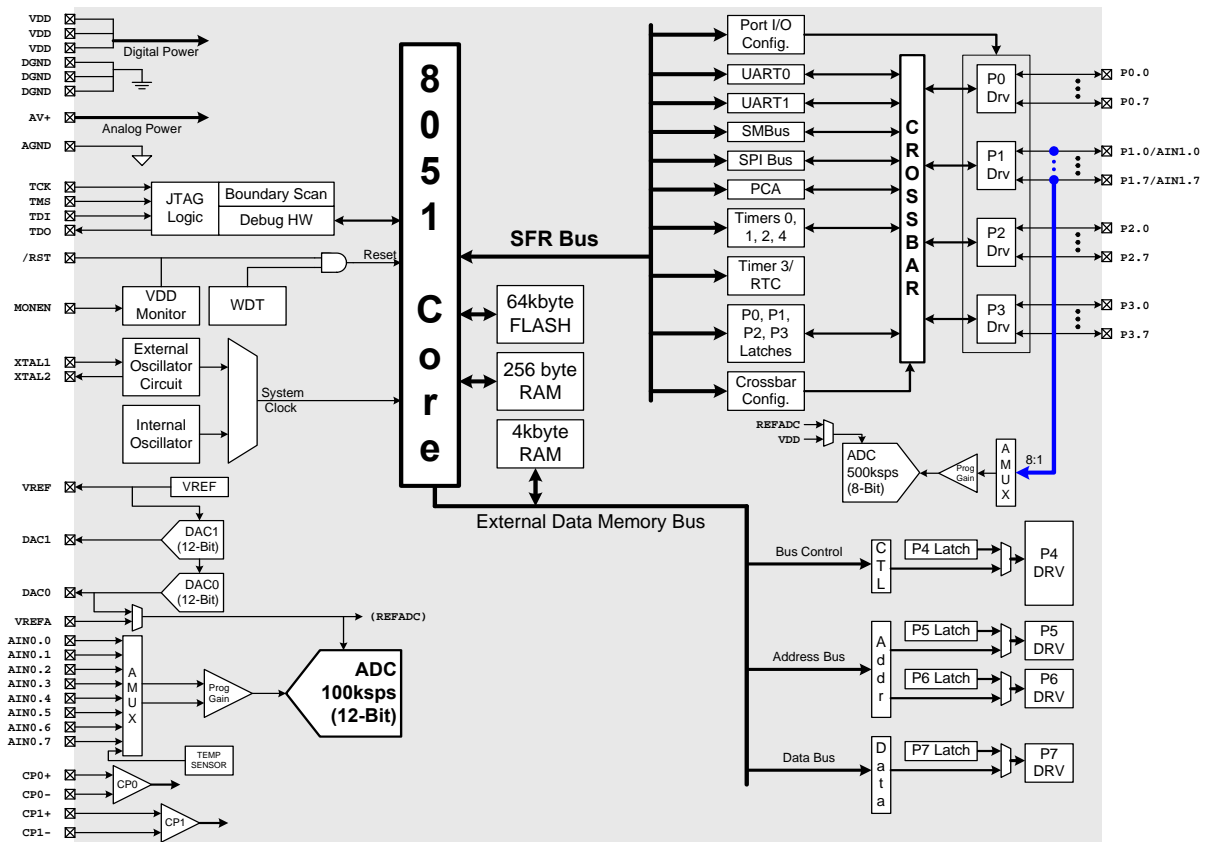
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F021-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### 8-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksp/s
- 8 external inputs
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

Temperature Range: **-40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- 22 vectored interrupt sources

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 64 port I/O; all are 5 V tolerant
- Hardware SMBus™ (<sup>12</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with 5 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using Timer 3 or PCA

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

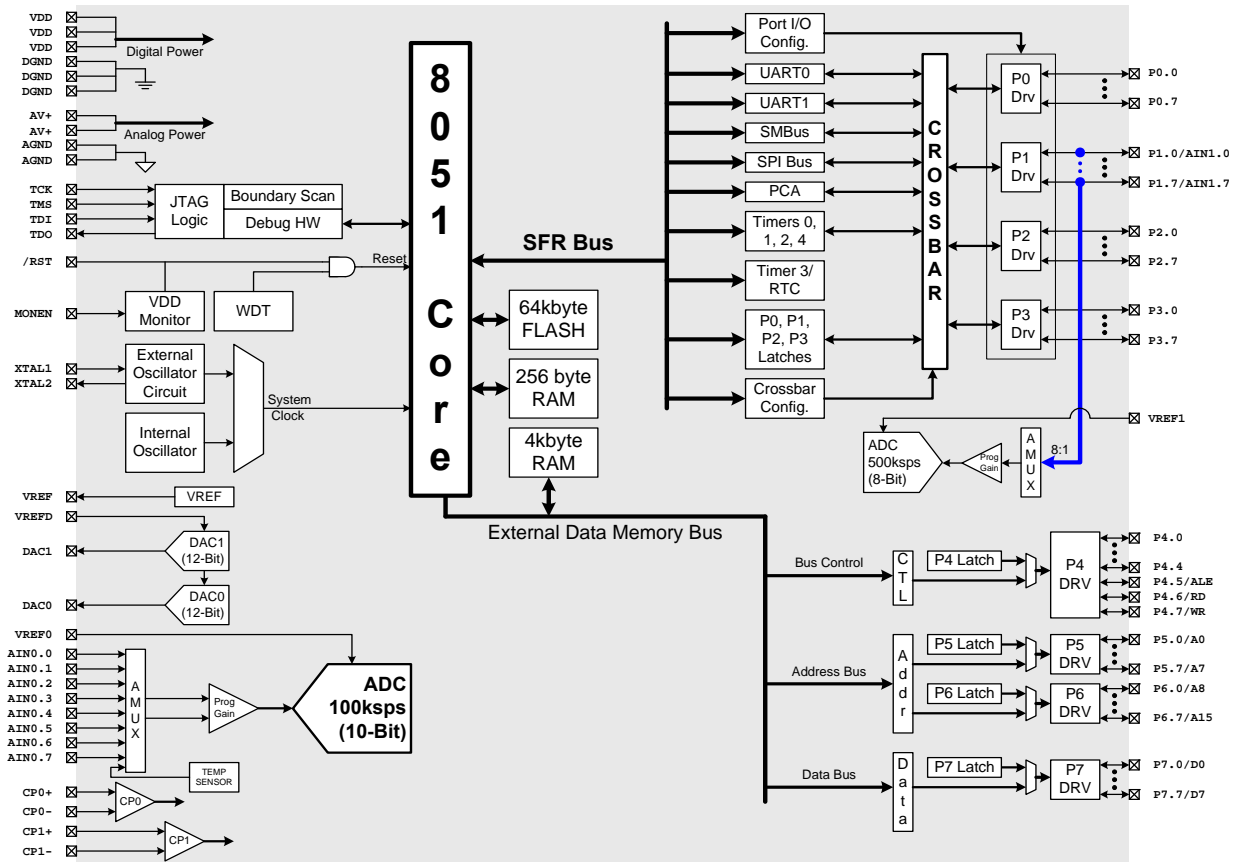
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F022-GQ



**Analog Peripherals**

**10-Bit ADC**

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

**8-Bit ADC**

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksps
- 8 external inputs
- Programmable amplifier gain: 4, 2, 1, 0.5

**Two 12-Bit DACs**

- Can synchronize outputs to timers for jitter-free waveform generation

**Two Comparators**

**Internal Voltage Reference**

**V<sub>DD</sub> Monitor/Brown-out Detector**

**On-Chip JTAG Debug & Boundary Scan**

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

**High-Speed 8051  $\mu$ C Core**

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- 22 vectored interrupt sources

**Memory**

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

**Digital Peripherals**

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with 5 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using Timer 3 or PCA

**Clock Sources**

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

**Supply Voltage: 2.7 to 3.6 V**

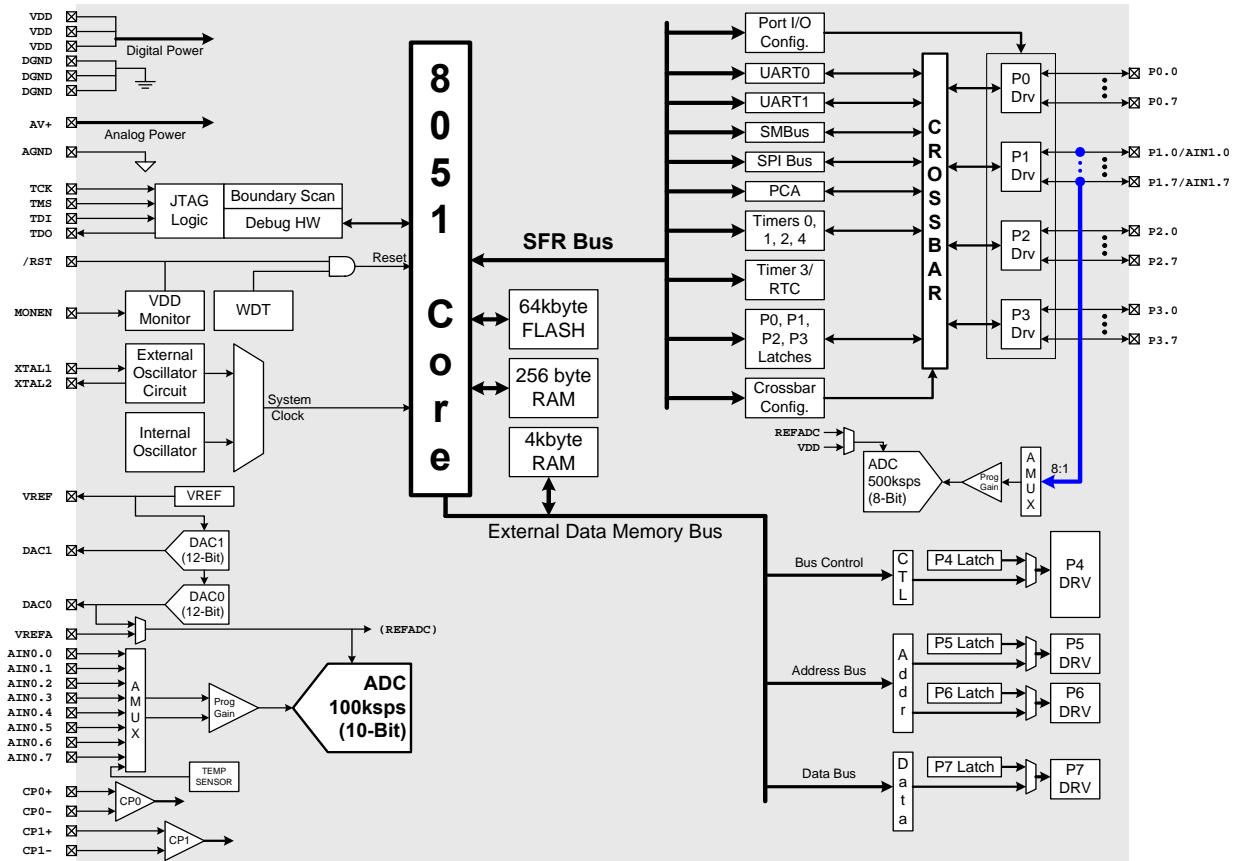
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

**Package**

- 64-pin TQFP (lead-free package)

**Ordering Part Number**

- C8051F023-GQ



### Analog Peripherals

#### 12-Bit ADC

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 100 ksp/s
- 13 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### High-Voltage Differential Amplifier

- 60 V common mode input range
- Offset adjust from -60 to +60 V
- 16 gain settings from 0.05 to 16

#### 8-Bit ADC

- Programmable throughput up to 500 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

#### Three Comparators

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor, program trace memory
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

### CAN Bus 2.0B

- 32 message objects
- "Mailbox" implementation only interrupts CPU when needed

### Digital Peripherals

- 64 port I/O; all are 5 V tolerant
- Hardware SMBus™ ( $I^2C$ ™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- Internal programmable 2% oscillator: up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

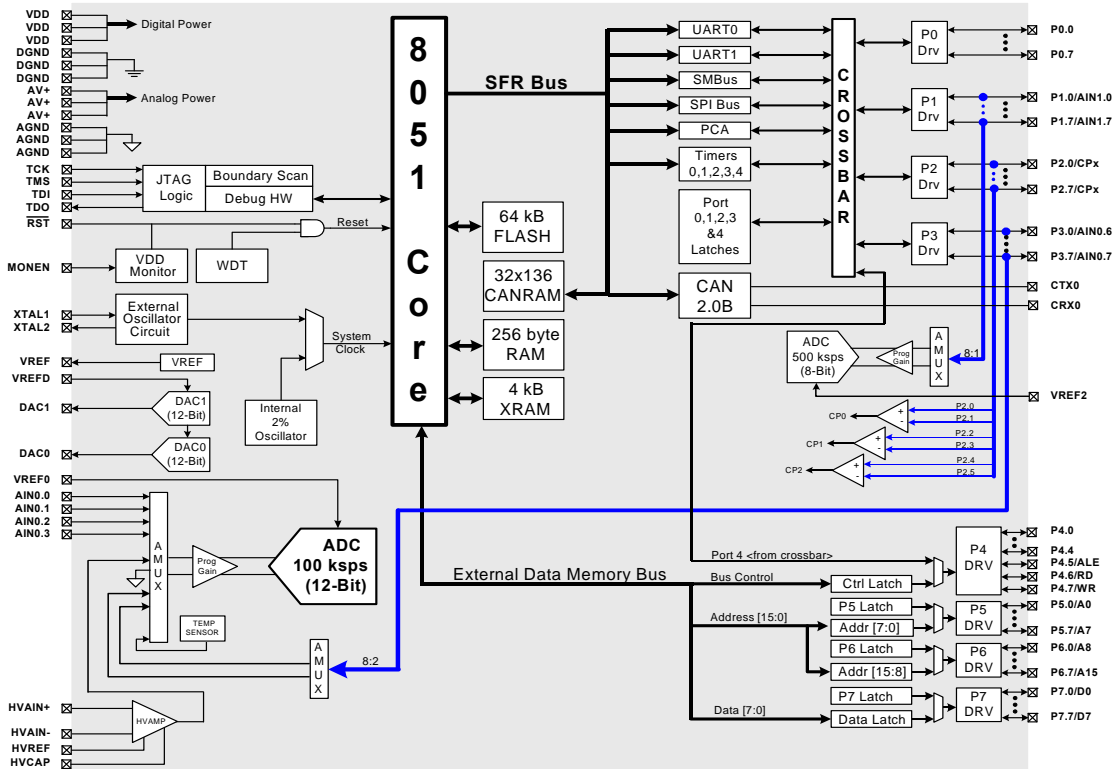
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

C8051F040-GQ



### Analog Peripherals

#### 12-Bit ADC

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 100 ksp/s
- 13 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### High-Voltage Differential Amplifier

- 60 V common mode input range
- Offset adjust from -60 to +60 V
- 16 gain settings from 0.05 to 16

#### 8-Bit ADC

- Programmable throughput up to 500 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

#### Three Comparators

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor, program trace memory
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

#### Temperature Range: -40 to +85 °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

### CAN Bus 2.0B

- 32 message objects
- "Mailbox" implementation only interrupts CPU when needed

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ ( $I^2C$ ™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- Internal programmable 2% oscillator: up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

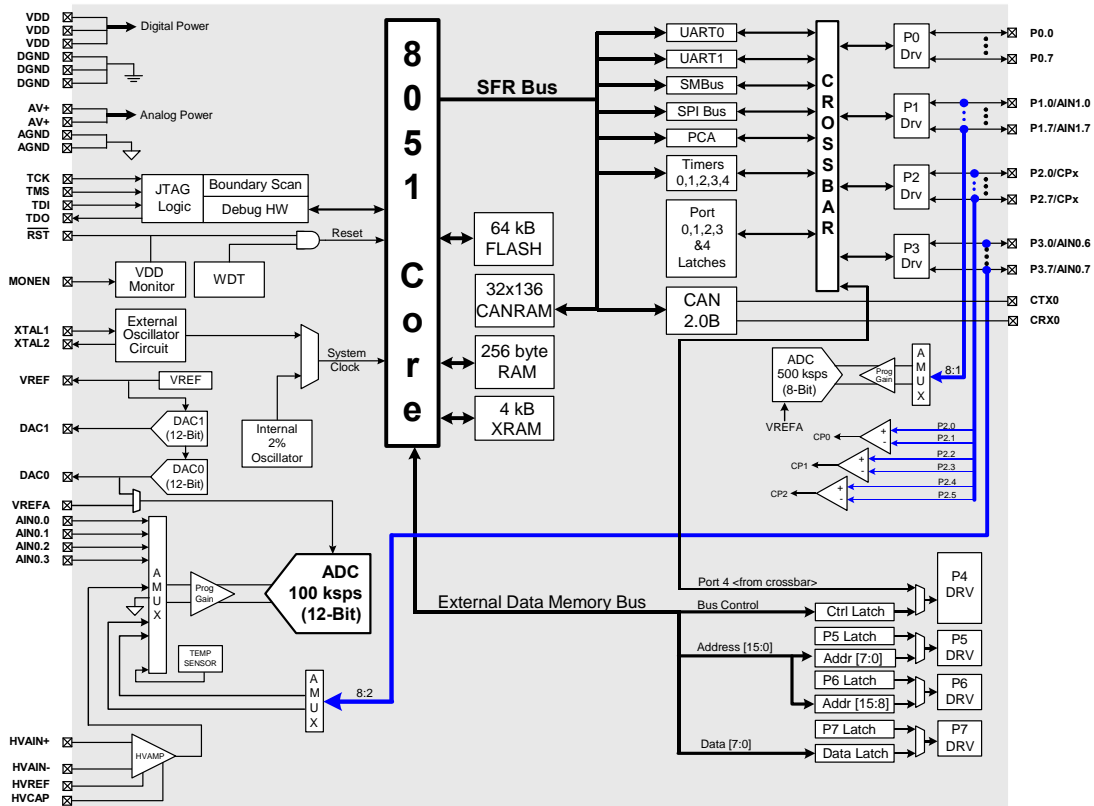
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown mode

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F041-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 100 ksps
- 13 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### High-Voltage Differential Amplifier

- 60 V common mode input range
- Offset adjust from -60 to +60 V
- 16 gain settings from 0.05 to 16

#### 8-Bit ADC

- Programmable throughput up to 500 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

#### Three Comparators

#### Internal Voltage Reference

#### Precision V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor, program trace memory
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

### CAN Bus 2.0B

- 32 message objects
- "Mailbox" implementation only interrupts CPU when needed

### Digital Peripherals

- 64 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- Internal programmable 2% oscillator: up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

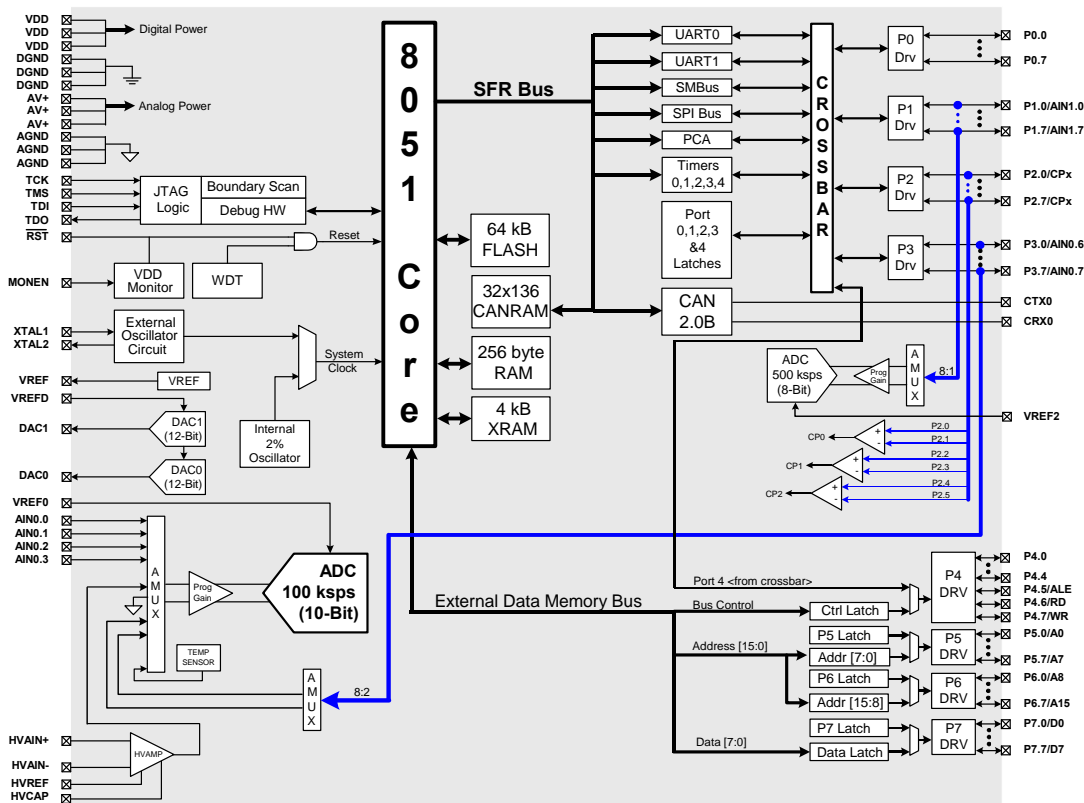
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown mode

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F042-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 100 ksps
- 13 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### High-Voltage Differential Amplifier

- 60 V common mode input range
- Offset adjust from -60 to +60 V
- 16 gain settings from 0.05 to 16

#### 8-Bit ADC

- Programmable throughput up to 500 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

#### Three Comparators

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor, program trace memory
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

#### Temperature Range: -40 to +85 °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

### CAN Bus 2.0B

- 32 message objects
- "Mailbox" implementation only interrupts CPU when needed

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ ( $I^2C$ ™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- Internal programmable 2% oscillator: up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

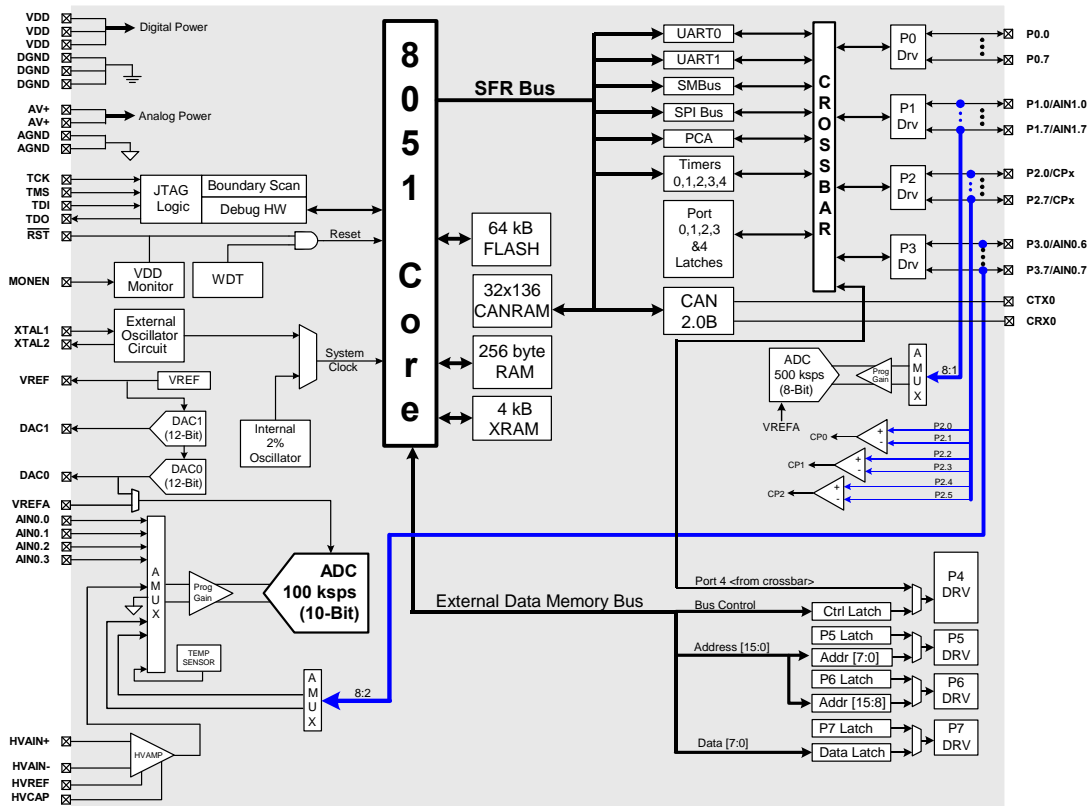
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown mode

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F043-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 100 ksp/s
- 13 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### High-Voltage Differential Amplifier

- 60 V common mode input range
- Offset adjust from -60 to +60 V
- 16 gain settings from 0.05 to 16

#### Three Comparators

#### Internal Voltage Reference

#### Precision V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor, program trace memory
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

### CAN Bus 2.0B

- 32 message objects
- "Mailbox" implementation only interrupts CPU when needed

### Digital Peripherals

- 64 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- Internal programmable 2% oscillator: up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

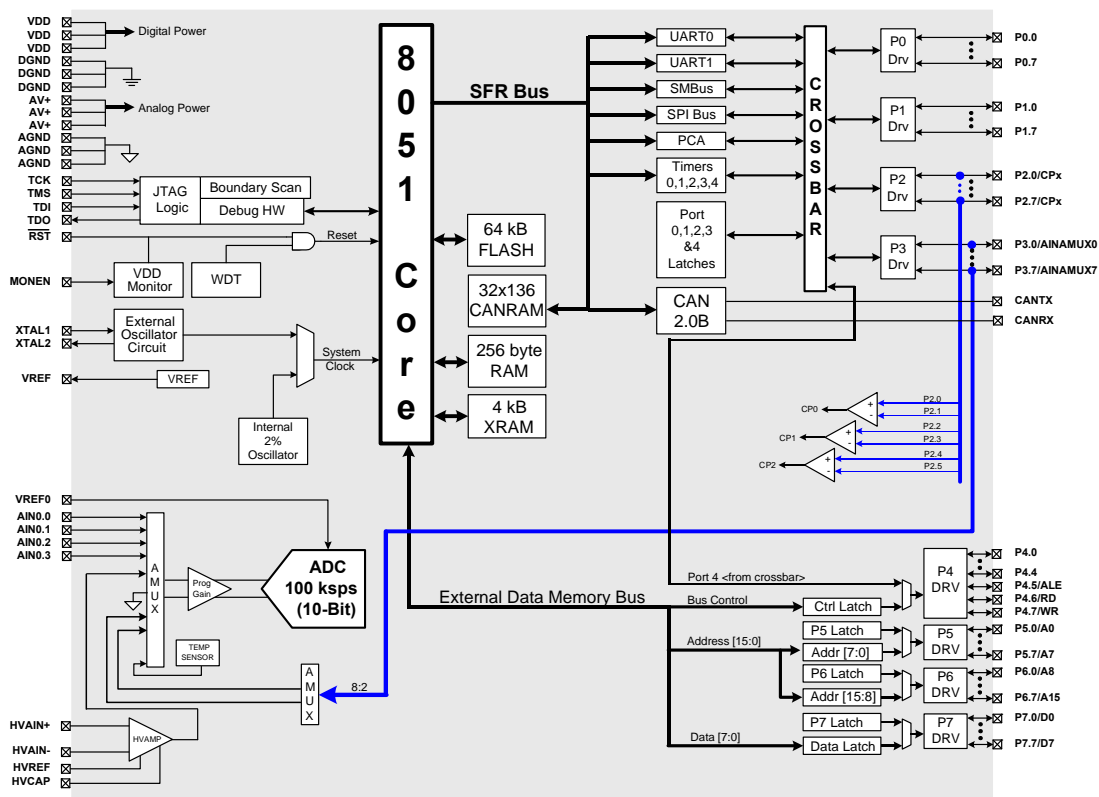
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F044-GQ





### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 100 ksps
- 13 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### High-Voltage Differential Amplifier

- 60 V common mode input range
- Offset adjust from -60 to +60 V
- 16 gain settings from 0.05 to 16

#### Three Comparators

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor, program trace memory
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

### CAN Bus 2.0B

- 32 message objects
- "Mailbox" implementation only interrupts CPU when needed

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- Internal programmable 2% oscillator: up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

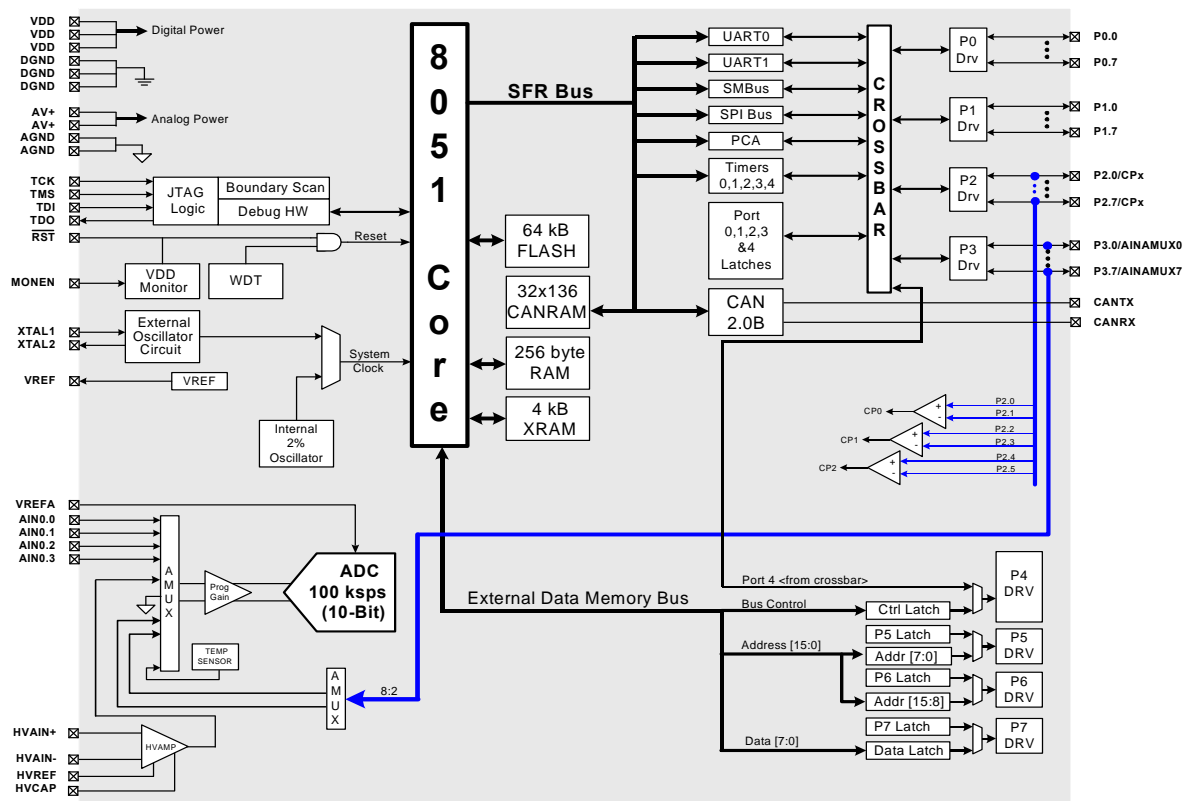
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown mode

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F045-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 100 ksp/s
- 13 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### High-Voltage Differential Amplifier

- 60 V common mode input range
- Offset adjust from -60 to +60 V
- 16 gain settings from 0.05 to 16

#### Three Comparators

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor, program trace memory
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

### CAN Bus 2.0B

- 32 message objects
- "Mailbox" implementation only interrupts CPU when needed

### Digital Peripherals

- 64 port I/O; all are 5 V tolerant
- Hardware SMBus™ ( $I^2C$ ™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- Internal programmable 2% oscillator: up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

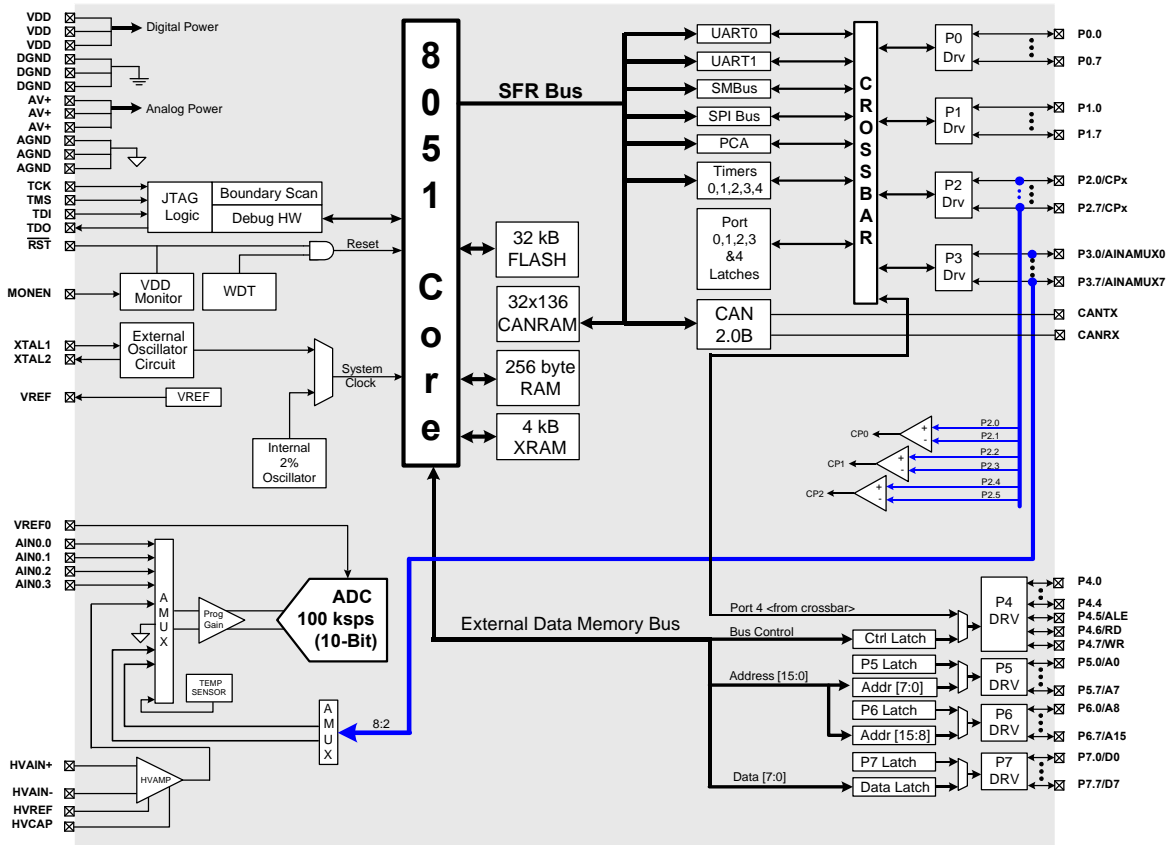
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown mode

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F046-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 100 ksps
- 13 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### High-Voltage Differential Amplifier

- 60 V common mode input range
- Offset adjust from -60 to +60 V
- 16 gain settings from 0.05 to 16

#### Three Comparators

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor, program trace memory
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

### CAN Bus 2.0B

- 32 message objects
- "Mailbox" implementation only interrupts CPU when needed

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- Internal programmable 2% oscillator: up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

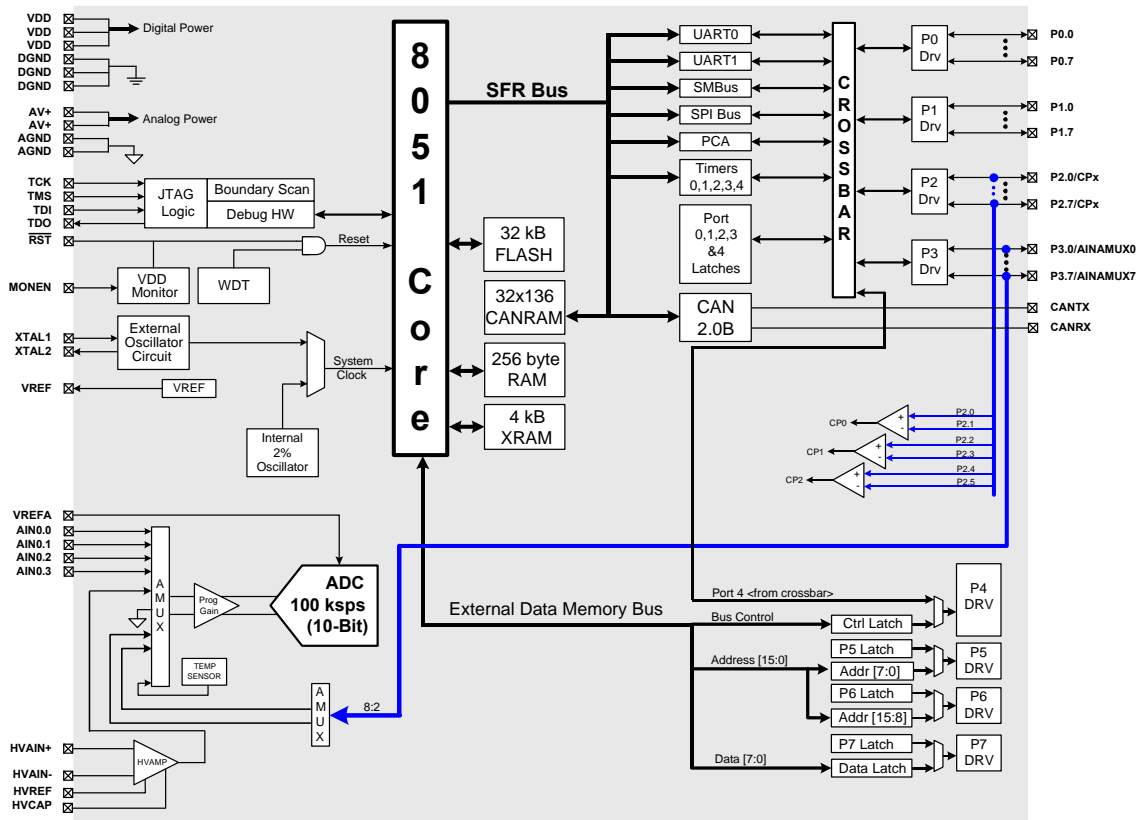
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown mode

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F047-GQ



### Analog Peripherals

#### Two 16-Bit ADCs

- $\pm 0.75$  LSB INL; guaranteed no missing codes
- Programmable throughput up to 1 Msps (each ADC)
- Configurable as two single-ended or one differential ADC
- DMA to XRAM or external memory interface
- Data-dependent windowed interrupt generator

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- 8 external inputs
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Three Comparators

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### CAN Bus 2.0B

- 32 message objects
- "Mailbox" implementation only interrupts CPU when needed

### Digital Peripherals

- 59 port I/O; all are 5 V tolerant
- Hardware SMBus™ ( $I^2C$ ™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timers or PCA

### Clock Sources

- Internal programmable 2% oscillator: up to 24.5 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

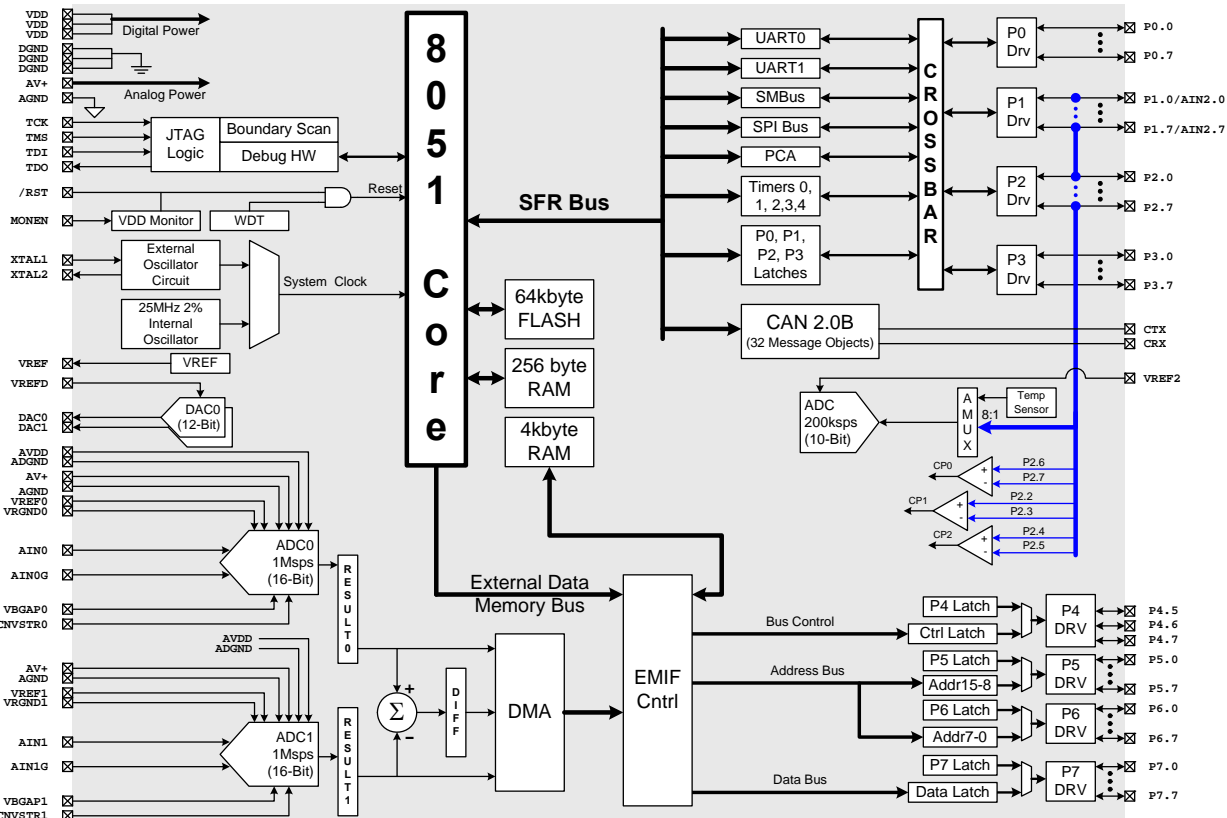
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F060-GQ



### Analog Peripherals

#### Two 16-Bit ADCs

- $\pm 0.75$  LSB INL; guaranteed no missing codes
- Programmable throughput up to 1 Msps (each ADC)
- Configurable as two single-ended or one differential ADC
- DMA to XRAM or external memory interface
- Data-dependent windowed interrupt generator

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- 8 external inputs
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Three Comparators

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### CAN Bus 2.0B

- 32 message objects
- "Mailbox" implementation only interrupts CPU when needed

### Digital Peripherals

- 24 port I/O; all are 5 V tolerant
- Hardware SMBus™ ( $I^2C$ ™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timers or PCA

### Clock Sources

- Internal programmable 2% oscillator: up to 24.5 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

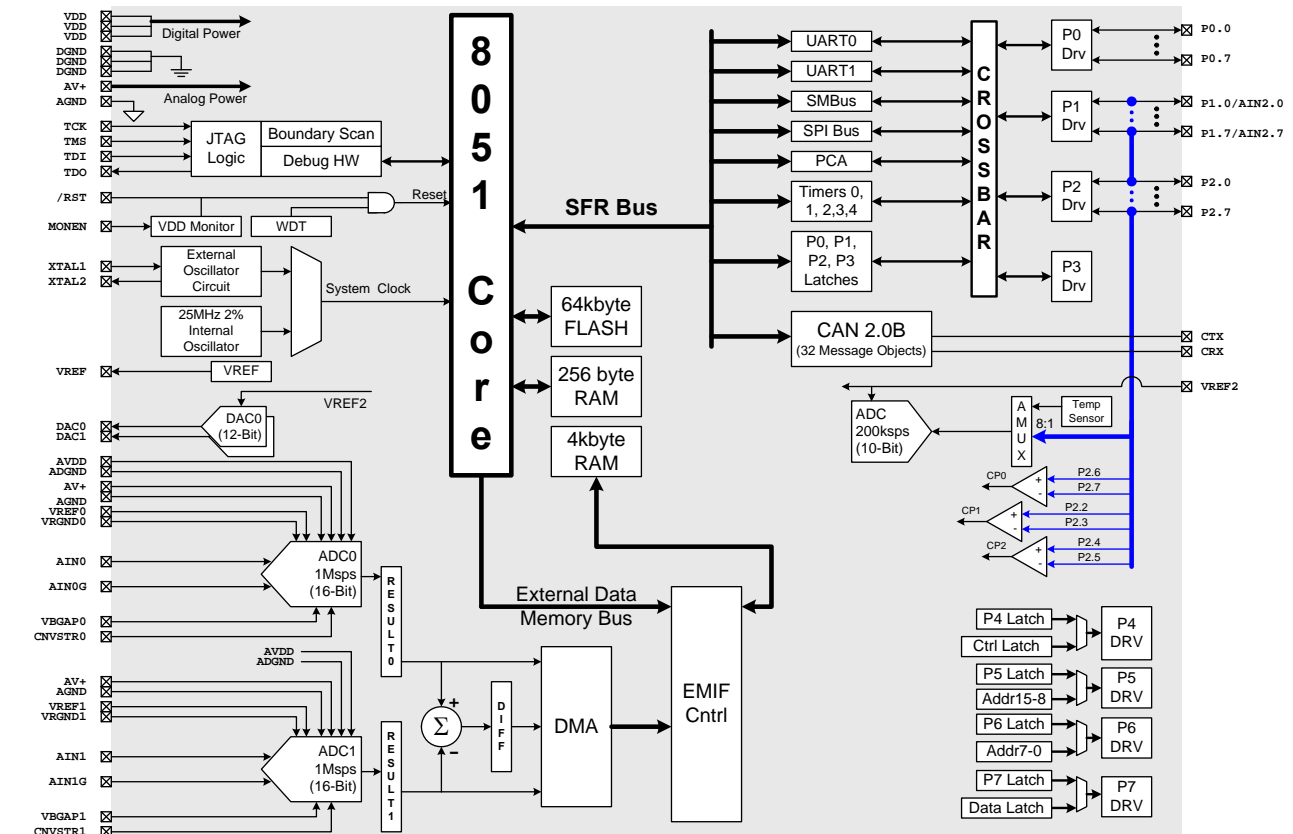
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F061-GQ



### Analog Peripherals

#### Two 16-Bit ADCs

- $\pm 1.5$  LSB INL; guaranteed no missing codes
- Programmable throughput up to 1 Msps (each ADC)
- Configurable as two single-ended or one differential ADC
- DMA to XRAM or external memory interface
- Data-dependent windowed interrupt generator

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- 8 external inputs
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Three Comparators

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### CAN Bus 2.0B

- 32 message objects
- "Mailbox" implementation only interrupts CPU when needed

### Digital Peripherals

- 24 port I/O; all are 5 V tolerant
- Hardware SMBus™ ( $I^2C$ ™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timers or PCA

### Clock Sources

- Internal programmable 2% oscillator: up to 24.5 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

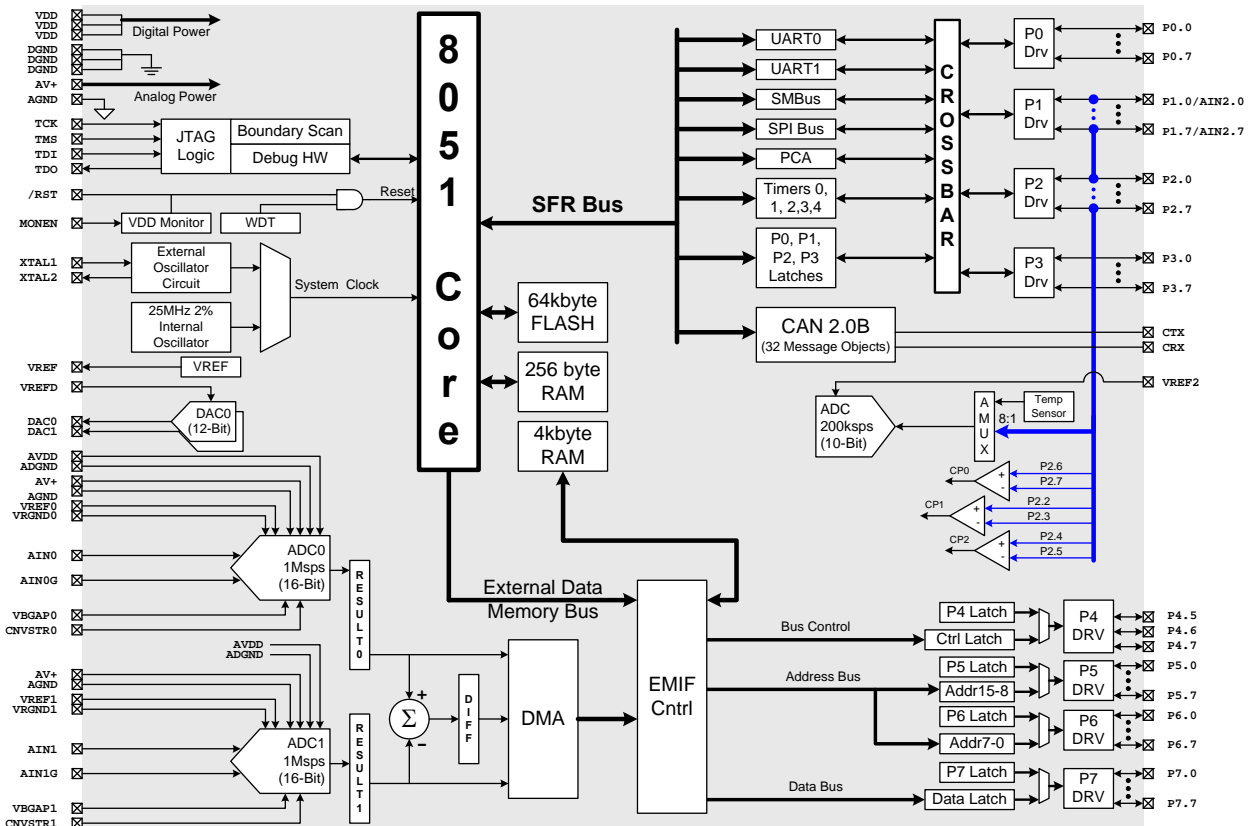
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F062-GQ



### Analog Peripherals

#### Two 16-Bit ADCs

- $\pm 1.5$  LSB INL; guaranteed no missing codes
- Programmable throughput up to 1 Msps (each ADC)
- Configurable as two single-ended or one differential ADC
- DMA to XRAM or external memory interface
- Data-dependent windowed interrupt generator

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- 8 external inputs
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Three Comparators

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### CAN Bus 2.0B

- 32 message objects
- "Mailbox" implementation only interrupts CPU when needed

### Digital Peripherals

- 24 port I/O; all are 5 V tolerant
- Hardware SMBus™ ( $I^2C$ ™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter array with 6 capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timers or PCA

### Clock Sources

- Internal programmable 2% oscillator: up to 24.5 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

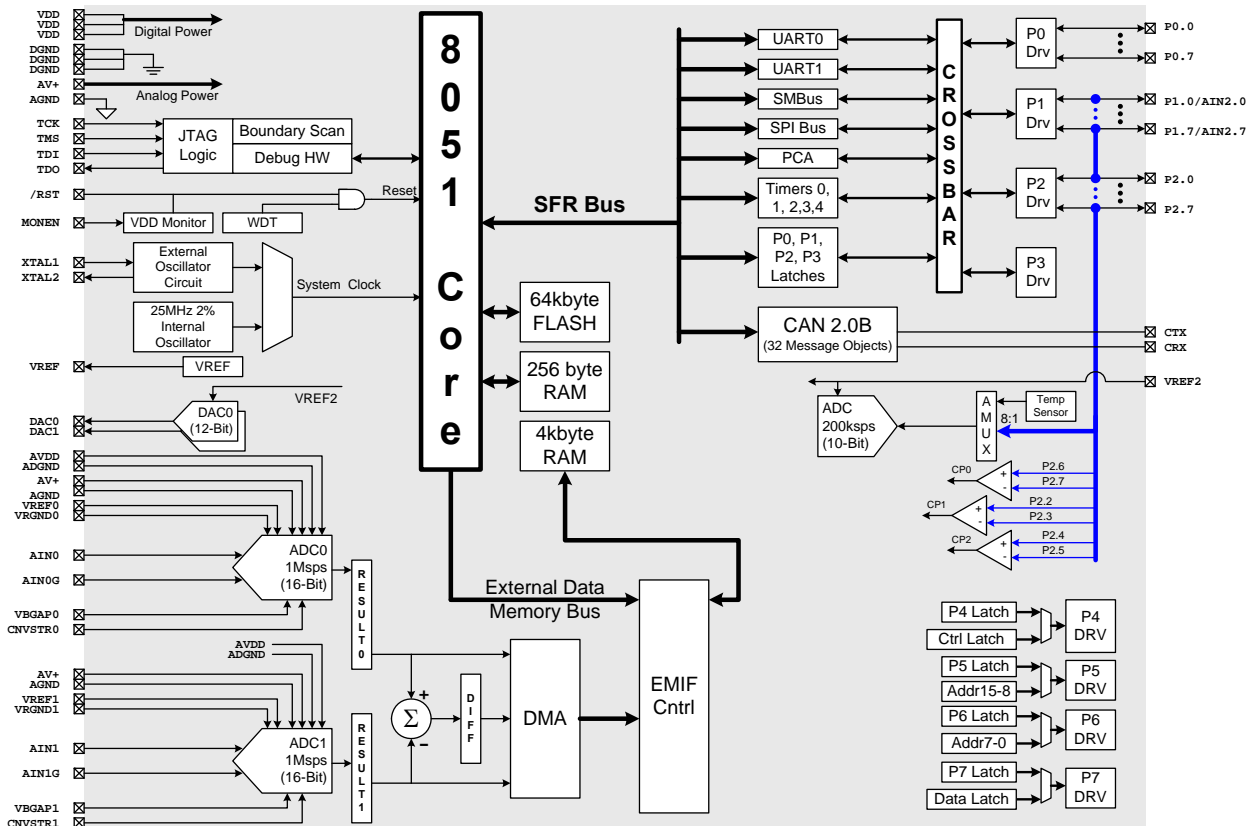
- Typical operating current: 10 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F063-GQ



### Analog Peripherals

#### Two 16-Bit ADCs

- $\pm 0.75$  LSB INL; no missing codes
- Programmable throughput up to 1 Msps (each ADC)
- 1 external input each; programmable as two single-ended or one differential ADC
- DMA to XRAM or external memory interface
- Data-dependent windowed interrupt generator

#### Three Comparators

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

Temperature Range:  $-40$  to  $+85$  °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 59 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timers or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

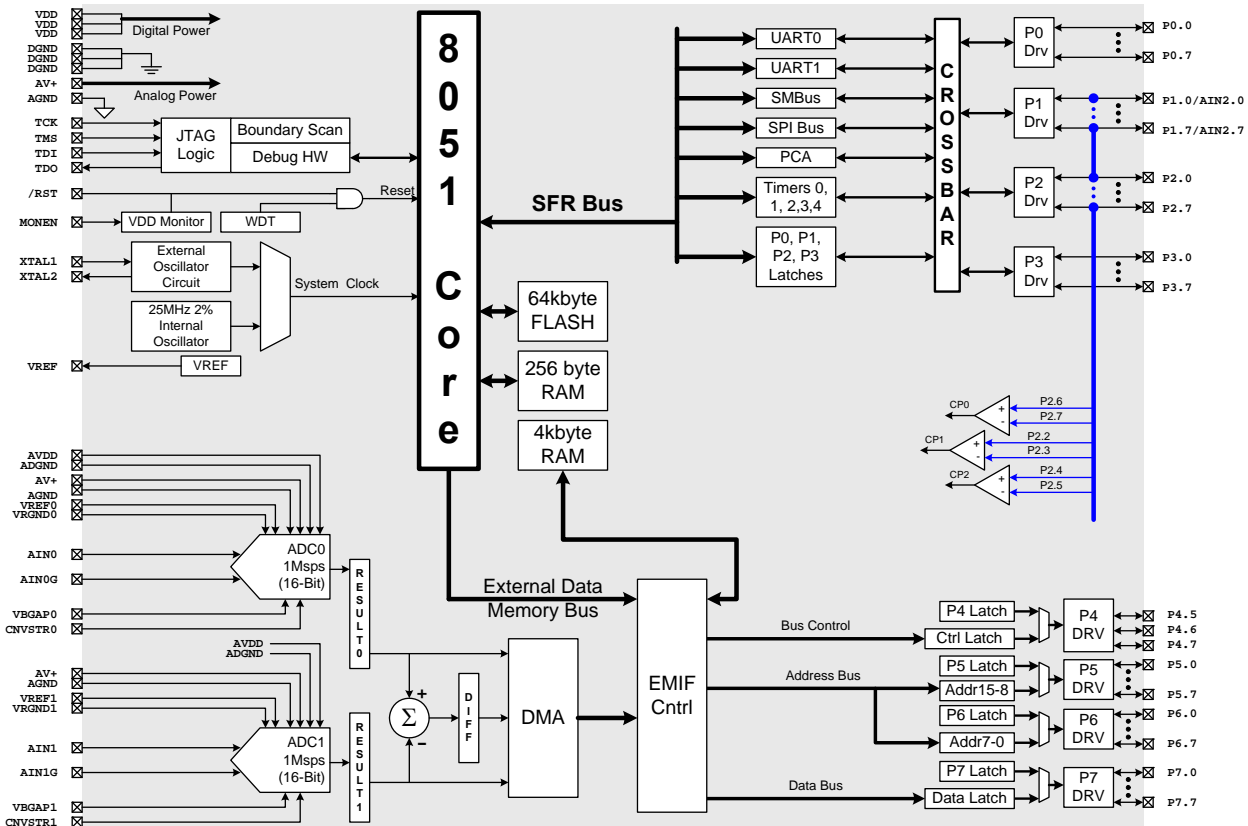
- Typical operating current: 18 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F064-GQ





### Analog Peripherals

#### Two 16-Bit ADCs

- $\pm 0.75$  LSB INL; no missing codes
- Programmable throughput up to 1 Msps (each ADC)
- 1 external input each; programmable as two single-ended or one differential ADC
- DMA to XRAM or external memory interface
- Data-dependent windowed interrupt generator

#### Three Comparators

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range:  $-40$  to  $+85$  °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)

### Digital Peripherals

- 24 port I/O; all are 5 V tolerant
- Hardware SMBus™ ( $I^2C$ ™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timers or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

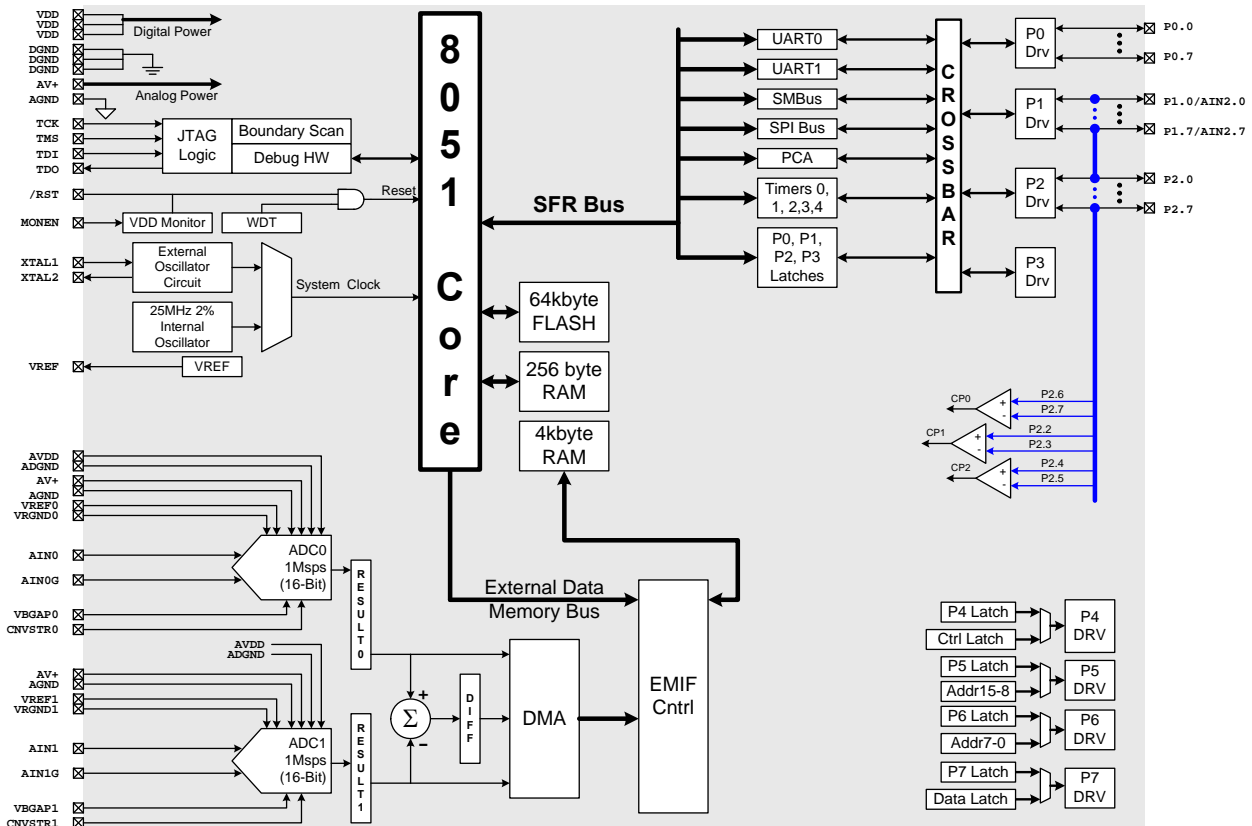
- Typical operating current: 18 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F065-GQ



### Analog Peripherals

#### Two 16-Bit ADCs

- $\pm 0.75$  LSB INL; no missing codes
- Programmable throughput up to 1 Msps (each ADC)
- 1 external input each; programmable as two single-ended or one differential ADC
- DMA to XRAM or external memory interface
- Data-dependent windowed interrupt generator

#### Three Comparators

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range:  $-40$  to  $+85$  °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 32 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 59 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timers or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

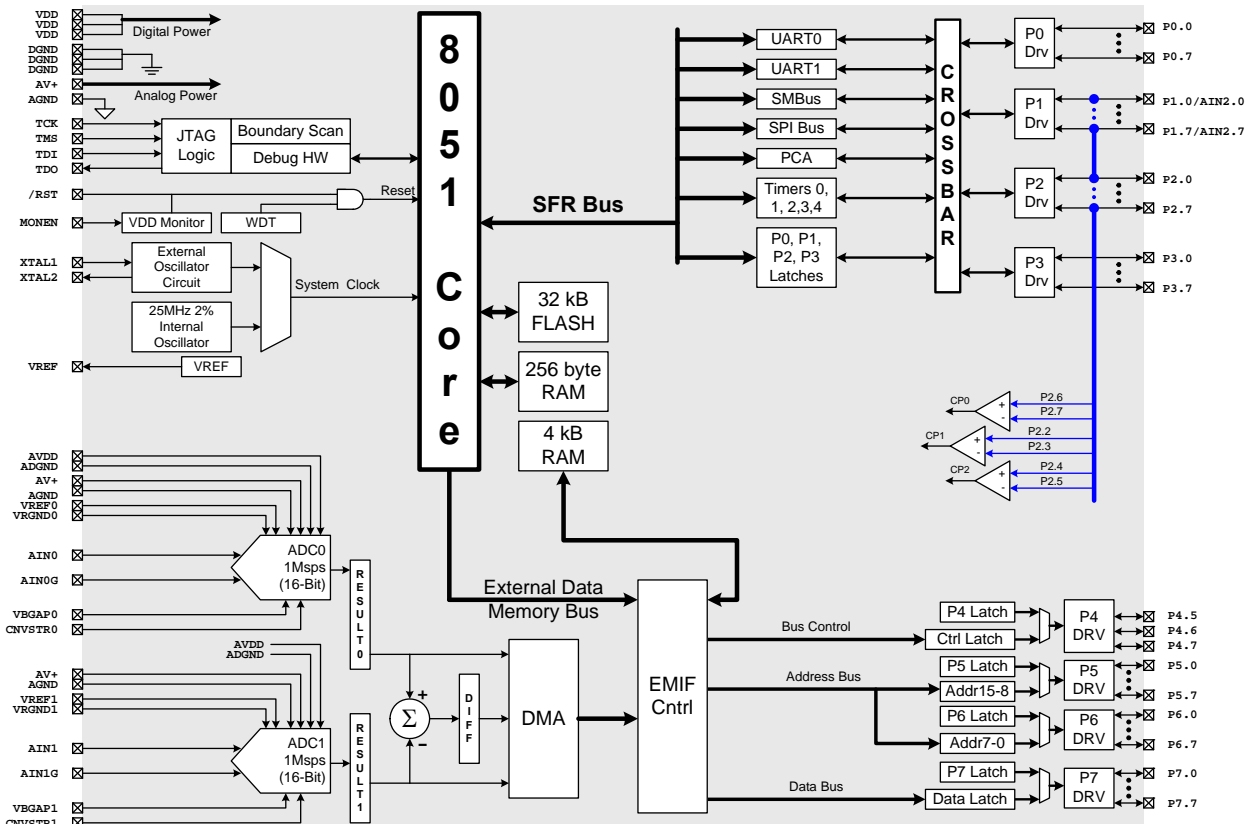
- Typical operating current: 18 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F066-GQ



### Analog Peripherals

#### Two 16-Bit ADCs

- $\pm 0.75$  LSB INL; no missing codes
- Programmable throughput up to 1 Msps (each ADC)
- 1 external input each; programmable as two single-ended or one differential ADC
- DMA to XRAM or external memory interface
- Data-dependent windowed interrupt generator

#### Three Comparators

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

#### Internal Voltage Reference

#### Precision $V_{DD}$ Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

**Temperature Range:  $-40$  to  $+85$  °C**

### High-Speed 8051 $\mu$ C Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM
- 32 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)

### Digital Peripherals

- 24 port I/O; all are 5 V tolerant
- Hardware SMBus™ ( $I^2C$ ™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timers or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

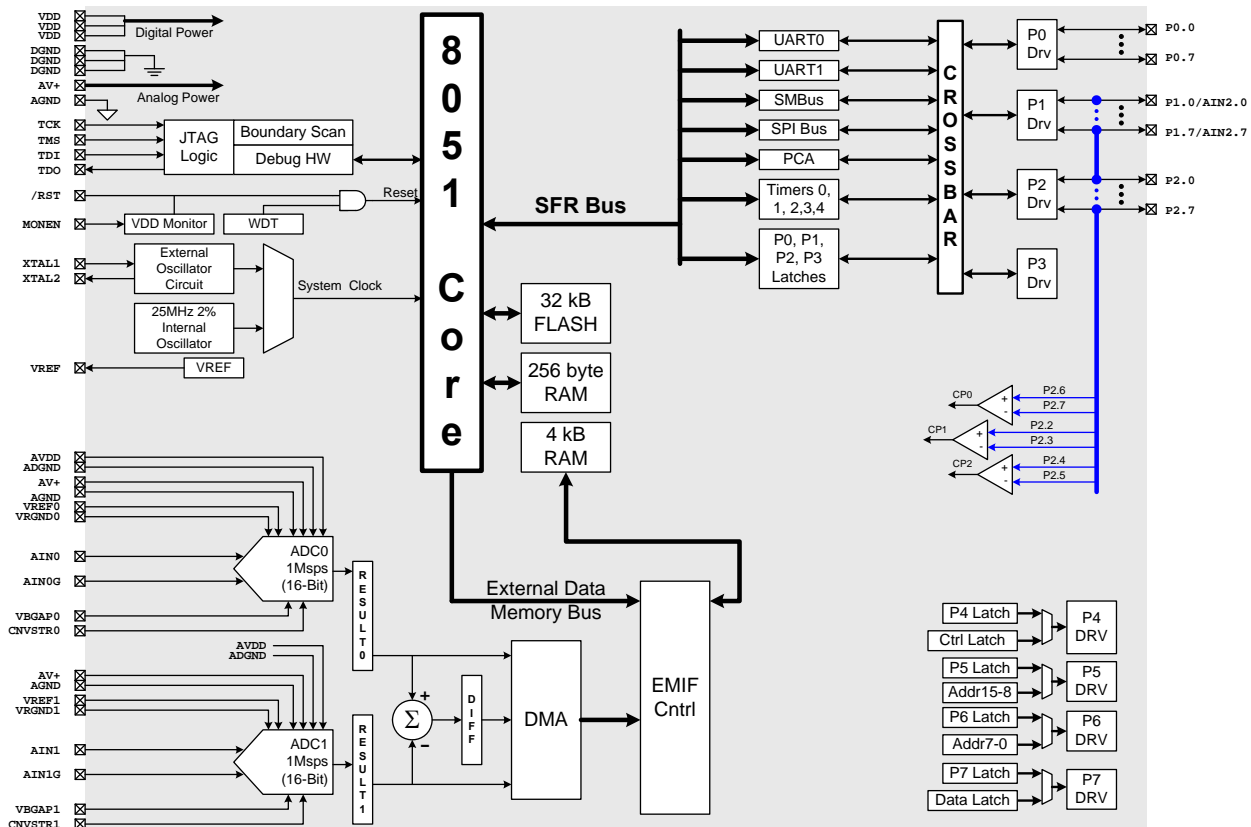
- Typical operating current: 18 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F067-GQ



### Analog Peripherals

#### 12-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### 8-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksp/s
- 8 external inputs
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

Temperature Range:  $-40$  to  $+85$  °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 8448 bytes data RAM
- 128 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 64 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- On-chip programmable PLL: up to 100 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 3.0 to 3.6 V

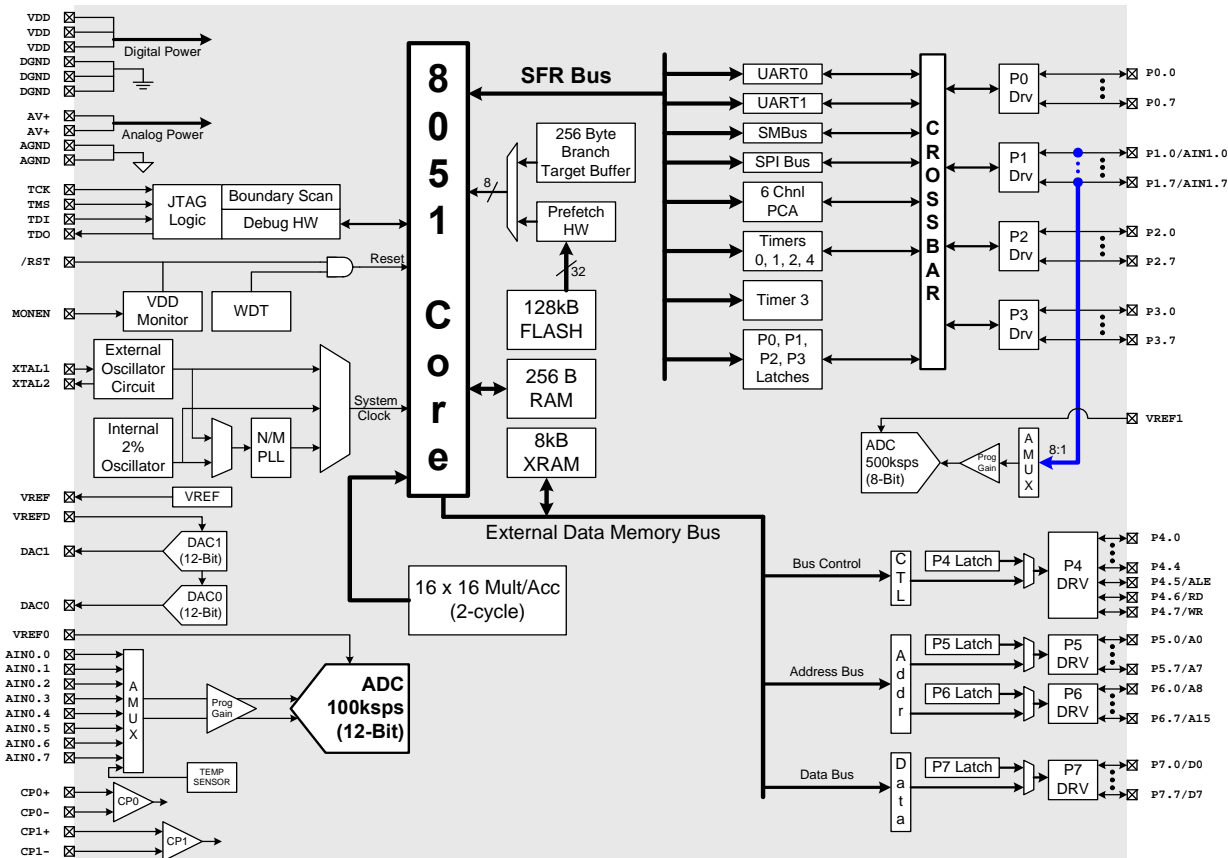
- Typical operating current: 50 mA at 100 MHz
- Typical stop mode current: 0.4  $\mu$ A

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F120-GQ



### Analog Peripherals

#### 12-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### 8-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksp/s
- 8 external inputs
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

Temperature Range:  $-40$  to  $+85$  °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 8448 bytes data RAM
- 128 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ Compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using Timer 3 or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- On-chip programmable PLL: up to 100 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 3.0 to 3.6 V

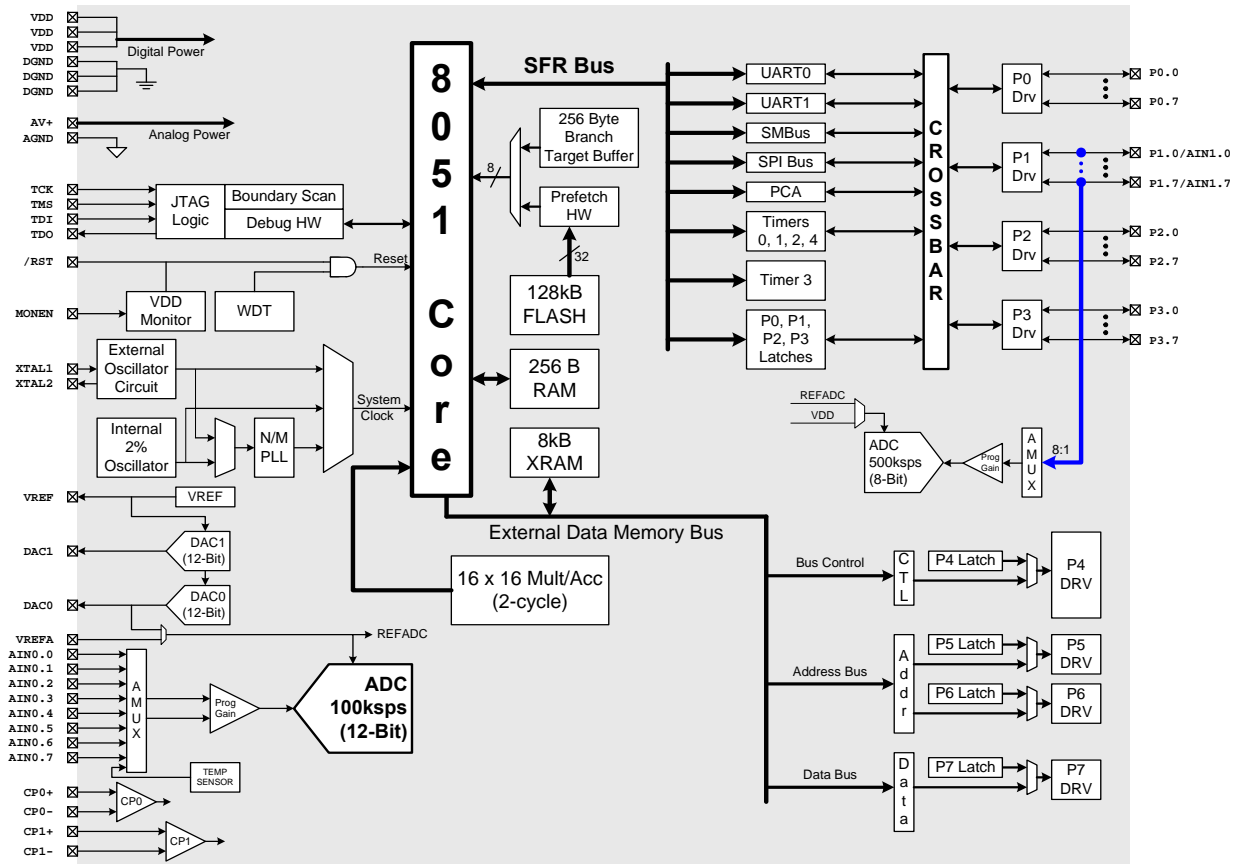
- Typical operating current: 50 mA at 100 MHz
- Typical stop mode current: 0.4  $\mu$ A

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F121-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### 8-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksps
- 8 external inputs
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-Out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

Temperature Range:  $-40$  to  $+85$  °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 8448 bytes data RAM
- 128 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 64 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using Timer 3 or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- On-chip programmable PLL: up to 100 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 3.0 to 3.6 V

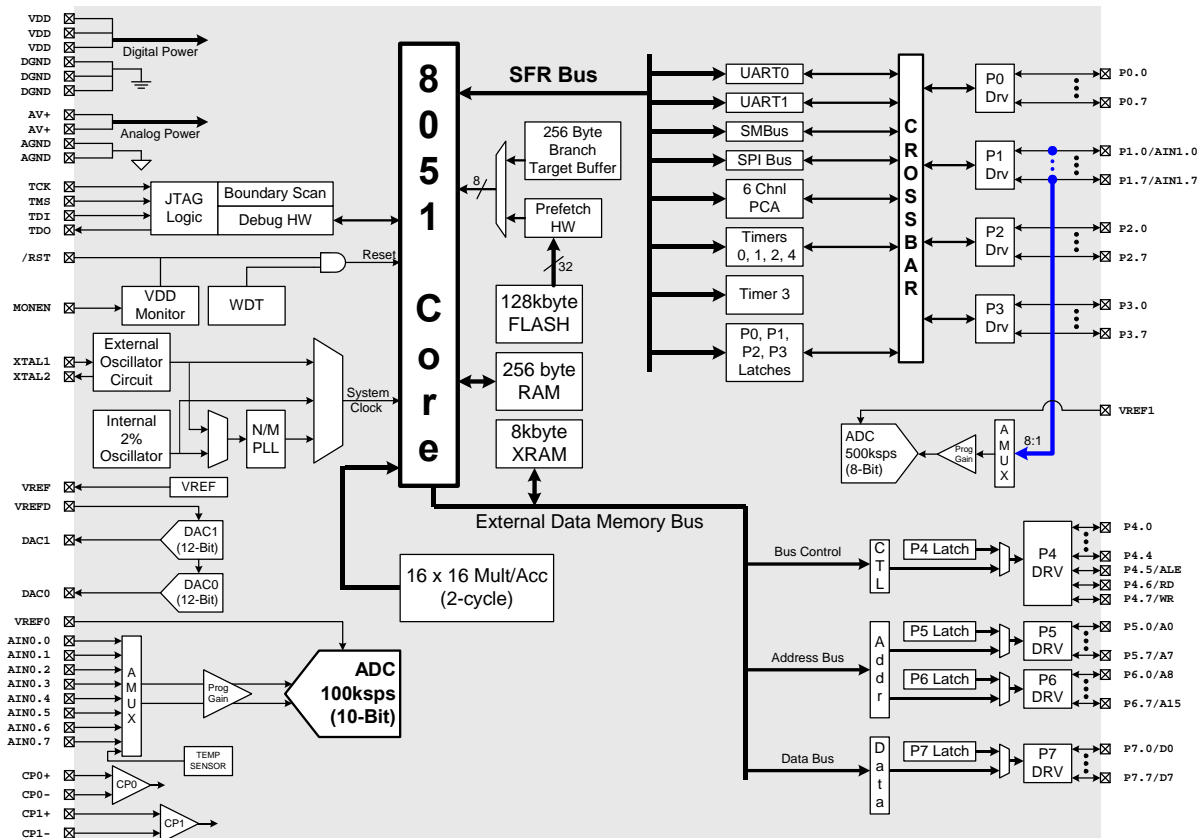
- Typical operating current: 50 mA at 100 MHz
- Typical stop mode current: 0.4  $\mu$ A

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F122-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3^\circ\text{C}$ )

#### 8-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksp/s
- 8 external inputs
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

Temperature Range:  $-40$  to  $+85^\circ\text{C}$

### High-Speed 8051 $\mu\text{C}$ Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 8448 bytes data RAM
- 128 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ Compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using Timer 3 or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- On-chip programmable PLL: up to 100 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 3.0 to 3.6 V

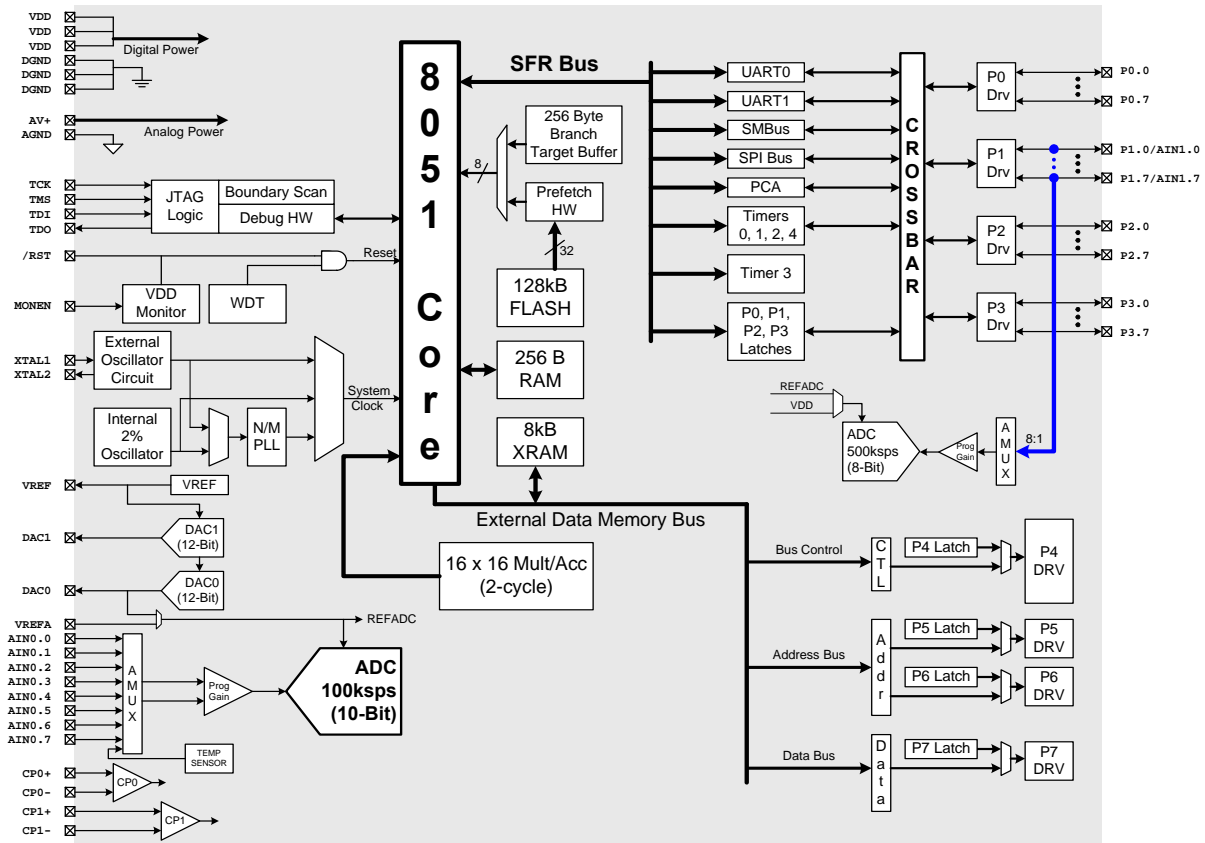
- Typical operating current: 50 mA at 100 MHz
- Typical stop mode current: 0.4  $\mu\text{A}$

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F123-GQ



### Analog Peripherals

#### 12-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### 8-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksp/s
- 8 external inputs
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Real-time instruction trace buffer
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz system clock
- Expanded interrupt handler

### Memory

- 8448 bytes data RAM
- 128 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 64 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using a timer or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- On-chip programmable PLL: up to 50 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

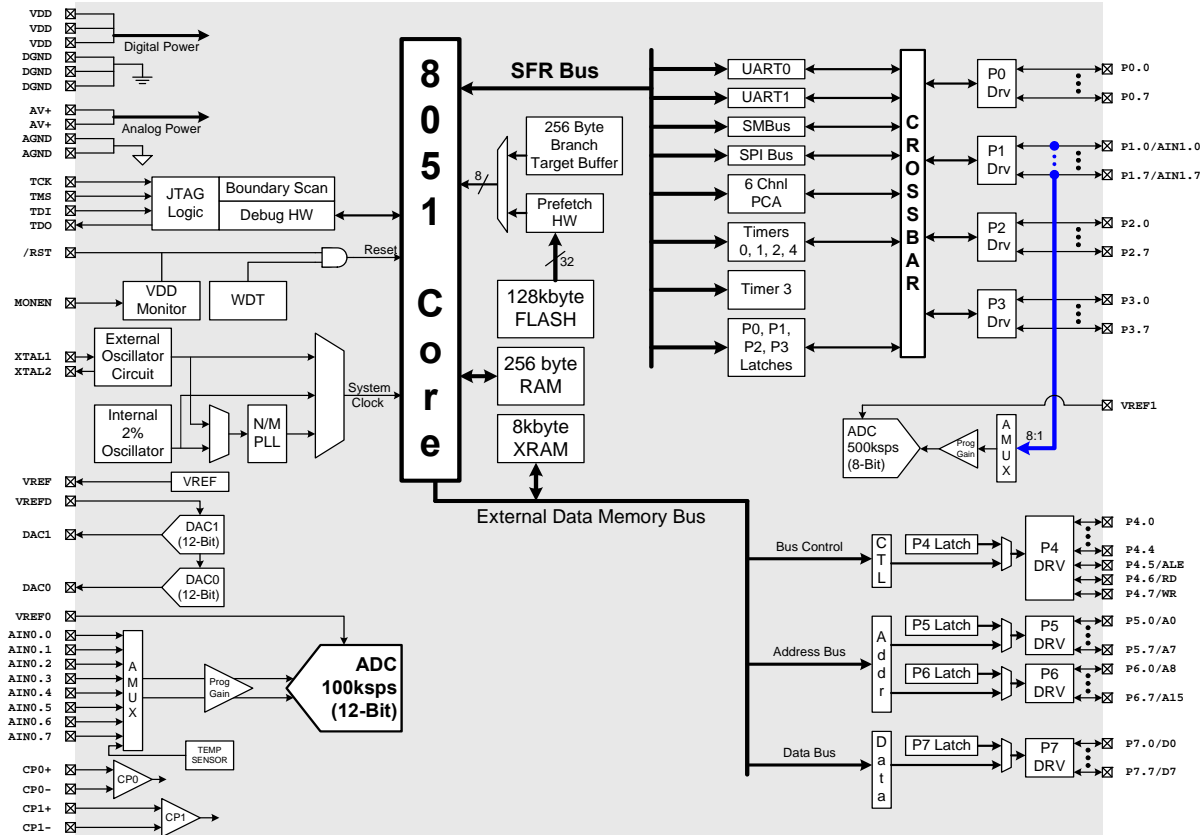
- Typical operating current: 25 mA at 50 MHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F124-GQ





### Analog Peripherals

#### 12-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### 8-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksps
- 8 external inputs
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Real-time instruction trace buffer
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz system clock
- Expanded interrupt handler

### Memory

- 8448 bytes data RAM
- 128 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using a timer or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- On-chip programmable PLL: up to 50 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

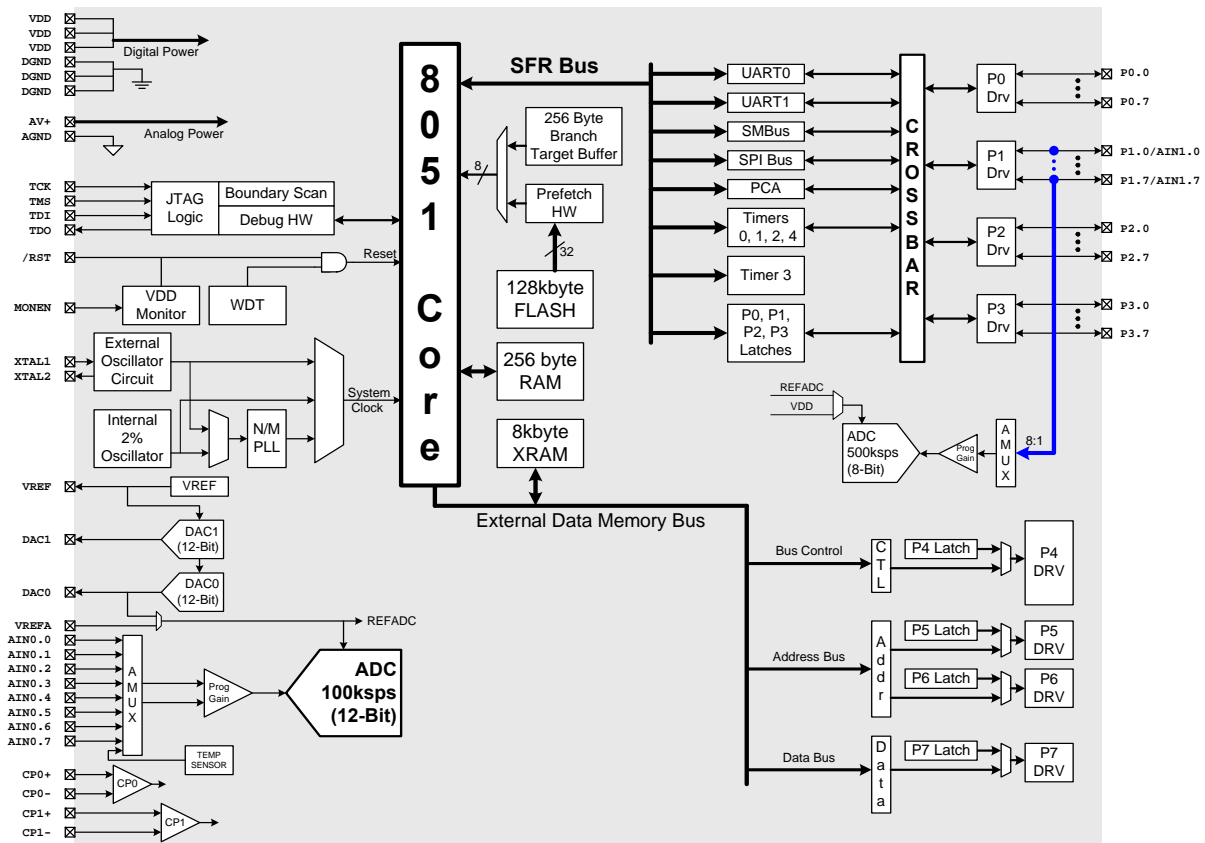
- Typical operating current: 25 mA at 50 MHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

C8051F125-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### 8-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksp/s
- 8 external inputs
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Real-time instruction trace buffer
- IEEE1149.1 compliant boundary scan

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS Throughput with 50 MHz system clock
- Expanded interrupt handler

### Memory

- 8448 bytes data RAM
- 128 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 64 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using a timer or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- On-chip programmable PLL: up to 50 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

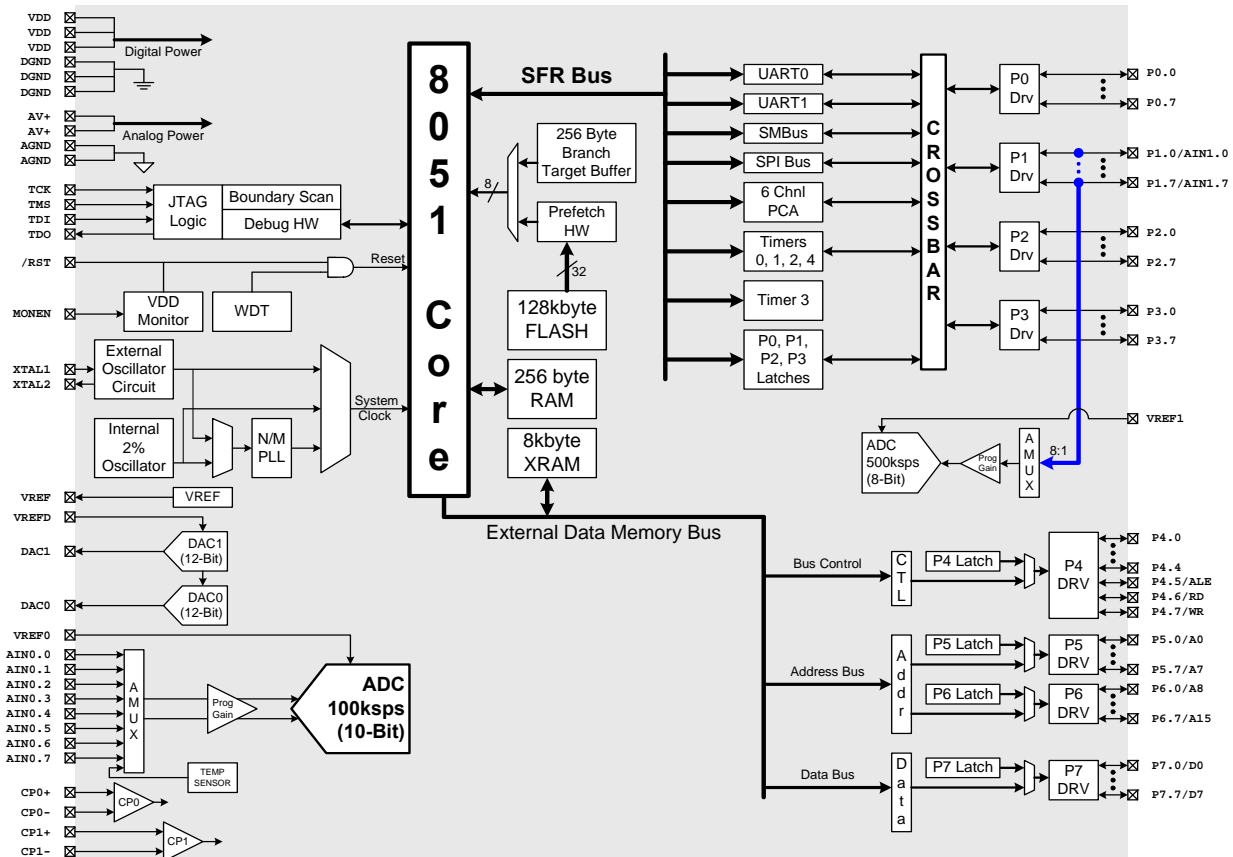
- Typical operating current: 25 mA at 50 MHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F126-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### 8-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksps
- 8 external inputs
- Programmable amplifier gain: 4, 2, 1, 0.5

#### Two 12-Bit DACs

- Can synchronize outputs to timers for jitter-free waveform generation

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Real-time instruction trace buffer
- IEEE1149.1 compliant boundary scan

#### Temperature Range: -40 to +85 °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz system clock
- Expanded interrupt handler

### Memory

- 8448 bytes data RAM
- 128 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (<sup>12</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using a timer or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- On-chip programmable PLL: up to 50 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 2.7 to 3.6 V

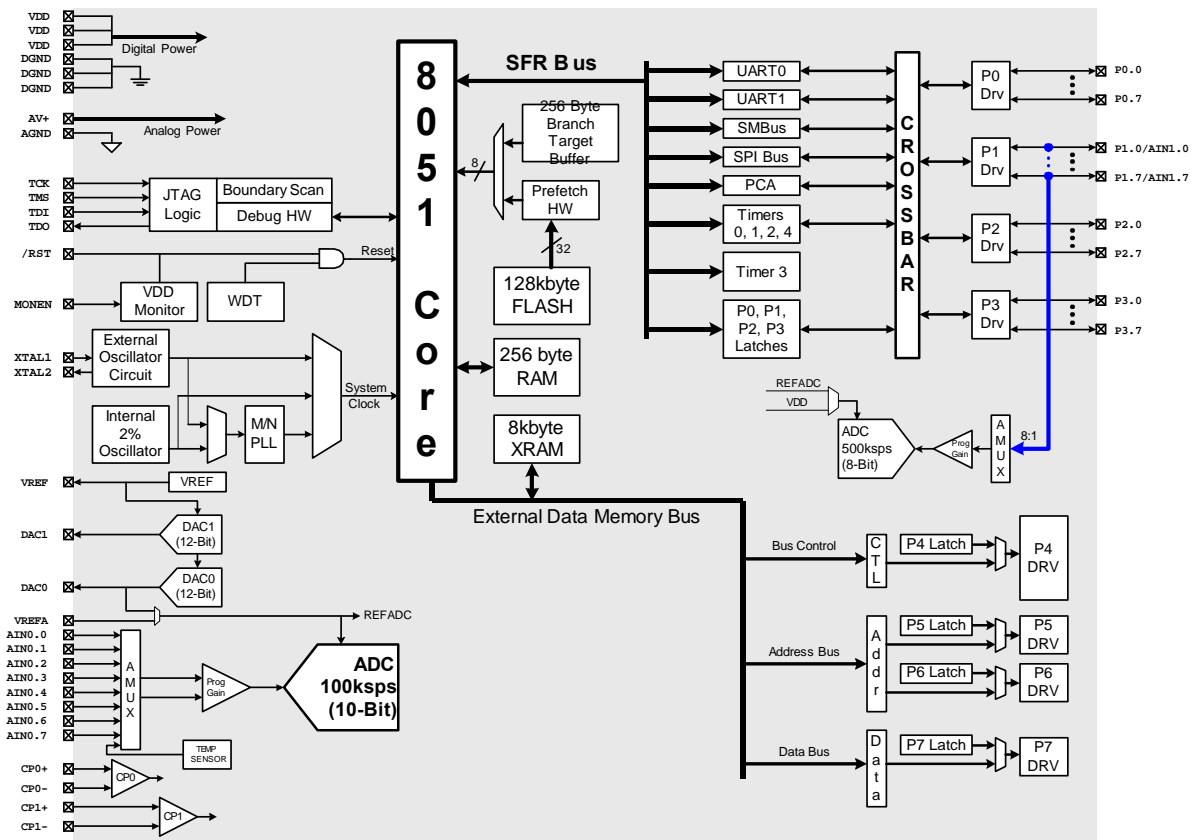
- Typical operating current: 25 mA at 50 MHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F127-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

Temperature Range: **-40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 8448 bytes data RAM
- 128 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 64 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- On-chip programmable PLL: up to 100 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 3.0 to 3.6 V

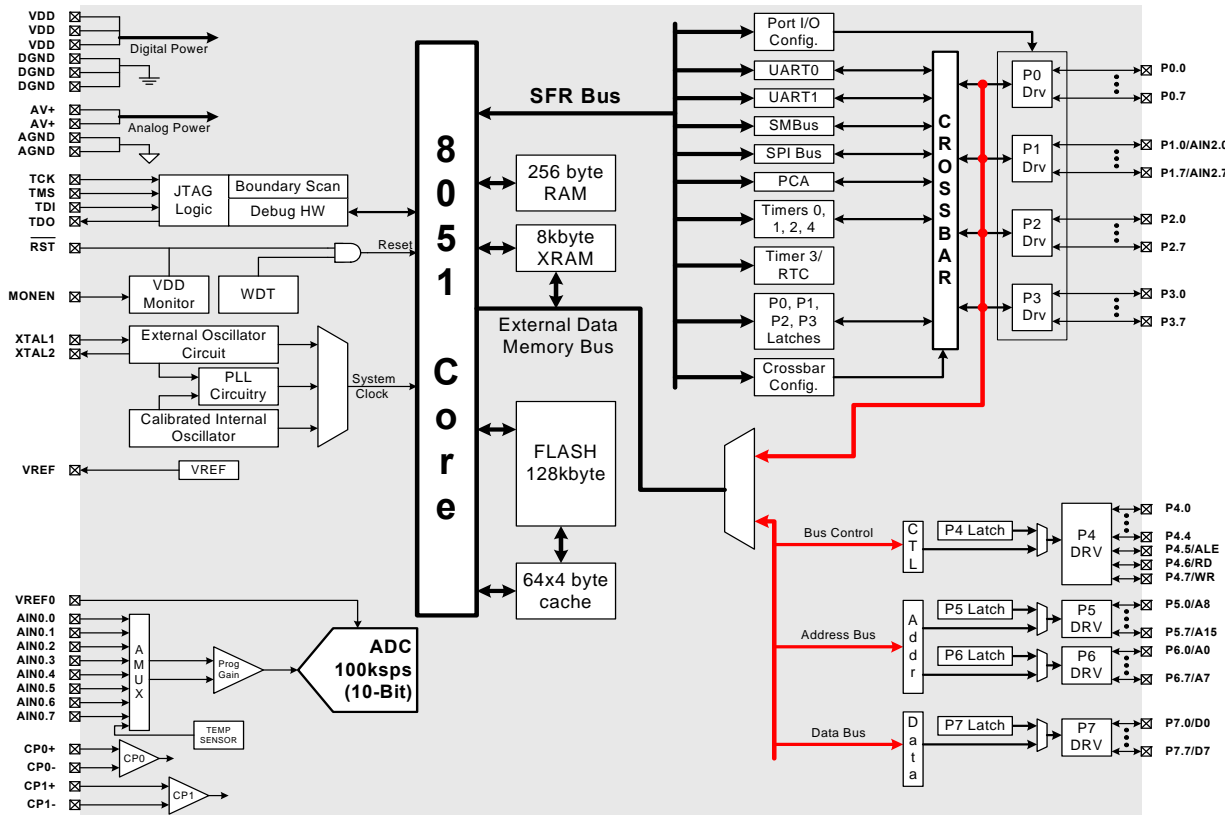
- Typical operating current: 50 mA at 100 MHz
- Typical stop mode current: 0.4  $\mu$ A

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F130-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

Temperature Range: **-40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 8448 bytes data RAM
- 128 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ Compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using Timer 3 or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- On-chip programmable PLL: up to 100 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 3.0 to 3.6 V

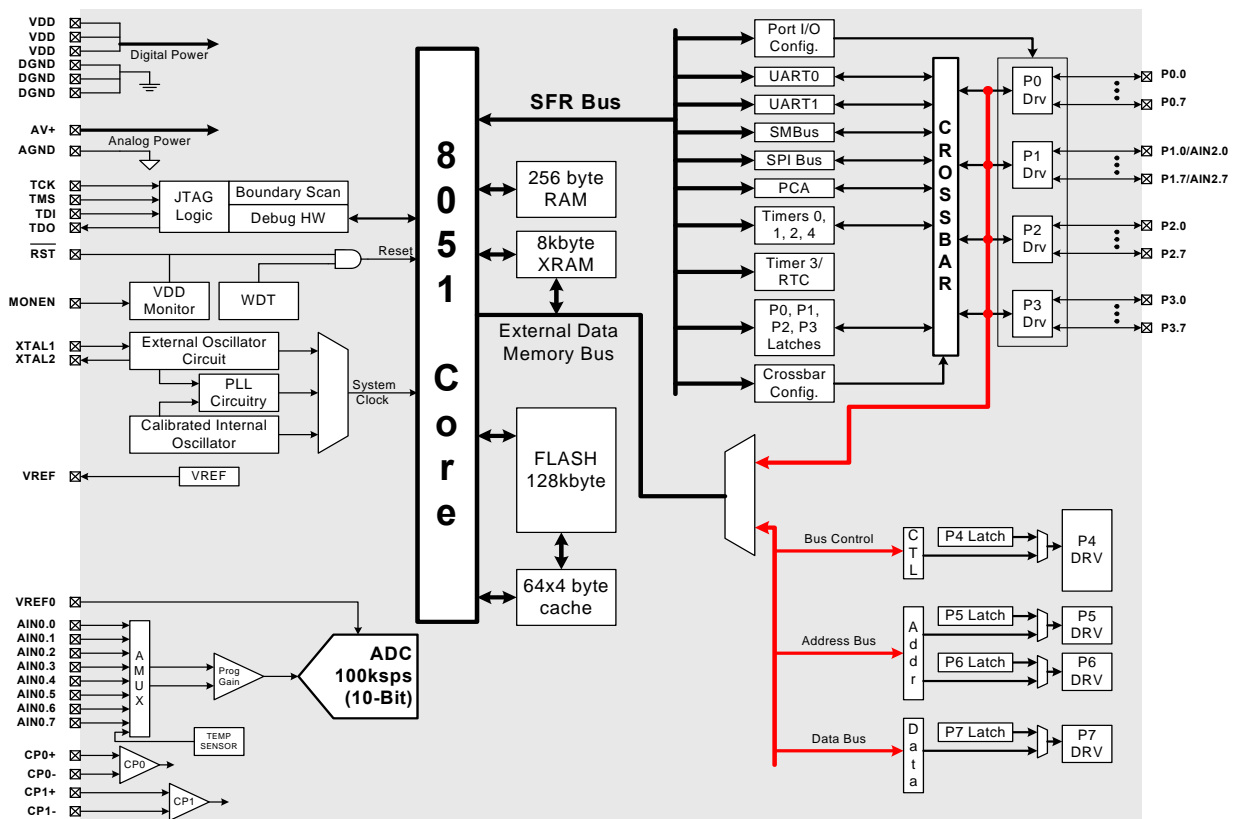
- Typical operating current: 50 mA at 100 MHz
- Typical stop mode current: 0.4  $\mu$ A

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F131-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

Temperature Range: **-40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 8448 bytes data RAM
- 64 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 64 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- On-chip programmable PLL: up to 100 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 3.0 to 3.6 V

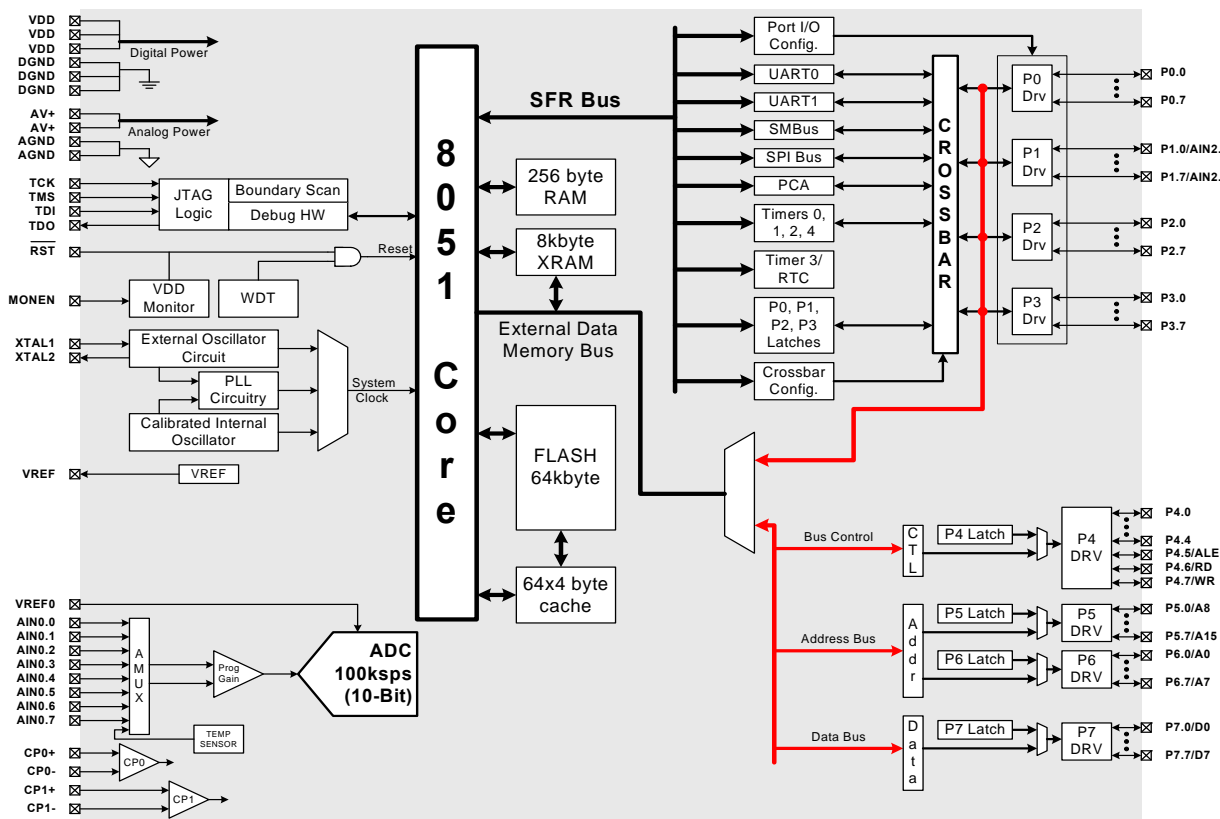
- Typical operating current: 50 mA at 100 MHz
- Typical stop mode current: 0.4  $\mu$ A

### Package

- 100-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F132-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

Temperature Range: **-40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 8448 bytes data RAM
- 64 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ Compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using Timer 3 or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- On-chip programmable PLL: up to 100 MHz
- External oscillator: Crystal, RC, C, or Clock

### Supply Voltage: 3.0 to 3.6 V

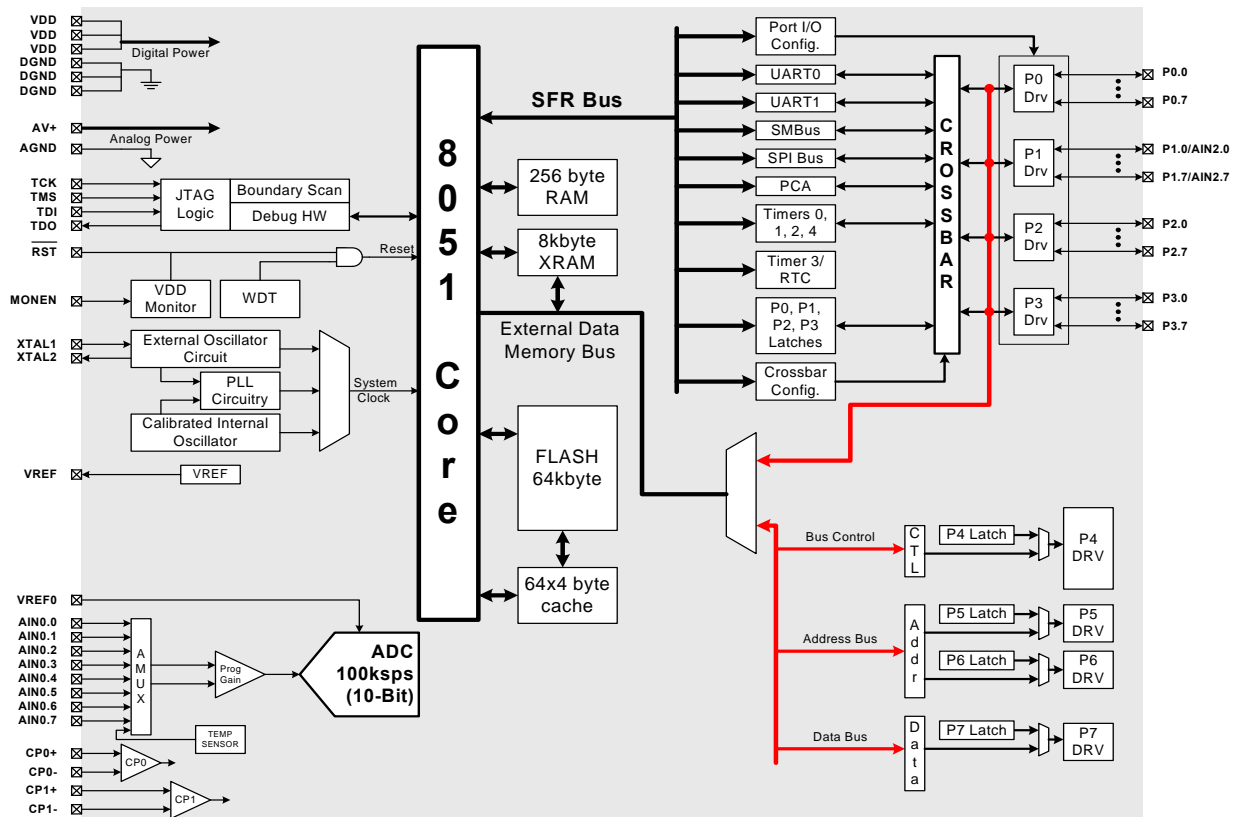
- Typical operating current: 50 mA at 100 MHz
- Typical stop mode current: 0.4  $\mu$ A

### Package

- 64-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F133-GQ



### Analog Peripherals

#### 24-Bit ADC

- 0.0015% nonlinearity
- Programmable throughput up to 1 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 128, 64, 32, 16, 8, 4, 2, 1
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3^\circ\text{C}$ )

#### Two 8-Bit Current DACs

#### Comparator

- 16 Programmable hysteresis values and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu\text{A}$ )

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range:  $-40$  to  $+85^\circ\text{C}$**

### High-Speed 8051 $\mu\text{C}$ Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 17 port I/O; all 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- 16-bit programmable counter array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Realtime clock mode using PCA or timer and external clock source

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- 2x clock multiplier to achieve 50 MHz internal clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

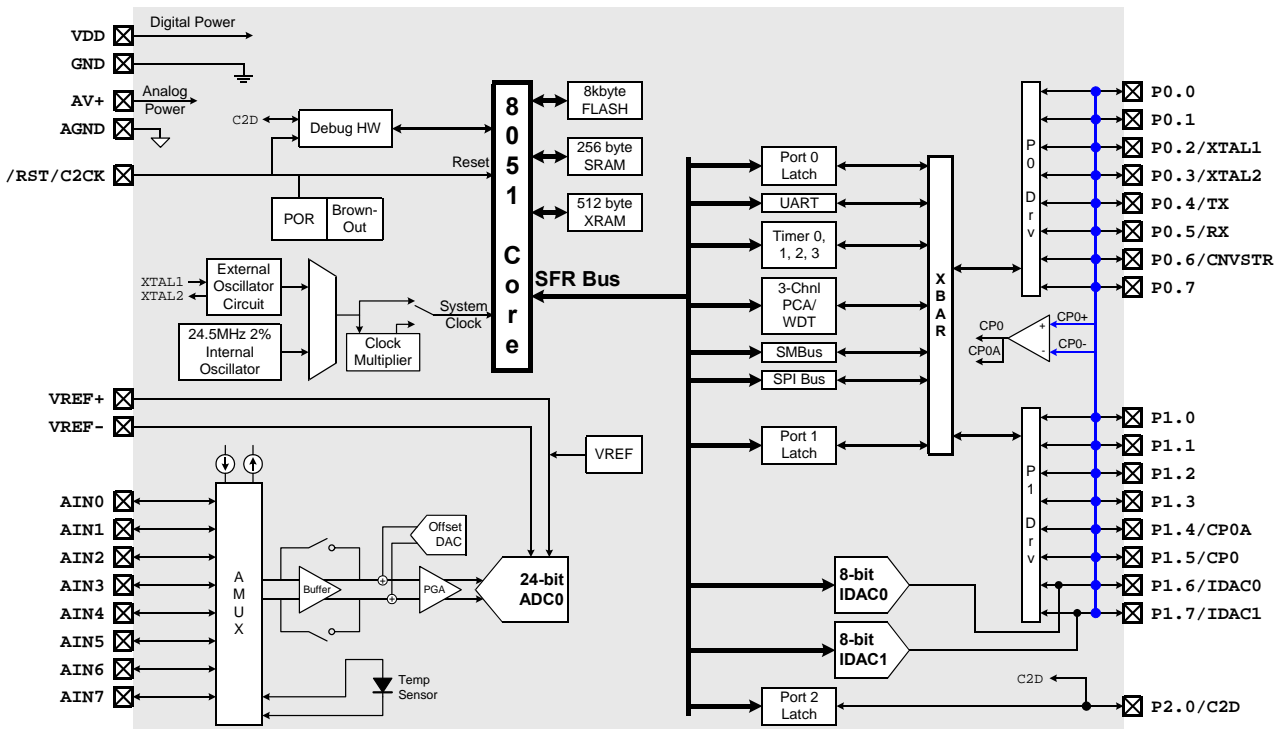
- Typical operating current: 17 mA at 50 MHz  
16  $\mu\text{A}$  at 32 kHz
- Typical stop mode current:  $<0.1 \mu\text{A}$

### Package

- 32-pin LQFP (lead-free package)

### Ordering Part Number

- C8051F350-GQ





### Analog Peripherals

#### 24-Bit ADC

- 0.0015% nonlinearity
- Programmable throughput up to 1 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 128, 64, 32, 16, 8, 4, 2, 1
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3^\circ\text{C}$ )

#### Two 8-Bit Current DACs

#### Comparator

- 16 Programmable hysteresis values and response time
- Configurable to generate interrupts or reset
- Low current ( $0.4\ \mu\text{A}$ )

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range:  $-40$  to  $+85^\circ\text{C}$**

### High-Speed 8051 $\mu\text{C}$ Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 17 port I/O; all 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- 16-bit programmable counter array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Realtime clock mode using PCA or timer and external clock source

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- 2x clock multiplier to achieve 50 MHz internal clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

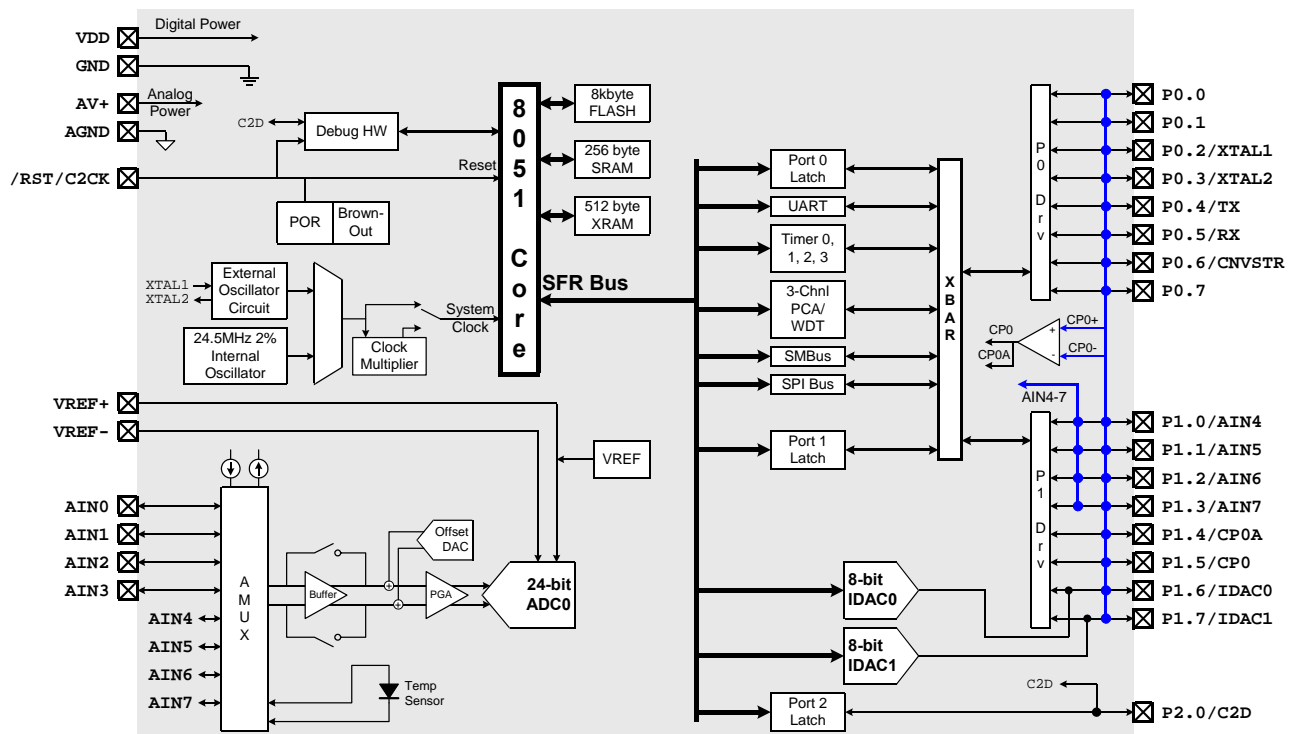
- Typical operating current: 17 mA at 50 MHz  
16  $\mu\text{A}$  at 32 kHz
- Typical stop mode current:  $<0.1\ \mu\text{A}$

### Package

- 28-pin QFN (lead-free package)

### Ordering Part Number

- C8051F351-GM



### Analog Peripherals

#### 16-Bit ADC

- 0.0015% nonlinearity
- Programmable throughput up to 1 ksp/s
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 128, 64, 32, 16, 8, 4, 2, 1
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3^\circ\text{C}$ )

#### Two 8-Bit Current DACs

#### Comparator

- 16 Programmable hysteresis values and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu\text{A}$ )

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range:  $-40$  to  $+85^\circ\text{C}$**

### High-Speed 8051 $\mu\text{C}$ Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 17 port I/O; all 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- 16-bit programmable counter array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Realtime clock mode using PCA or timer and external clock source

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- 2x clock multiplier to achieve 50 MHz internal clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

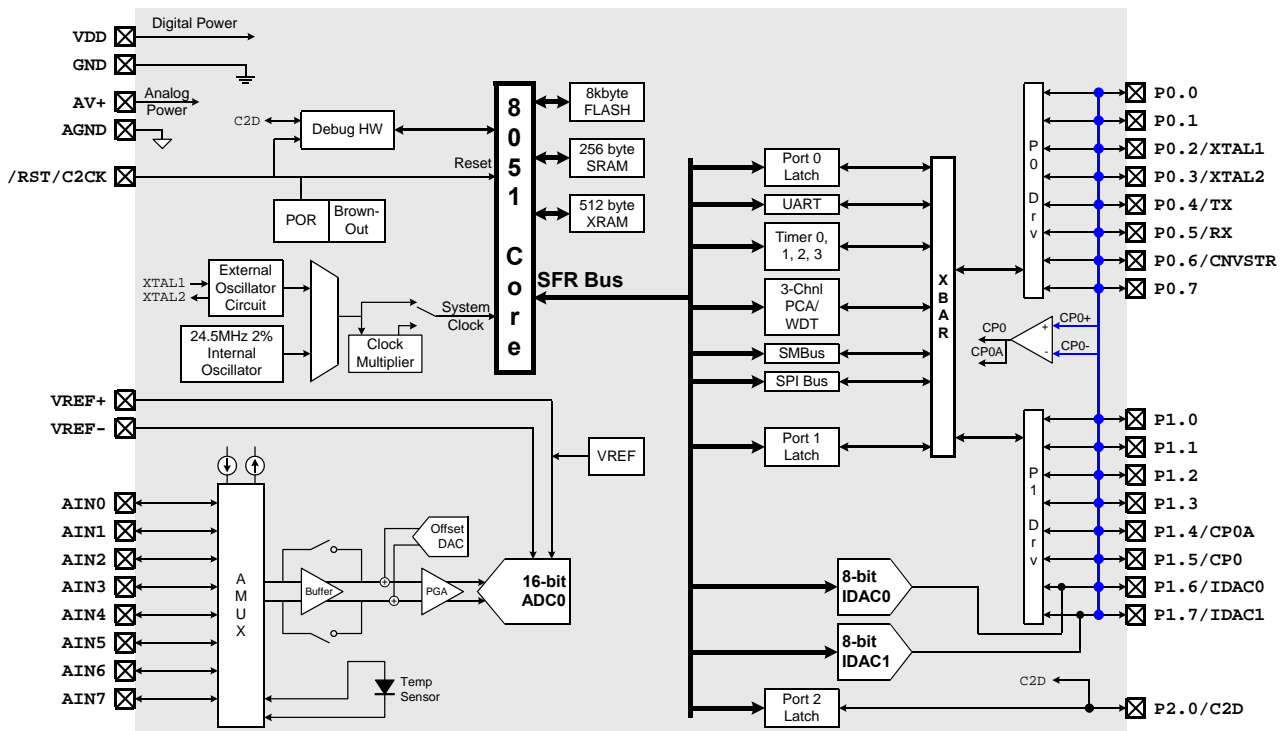
- Typical operating current: 17 mA at 50 MHz  
16  $\mu\text{A}$  at 32 kHz
- Typical stop mode current:  $<0.1 \mu\text{A}$

### Package

- 32-pin LQFP (lead-free package)

### Ordering Part Number

- C8051F352-GQ



### Analog Peripherals

#### 16-Bit ADC

- 0.0015% nonlinearity
- Programmable throughput up to 1 ksps
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 128, 64, 32, 16, 8, 4, 2, 1
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two 8-Bit Current DACs

#### Comparator

- 16 Programmable hysteresis values and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 17 port I/O; all 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- 16-bit programmable counter array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Realtime clock mode using PCA or timer and external clock source

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- 2x clock multiplier to achieve 50 MHz internal clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

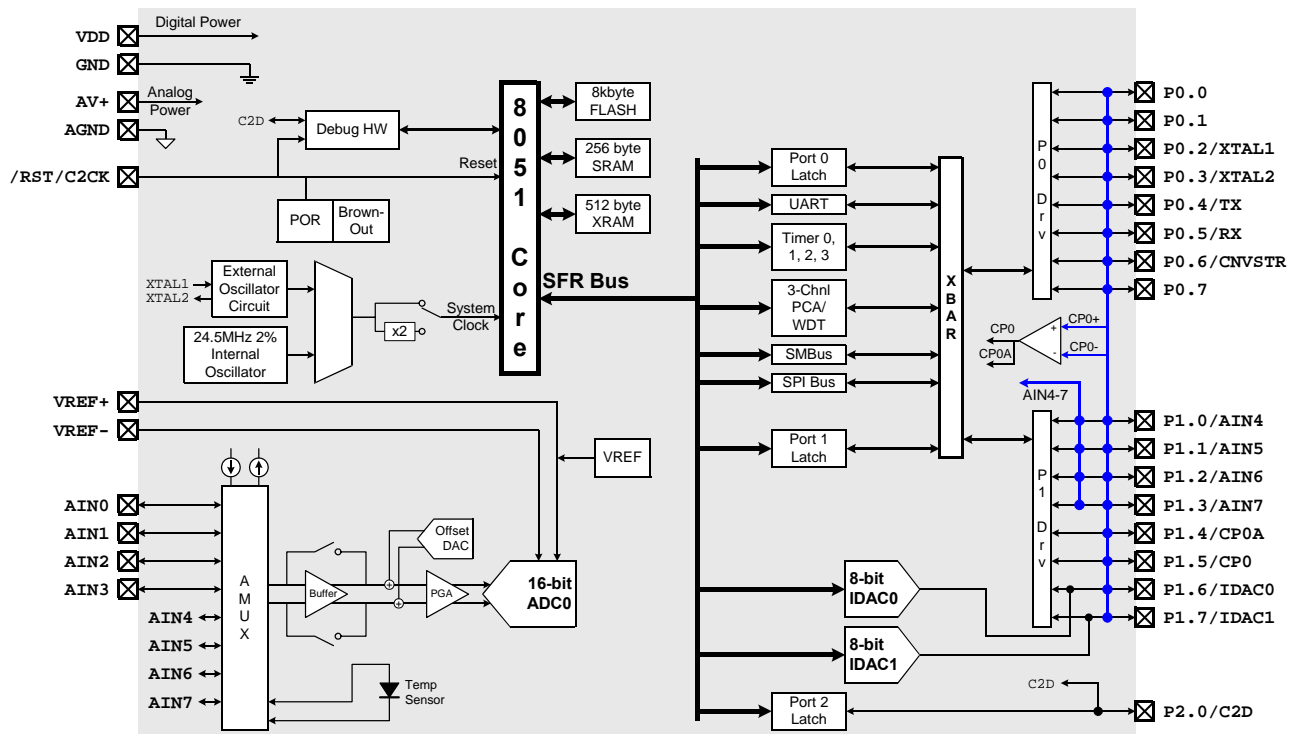
- Typical operating current: 17 mA at 50 MHz  
16  $\mu$ A at 32 kHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 28-pin QFN (lead-free package)

### Ordering Part Number

- C8051F353-GM







# Small Form Factor MCUs

### Analog Peripherals

#### 12-Bit ADC

- No missing codes
- Programmable throughput up to 100 ksps
- 32 external inputs (each port I/O can be configured as an ADC input on-the-fly)
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- $V_{REF}$  from external pin or  $V_{DD}$

#### Two comparators

- Programmable hysteresis
- Configurable to generate interrupts or reset

#### $V_{DD}$ Monitor and Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 1280 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SPI™ and UART serial ports available concurrently
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

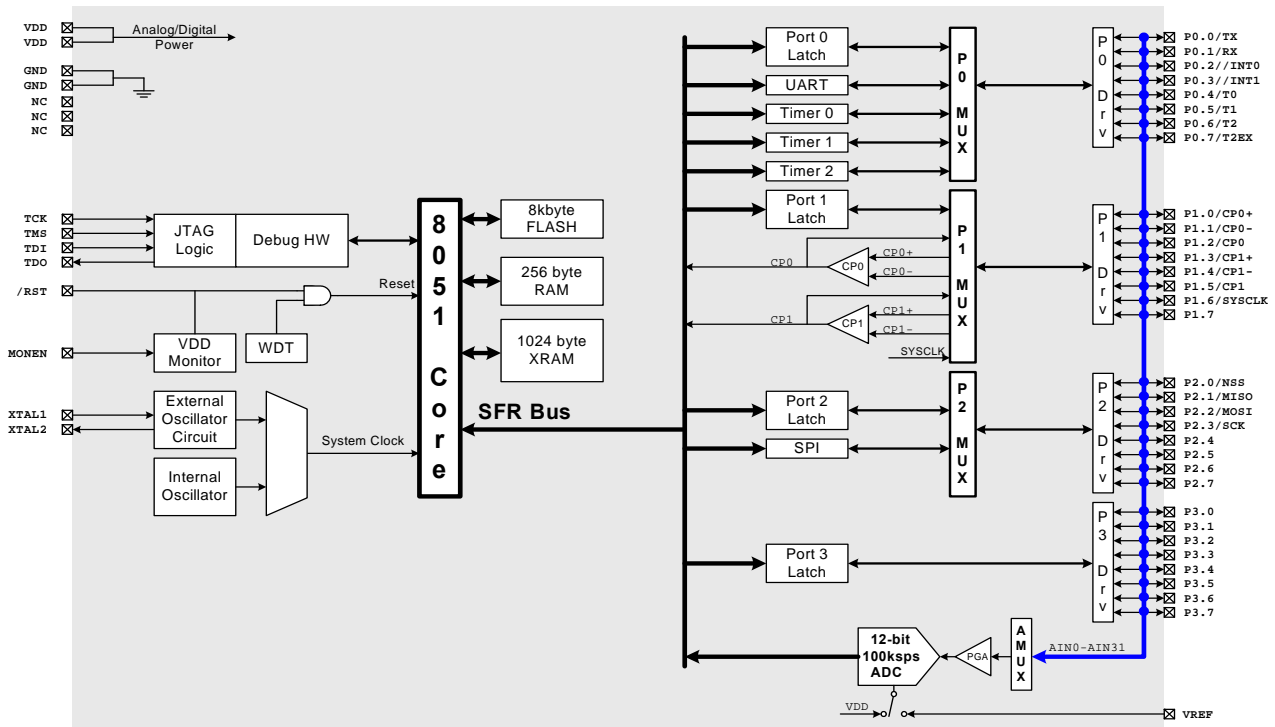
- Typical operating current: 9 mA at 25 MHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 48-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F206-GQ



### Analog Peripherals

#### 8-Bit ADC

- $\pm 1/2$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 32 external inputs (each port I/O can be configured as an ADC input on-the-fly)
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- $V_{REF}$  from external pin or  $V_{DD}$

#### Two comparators

- Programmable hysteresis
- Configurable to generate interrupts or reset

#### $V_{DD}$ Monitor and Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 256 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SPI™ and UART serial ports available concurrently
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

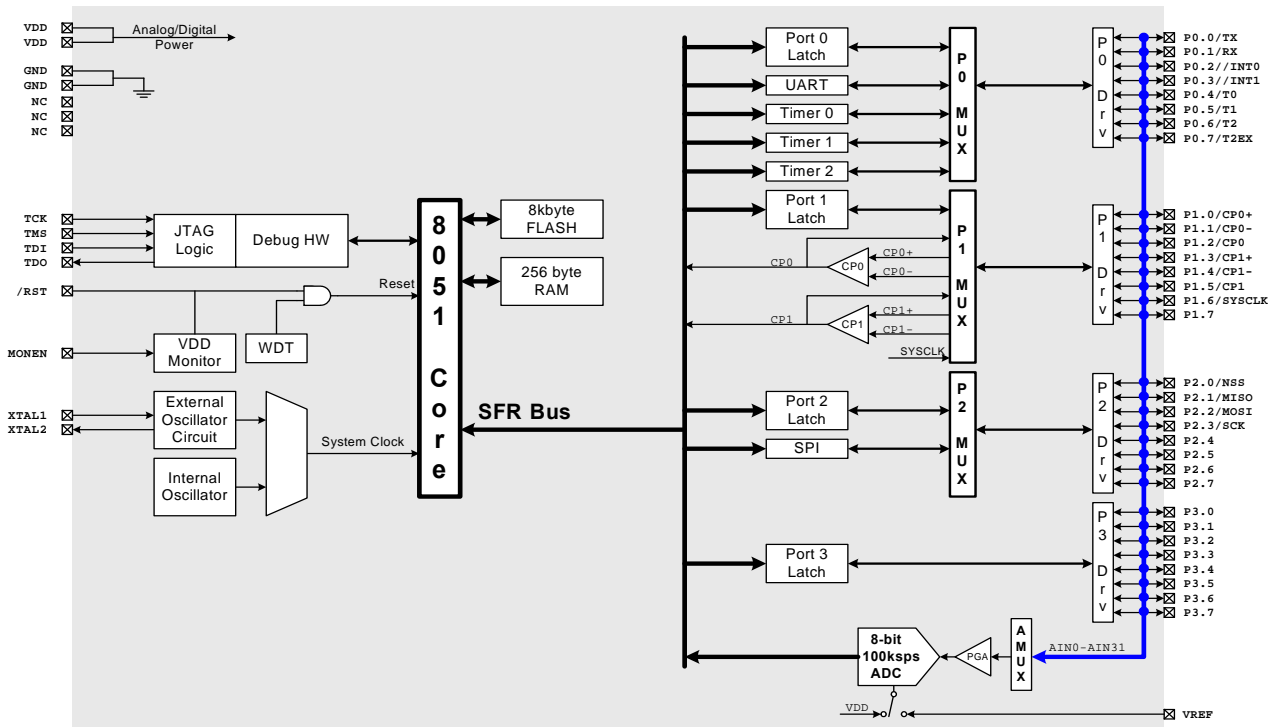
- Typical operating current: 9 mA at 25 MHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 48-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F220-GQ



### Analog Peripherals

#### 8-Bit ADC

- $\pm 1/2$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 32 external inputs (each port I/O can be configured as an ADC input on-the-fly)
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- $V_{REF}$  from external pin or  $V_{DD}$

#### Two comparators

- Programmable hysteresis
- Configurable to generate interrupts or reset

#### $V_{DD}$ Monitor and Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 256 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 22 port I/O; all are 5 V tolerant
- Hardware SPI™ and UART serial ports available concurrently
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

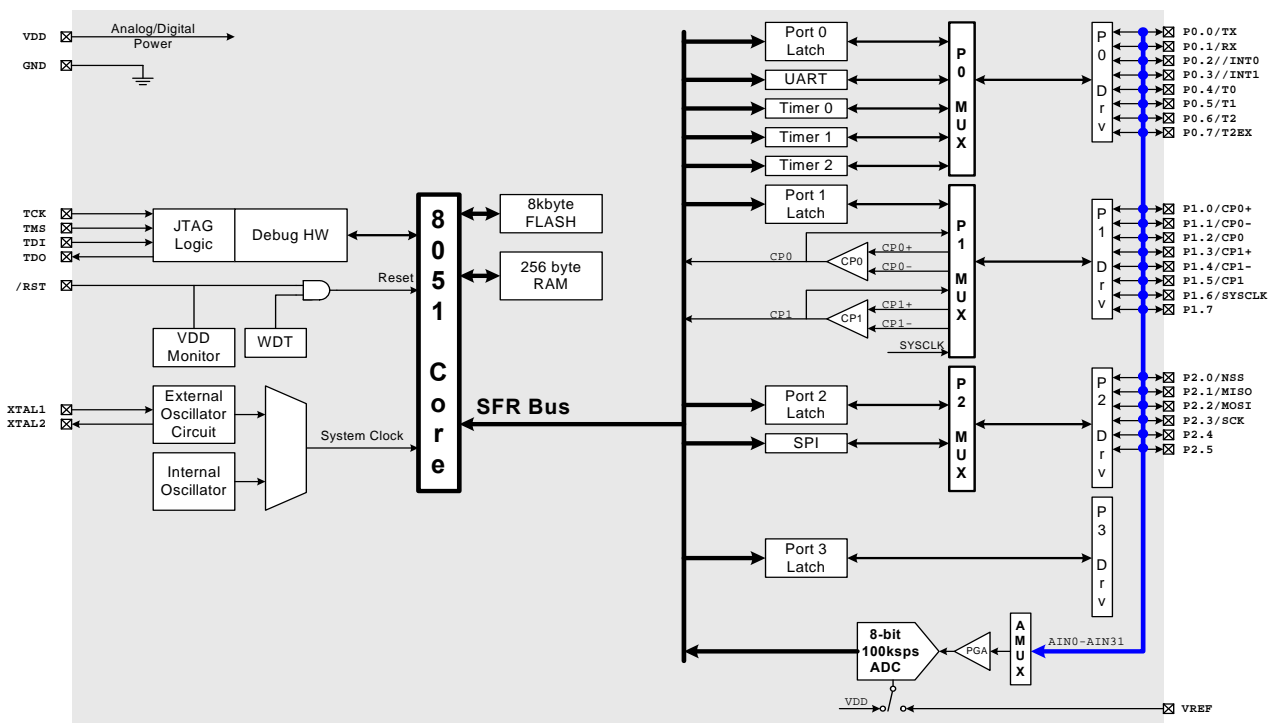
- Typical operating current: 9 mA at 25 MHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 32-pin LQFP (lead-free package)

### Ordering Part Number

- C8051F221-GQ





### Analog Peripherals

#### 8-Bit ADC

- $\pm 1/2$  LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 32 external inputs (each port I/O can be configured as an ADC input on-the-fly)
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- $V_{REF}$  from external pin or  $V_{DD}$

#### Two comparators

- Programmable hysteresis
- Configurable to generate interrupts or reset

#### $V_{DD}$ Monitor and Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 1280 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SPI™ and UART serial ports available concurrently
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

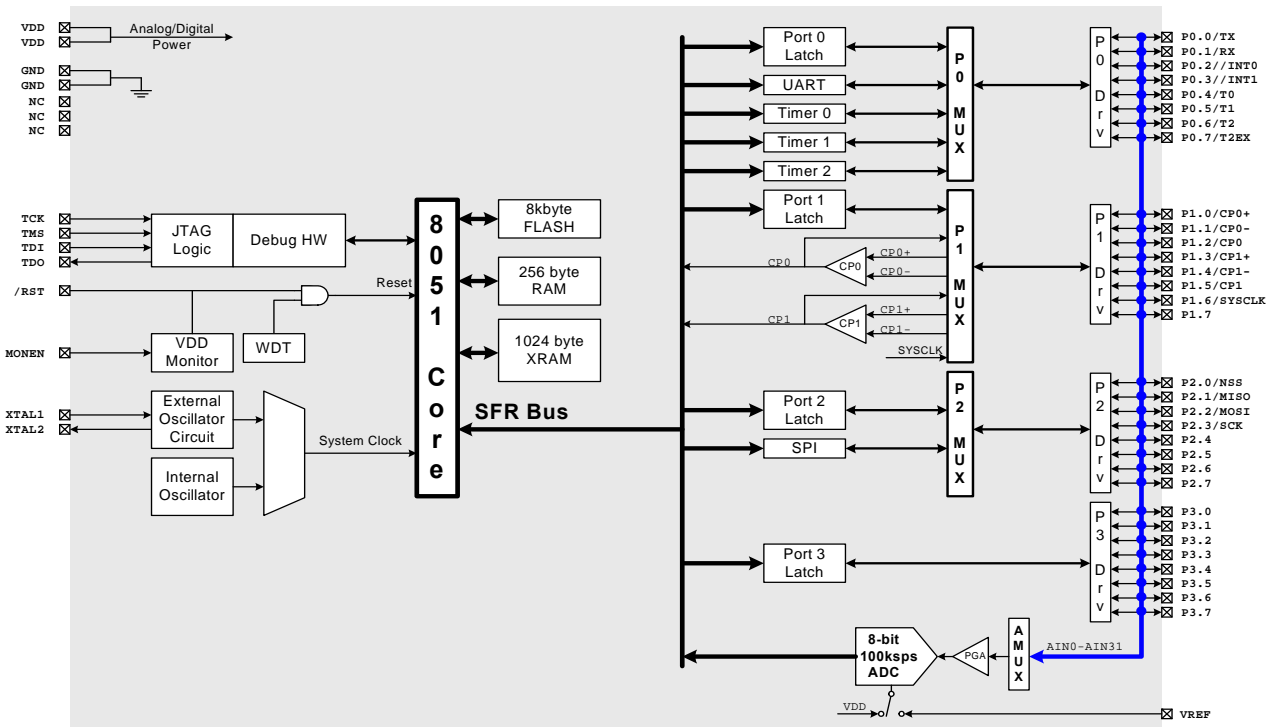
- Typical operating current: 9 mA at 25 MHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 48-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F226-GQ



### Analog Peripherals

#### Two comparators

- Programmable hysteresis
- Configurable to generate interrupts or reset

#### V<sub>DD</sub> Monitor and Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 256 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SPI™ and UART serial ports available concurrently
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

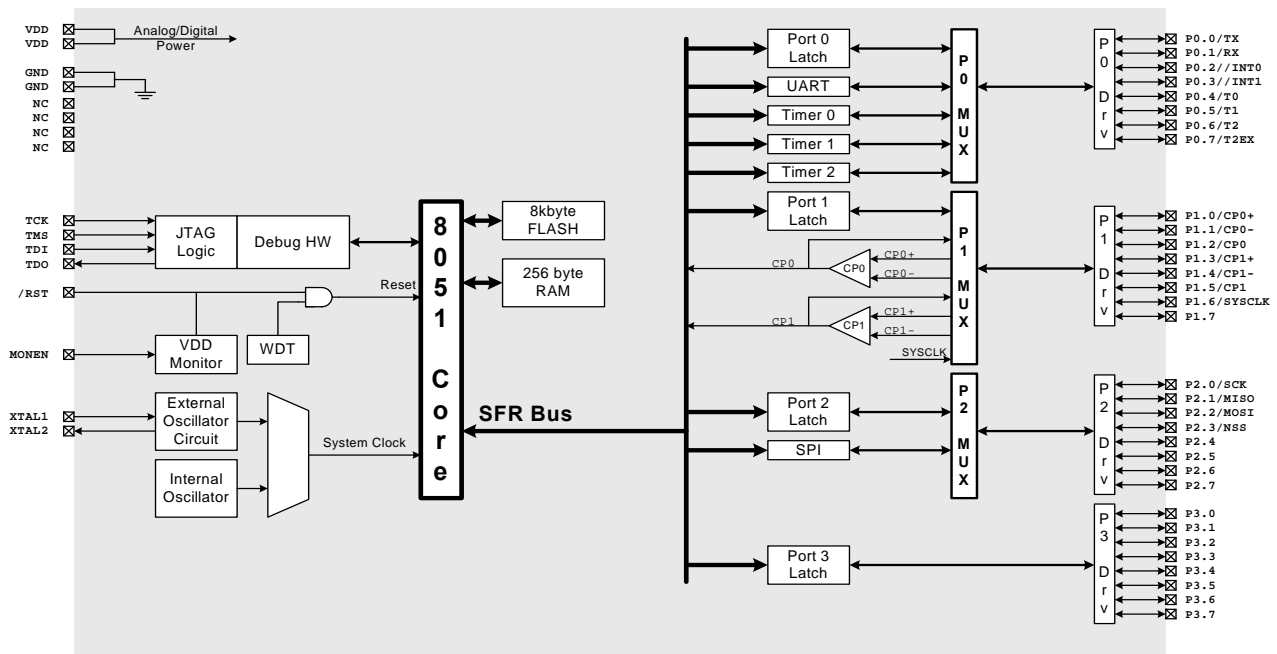
- Typical operating current: 9 mA at 25 MHz
- Typical stop mode current: <0.1 µA

### Package

- 48-pin TQFP (lead-free package)

### Ordering Part Number

- C8051F230-GQ



### Analog Peripherals

#### Two comparators

- Programmable hysteresis
- Configurable to generate interrupts or reset

#### V<sub>DD</sub> Monitor and Brown-out Detector

#### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler; up to 21 interrupt sources

### Memory

- 256 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 22 port I/O; all are 5 V tolerant
- Hardware SPI™ and UART serial ports available concurrently
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

### Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

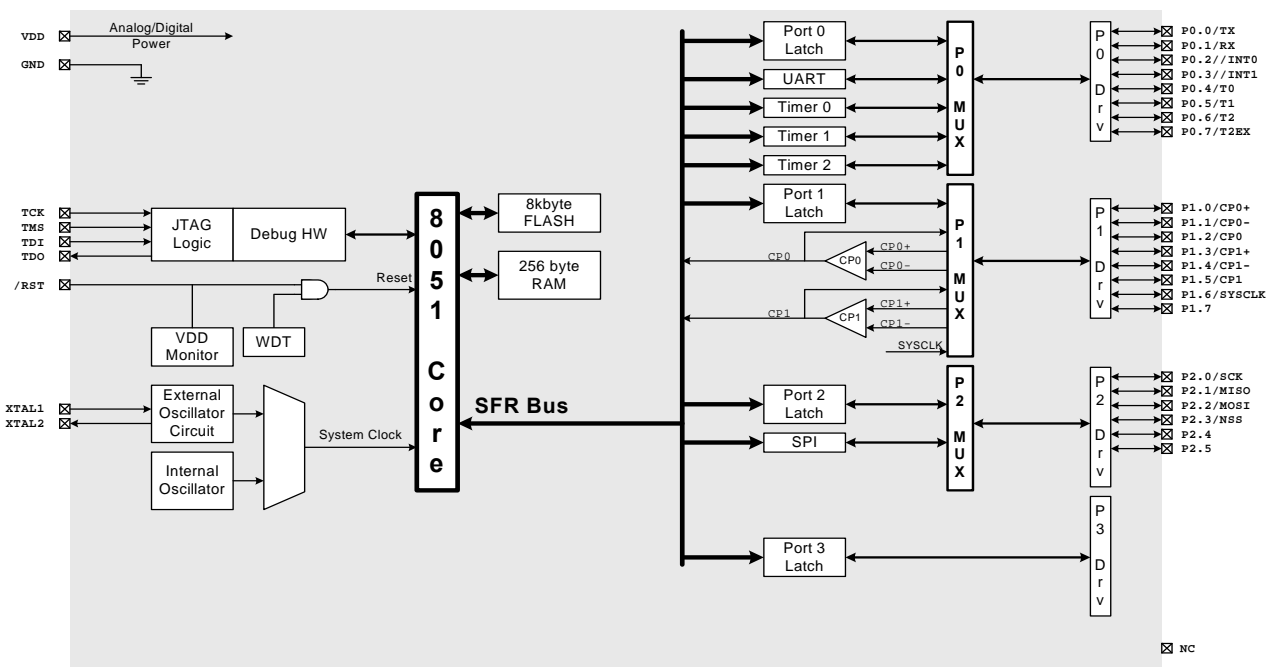
- Typical operating current: 9 mA at 25 MHz
- Typical stop mode current: <0.1 µA

### Package

- 32-pin LQFP (lead-free package)

### Ordering Part Number

- C8051F231-GQ



# C8051F236

25 MIPS, 8 kB Flash, 48-Pin Mixed-Signal MCU



## Analog Peripherals

### Two comparators

- Programmable hysteresis
- Configurable to generate interrupts or reset

### V<sub>DD</sub> Monitor and Brown-out Detector

### On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

**Temperature Range: -40 to +85 °C**

## High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler; up to 21 interrupt sources

## Memory

- 1280 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

## Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SPI™ and UART serial ports available concurrently
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

## Clock Sources

- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

## Supply Voltage: 2.7 to 3.6 V

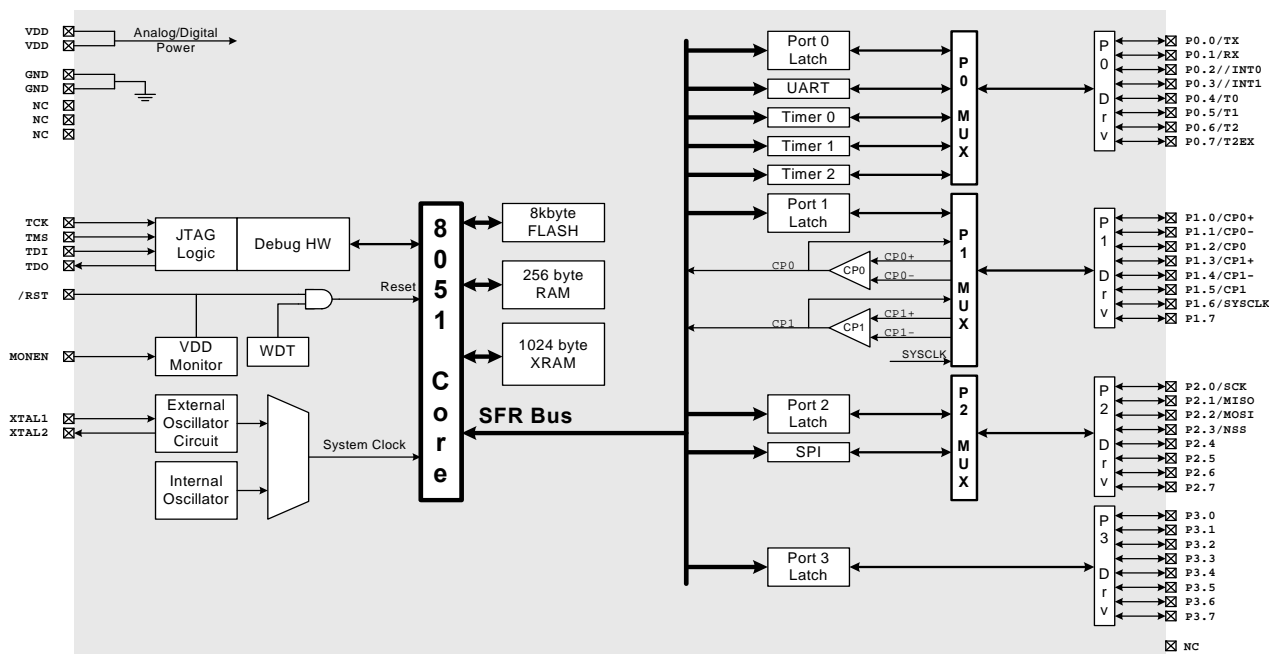
- Typical operating current: 9 mA at 25 MHz
- Typical stop mode current: <0.1 µA

## Package

- 48-pin TQFP (lead-free package)

## Ordering Part Number

- C8051F236-GQ



### Analog Peripherals

#### 8-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksps
- Up to 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 4, 2, 1, 0.5
- $V_{REF}$  from external pin or  $V_{DD}$
- Internal or external start of conversion sources
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### POR/Brown-Out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 256 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 8 port I/O; all are 5 V tolerant
- Enhanced Hardware SMBus™ (I<sup>2</sup>C™ compatible) and UART serial ports
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Internal oscillator: 25 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock (1 or 2 Pin Modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

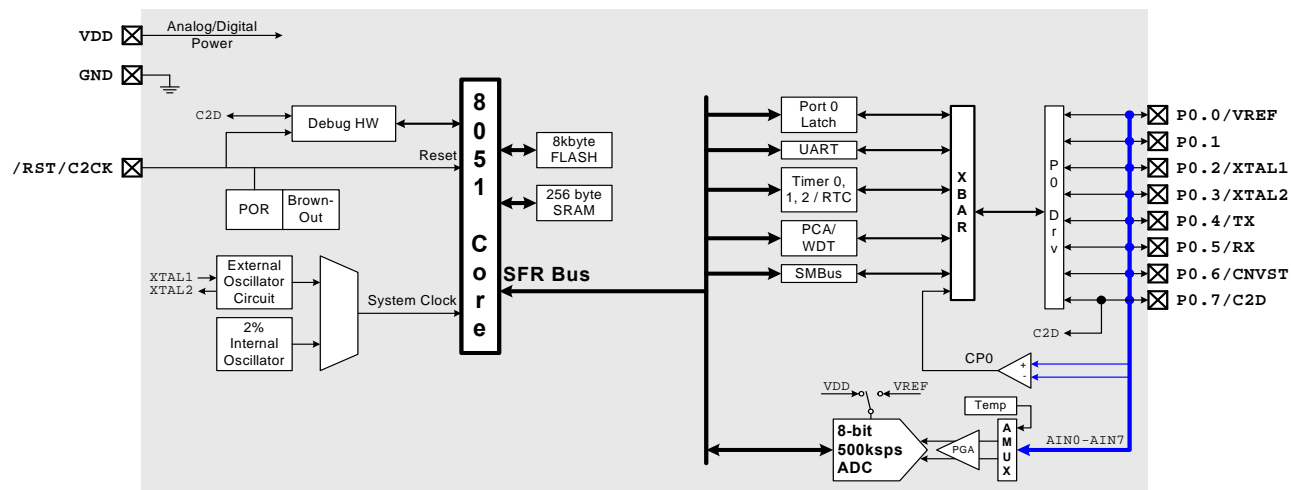
- Typical operating current: 5.8 mA at 25 MHz  
11  $\mu$ A at 32 kHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 11-pin QFN (lead-free package)

### Ordering Part Number

- C8051F300-GM



### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### POR/Brown-Out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined Instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 256 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 8 port I/O; all are 5 V tolerant
- Enhanced Hardware SMBus™ (I<sup>2</sup>C™ compatible) and UART serial ports
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Internal oscillator: 25 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

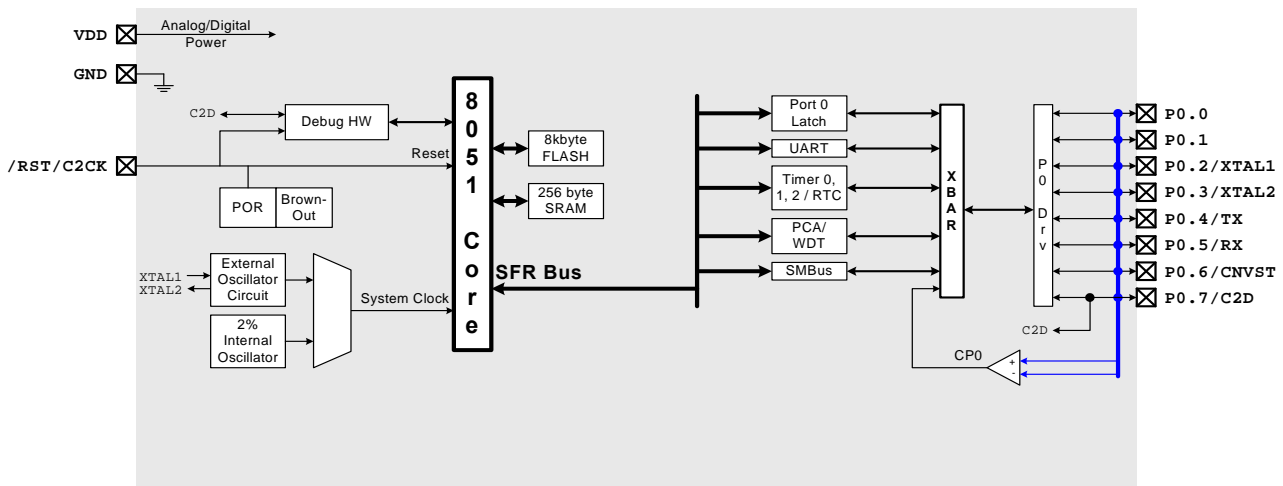
- Typical operating current: 5.8 mA at 25 MHz  
11  $\mu$ A at 32 kHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 11-pin QFN (lead-free package)

### Ordering Part Number

- C8051F301-GM



### Analog Peripherals

#### 8-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 500 ksps
- Up to 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 4, 2, 1, 0.5
- $V_{REF}$  from external pin or  $V_{DD}$
- Internal or external start of conversion sources
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### POR/Brown-Out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 256 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 8 port I/O; all are 5 V tolerant
- Enhanced Hardware SMBus™ (I<sup>2</sup>C™ compatible) and UART serial ports
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Internal oscillator: 20 MHz nominal
- External oscillator: Crystal, RC, C, or Clock (1 or 2 Pin Modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

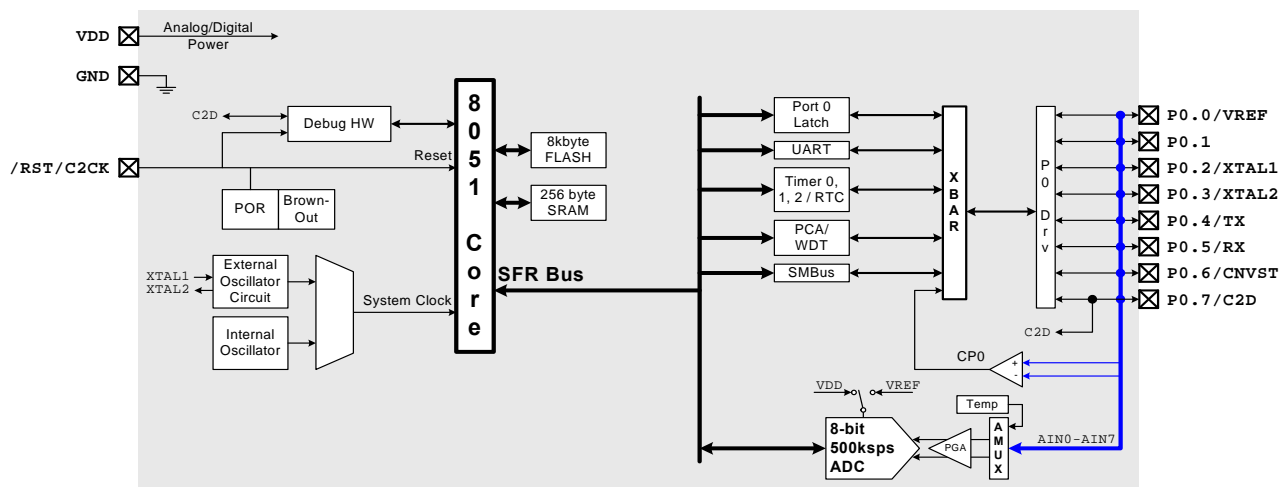
- Typical operating current: 5.8 mA at 25 MHz  
11  $\mu$ A at 32 kHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 11-pin QFN (lead-free package)

### Ordering Part Number

- C8051F302-GM



### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### POR/Brown-Out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined Instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 256 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 8 port I/O; all are 5 V tolerant
- Enhanced Hardware SMBus™ (I<sup>2</sup>C™ compatible) and UART serial ports
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Internal oscillator: 20 MHz nominal
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

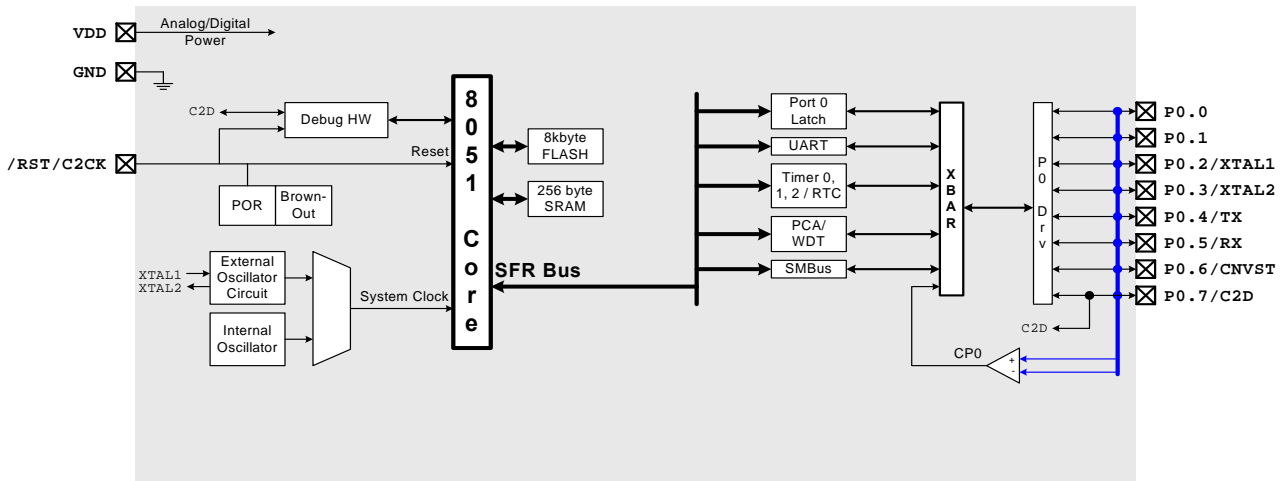
- Typical operating current: 5.8 mA at 25 MHz  
11  $\mu$ A at 32 kHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 11-pin QFN (lead-free package)

### Ordering Part Number

- C8051F303-GM





### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### POR/Brown-Out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined Instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 256 bytes data RAM
- 4 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 8 port I/O; all are 5 V tolerant
- Enhanced Hardware SMBus™ (I<sup>2</sup>C™ compatible) and UART serial ports
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Internal oscillator: 20 MHz nominal
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

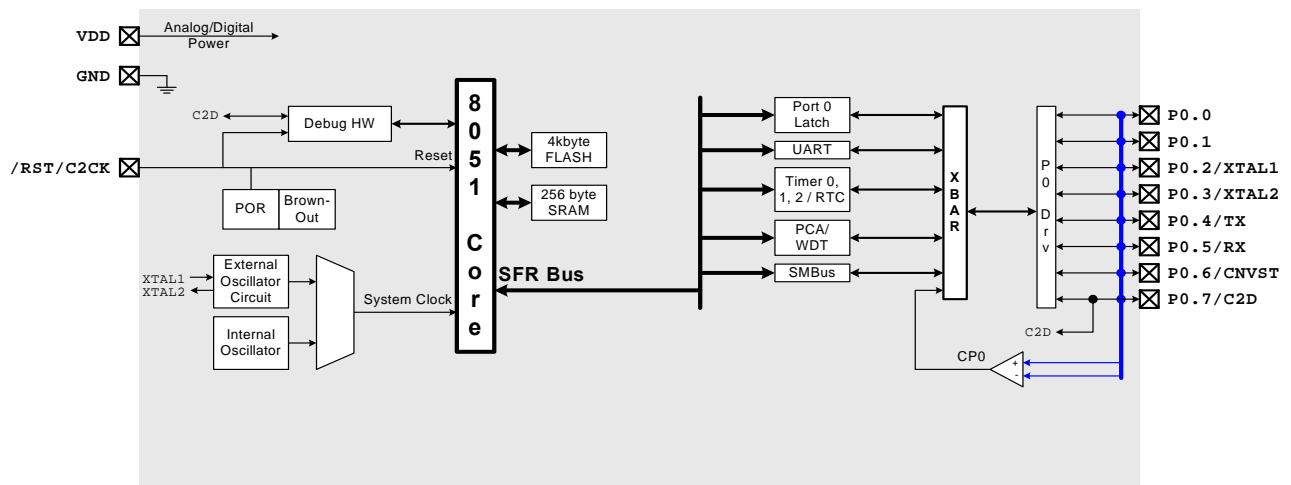
- Typical operating current: 5.8 mA at 25 MHz  
11  $\mu$ A at 32 kHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 11-pin QFN (lead-free package)

### Ordering Part Number

- C8051F304-GM



### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### POR/Brown-Out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined Instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 256 bytes data RAM
- 2 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 8 port I/O; all are 5 V tolerant
- Enhanced Hardware SMBus™ (I<sup>2</sup>C™ compatible) and UART serial ports
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Internal oscillator: 20 MHz nominal
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

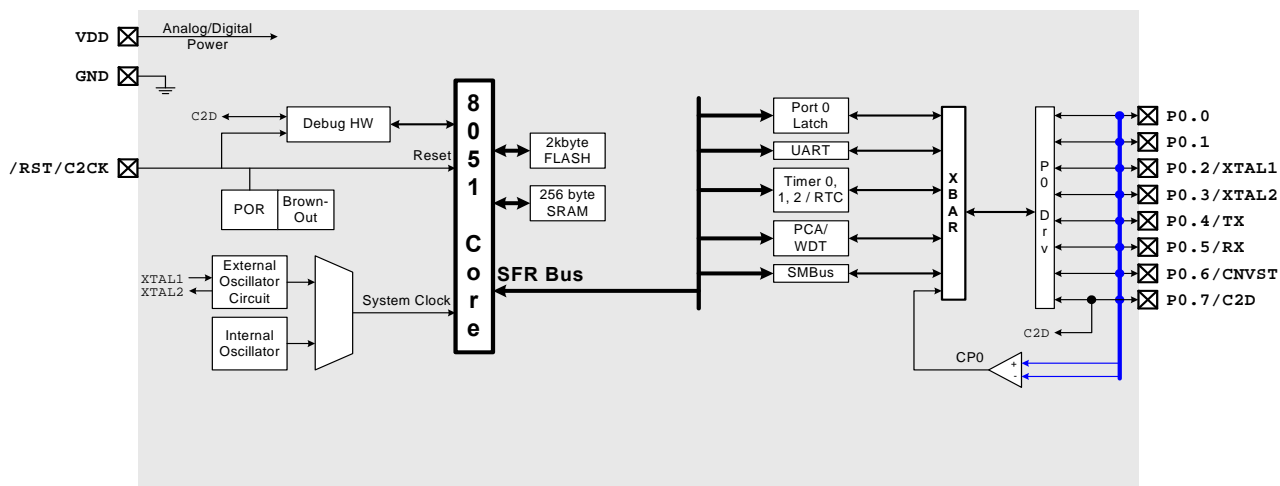
- Typical operating current: 5.8 mA at 25 MHz  
11  $\mu$ A at 32 kHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 11-pin QFN (lead-free package)

### Ordering Part Number

- C8051F305-GM



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksps
- Up to 21 external inputs; programmable as single-ended or differential
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### POR/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 1280 bytes data RAM
- 16 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 29 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Realtime clock mode using timer or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

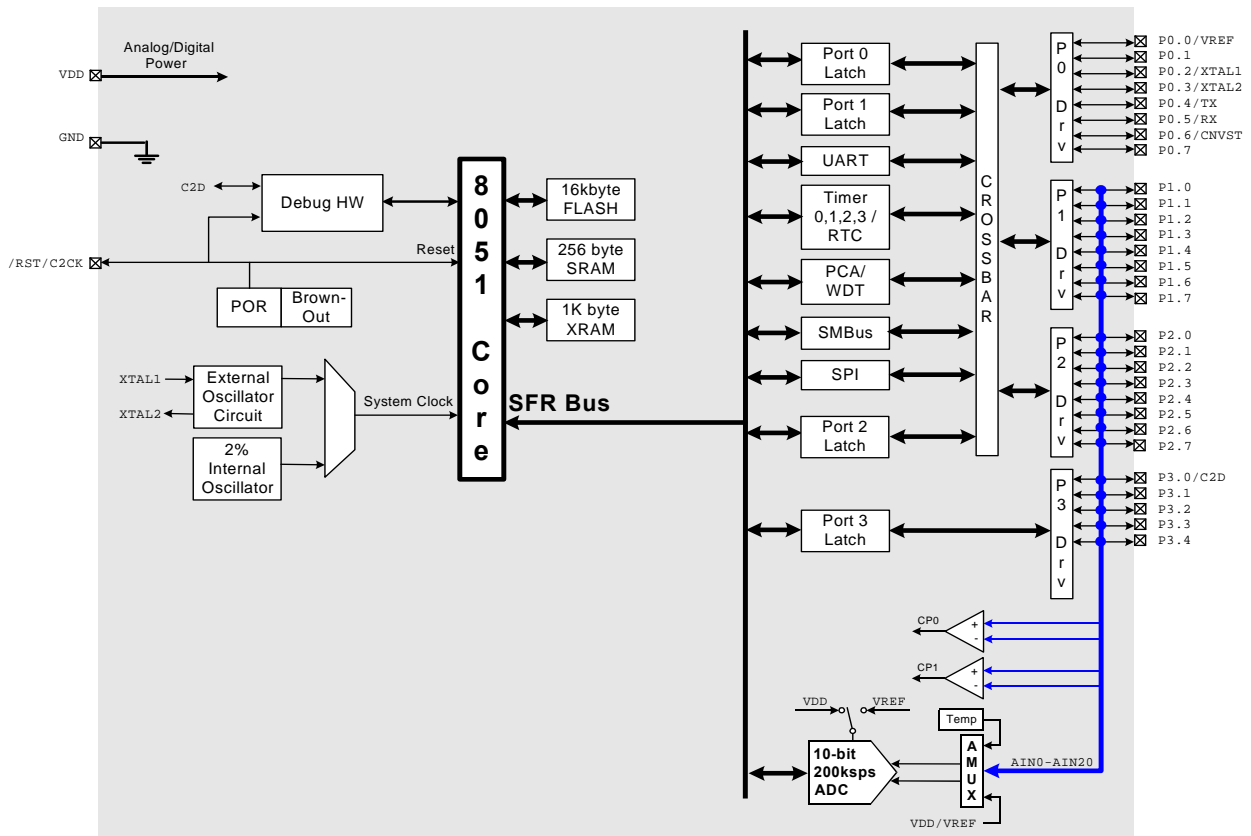
- Typical Operating Current: 7 mA at 25 MHz  
15  $\mu$ A at 32 kHz
- Typical Stop Mode Current: <0.1  $\mu$ A

### Package

- 32-pin LQFP (lead-free package)

### Ordering Part Number

- C8051F310-GQ





### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksps
- Up to 21 external inputs; programmable as single-ended or differential
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### POR/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 1280 bytes data RAM
- 8 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 29 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Realtime clock mode using timer or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

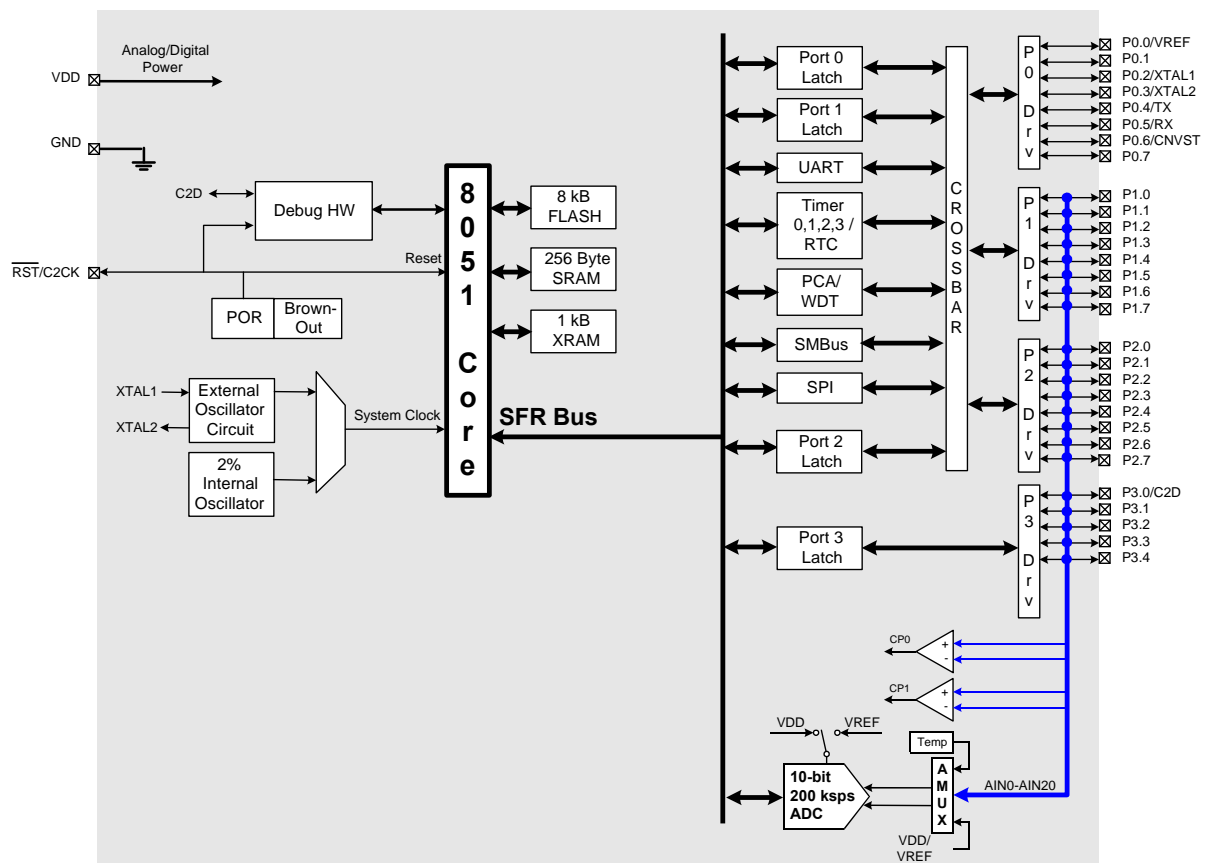
- Typical Operating Current: 7 mA at 25 MHz  
15  $\mu$ A at 32 kHz
- Typical Stop Mode Current: <0.1  $\mu$ A

### Package

- 32-pin LQFP (lead-free package)

### Ordering Part Number

- C8051F312-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksp/s
- Up to 17 external inputs; programmable as single-ended or differential
- Data-dependent windowed interrupt generator
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### POR/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 1280 bytes internal data RAM (256 + 1 k)
- 8 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 25 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Realtime clock mode using timer or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

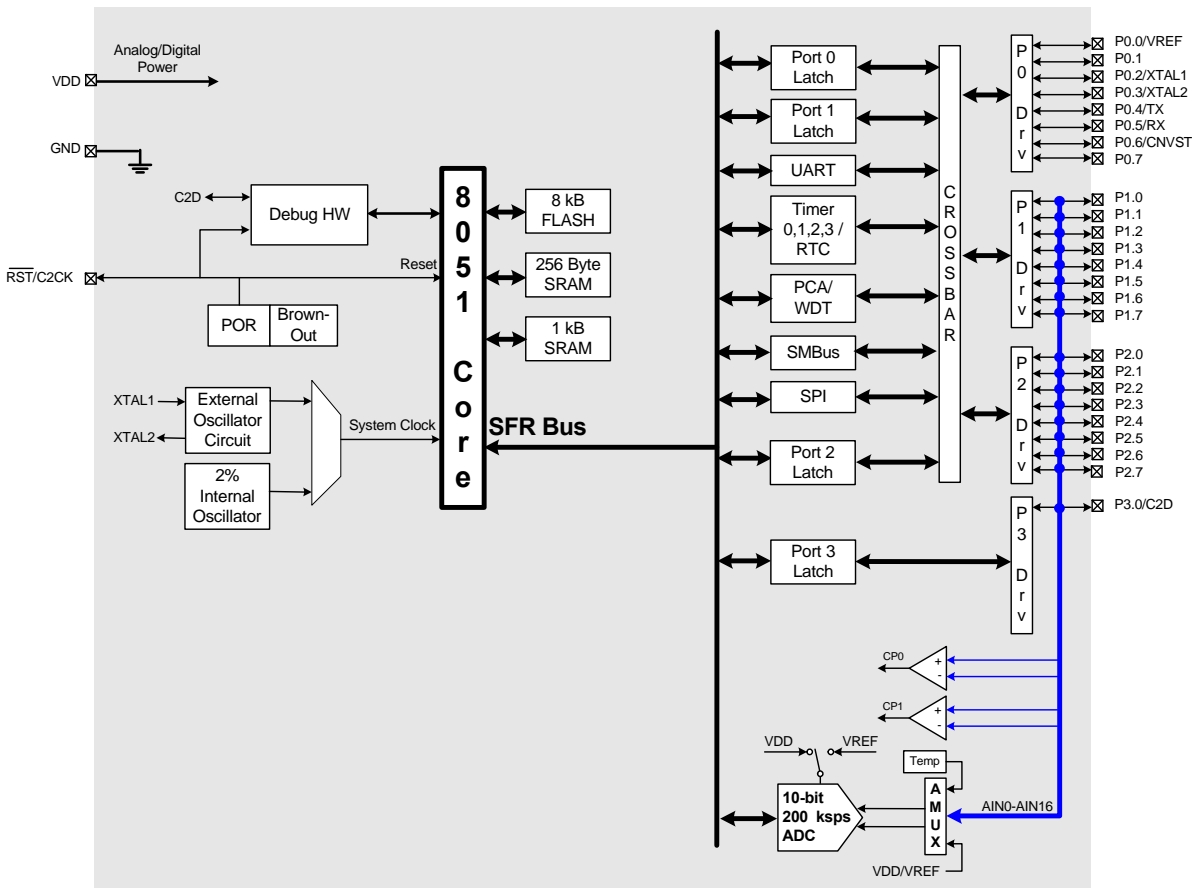
- Typical Operating Current: 7 mA at 25 MHz  
15  $\mu$ A at 32 kHz
- Typical Stop Mode Current: <0.1  $\mu$ A

### Package

- 28-pin QFN (lead-free package)

### Ordering Part Number

- C8051F313-GM



### Analog Peripherals

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### POR/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 1280 bytes data RAM
- 8 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 29 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Realtime clock mode using timer or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

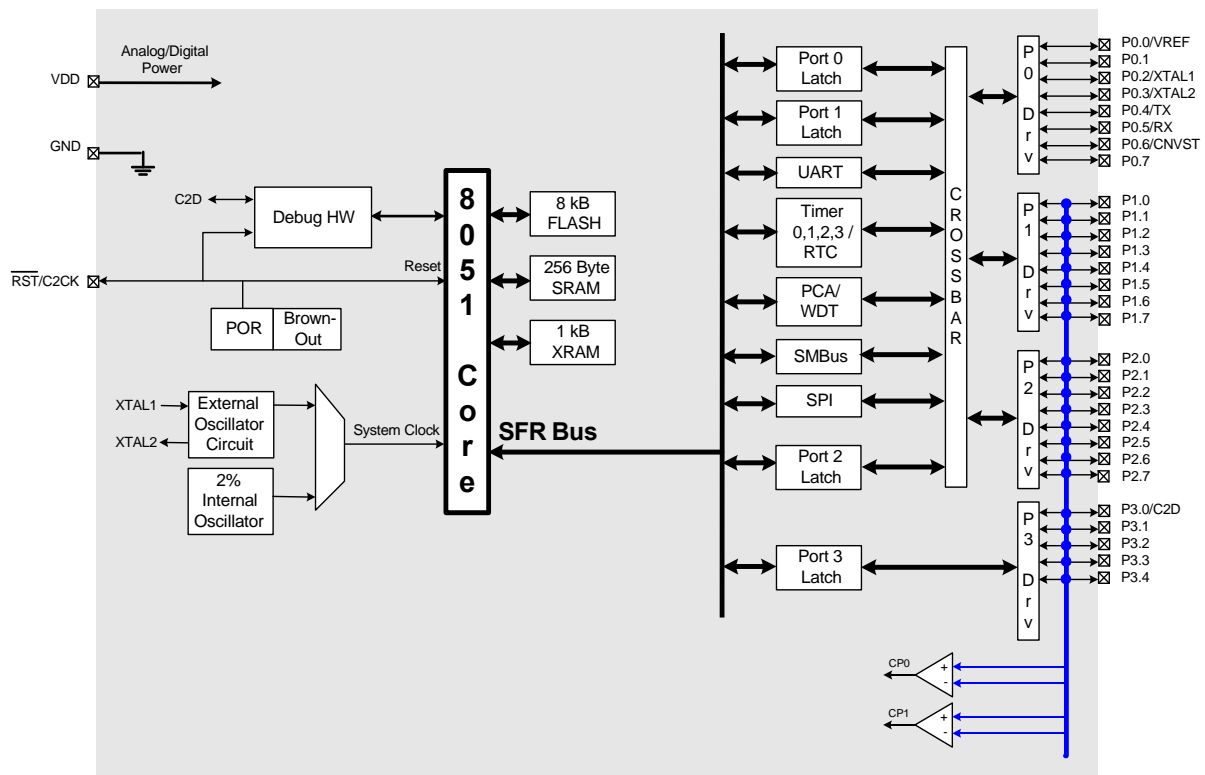
- Typical Operating Current: 7 mA at 25 MHz  
15  $\mu$ A at 32 kHz
- Typical Stop Mode Current: <0.1  $\mu$ A

### Package

- 32-pin LQFP (lead-free package)

### Ordering Part Number

- C8051F314-GQ



### Analog Peripherals

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### POR/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 1280 bytes internal data RAM (256 + 1 k)
- 8 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 25 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Realtime clock mode using timer or PCA

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

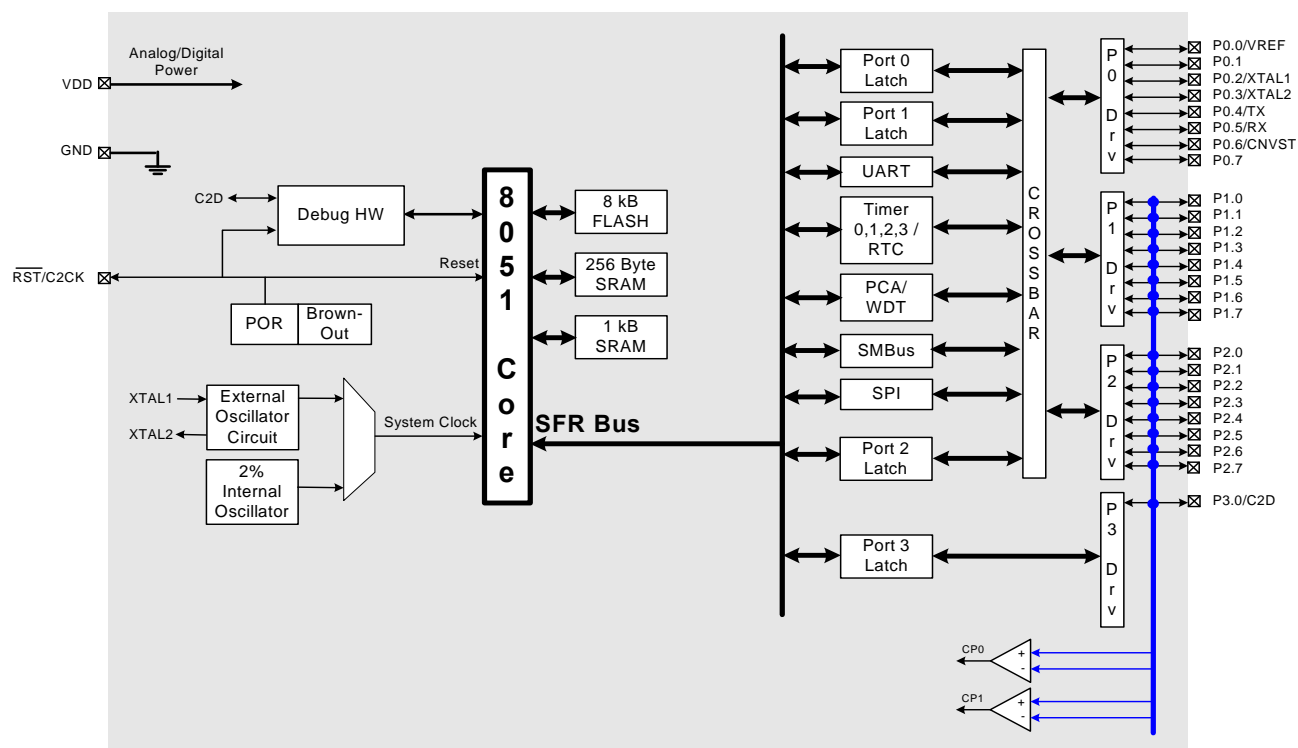
- Typical Operating Current: 7 mA at 25 MHz  
15  $\mu$ A at 32 kHz
- Typical Stop Mode Current: <0.1  $\mu$ A

### Package

- 28-pin QFN (lead-free package)

### Ordering Part Number

- C8051F315-GM





### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksps
- Up to 13 external inputs
- VREF from external pin or VDD
- Internal or external start of conversion sources
- Data-dependent windowed interrupt generator

#### Built-in temperature sensor ( $\pm 3$ °C)

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current ( $<0.5$   $\mu$ A)

#### POR/Brown-Out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 1280 bytes data RAM (1024 + 256)
- 16 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 21 port I/O; all are 5 V tolerant
- 1 Enhanced Hardware SMBus™ (I<sup>2</sup>C™ compatible) and UART serial port
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode for maximum power saving

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

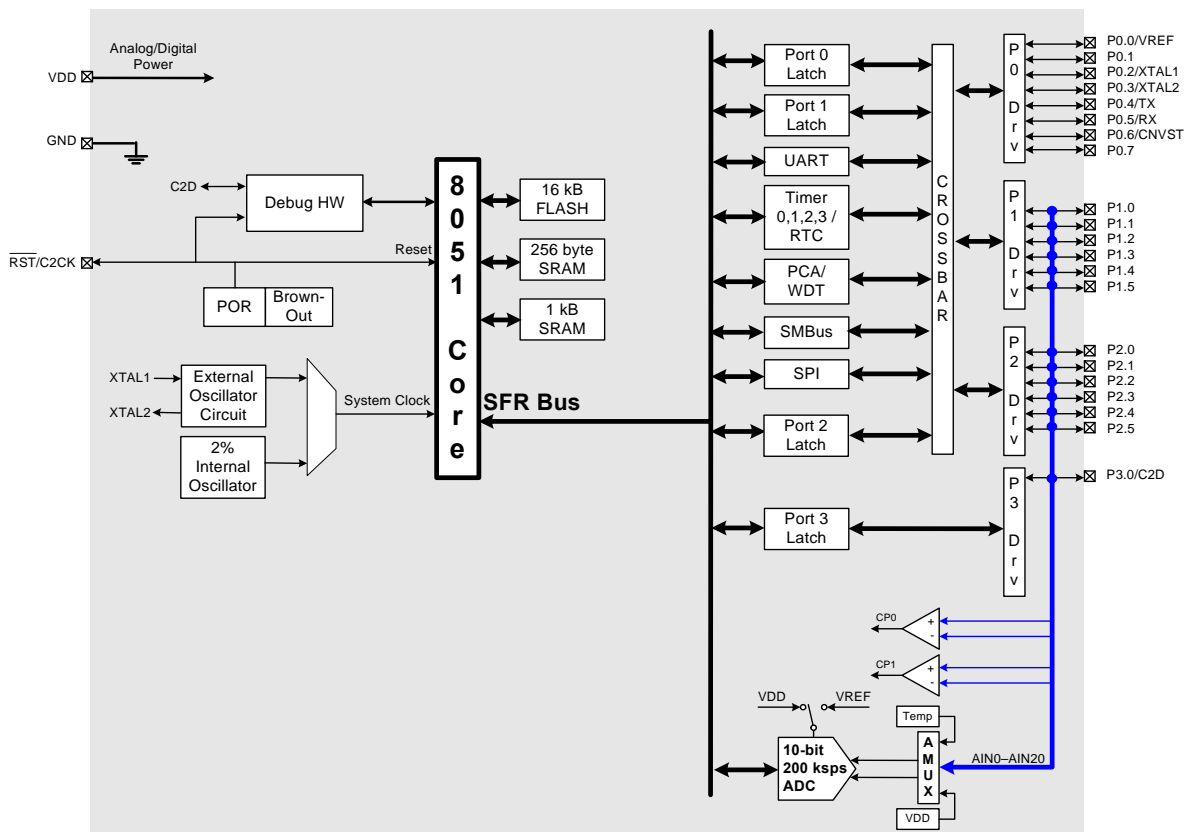
- Typical operating current: 5 mA at 25 MHz
- Typical: 11  $\mu$ A at 32 kHz
- Target stop mode current:  $<0.1$   $\mu$ A

### Package

- 24-pin QFN (lead-free package)

### Ordering Part Number

- C8051F316-GM



### Analog Peripherals

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (<0.5  $\mu$ A)

#### POR/Brown-Out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack

Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 1280 bytes data RAM (1024 + 256)
- 16 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 21 port I/O; all are 5 V tolerant
- 1 Enhanced Hardware SMBus™ (I<sup>2</sup>C™ compatible) and UART serial port
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode for maximum power saving

### Clock Sources

- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

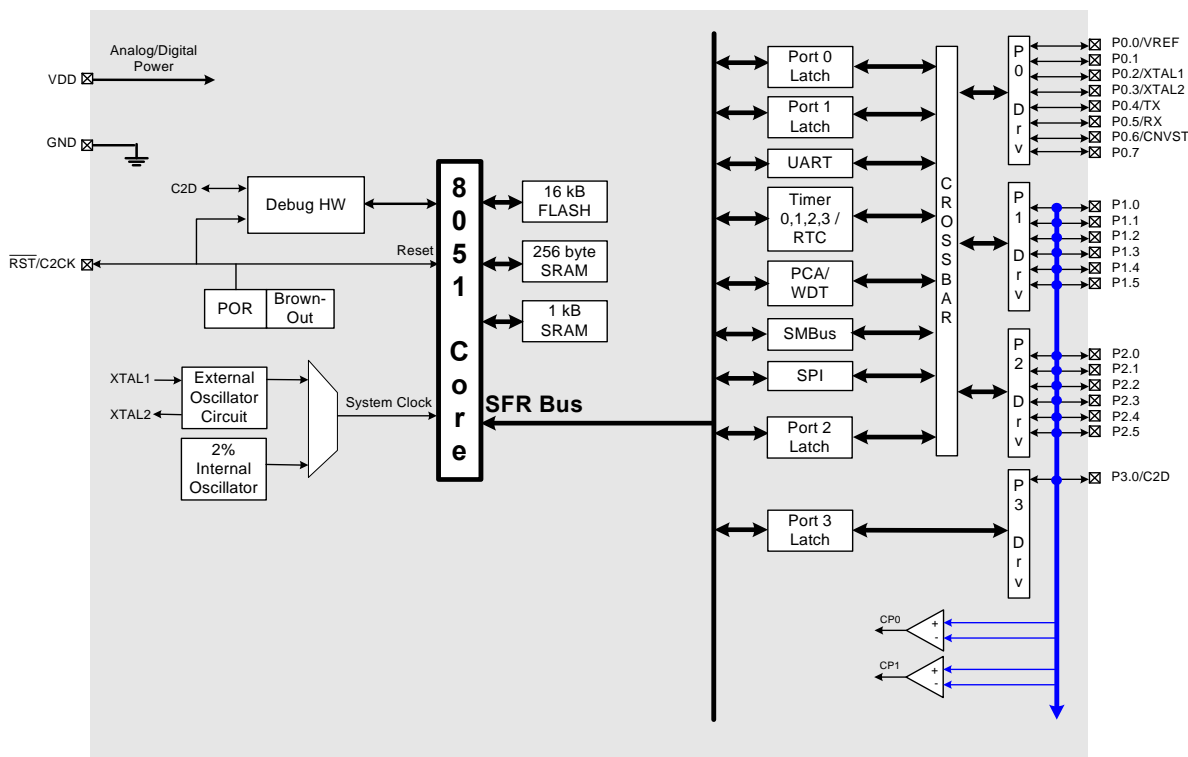
- Typical operating current: 5 mA at 25 MHz
- Typical: 11  $\mu$ A at 32 kHz
- Target stop mode current: <0.1  $\mu$ A

### Package

- 24-pin QFN (lead-free package)

### Ordering Part Number

- C8051F317-GM



### Analog Peripherals

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 16 external inputs; programmable as single-ended or differential
- Reference from internal  $V_{REF}$ ,  $V_{DD}$ , or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor ( $\pm 3^\circ\text{C}$ )

#### 10-bit DAC (Current Mode)

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu\text{A}$ )

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range:  $-40$  to  $+85^\circ\text{C}$**

### High-Speed 8051 $\mu\text{C}$ Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 17 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

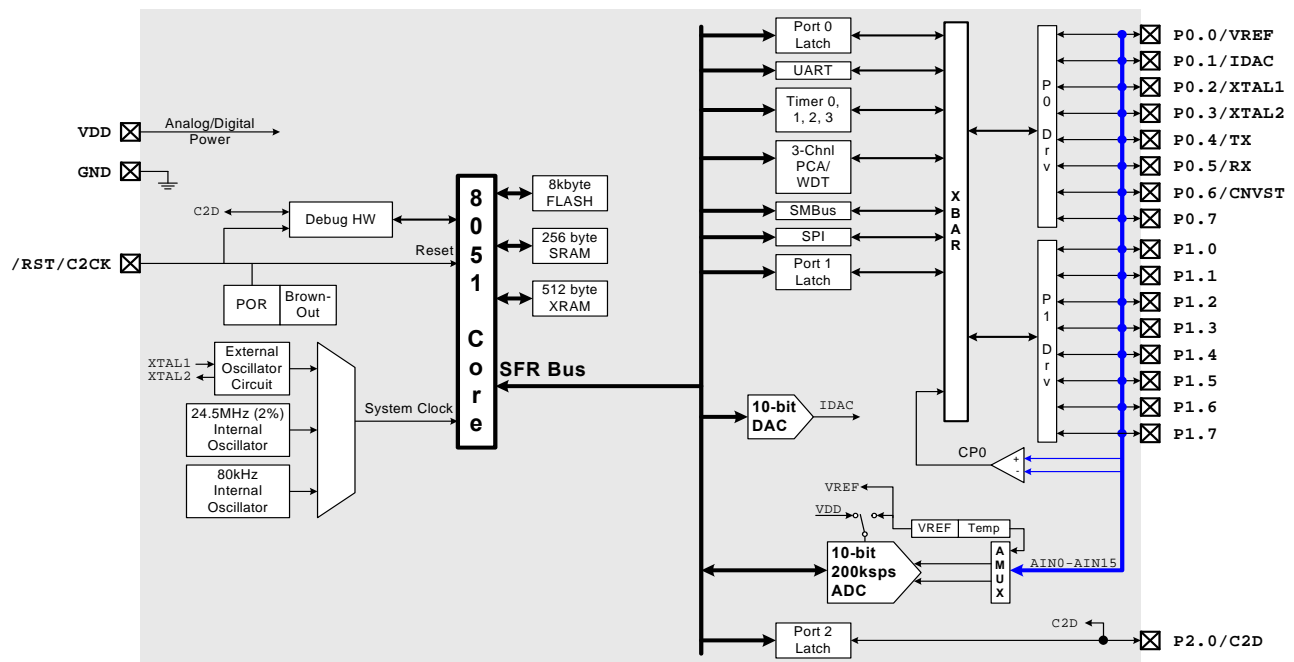
- Typical operating current: 6.4 mA at 25 MHz  
9  $\mu\text{A}$  at 32 kHz
- Typical stop mode current:  $<0.1 \mu\text{A}$

### Package

- 20-pin QFN (lead-free package)

### Ordering Part Number

- C8051F330-GM



### Analog Peripherals

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 16 external inputs; programmable as single-ended or differential
- Reference from internal  $V_{REF}$ ,  $V_{DD}$ , or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor ( $\pm 3$  °C)

#### 10-bit DAC (Current Mode)

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 17 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

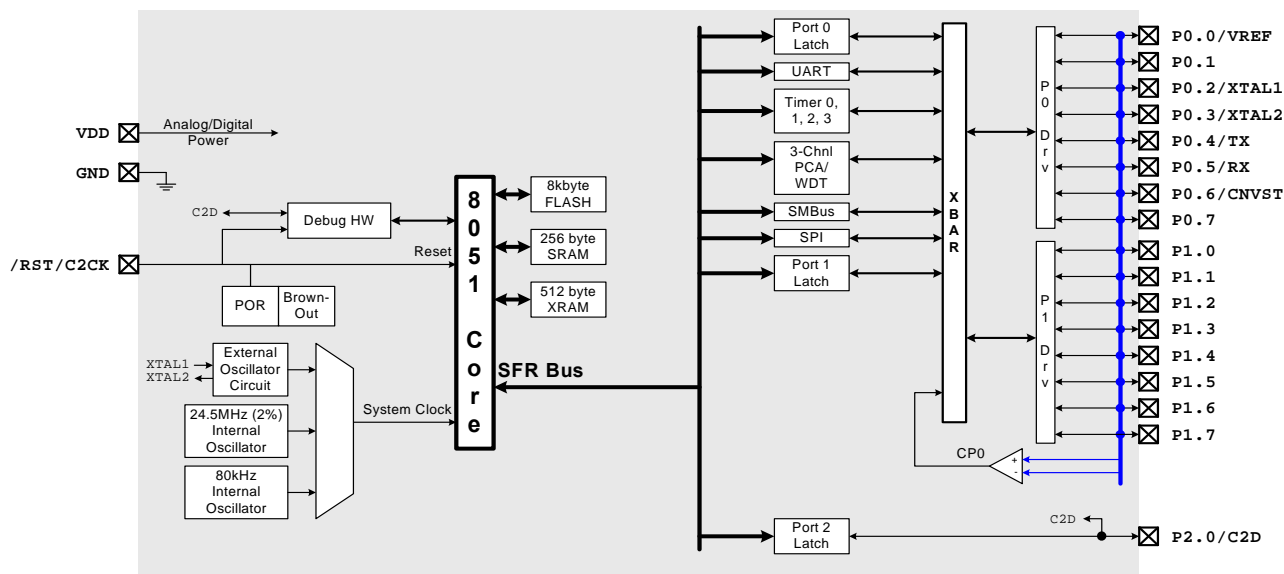
- Typical operating current: 6.4 mA at 25 MHz  
9  $\mu$ A at 32 kHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 20-pin DIP (lead-free package)

### Ordering Part Number

- C8051F330-GP



### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

#### Memory

- 768 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

#### Digital Peripherals

- 17 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

#### Clock Sources

- Two internal oscillators:
  - 25 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

#### Supply Voltage: 2.7 to 3.6 V

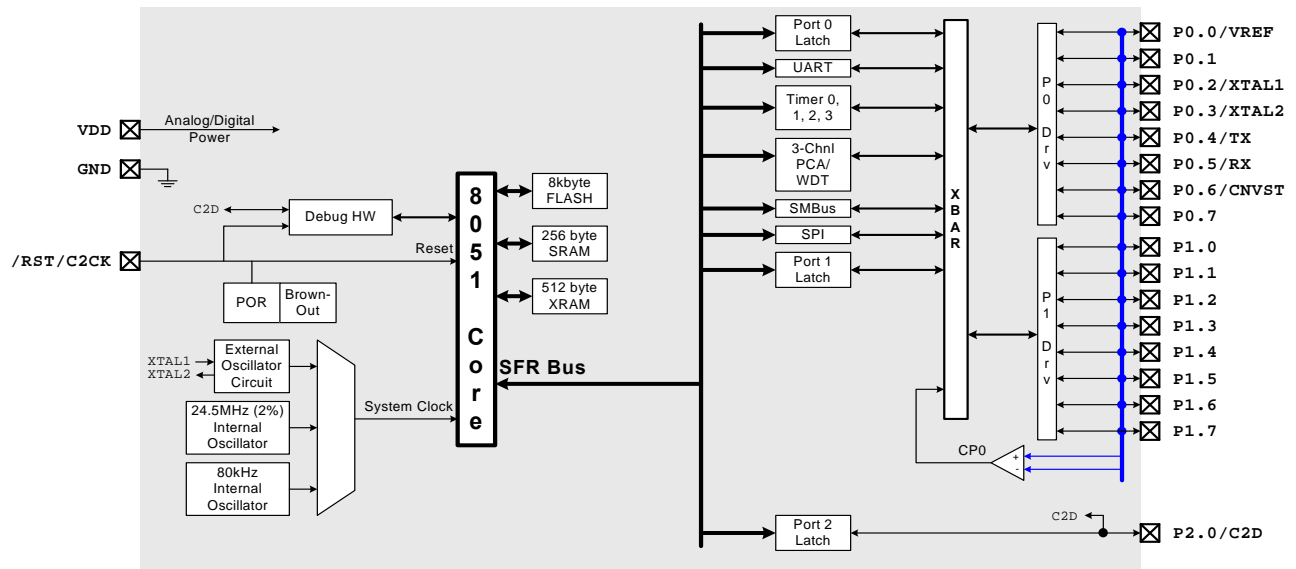
- Typical operating current: 6.4 mA at 25 MHz  
9  $\mu$ A at 32 kHz
- Typical stop mode current: <0.1  $\mu$ A

#### Package

- 20-pin QFN (lead-free package)

#### Ordering Part Number

- C8051F331-GM





### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 4 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 17 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

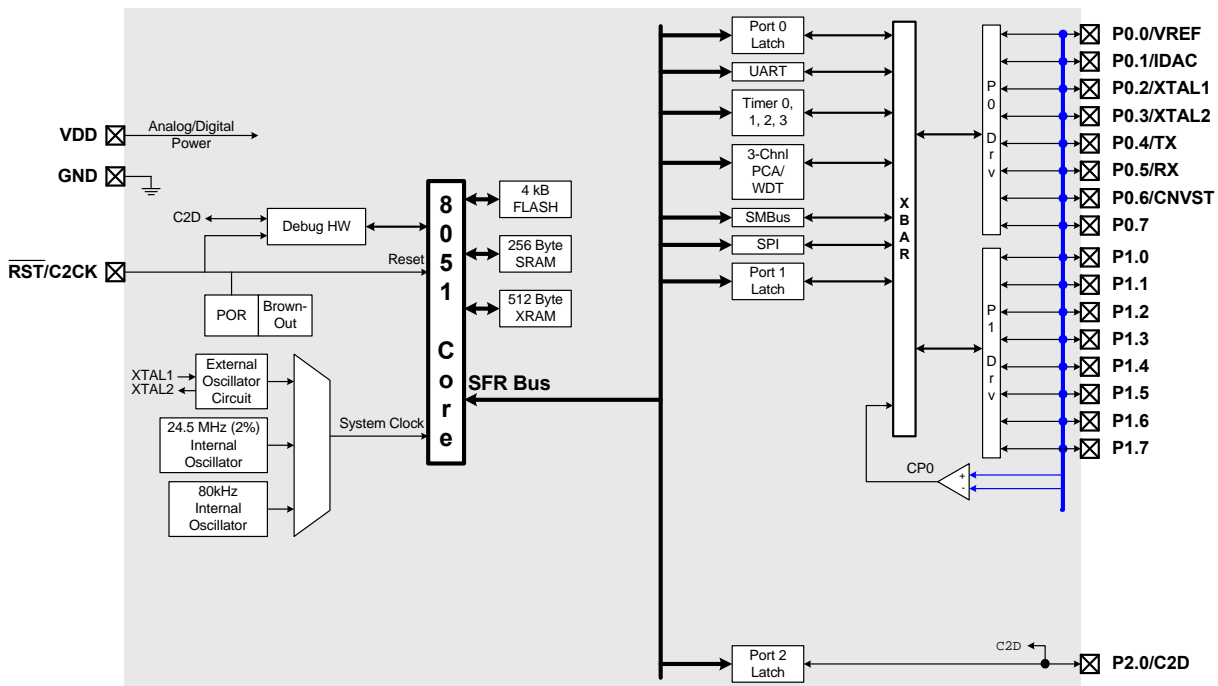
- Typical operating current: 6.4 mA at 25 MHz  
9  $\mu$ A at 32 kHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 20-pin QFN (lead-free package)

### Ordering Part Number

- C8051F333-GM



### Analog Peripherals

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 16 external inputs; programmable as single-ended or differential
- Reference from internal  $V_{REF}$ ,  $V_{DD}$ , or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor ( $\pm 3^\circ\text{C}$ )

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current ( $0.4\ \mu\text{A}$ )

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range:  $-40$  to  $+85^\circ\text{C}$**

### High-Speed 8051 $\mu\text{C}$ Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 2 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 17 port I/O; all are 5 V tolerant
- Hardware SMBus™ ( $I^2\text{C}^{\text{TM}}$  compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

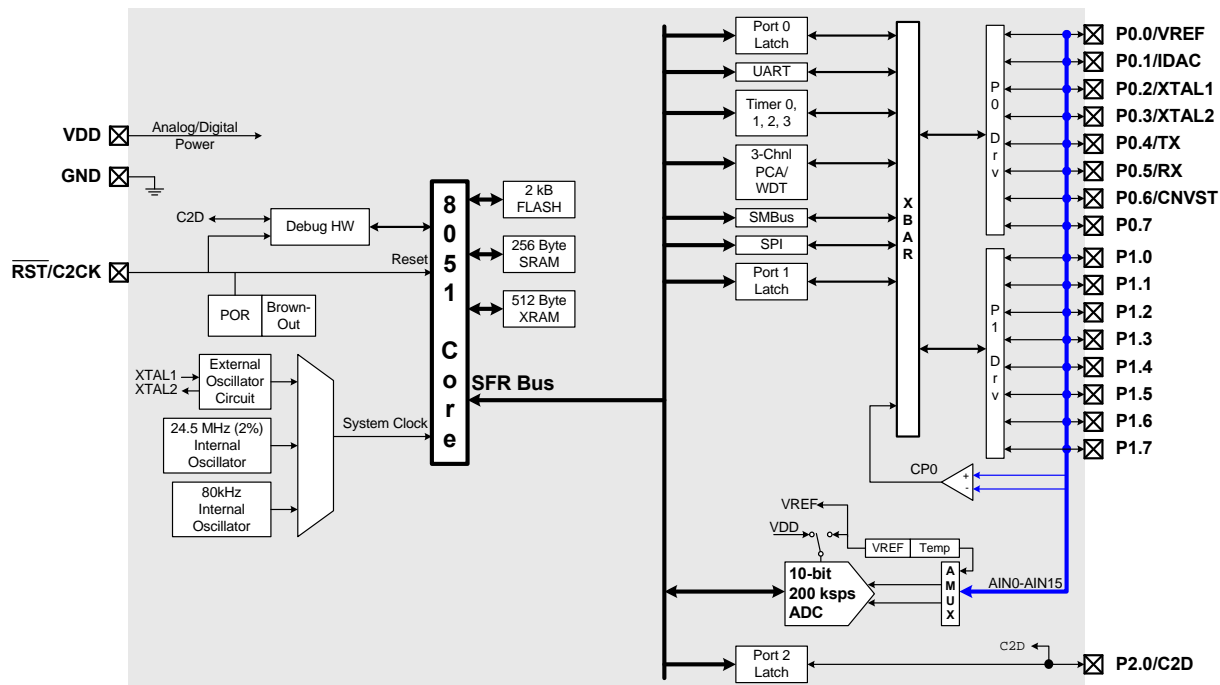
- Typical operating current: 6.4 mA at 25 MHz  
9  $\mu\text{A}$  at 32 kHz
- Typical stop mode current:  $<0.1\ \mu\text{A}$

### Package

- 20-pin QFN (lead-free package)

### Ordering Part Number

- C8051F334-GM





### Analog Peripherals

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current (0.4  $\mu$ A)

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 2 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 17 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Supply Voltage: 2.7 to 3.6 V

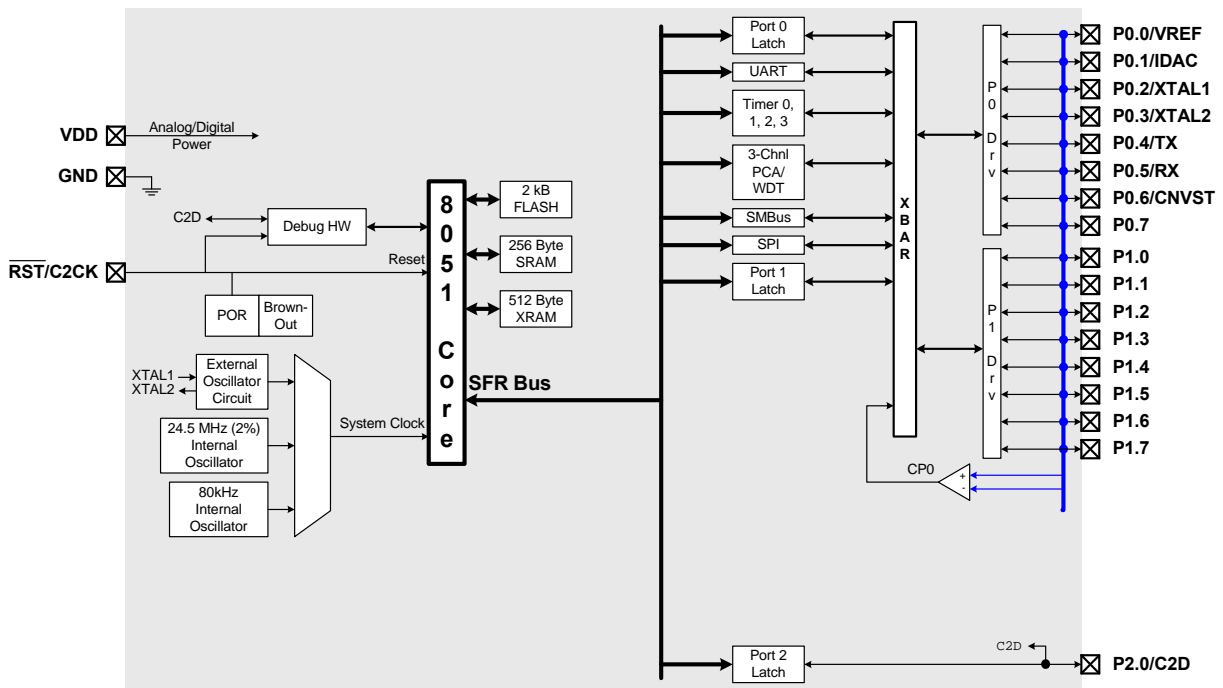
- Typical operating current: 6.4 mA at 25 MHz  
9  $\mu$ A at 32 kHz
- Typical stop mode current: <0.1  $\mu$ A

### Package

- 20-pin QFN (lead-free package)

### Ordering Part Number

- C8051F335-GM



### Analog Peripherals

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 16 external inputs; programmable as single-ended or differential
- Reference from internal  $V_{REF}$ ,  $V_{DD}$ , or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor

#### 10-bit DAC (Current Mode)

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 16 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

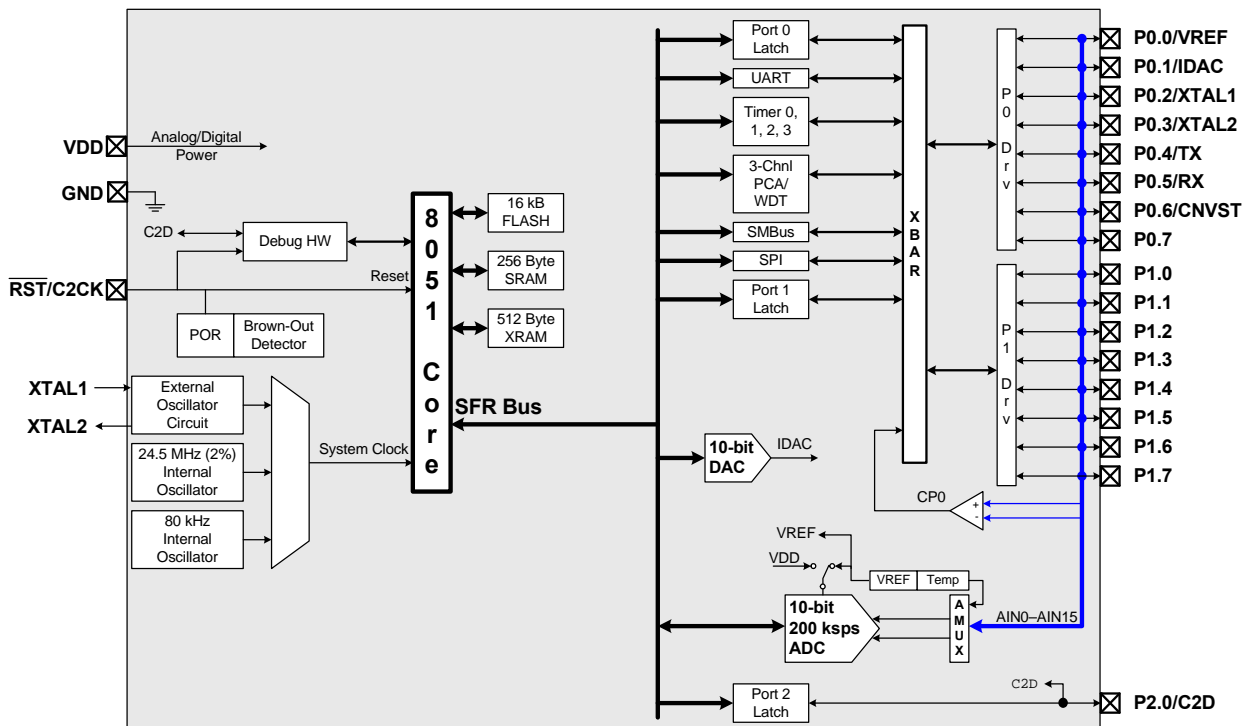
- Up to 21 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and crystalless-UART serial ports available concurrently
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Timer with real-time clock mode
- Clock sources
- Two internal oscillators:
  - Precision 24.5 MHz, 2% accuracy over  $V_{DD}$  and temperature
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly
- Suspend mode for maximum power savings with fast wake-up (<1  $\mu$ s)

**Supply Voltage: 2.7 to 3.6 V**

### Package

- 20-pin QFN

Pin compatible with C8051F33x family of devices



### Analog Peripherals

#### 10-bit DAC (Current Mode)

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Temperature Range: **-40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 16 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

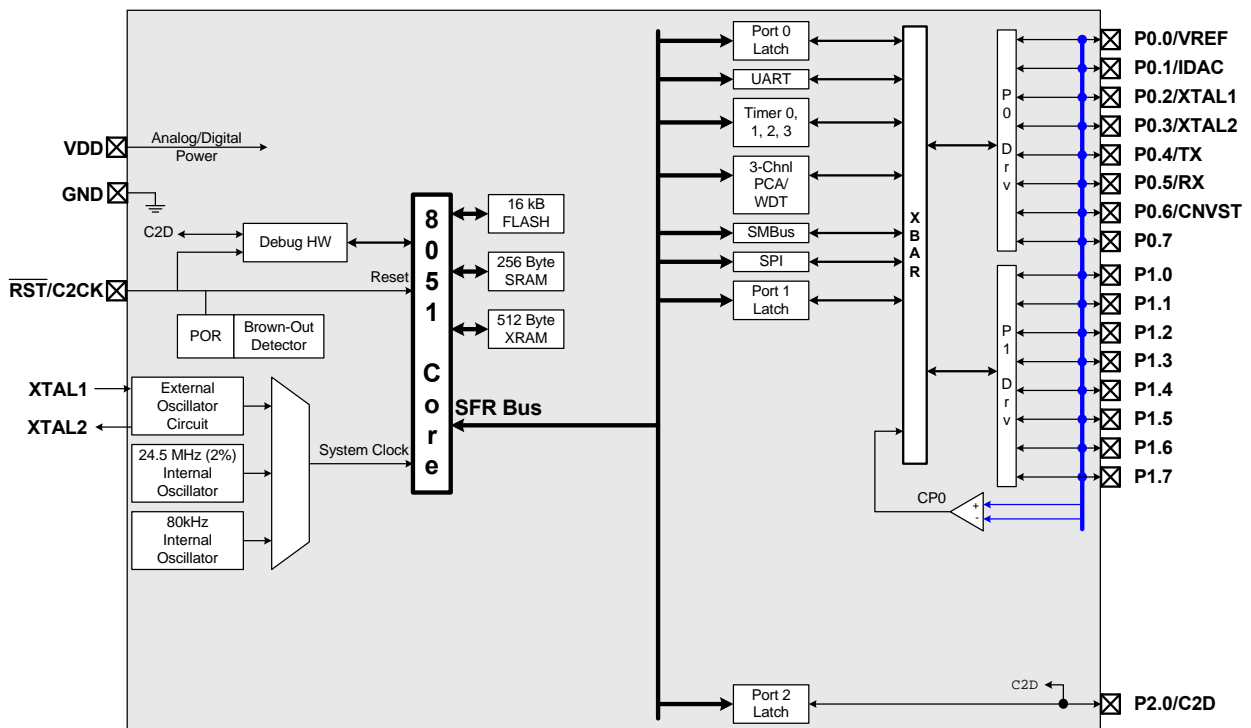
- 17 port I/Os; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and crystalless-UART serial ports available concurrently
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Timer with real-time clock mode
- Clock sources
- Two internal oscillators:
  - Precision 24.5 MHz, 2% accuracy over V<sub>DD</sub> and temperature
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly
- Suspend mode for maximum power savings with fast wake-up (<1 us)

Supply Voltage: **2.7 to 3.6 V**

### Package

- 20-pin QFN

Pin compatible with C8051F33x family of devices



### Analog Peripherals

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 16 external inputs; programmable as single-ended or differential
- Reference from internal  $V_{REF}$ ,  $V_{DD}$ , or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor

#### 10-bit DAC (Current Mode)

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
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- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 16 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

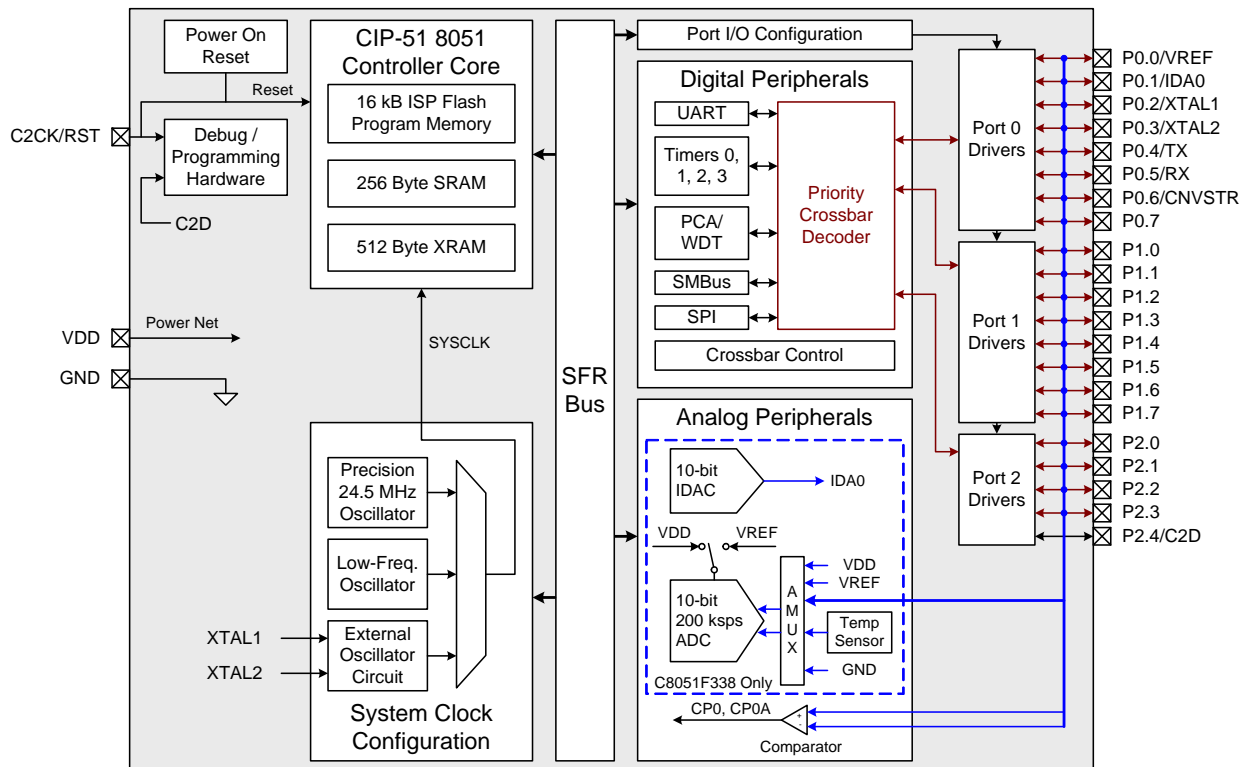
### Digital Peripherals

- 21 port I/O; all are 5 V tolerant
- Hardware SMBus™ ( $I^2C$ ™ compatible), SPI™, and crystalless-UART serial ports available concurrently
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Timer with real-time clock mode
- Clock sources
- Two internal oscillators:
  - Precision 24.5 MHz, 2% accuracy over  $V_{DD}$  and temperature
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly
- Suspend mode for maximum power savings with fast wake-up (<1  $\mu$ s)

**Supply Voltage: 2.7 to 3.6 V**

### Package

24-pin QFN



### Analog Peripherals

#### 10-bit DAC (Current Mode)

#### Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
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- Inspect/modify memory, registers, and stack
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**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes data RAM
- 16 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

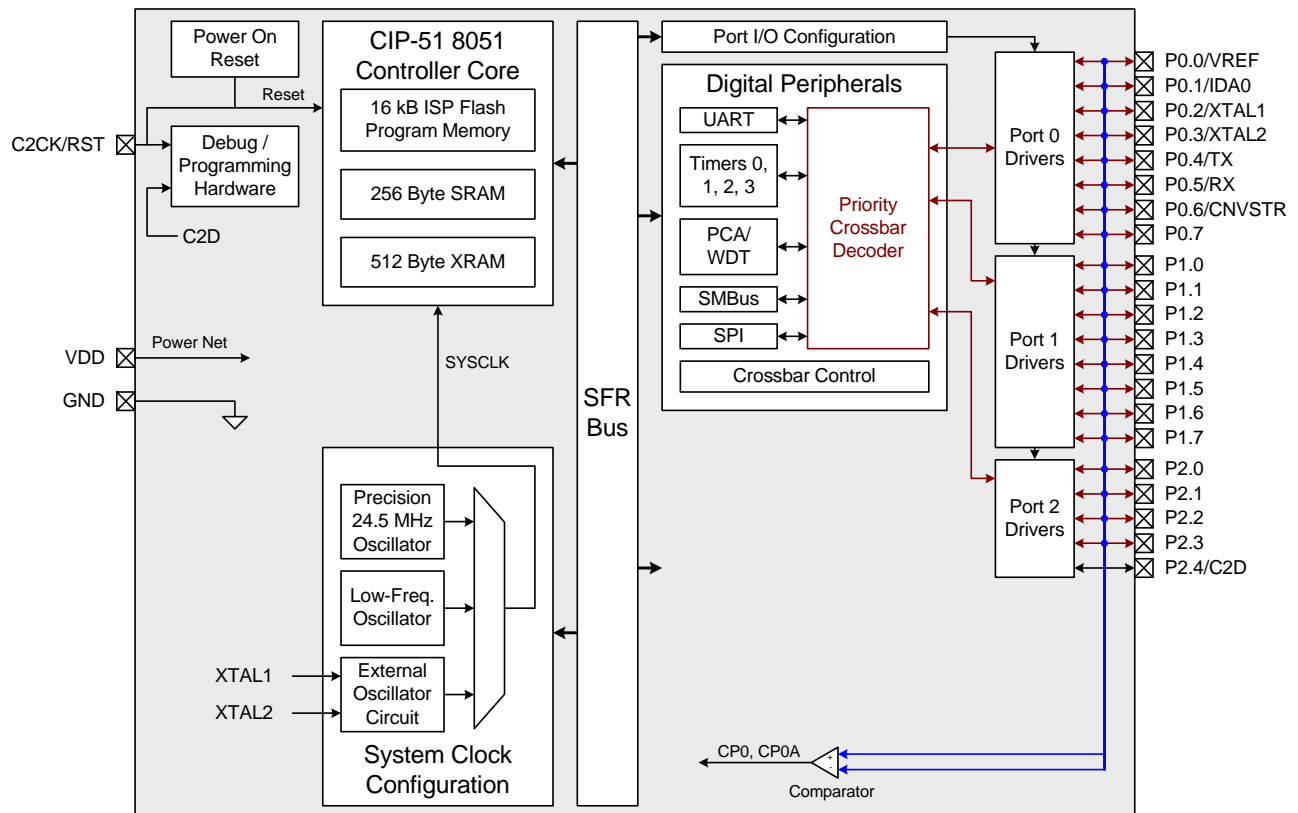
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- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly
- Suspend mode for maximum power savings with fast wake-up (<1  $\mu$ s)

**Supply Voltage: 2.7 to 3.6 V**

### Package

24-pin QFN



### Analog Peripherals

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 17 external inputs; programmable as single-ended or differential
- Reference from internal V<sub>REF</sub>, V<sub>DD</sub>, or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor ( $\pm 3$  °C)

#### 10-bit DAC (Current Mode)

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 1280 bytes data RAM with external memory I/F
- 32 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 39 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- On-Chip programmable PLL: up to 100 MHz

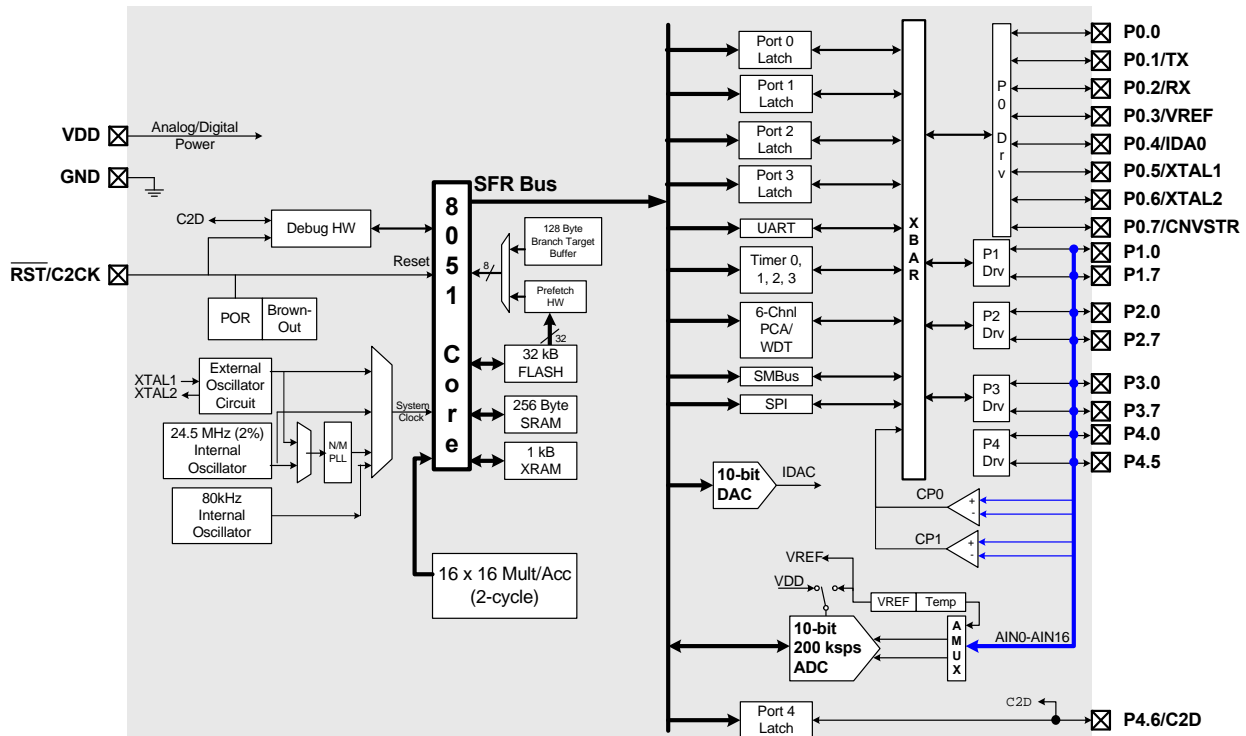
**Supply Voltage: 2.7 to 3.6 V**

### Package

- 48-pin TQFP

### Ordering Part Number

- C8051F360-GQ



### Analog Peripherals

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 21 external inputs; programmable as single-ended or differential
- Reference from internal  $V_{REF}$ ,  $V_{DD}$ , or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor ( $\pm 3$  °C)

#### 10-bit DAC (Current Mode)

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 1280 bytes data RAM
- 32 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 27 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- On-Chip programmable PLL: up to 100 MHz

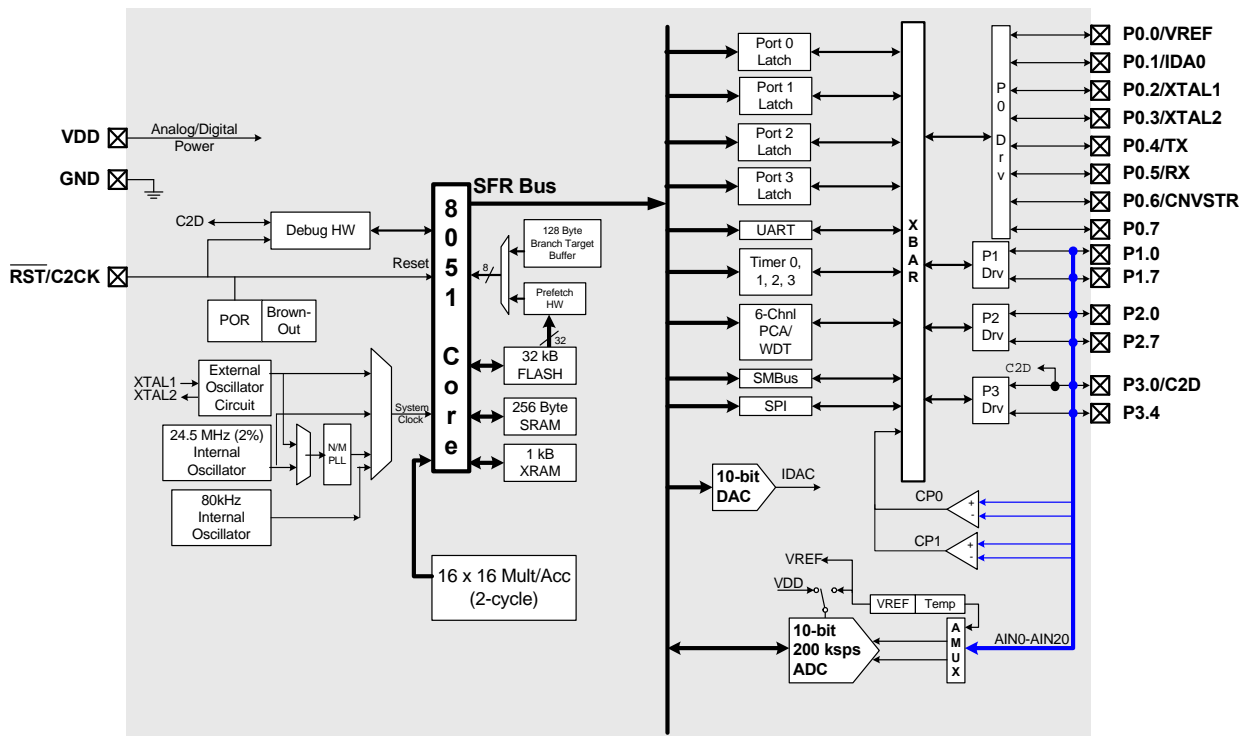
### Supply Voltage: 2.7 to 3.6 V

### Package

- 32-pin LQFP
- Pin compatible with C8051F310

### Ordering Part Number

- C8051F361-GQ



### Analog Peripherals

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 17 external inputs; programmable as single-ended or differential
- Reference from internal V<sub>REF</sub>, V<sub>DD</sub>, or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor ( $\pm 3$  °C)

#### 10-bit DAC (Current Mode)

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 1280 bytes data RAM
- 32 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 24 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- On-Chip programmable PLL: up to 100 MHz

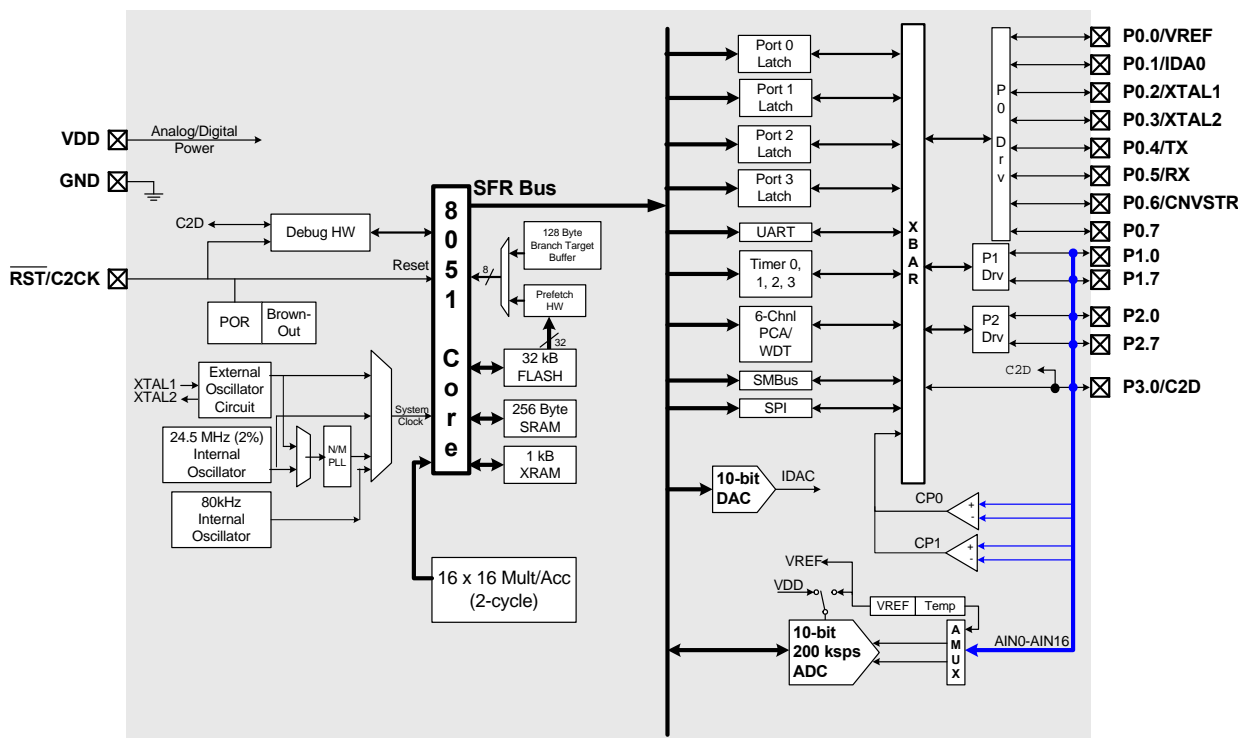
**Supply Voltage: 2.7 to 3.6 V**

### Package

- 28-pin QFN
- Pin compatible with C8051F311

### Ordering Part Number

- C8051F362-GM





### Analog Peripherals

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 1280 bytes data RAM with external memory I/F
- 32 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 39 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- On-Chip programmable PLL: up to 100 MHz

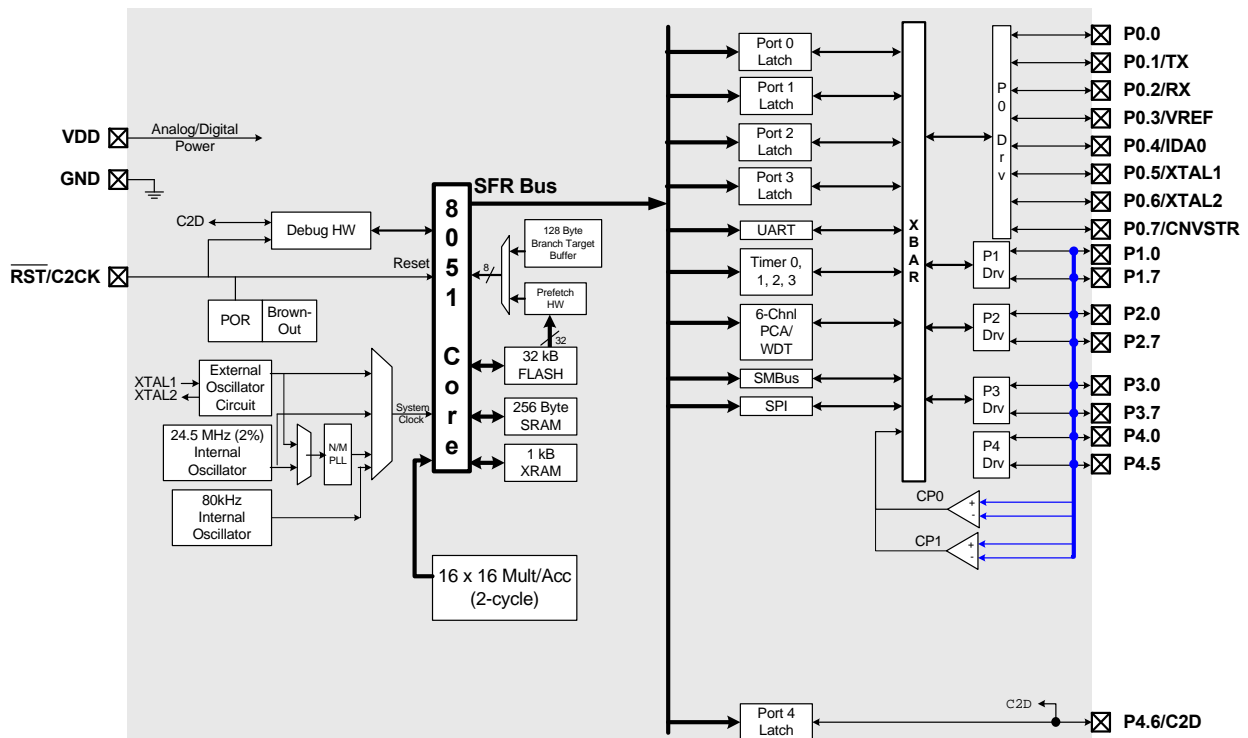
**Supply Voltage: 2.7 to 3.6 V**

### Package

- 48-pin TQFP

### Ordering Part Number

- C8051F363-GQ



### Analog Peripherals

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 1280 bytes data RAM
- 32 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 27 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- On-Chip programmable PLL: up to 100 MHz

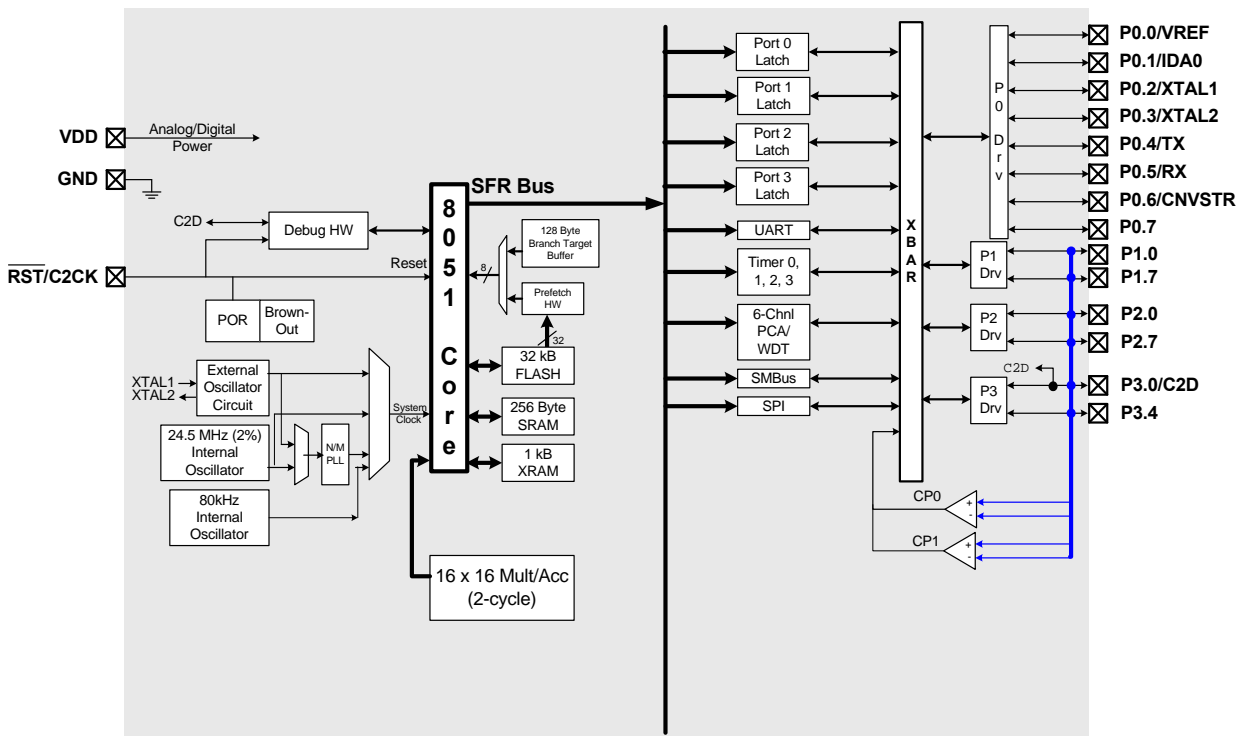
**Supply Voltage: 2.7 to 3.6 V**

### Package

- 32-pin LQFP
- Pin compatible with C8051F310

### Ordering Part Number

- C8051F364-GQ



### Analog Peripherals

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 1280 bytes data RAM
- 32 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 24 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- On-Chip programmable PLL: up to 100 MHz

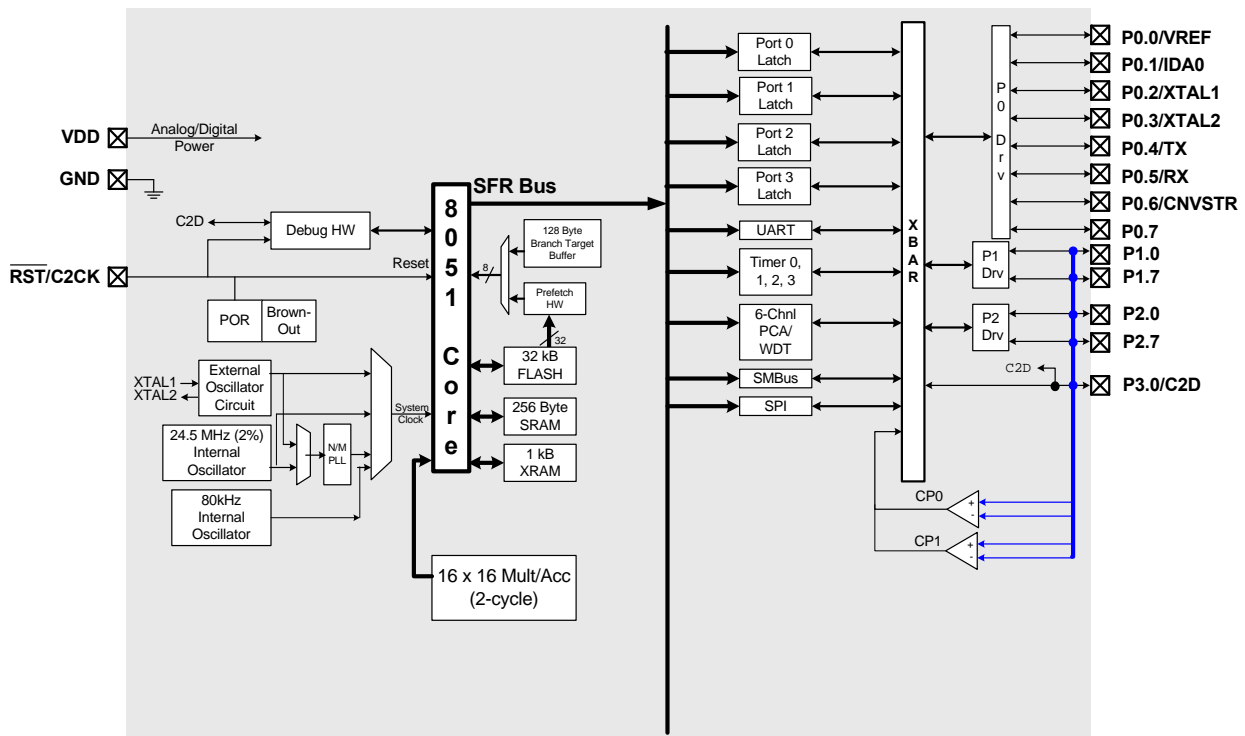
### Supply Voltage: 2.7 to 3.6 V

### Package

- 28-pin QFN
- Pin compatible with C8051F311

### Ordering Part Number

- C8051F365-GM



### Analog Peripherals

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 21 external inputs; programmable as single-ended or differential
- Reference from internal V<sub>REF</sub>, V<sub>DD</sub>, or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor (±3 °C)

#### 10-bit DAC (Current Mode)

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 1280 bytes data RAM
- 32 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 29 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- On-Chip programmable PLL: up to 50 MHz

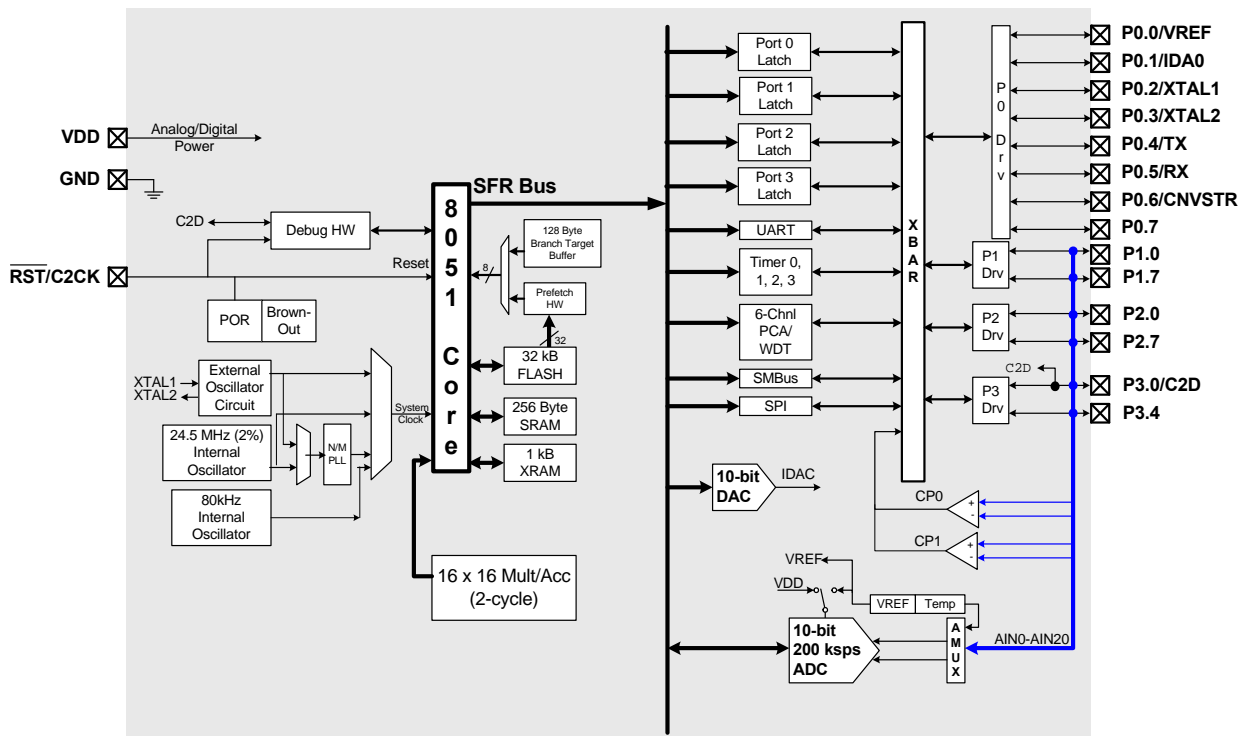
**Supply Voltage: 2.7 to 3.6 V**

### Package

- 32-pin LQFP
- Pin compatible with C8051F310

### Ordering Part Number

- C8051F366-GQ



### Analog Peripherals

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 17 external inputs; programmable as single-ended or differential
- Reference from internal  $V_{REF}$ ,  $V_{DD}$ , or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor ( $\pm 3\text{ }^{\circ}\text{C}$ )

#### 10-bit DAC (Current Mode)

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range:  $-40$  to  $+85\text{ }^{\circ}\text{C}$**

### High-Speed 8051 $\mu\text{C}$ Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 1280 bytes data RAM
- 32 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 25 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- On-Chip programmable PLL: up to 50 MHz

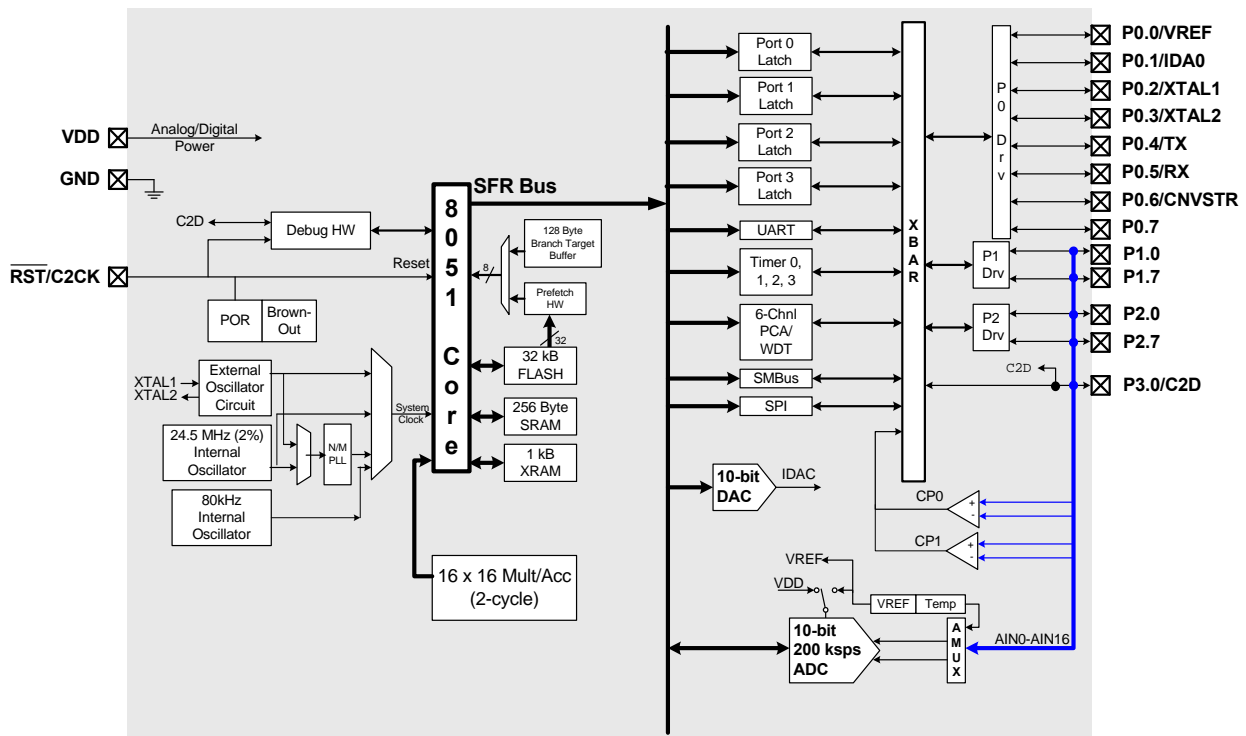
### Supply Voltage: 2.7 to 3.6 V

### Package

- 28-pin QFN
- Pin compatible with C8051F311

### Ordering Part Number

- C8051F367-GM



### Analog Peripherals

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 21 external inputs; programmable as single-ended or differential
- Reference from internal V<sub>REF</sub>, V<sub>DD</sub>, or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor ( $\pm 3$  °C)

#### 10-bit DAC (Current Mode)

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 1280 bytes data RAM
- 16 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 29 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- On-Chip programmable PLL: up to 50 MHz

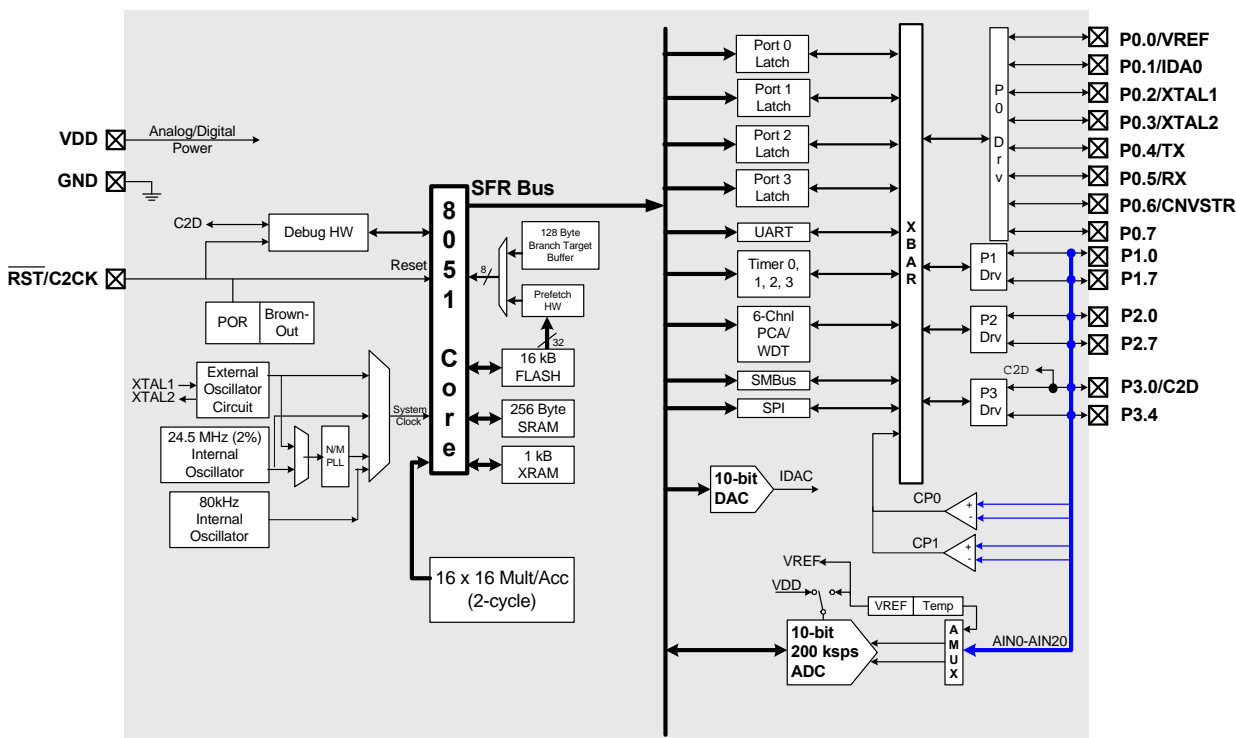
**Supply Voltage: 2.7 to 3.6 V**

### Package

- 32-pin LQFP
- Pin compatible with C8051F310

### Ordering Part Number

- C8051F368-GQ



### Analog Peripherals

#### 10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 17 external inputs; programmable as single-ended or differential
- Reference from internal  $V_{REF}$ ,  $V_{DD}$ , or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor ( $\pm 3$  °C)

#### 10-bit DAC (Current Mode)

#### Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

### Memory

- 1280 bytes data RAM
- 16 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

### Digital Peripherals

- 25 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz, 2% accuracy supports UART operation
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- On-Chip programmable PLL: up to 50 MHz

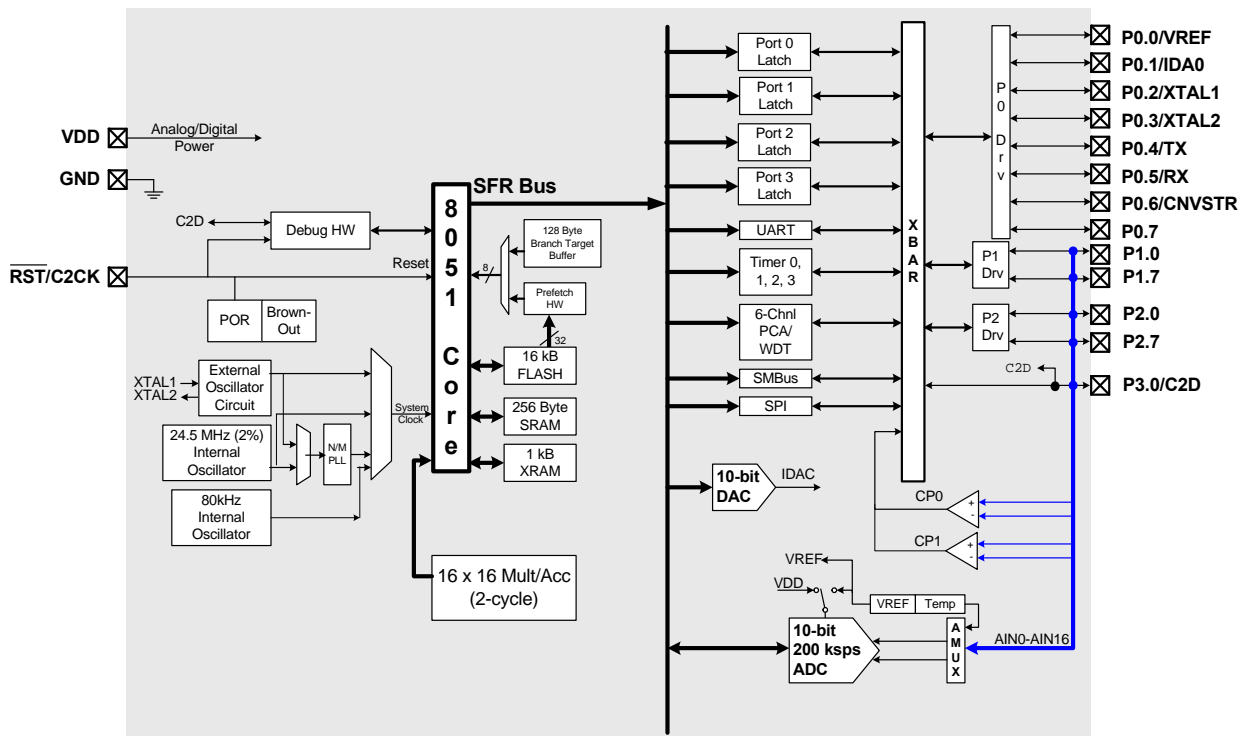
### Supply Voltage: 2.7 to 3.6 V

### Package

- 28-pin QFN
- Pin compatible with C8051F311

### Ordering Part Number

- C8051F369-GM



### Analog Peripherals

#### 12-bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable Throughput up to 200 ksp/s
- Up to 24 External Inputs; programmable as single-ended or differential
- Data Dependent Windowed Interrupt Generator
- Built-in Temperature Sensor ( $\pm 3$  °C)
- Internal Voltage Reference—1.5 V, 2.2 V (programmable)

#### Two 12-Bit Current Mode DACs

#### Two Comparators

- Programmable hysteresis values and response time
- Configurable to generate interrupts or reset

#### POR/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

#### smaRTClock™

- Battery switchover circuit
- Back-up power supply
- Oscillator failure detect
- Operates down to 1 V

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 CPU

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz system clock
- Expanded interrupt handler

### Memory

- 2304 bytes data RAM
- 32 kB Flash; in-system programmable in 512-Byte Sectors; Full Read/Write/Erase Functionality at  $2.25 V_{DD}$
- 64 bytes battery-backed RAM

### Digital Peripherals

- 24 port I/O; up to 5.25 V tolerance
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- 16-bit programmable counter array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers

### Clock Sources

- Internal Oscillators: 24.5 MHz, 2% Accuracy Supports UART Operation; Clock Multiplier up to 50 MHz
- External Oscillator1: Crystal, RC, C, or Clock (1 or 2 pin modes)
- External Oscillator2: 32 kHz Crystal or C, 5  $\mu$ A
- Fast wake up from suspend mode in <1  $\mu$ s

### Supply Voltage: 2.0–5.25 V

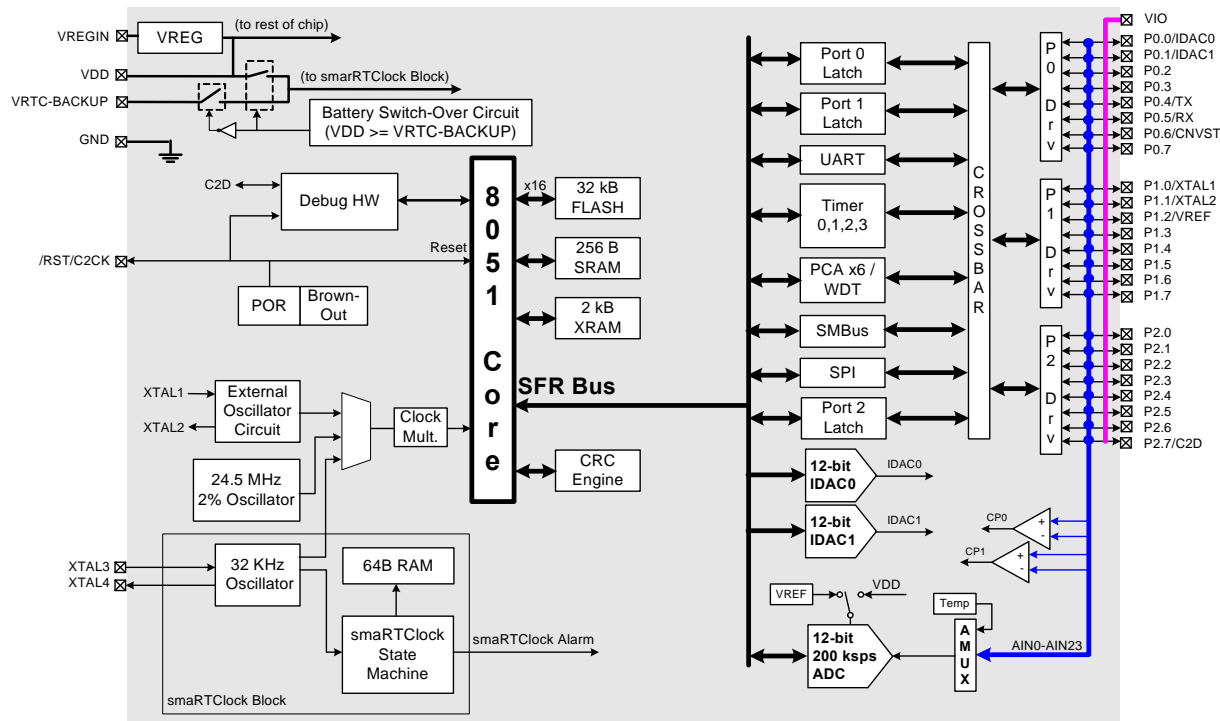
- Built-in LDO regulator: 2.1 V or 2.5 V

### Package

- 32-pin LQFP (lead-free package)

### Ordering Part Number

- C8051F410-GQ





### Analog Peripherals

#### 12-bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable Throughput up to 200 ksps
- Up to 24 External Inputs; programmable as single-ended or differential
- Data Dependent Windowed Interrupt Generator
- Built-in Temperature Sensor ( $\pm 3$  °C)
- Internal Voltage Reference—1.5 V, 2.2 V (programmable)

#### Two 12-Bit Current Mode DACs

#### Two Comparators

- Programmable hysteresis values and response time
- Configurable to generate interrupts or reset

#### POR/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

#### smaRTClock™

- Battery switchover circuit
- Back-up power supply
- Oscillator failure detect
- Operates down to 1 V

Temperature Range: **-40 to +85 °C**

### High-Speed 8051 CPU

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz system clock
- Expanded interrupt handler

### Memory

- 2304 bytes data RAM
- 32 kB Flash; in-system programmable in 512-Byte Sectors; Full Read/Write/Erase Functionality at  $2.25 V_{DD}$
- 64 bytes battery-backed RAM

### Digital Peripherals

- 24 port I/O; up to 5.25 V tolerance
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- 16-bit programmable counter array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers

### Clock Sources

- Internal Oscillators: 24.5 MHz, 2% Accuracy Supports UART Operation; Clock Multiplier up to 50 MHz
- External Oscillator1: Crystal, RC, C, or Clock (1 or 2 pin modes)
- External Oscillator2: 32 kHz Crystal or C, 5  $\mu$ A
- Fast wake up from suspend mode in  $< 1 \mu$ s

### Supply Voltage: 2.0–5.25 V

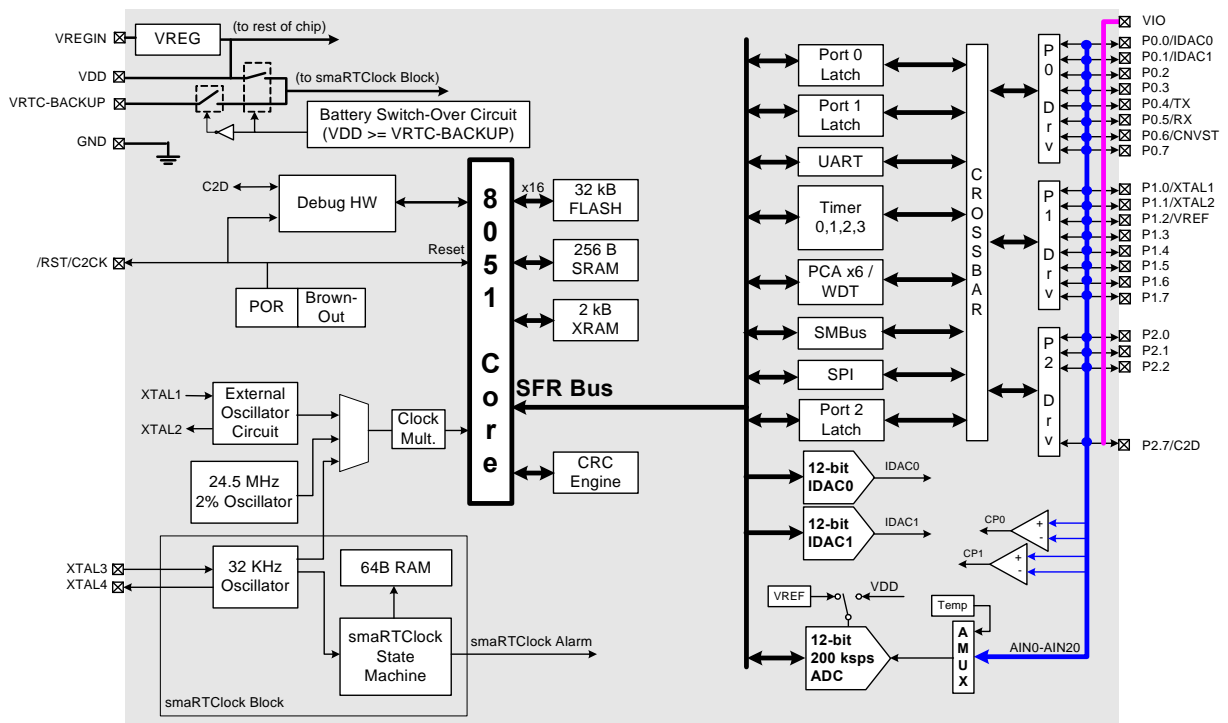
- Built-in LDO regulator: 2.1 V or 2.5 V

### Package

- 28-pin QFN (lead-free package)

### Ordering Part Number

- C8051F411-GM



### Analog Peripherals

#### 12-bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable Throughput up to 200 ksps
- Up to 24 External Inputs; programmable as single-ended or differential
- Data Dependent Windowed Interrupt Generator
- Built-in Temperature Sensor ( $\pm 3$  °C)
- Internal Voltage Reference—1.5 V, 2.2 V (programmable)

#### Two 12-Bit Current Mode DACs

#### Two Comparators

- Programmable hysteresis values and response time
- Configurable to generate interrupts or reset

#### POR/Brown-out Detector

#### On-Chip Debug

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#### smaRTClock™

- Battery switchover circuit
- Back-up power supply
- Oscillator failure detect
- Operates down to 1 V

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 CPU

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz system clock
- Expanded interrupt handler

### Memory

- 2304 bytes data RAM
- 16 kB Flash; in-system programmable in 512-Byte Sectors; Full Read/Write/Erase Functionality at 2.25 V<sub>DD</sub>
- 64 bytes battery-backed RAM

### Digital Peripherals

- 24 port I/O; up to 5.25 V tolerance
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- 16-bit programmable counter array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers

### Clock Sources

- Internal Oscillators: 24.5 MHz, 2% Accuracy Supports UART Operation; Clock Multiplier up to 50 MHz
- External Oscillator1: Crystal, RC, C, or Clock (1 or 2 pin modes)
- External Oscillator2: 32 kHz Crystal or C, 5  $\mu$ A
- Fast wake up from suspend mode in <1  $\mu$ s

### Supply Voltage: 2.0–5.25 V

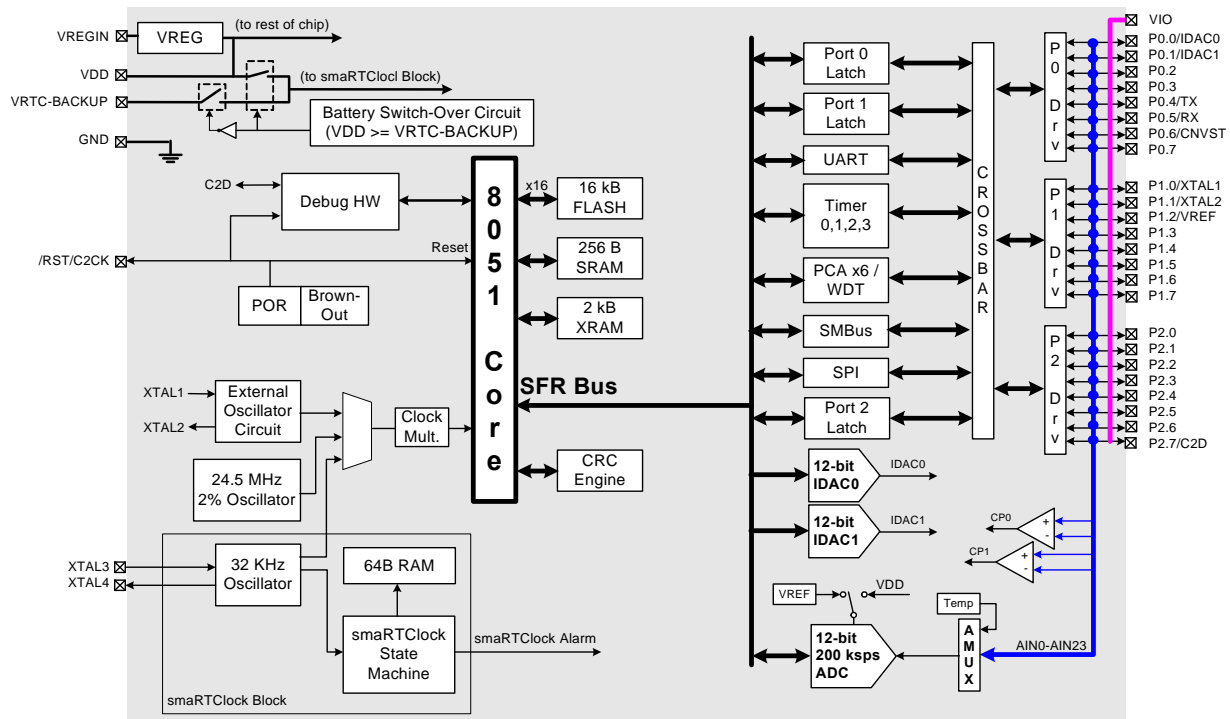
- Built-in LDO regulator: 2.1 V or 2.5 V

### Package

- 32-pin LQFP (lead-free package)

### Ordering Part Number

- C8051F412-GQ



### Analog Peripherals

#### 12-bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable Throughput up to 200 ksps
- Up to 24 External Inputs; programmable as single-ended or differential
- Data Dependent Windowed Interrupt Generator
- Built-in Temperature Sensor ( $\pm 3$  °C)
- Internal Voltage Reference—1.5 V, 2.2 V (programmable)

#### Two 12-Bit Current Mode DACs

#### Two Comparators

- Programmable hysteresis values and response time
- Configurable to generate interrupts or reset

#### POR/Brown-out Detector

#### On-Chip Debug

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- Battery switchover circuit
- Back-up power supply
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### High-Speed 8051 CPU

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
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- Expanded interrupt handler

### Memory

- 2304 bytes data RAM
- 16 kB Flash; in-system programmable in 512-Byte Sectors; Full Read/Write/Erase Functionality at  $2.25 V_{DD}$
- 64 bytes battery-backed RAM

### Digital Peripherals

- 24 port I/O; up to 5.25 V tolerance
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- 16-bit programmable counter array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers

### Clock Sources

- Internal Oscillators: 24.5 MHz, 2% Accuracy Supports UART Operation; Clock Multiplier up to 50 MHz
- External Oscillator1: Crystal, RC, C, or Clock (1 or 2 pin modes)
- External Oscillator2: 32 kHz Crystal or C, 5  $\mu$ A
- Fast wake up from suspend mode in  $< 1 \mu$ s

### Supply Voltage: 2.0–5.25 V

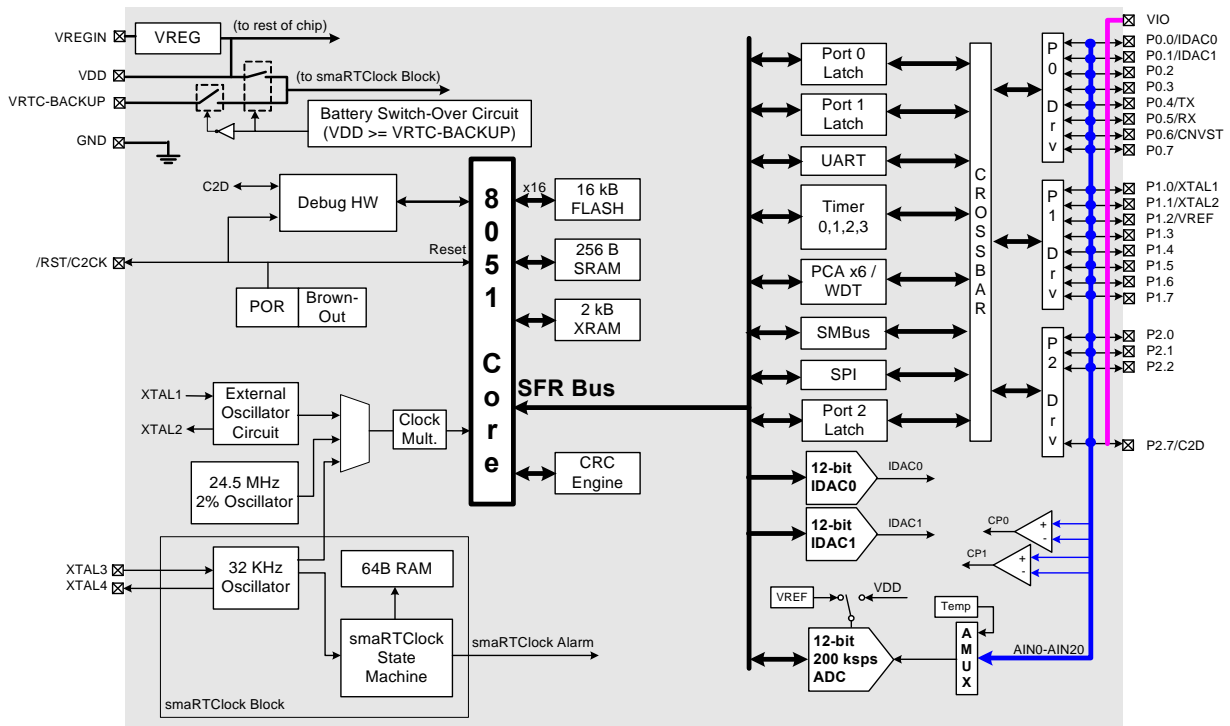
- Built-in LDO regulator: 2.1 V or 2.5 V

### Package

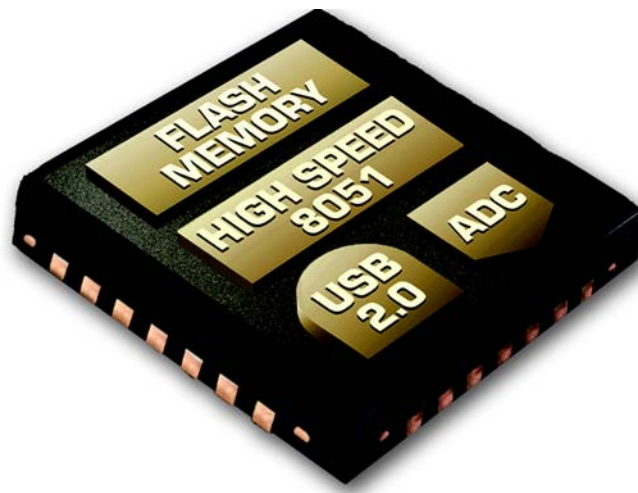
- 28-pin QFN (lead-free package)

### Ordering Part Number

- C8051F413-GM







# USB MCUs

### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksps
- Up to 17 external inputs; programmable as single-ended or differential
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

Internal Voltage Reference: 2.4 V

#### POR/Brown-out Detector

#### USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports eight flexible endpoints
- Dedicated 1 kB USB buffer memory
- Integrated transceiver; no external resistors required

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Temperature Range:  $-40$  to  $+85$  °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz Clock
- Expanded interrupt handler

#### Memory

- 1280 bytes data RAM
- 16 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

#### Digital Peripherals

- 25 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers

#### Clock Sources

- Internal oscillator: 0.25% accuracy with clock recovery enabled; supports all USB and UART modes
- External oscillator: Crystal, RC, C, or Clock
- On-chip clock multiplier for USB controller

#### Operating Voltage: 2.7 to 5.25 V

#### Voltage Regulator

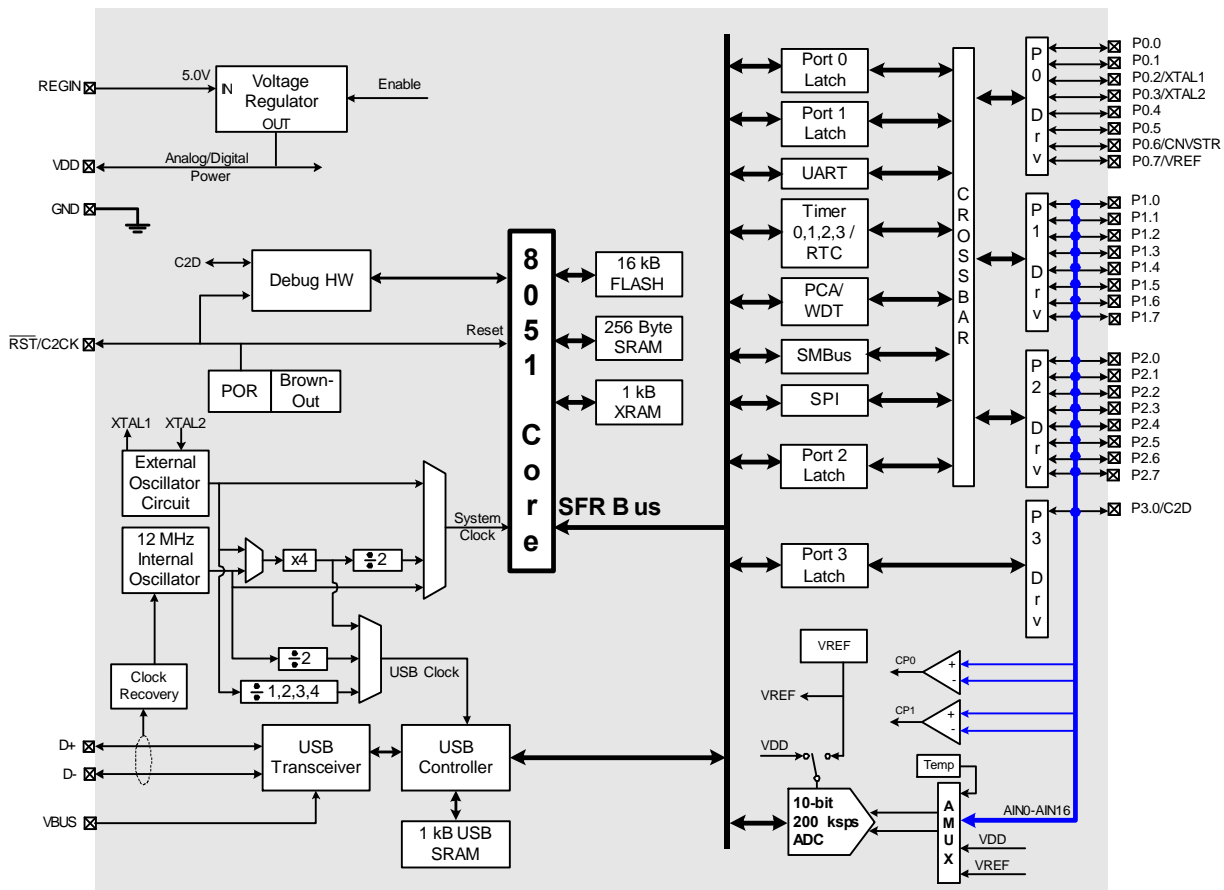
- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

#### Package

- 32-pin LQFP (lead-free package)

#### Ordering Part Number

- C8051F320-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksps
- Up to 13 external inputs; programmable as single-ended or differential
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

Internal Voltage Reference: 2.4 V

#### POR/Brown-out Detector

#### USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports eight flexible endpoints
- Dedicated 1 kB USB buffer memory
- Integrated transceiver; no external resistors required

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Temperature Range:  $-40$  to  $+85$  °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz Clock
- Expanded interrupt handler

#### Memory

- 1280 bytes data RAM
- 16 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

#### Digital Peripherals

- 21 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with five capture/compare modules
- 4 general-purpose 16-bit counter/timers

#### Clock Sources

- Internal oscillator: 0.25% accuracy with clock recovery enabled; supports all USB and UART modes
- External oscillator: Crystal, RC, C, or Clock
- On-chip clock multiplier for USB controller

Operating Voltage: 2.7 to 5.25 V

#### Voltage Regulator

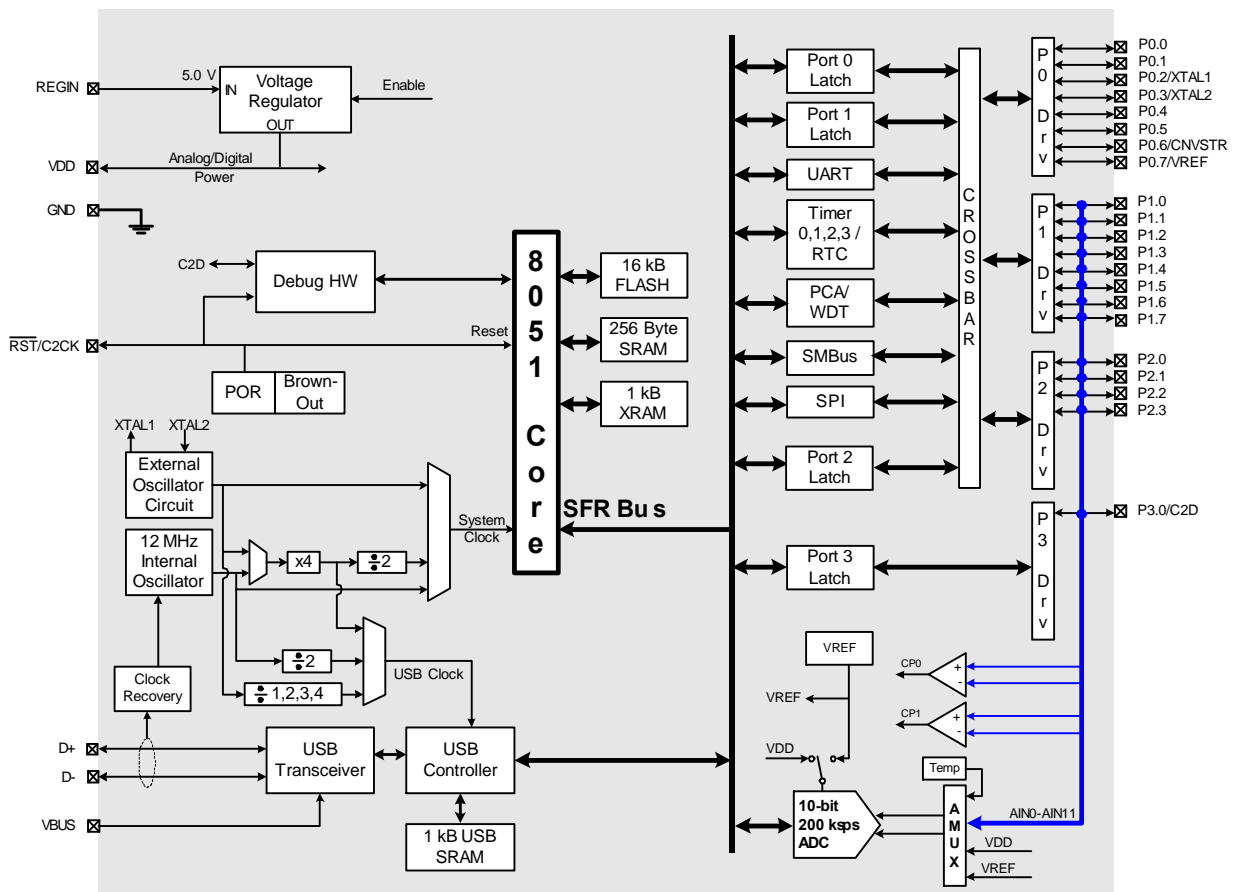
- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

#### Package

- 28-pin QFN (lead-free package)

#### Ordering Part Number

- C8051F321-GM



### USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports two fixed-function endpoints
- Dedicated 256 byte USB buffer memory
- Integrated transceiver; no external resistors required

### POR/Brown-Out Detector

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

### Separate I/O Supply Pin (V<sub>DDIO</sub>)

- Enables interfacing to external logic that operates between 2.0 V and V<sub>DD</sub> without the need for external circuitry

### Temperature Range: -40 to 85 °C

### High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 1280 bytes internal data RAM (256 + 1K)
- 16 kB bytes in-system programmable Flash program memory

### Digital Peripherals

- 15 port I/O; all 5 V tolerant with high sink current
- Hardware enhanced UART (up to 3 Mbps)
- Two general purpose 16-Bit counter/timers

### Clock Sources

- Internal clock: 0.25% accuracy with clock recovery enabled. Supports all USB and UART modes
- On-Chip Clock Multiplier for USB Controller
- Internal 22 kHz Clock for low power suspend modes

### Operating Voltage: 2.7 to 5.25 V

### Voltage Regulator

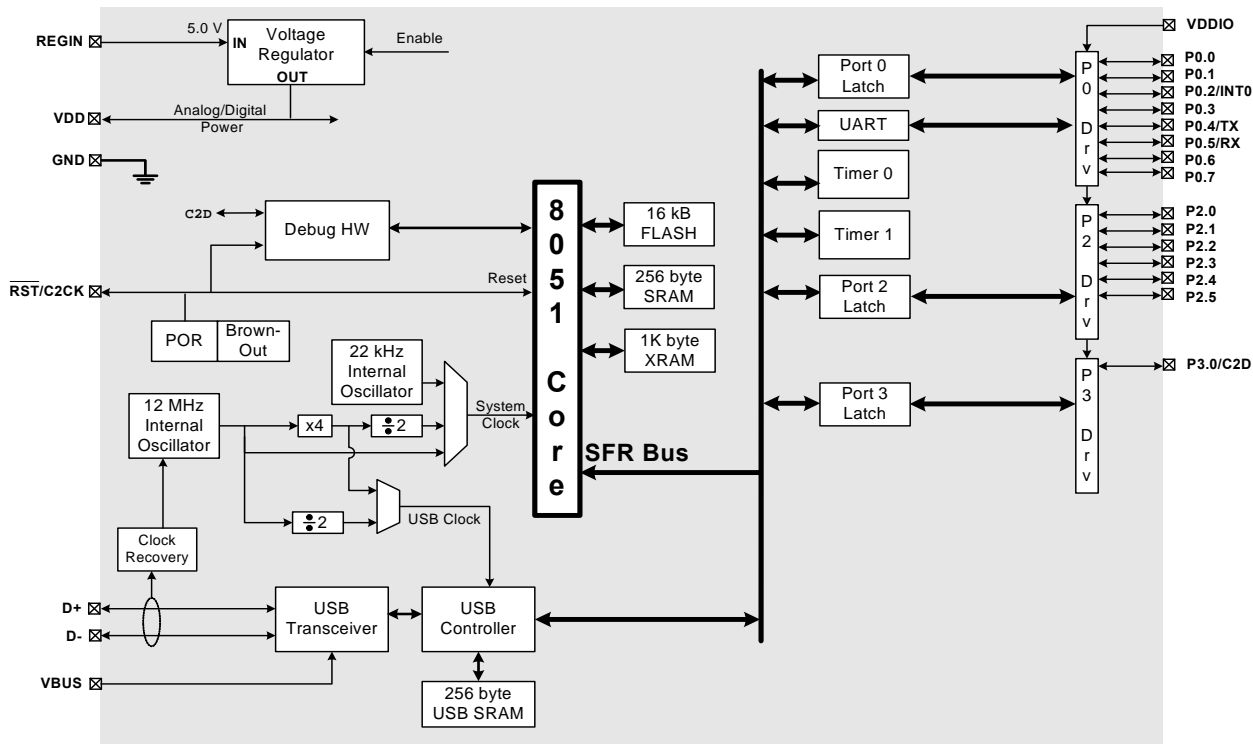
- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

### Package

- 28-Pin QFN (lead-free package)

### Ordering Part Number

C8051F326-GM





### USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports two fixed-function endpoints
- Dedicated 256 byte USB buffer memory
- Integrated transceiver; no external resistors required

### POR/Brown-Out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Temperature Range: -40 to 85 °C

### High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 1280 bytes internal data RAM (256 + 1K)
- 16 kB bytes in-system programmable Flash program memory

### Digital Peripherals

- 15 port I/O; all 5 V tolerant with high sink current
- Hardware enhanced UART (up to 3 Mbps)
- Two general purpose 16-Bit counter/timers

### Clock Sources

- Internal clock: 0.25% accuracy with clock recovery enabled. Supports all USB and UART modes
- On-Chip Clock Multiplier for USB Controller
- Internal 22 kHz Clock for low power suspend modes

Operating Voltage: 2.7 to 5.25 V

### Voltage Regulator

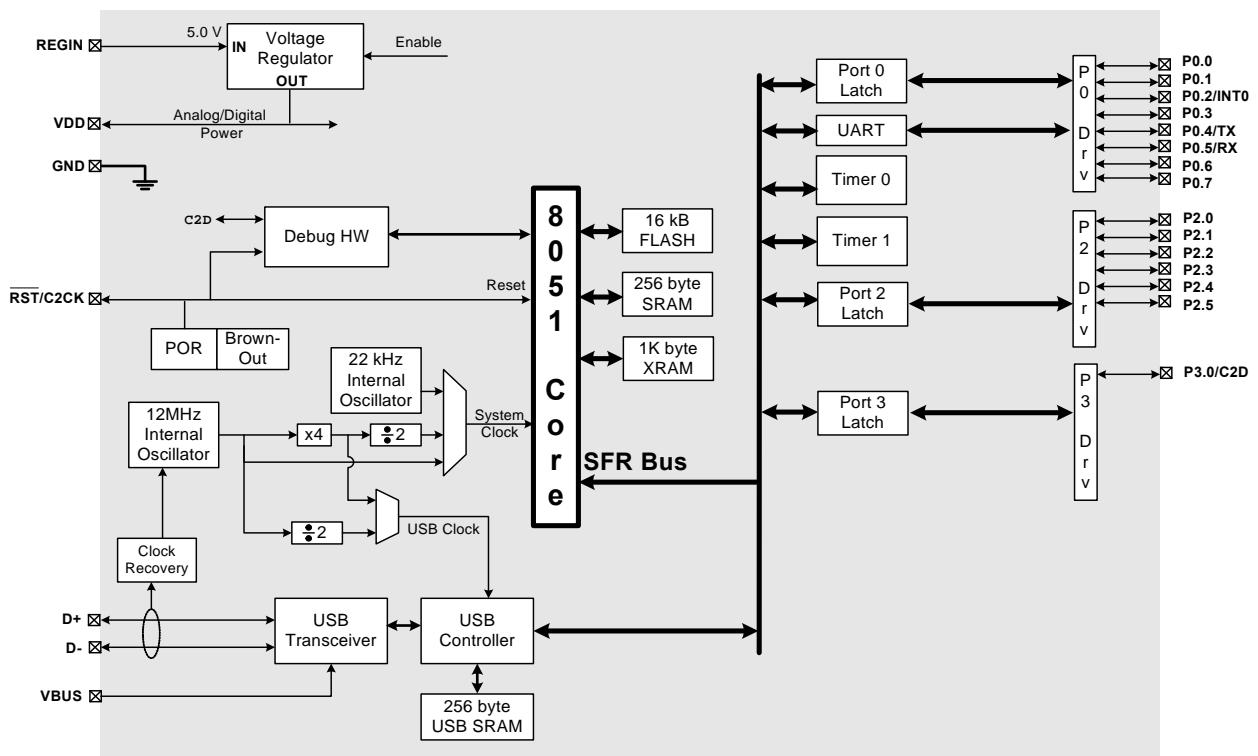
- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

### Package

- 28-Pin QFN (lead-free package)

### Ordering Part Number

- C8051F327-GM



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksps
- Up to 17 external inputs; programmable as single-ended or differential
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

**Internal Voltage Reference: 2.4 V**

#### POR/Brown-out Detector

#### USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports eight flexible endpoints
- Dedicated 1 kB USB buffer memory
- Integrated transceiver; no external resistors required

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 48 MIPS throughput with 48 MHz Clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM (256 + 4 kB)
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 40 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and 2 UART serial ports available concurrently
- 4 general-purpose 16-bit counter/timers
- Programmable 16-bit counter array with 5 capture/compare modules

### Clock Sources

- Internal oscillator: 0.25% accuracy with clock recovery enabled; supports all USB and UART modes
- External oscillator: Crystal, RC, C, or Clock
- On-chip clock multiplier: up to 48 MHz

**Operating Voltage: 2.7 to 5.25 V**

### Voltage Regulator

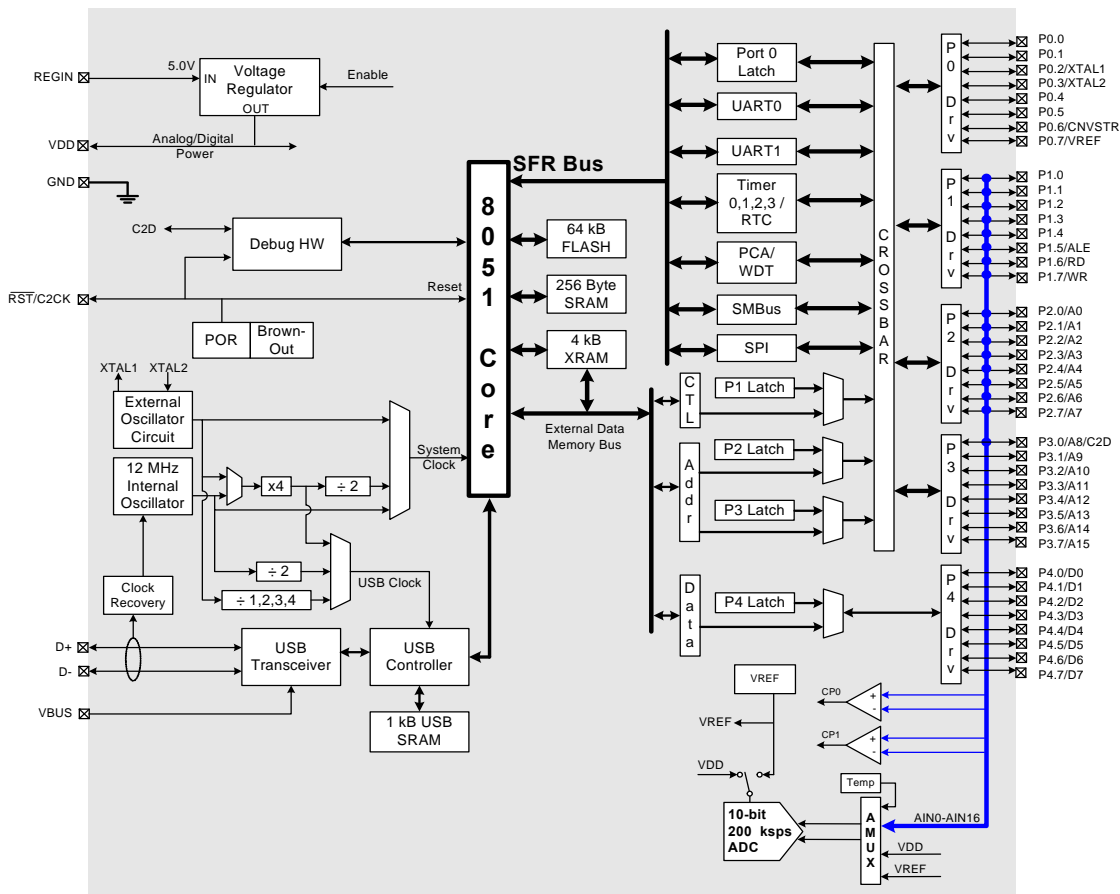
- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

### Package

- 48-Pin TQFP (lead-free package)

### Ordering Part Number

C8051F340-GQ





### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksps
- Up to 17 external inputs; programmable as single-ended or differential
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

Internal Voltage Reference: 2.4 V

#### POR/Brown-out Detector

#### USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports eight flexible endpoints
- Dedicated 1 kB USB buffer memory
- Integrated transceiver; no external resistors required

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- **Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 48 MIPS throughput with 48 MHz Clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM (256 + 4 kB)
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 25 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- 4 general-purpose 16-bit counter/timers
- Programmable 16-bit counter array with 5 capture/compare modules

### Clock Sources

- Internal oscillator: 0.25% accuracy with clock recovery enabled; supports all USB and UART modes
- External oscillator: Crystal, RC, C, or Clock
- On-chip clock multiplier: up to 48 MHz

### Operating Voltage: 2.7 to 5.25 V

### Voltage Regulator

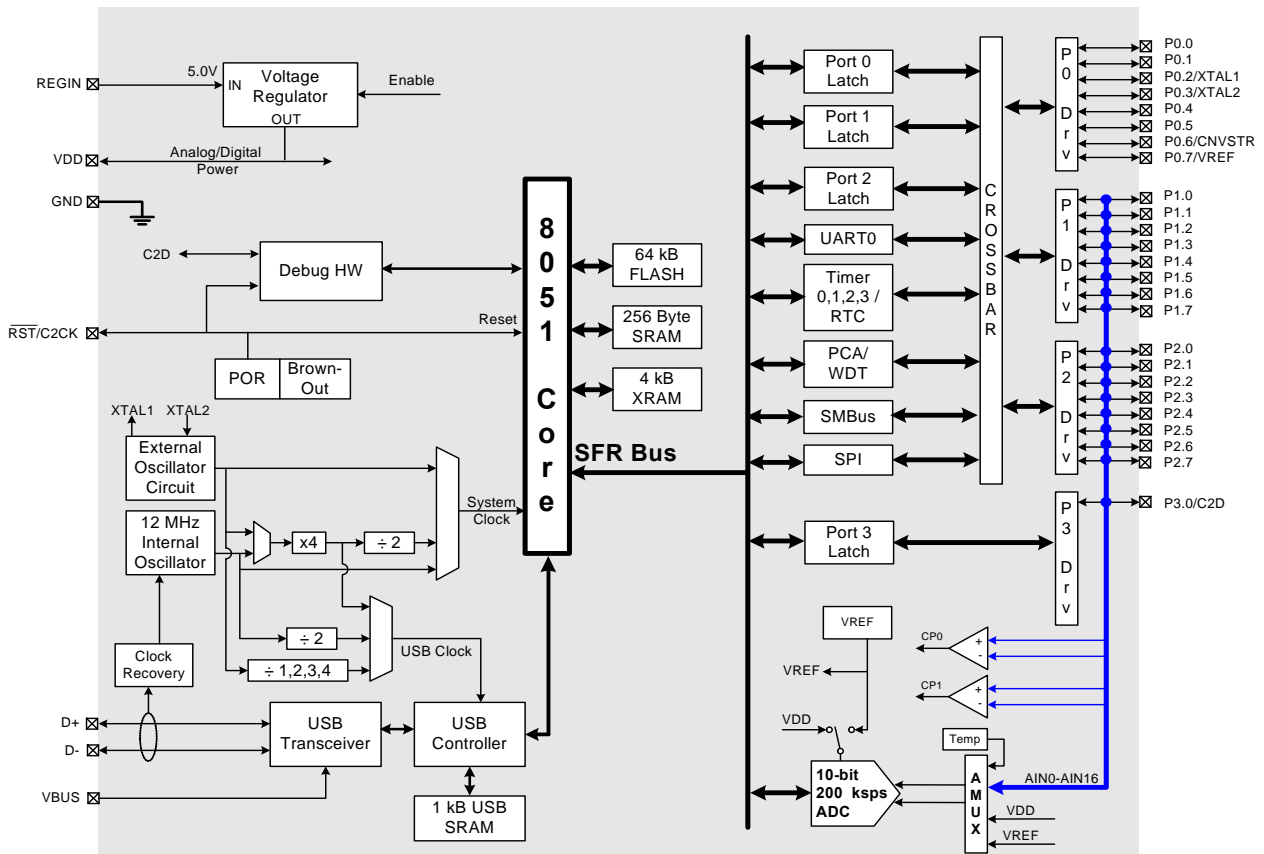
- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

### Package

- 32-Pin LQFP (lead-free package)

### Ordering Part Number

- C8051F342-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksps
- Up to 17 external inputs; programmable as single-ended or differential
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

Internal Voltage Reference: 2.4 V

#### POR/Brown-out Detector

#### USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports eight flexible endpoints
- Dedicated 1 kB USB buffer memory
- Integrated transceiver; no external resistors required

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Temperature Range:  $-40$  to  $+85$  °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 48 MIPS throughput with 48 MHz Clock
- Expanded interrupt handler

#### Memory

- 2304 bytes data RAM (256 + 2 kB)
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

#### Digital Peripherals

- 25 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- 4 general-purpose 16-bit counter/timers
- Programmable 16-bit counter array with 5 capture/compare modules

#### Clock Sources

- Internal oscillator: 0.25% accuracy with clock recovery enabled; supports all USB and UART modes
- External oscillator: Crystal, RC, C, or Clock
- On-chip clock multiplier: up to 48 MHz

Operating Voltage: 2.7 to 5.25 V

#### Voltage Regulator

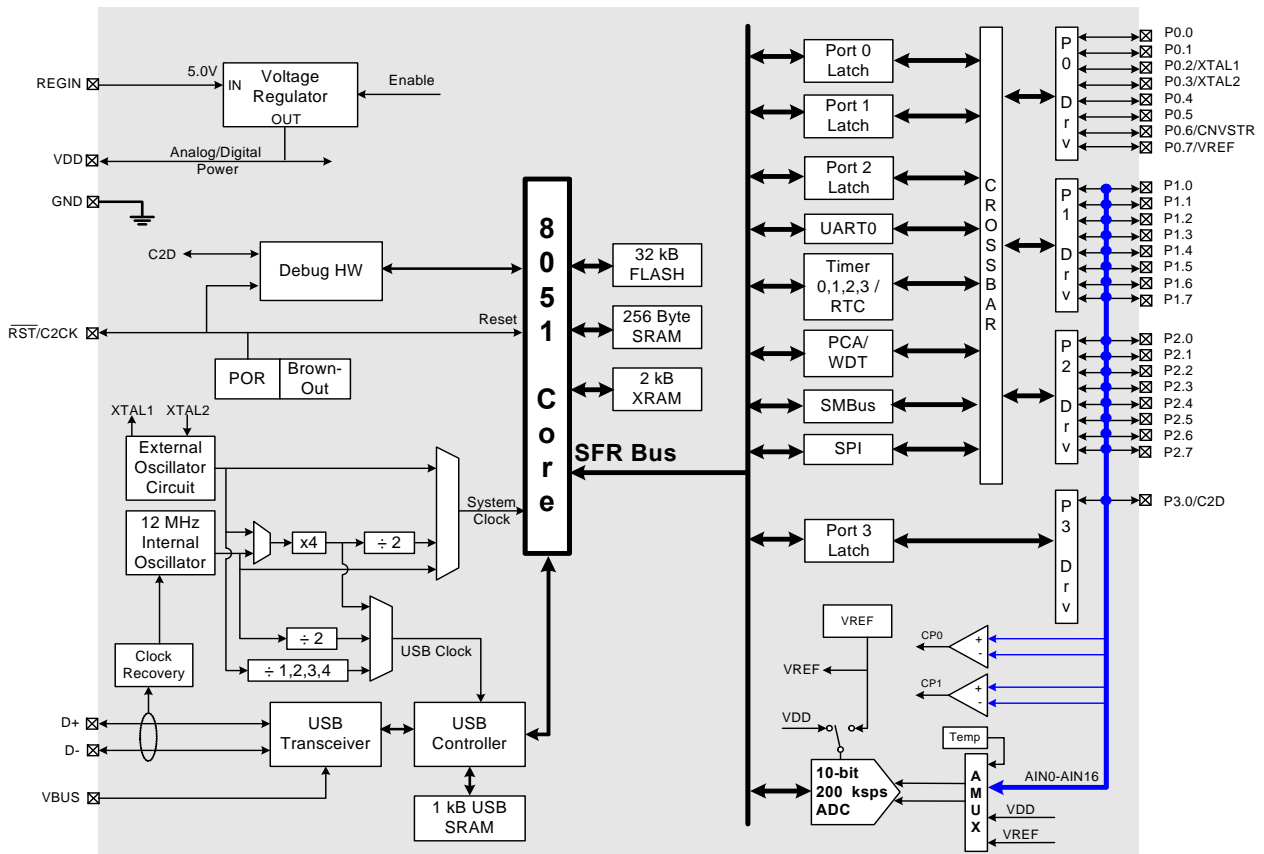
- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

#### Package

- 32-Pin LQFP (lead-free package)

#### Ordering Part Number

- C8051F343-GQ





### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksps
- Up to 17 external inputs; programmable as single-ended or differential
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

#### Internal Voltage Reference: 2.4 V

#### POR/Brown-out Detector

#### USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports eight flexible endpoints
- Dedicated 1 kB USB buffer memory
- Integrated transceiver; no external resistors required

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

#### Temperature Range: -40 to +85 °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz Clock
- Expanded interrupt handler

### Memory

- 2304 bytes data RAM (256 + 2 kB)
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)
- External parallel data memory interface

### Digital Peripherals

- 40 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and 2 UART serial ports available concurrently
- 4 general-purpose 16-bit counter/timers
- Programmable 16-bit counter array with 5 capture/compare modules

### Clock Sources

- Internal oscillator: 0.25% accuracy with clock recovery enabled; supports all USB and UART modes
- External oscillator: Crystal, RC, C, or Clock
- On-chip clock multiplier: up to 48 MHz

### Operating Voltage: 2.7 to 5.25 V

### Voltage Regulator

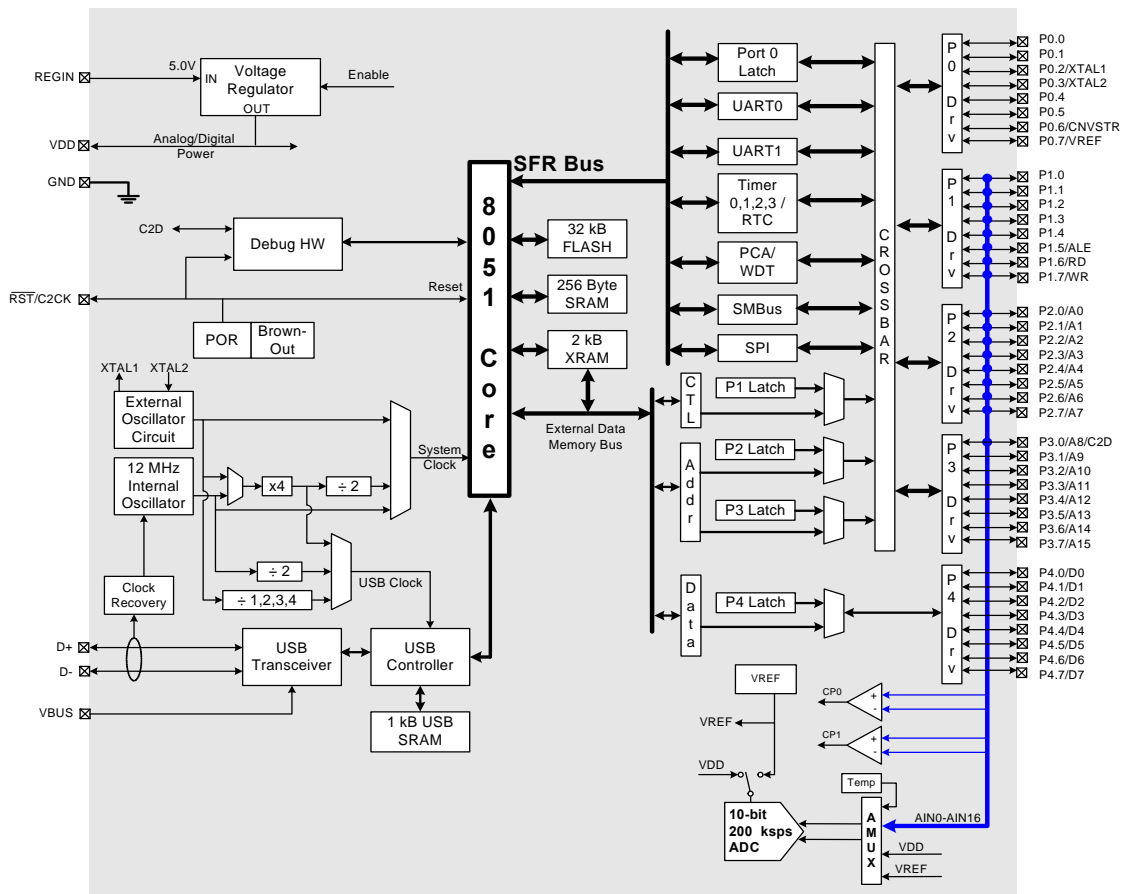
- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

### Package

- 48-Pin TQFP (lead-free package)

### Ordering Part Number

- C8051F345-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksps
- Up to 17 external inputs; programmable as single-ended or differential
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

Internal Voltage Reference: 2.4 V

#### POR/Brown-out Detector

#### USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports eight flexible endpoints
- Dedicated 1 kB USB buffer memory
- Integrated transceiver; no external resistors required

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Temperature Range:  $-40$  to  $+85$  °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz Clock
- Expanded interrupt handler

### Memory

- 4352 bytes data RAM (256 + 4 kB)
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 25 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- 4 general-purpose 16-bit counter/timers
- Programmable 16-bit counter array with 5 capture/compare modules

### Clock Sources

- Internal oscillator: 0.25% accuracy with clock recovery enabled; supports all USB and UART modes
- External oscillator: Crystal, RC, C, or Clock
- On-chip clock multiplier: up to 48 MHz

Operating Voltage: 2.7 to 5.25 V

### Voltage Regulator

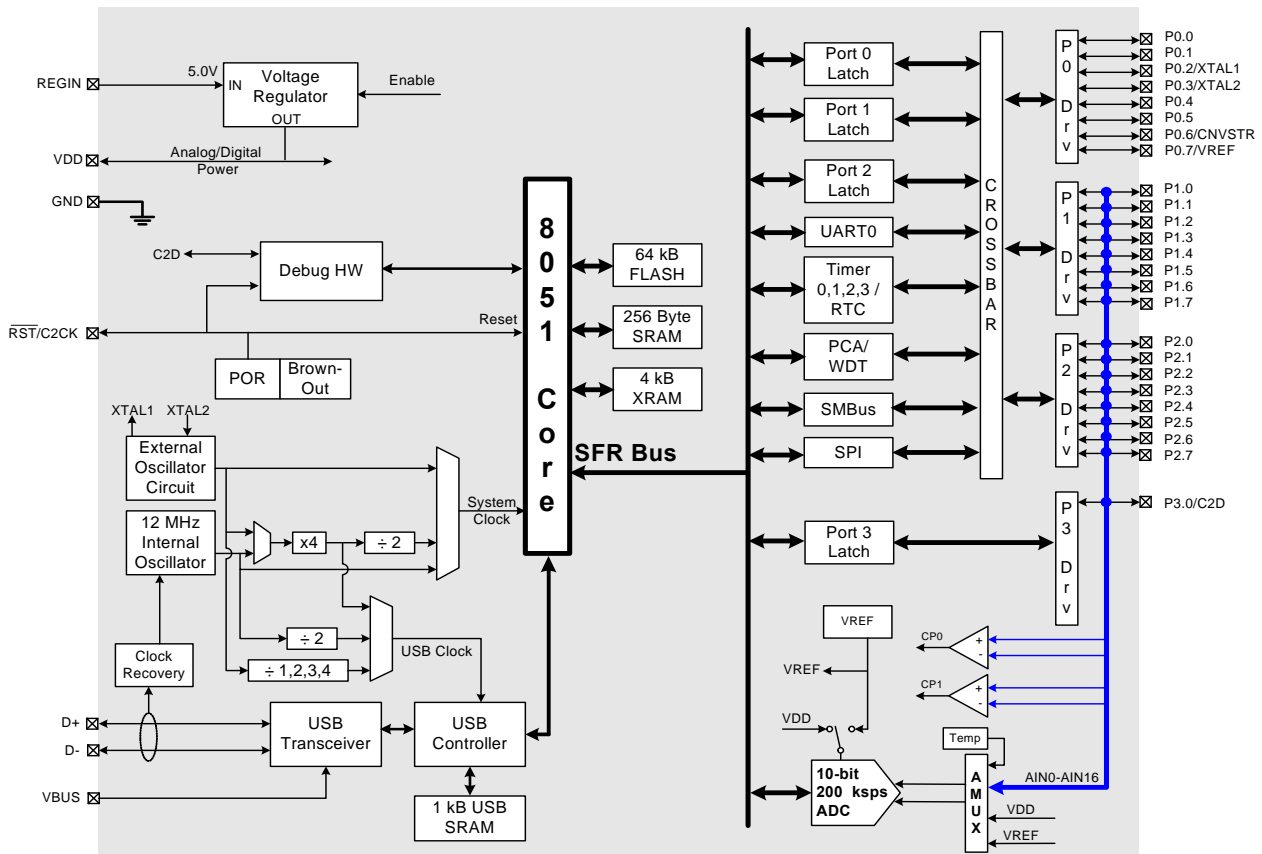
- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

### Package

- 32-Pin LQFP (lead-free package)

### Ordering Part Number

- C8051F346-GQ





### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksps
- Up to 17 external inputs; programmable as single-ended or differential
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

#### Internal Voltage Reference: 2.4 V

#### POR/Brown-out Detector

#### USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
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- Superior performance to emulation systems using ICE-chips, target pods, and sockets

### Temperature Range: -40 to +85 °C

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz Clock
- Expanded interrupt handler

### Memory

- 2304 bytes data RAM (256 + 2 kB)
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

### Digital Peripherals

- 25 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- 4 general-purpose 16-bit counter/timers
- Programmable 16-bit counter array with 5 capture/compare modules

### Clock Sources

- Internal oscillator: 0.25% accuracy with clock recovery enabled; supports all USB and UART modes
- External oscillator: Crystal, RC, C, or Clock
- On-chip clock multiplier: up to 48 MHz

### Operating Voltage: 2.7 to 5.25 V

### Voltage Regulator

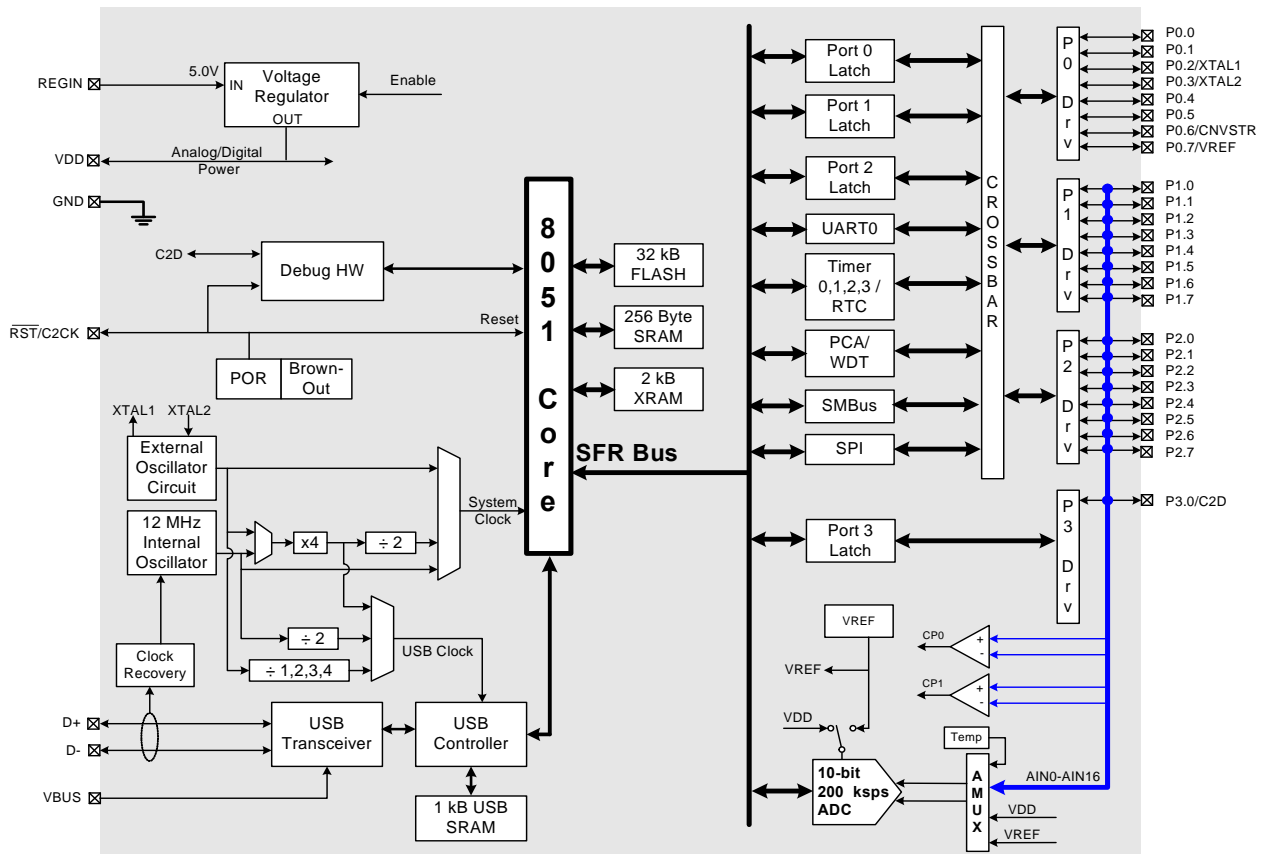
- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

### Package

- 32-Pin LQFP (lead-free package)

### Ordering Part Number

- C8051F347-GQ



### Analog Peripherals

#### Two Comparators

#### POR/Brown-out Detector

#### USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports eight flexible endpoints
- Dedicated 1 kB USB buffer memory
- Integrated transceiver; no external resistors required

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

**Development Kit: C8051F340DK**

### High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz Clock
- Expanded interrupt handler

### Memory

- 2304 bytes data RAM (256 + 2 kB)
- 32 kB Flash; in-system programmable in 512-byte sectors
- External parallel data memory interface

### Digital Peripherals

- 40 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and 2 UART serial ports available concurrently
- 4 general-purpose 16-bit counter/timers
- Programmable 16-bit counter array with 5 capture/compare modules

### Clock Sources

- Internal oscillator: 0.25% accuracy with clock recovery enabled; supports all USB and UART modes
- External oscillator: Crystal, RC, C, or Clock
- On-chip clock multiplier: up to 48 MHz

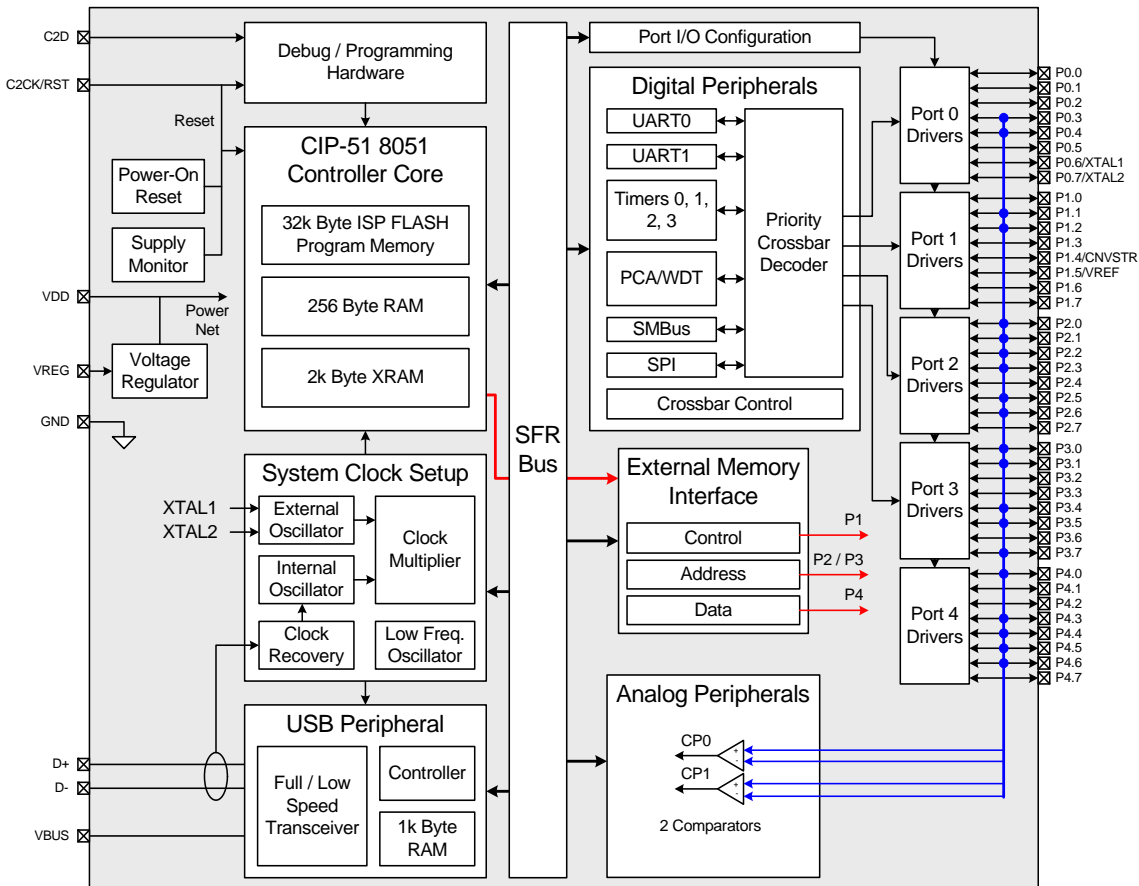
### Voltage Regulator

- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

**Operating Voltage: 2.7 to 5.25 V**

### Ordering Part Number

- C8051F348-GQ, 48-Pin QFP (RoHS-compliant), 9x9 mm<sup>2</sup>



**Analog Peripherals**

10-Bit ADC

Two Comparators

POR/Brown-out Detector

**USB Function Controller**

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports eight flexible endpoints
- Dedicated 1 kB USB buffer memory
- Integrated transceiver; no external resistors required

**On-Chip Debug**

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Temperature Range: -40 to +85 °C

Development Kit: C8051F340DK

**High-Speed 8051 µC Core**

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz Clock
- Expanded interrupt handler

**Memory**

- 2304 bytes data RAM (256 + 2 kB)
- 32 kB Flash; in-system programmable in 512-byte sectors

**Digital Peripherals**

- 25 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and UART serial ports available concurrently
- 4 general-purpose 16-bit counter/timers
- Programmable 16-bit counter array with 5 capture/compare modules

**Clock Sources**

- Internal oscillator: 0.25% accuracy with clock recovery enabled; supports all USB and UART modes
- External oscillator: Crystal, RC, C, or Clock
- On-chip clock multiplier: up to 48 MHz

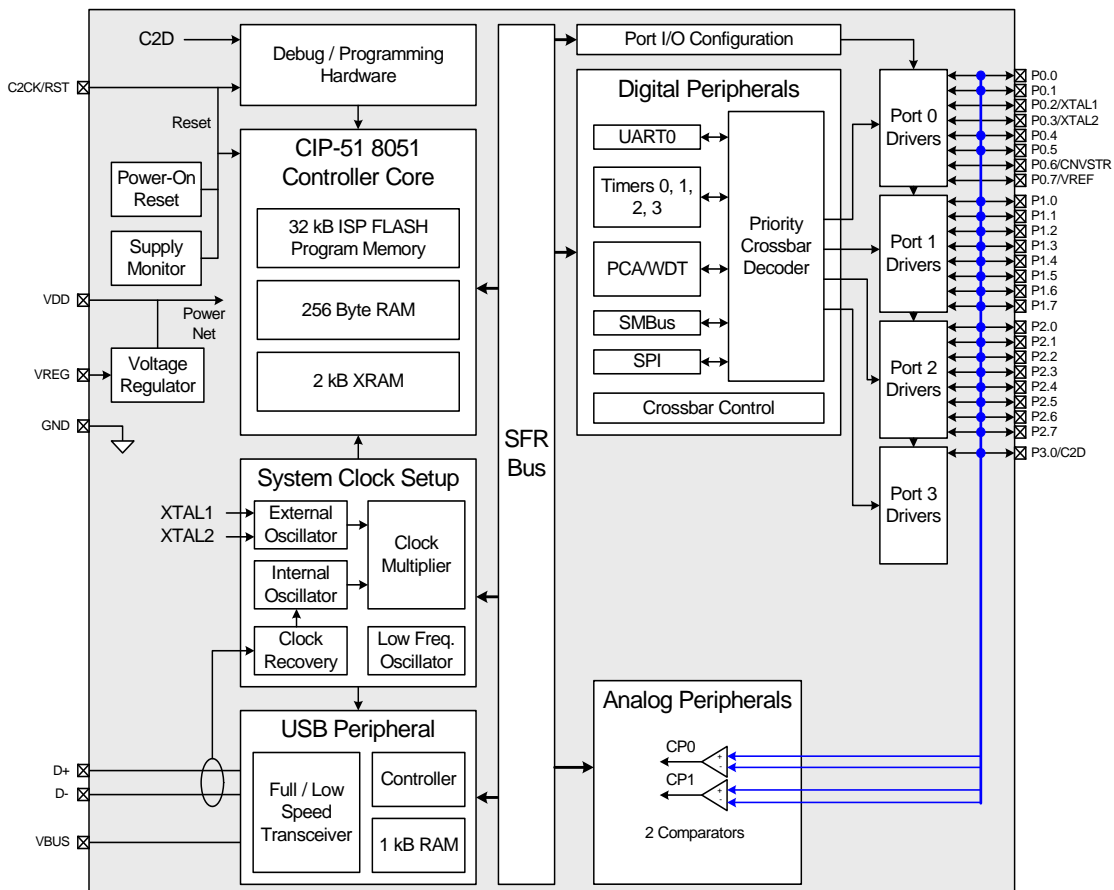
**Voltage Regulator**

- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

Operating Voltage: 2.7 to 5.25 V

**Ordering Part Number**

- C8051F349-GQ, 32-Pin QFP (RoHS-compliant), 9x9 mm<sup>2</sup>



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksp/s
- Up to 17 external inputs; programmable as single-ended or differential
- Built-in temperature sensor ( $\pm 3^\circ\text{C}$ )

#### Two Comparators

Internal Voltage Reference: 2.4 V

#### POR/Brown-out Detector

#### USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports eight flexible endpoints
- Dedicated 1 kB USB buffer memory
- Integrated transceiver; no external resistors required

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- **Temperature Range:  $-40$  to  $+85^\circ\text{C}$**

### High-Speed 8051 $\mu\text{C}$ Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 48 MIPS throughput with 48 MHz Clock
- Expanded interrupt handler

#### Memory

- 4352 bytes data RAM (256 + 4 kB)
- 64 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

#### Digital Peripherals

- 25 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and 2 UART serial ports available concurrently
- 4 general-purpose 16-bit counter/timers
- Programmable 16-bit counter array with 5 capture/compare modules

#### Clock Sources

- Internal oscillator: 0.25% accuracy with clock recovery enabled; supports all USB and UART modes
- External oscillator: Crystal, RC, C, or Clock
- On-chip clock multiplier: up to 48 MHz

#### Voltage Regulator

- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

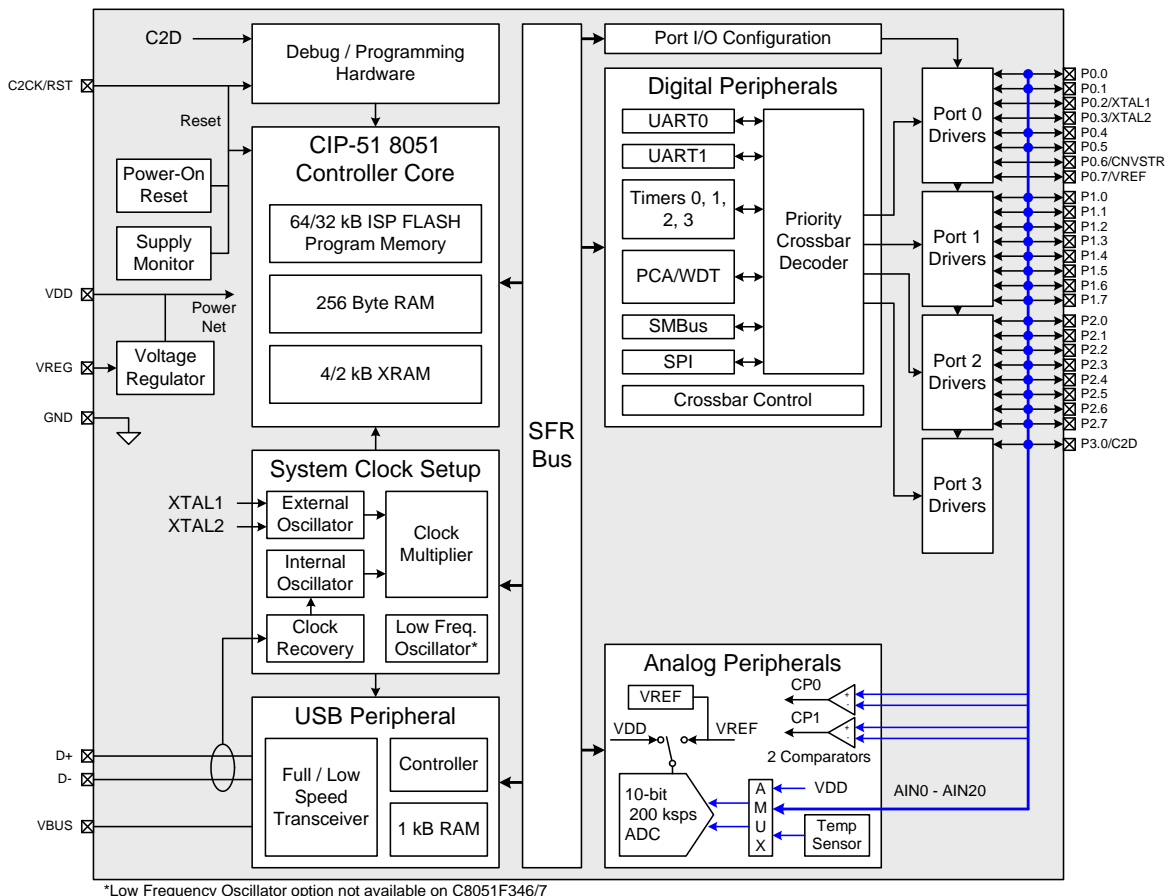
#### Operating Voltage: 2.7 to 5.25 V

#### Package

- 32-Pin LQFP (lead-free package)

#### Ordering Part Number

- C8051F342-GQ



### Analog Peripherals

#### 10-Bit ADC

- $\pm 1$  LSB INL; no missing codes
- Programmable throughput up to 200 ksps
- Up to 17 external inputs; programmable as single-ended or differential
- Built-in temperature sensor ( $\pm 3$  °C)

#### Two Comparators

**Internal Voltage Reference: 2.4 V**

#### POR/Brown-out Detector

#### USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports eight flexible endpoints
- Dedicated 1 kB USB buffer memory
- Integrated transceiver; no external resistors required

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 48 MIPS throughput with 48 MHz Clock
- Expanded interrupt handler

#### Memory

- 2304 bytes data RAM (256 + 2 kB)
- 32 kB Flash; in-system programmable in 512-byte sectors (512 bytes are reserved)

#### Digital Peripherals

- 25 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I<sup>2</sup>C™ compatible), SPI™, and 2 UART serial ports available concurrently
- 4 general-purpose 16-bit counter/timers
- Programmable 16-bit counter array with 5 capture/compare modules

#### Clock Sources

- Internal oscillator: 0.25% accuracy with clock recovery enabled; supports all USB and UART modes
- External oscillator: Crystal, RC, C, or Clock
- On-chip clock multiplier: up to 48 MHz

#### Voltage Regulator

- On-chip voltage regulator supports USB bus-powered operation
- Regulator bypass mode supports USB self-powered operation

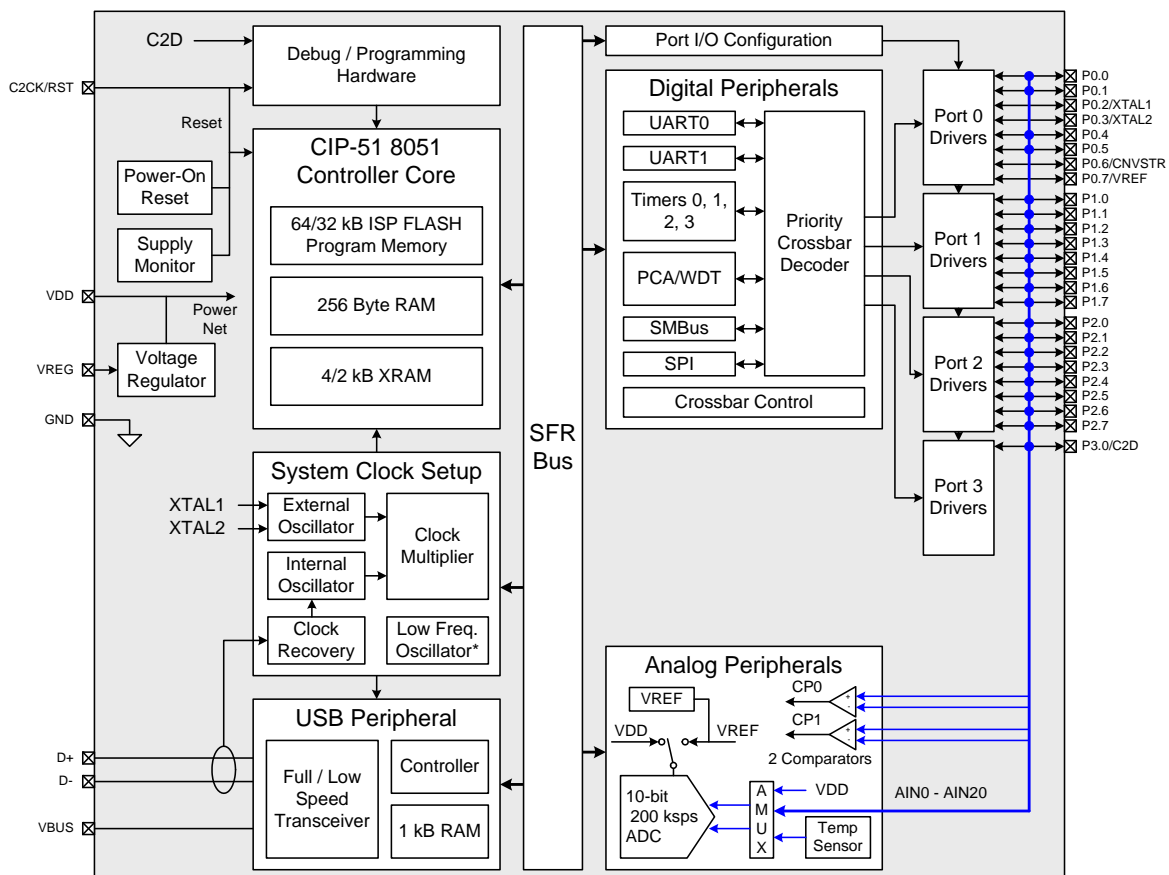
**Operating Voltage: 2.7 to 5.25 V**

#### Package

- 32-Pin LQFP (lead-free package)

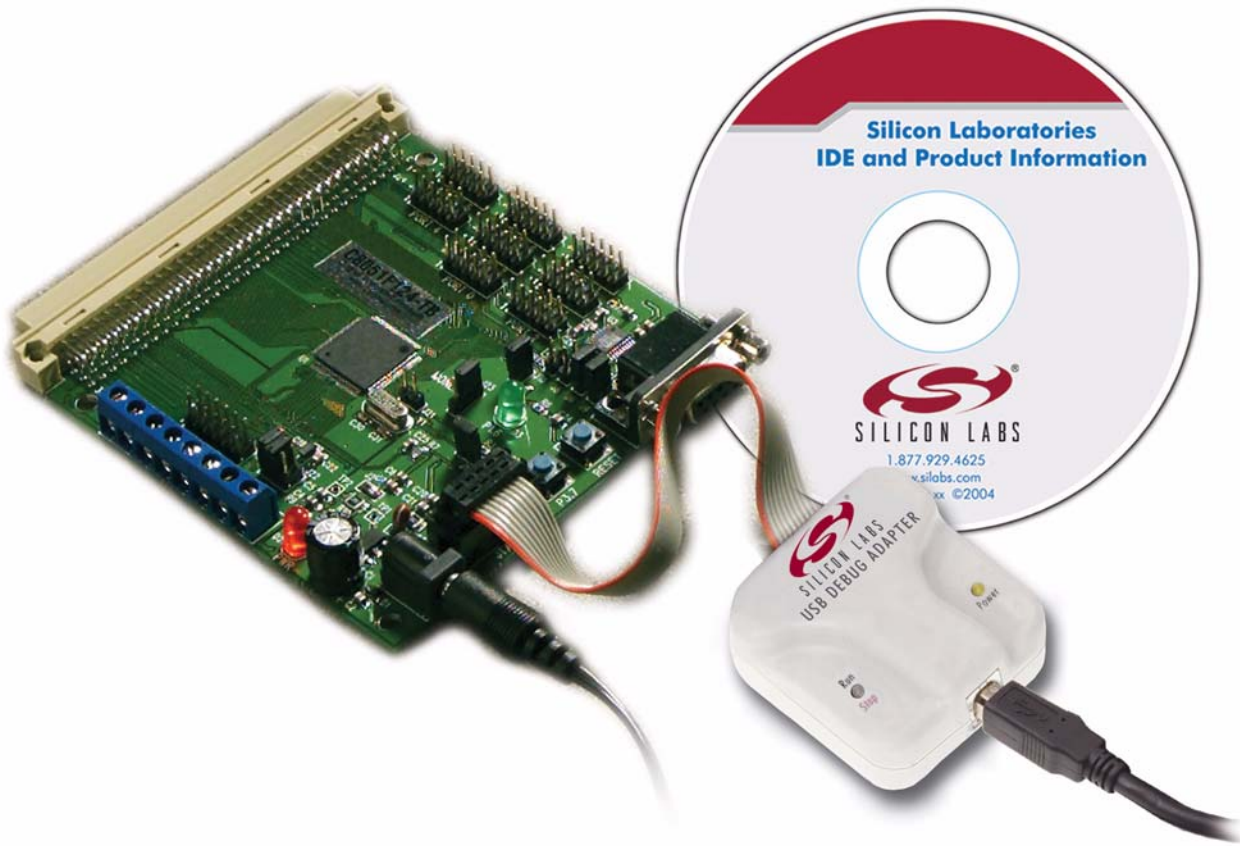
#### Ordering Part Number

- C8051F343-GQ



\*Low Frequency Oscillator option not available on C8051F346/7





# Development Tools

## Comprehensive Development Kits

Silicon Laboratories' comprehensive development kits provide everything needed to develop complex electronic systems quickly and easily. These kits come complete with all required hardware and software and outperform traditional "emulators" at a fraction of the cost. Development kits are available for sale at [www.silabs.com](http://www.silabs.com).

## Integrated Development Environment (IDE)

Silicon Laboratories IDE combines an editor, project manager, code development tools, and a debugger into a single intuitive environment for code development and in-system debug. No additional target RAM, program memory, or communications channels are required.

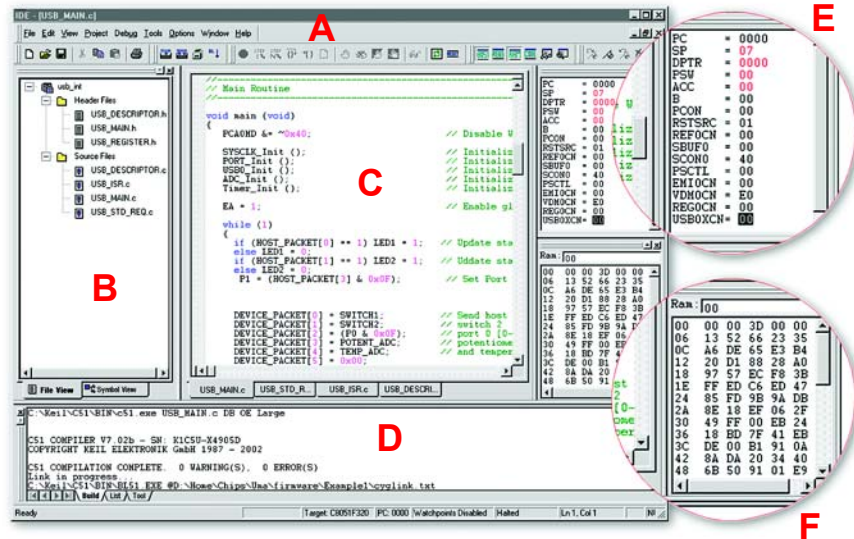
**A.** Standard Windows® Menus and Toolbars provide optimum access to all IDE features including the editor, debugger, customizable tool menu, and online help.

**B.** Project Window offers clear visibility and easy management of all files associated with your design project.

**C.** Edit Source Debugger Window helps create programs using the language-sensitive, full-featured editor (debug assembly or C language programs with the source in full view). Useful debug features, such as breakpoint markers and program counter location, dramatically speed debugging.

**D.** Output Window conveniently displays the assembler output and listing file.

**E, F.** Register Window and Memory Window help in examining and directly modifying memory, register, and Flash contents during debugging. These flexible windows are automatically updated each time program execution stops, and changed values are highlighted.



### System Requirements:

- A Pentium-class host PC running Windows Operating System
- One available COM port (1-4)
- 64 MB RAM and 40 MB free hard drive space recommended

## Built-in Debug

Every microcontroller from Silicon Laboratories includes on-chip debug circuitry that supports non-intrusive, full-speed, in-circuit debugging of the production part installed in the user's end application, eliminating the sockets, external emulation hardware, and performance-degrading cables typical of emulators. Emulators are never required.



## Features

### Development Kits

- Complete development/prototyping system
- Prototyping/demonstration board
- In-system Flash programming
- In-circuit debugging
  - Run control
  - Single-stepping
  - Real-time breakpoints
  - Stack monitor
  - Register/memory inspection & modification
- Includes Silicon Laboratories IDE
- MCU configuration wizard

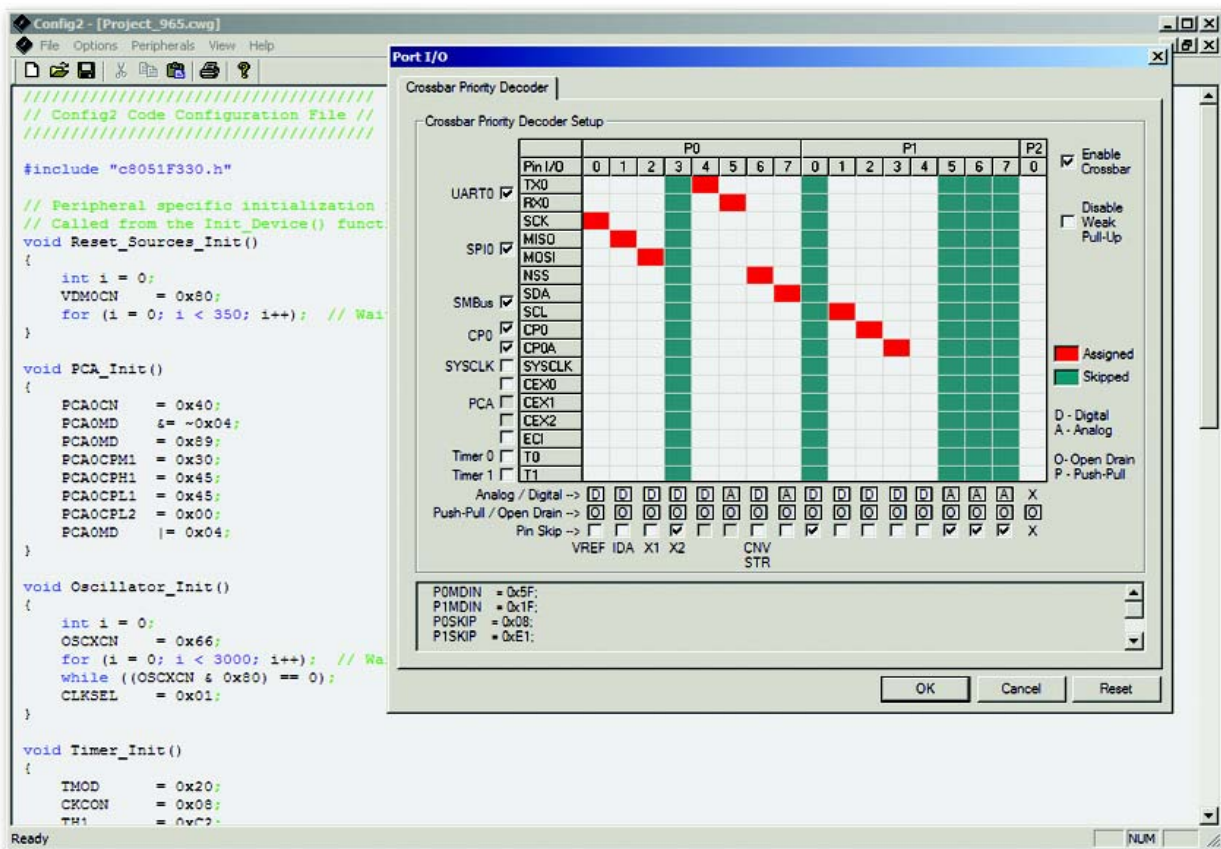
### IDE

- Source code editor
- Project manager

- Integrated Keil 8051 macro assembler and linker
- Flash programmer
- Supports full-speed, non-intrusive, in-circuit debug logic
- Real-time breakpoints
- Source-level debug
- Conditional memory watchpoints
- Memory and register inspect/modify
- Single-step and animated execution modes
- Variable watch window
- Supports third-party development tools

### Third Party tool support

- Broad range of third-party compilers and development tools available
- Flash programming and source-level debug of OMF-51 object files is fully supported



A configuration wizard automatically generates MCU and on-chip peripheral initialization code. Clicking on checkboxes and entering values in scripted dialogs generates fully-commented assembly or C language code needed to enable and configure peripherals, assign functions to I/O pins, and specify MCU operation.

## Development Kit and Evaluation Kit Part Numbers

Development Kits	
Part Number	Description
C8051F005DK	Development Kit for C8051F000, F001, F002, F003, F004, F005, F006, F007, F010, F011, F012, F015, F016, F017, F018 and F019 MCUs
C8051F020DK	Development Kit for C8051F020, F021, F022 and F023 MCUs
C8051F040DK	Development Kit for C8051F040, F041, F042, F043, F044, F045, F046 and F047 MCUs
C8051F060DK	Development Kit for C8051F060, F061, F062, F063, F064, F065, F066 and F067 MCUs
C8051F120DK	Development Kit for C8051F120, F121, F122, F123, F124, F125, F126, F127, F130, F131, F132 and F133 MCUs
C8051F206DK	Development Kit for C8051F206 MCU
C8051F226DK	Development Kit for C8051F220, F221, F226, F230, F231, and F236 MCUs
C8051F300DK	Development Kit for C8051F300, F301, F302, F303, F304, and F305 MCUs
C8051F310DK	Development Kit for C8051F310, F311, F312, F313, F314, F315, F316, and F317 MCUs
C8051F320DK	Development Kit for C8051F320 and F321 MCUs
C8051F326DK	Development Kit for C8051F326 and F327 MCUs
C8051F330DK	Development Kit for C8051F330, F330D, F331, F332, F333, F334, and F335 MCUs
C8051F340DK	Development Kit for C8051F340, F341, F342, F343, F344, F345, F346, F347, F348, F349, F34A, and F34B MCUs
C8051F350DK	Development Kit for C8051F350, F351, F352 and F353 MCUs
C8051F360DK	Development Kit for C8051F360, F361, F362, F363, F364, F365, F366, F367, F368 and F369 MCUs
C8051F500DK	Development Kit for C8051F500, F501, F502, F503, F504, F505, F506, and F507 MCUs
C8051F530DK	Development Kit for C8051F520, F521, F523, F524, F526, F527, F530, F531, F533, F534, F536, and F537 MCUs
C8051F930DK	Development Kit for C8051F920, F921, F930 and F931 MCUs
C8051T600DK	Development Kit for C8051T600, T601, T602, T603, T604 and T605 MCUs
C8051T610DK	Development Kit for C8051T610, T611, T612, T613, T614, T615, T616 and T617 MCUs
C8051T630DK	Development Kit for C8051T630, T631, T632, T633, T634 and T635 MCUs
F350-COMPASS-RD	Digital Compass Reference Design
C8051F410DK	Development Kit for C8051F410, F411, F412, and F413 MCUs
ETHERNETDK	Embedded Ethernet Development Kit
MODEM-DK	Embedded Modem Development Kit
ZigBee-2.4-DK	2.4 GHz ZigBee Development Kit
802.15.4-2.4-DK	2.4 GHz 802.15.4 Development Kit

Evaluation Kits	
Part Number	Description
C8051F064EK	Evaluation Kit for C8051F064 MCU
C8051F411EK	Evaluation Kit for C8051F411 MCU
CP2102EK	Evaluation Kit for CP2102 USB-to-UART Bridge Chip
CP2103EK	Evaluation Kit for CP2103 USB-to-UART Bridge Chip
CP2201EK	Evaluation Kit for CP2201 Embedded Ethernet Controller
ToolStick	Fully Contained Evaluation System in a USB Stick

Reference Design			
Description	Reference Designs	Software	
USB Firmware Programmer's Guide	AN139	AN139SW	
Three-Channel Power Sequencer	AN145	AN145SW	
High-Speed Lithium Ion Battery Charger	AN146	AN146SW	
Magnetic Stripe Reader	AN148	AN148SW	
Stepper Motor	AN155	AN155SW	
Motor Control Software Examples	AN191	AN191SW	
Human Interface Device Tutorials	AN249	AN249SW	

Application Notes			
Category	Description	App Note	Software
<b>ADC and DAC</b>	Calculating Settling Time For Switched Capacitor ADCs	AN119	
	Improving ADC Resolution by Oversampling and Averaging	AN118	AN118SW
	Using the DAC as a Function Generator	AN123	AN123SW
	Using the On-Chip Temperature Sensor	AN103	AN103SW
	C8051F35x Delta-Sigma ADC User's Guide	AN217	
<b>Commercial Applications</b>	Digital Counting Scale	AN184	
	Lithium Ion Battery Charger Using C8051F300	AN137	AN137SW
<b>Flash</b>	Flash Securities User's Guide	AN120	
	Writing to Flash from Application Code	AN129	AN129SW
	Writing to Flash from Firmware	AN201	AN201SW
<b>Hardware Development</b>	Hand Soldering Tutorial for the Fine Pitch QFP Devices	AN114	
	Configuring the Port I/O Crossbar Decoder	AN101	AN101SW
<b>Interfacing</b>	Interfacing an External SRAM to the C8051Fxxx	AN106	AN106SW
	Using C8051Fxxx in 5 Volt Systems	AN111	
	Low Pin-Count LCD Interface	AN202	AN202SW
	C8051F32x and CP210x USB Driver Customization	AN220	AN220SW
	Port Configuration and GPIO for CP210x	AN223	AN223SW
<b>Motor Control</b>	Motor Control Software Examples	AN191	AN191SW
	Stepper Motor Reference Design	AN155	AN155SW
<b>Optimization or Performance</b>	Cache Optimizations for C8051F12x	AN135	AN135SW
	Configuring the Internal and External Oscillators	AN102	AN102SW
<b>Oscillator</b>	Implementing a Real-Time Clock	AN108	AN108SW
	Power Management Techniques and Calculation	AN116	
<b>Power Management</b>	Power Management Techniques for the 'F30x and 'F31x	AN138	AN138SW
	FLASH Programming via the C2 Interface	AN127	AN127SW
<b>Programming your MCU</b>	Multiple-Device JTAG Configuration in the Silicon Labs IDE	AN134	
	Pin Sharing Techniques for the C2 Interface	AN124	
	Production Programming Options for Silicon Labs Devices	AN136	
	Using C8051Fxxx On-Chip Interface Utilities DLL	AN117	AN117SW
	Programming Flash through the JTAG Interface	AN105	AN105SW
	Serial Communication with the SMBus	AN113	AN113SW
	SMBus Communication for the 'F30x and 'F31x	AN141	AN141SW
	Software SPI Examples for the C8051F30x Family	AN128	AN128SW
	Software UART Examples	AN115	AN115SW
	UART In-Application Code Loading Examples	AN112	AN112SW
	CP2101 Customization Guide	AN144	AN144SW
	USBXpress Development Kit User's Guide	AN169	AN169SW
	MMC Data Logger Example	AN189	AN189SW
	Serial Communications Guide for CP210x	AN197	AN197SW
	CP210x Baud Rate Support	AN205	AN205SW
<b>Signal Processing</b>	FFT Routines for the C8051F12x Family	AN142	AN142SW
	Annotated 'C' examples for the 'F02x Family	AN122	AN122SW
	Code Banking Using the Keil 8051 Tools	AN130	AN130SW
	Code Banking Using the Tasking 8051 Tools	AN143	AN143SW
	Converting from the Metalink ASM51 Assembler to the Keil A51 Assembler	AN121	
	Integrating Dunfield 8051 Tools into the Silicon Labs IDE	AN132	AN132SW
	Integrating HI-TECH 8051 Tools into the Silicon Labs IDE	AN140	AN140SW
	Integrating Keil 8051 Tools into the Silicon Labs IDE	AN104	
	Integrating Raisonance 8051 Tools into the Silicon Labs IDE	AN125	
	Integrating Tasking 8051 Tools into the Silicon Labs IDE	AN126	AN126SW
	Integrating IAR 8051 Tools into the Silicon Labs IDE	AN236	AN236SW
	Multiple-Device JTAG Configuration in the Silicon Labs IDE	AN134	
	Pin Sharing Techniques for the C2 Interface	AN124	
	Porting Considerations from 'F02x to 'F12x	AN131	AN131SW
	Integrating SDCC 8051 Tools Into The Silicon Labs IDE	AN198	AN198SW
<b>Software Development</b>	TCP/IP Library Programmer's Guide	AN237	AN237SW
	Human Interface Device Tutorials	AN249	AN249SW
	Using the On-Chip Temperature Sensor	AN103	AN103SW
	16-Bit PWM Using an On-Chip Timer	AN110	AN110SW
	Timer Functions		

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