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PanelLink®
Technology

SiI 1178

Dual Link PanelLink Transmitter

Data Sheet

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Revision History

Revision	Date	Comment
A	09/20/05	Data Sheet

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General Description

The SiI 1178 transmitter uses PanelLink Digital technology to support displays ranging from single link resolutions of VGA to UXGA resolution (25 - 165Mpps) and dual link resolutions of up to QUXGA (330Mpps).

The SiI 1178 Tx is pin-compatible with the SiI 1178 Tx, supporting 12-bit mode (½ pixel per clock edge at double data rates) for true color (16.7 million) support.. Input jitter tolerance is greatly enhanced over the SiI 1178 Tx, enabling spread spectrum applications. Single-clock/dual-edge clocking is supported in both high swing and low swing modes.

Used in pairs, SiI 1178 transmitters support dual link mode and allow dynamic switching between single link and dual link operation by way of their I^2C interfaces.

PanelLink Digital technology simplifies PC design by resolving many of the system level issues associated with high-speed mixed signal design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

Features

- Scaleable bandwidth:
  - Single link operation from 25 - 165 Mega-pixels per second (VGA to UXGA)
  - Dual link operation up to 330 Mega-pixels per second
- 12-bit (½ pixel) DDR input with flexible input clocking: Single-clock/dual-edge or dual-clock/single-edge
- Full support for low swing DVO 2.0 mode
- I^2C slave programming interface
- Selectable input level voltage swing:
  - Low voltage interface: 1.0 to 1.9V
  - High swing interface: 3.3V
- Monitor detection supported through Hot Plug and receiver sense
- Cable distance support: Over 10m
- Compliant with DVI 1.0
- Space saving and environmentally safe 48-pin TSSOP Pb-free package

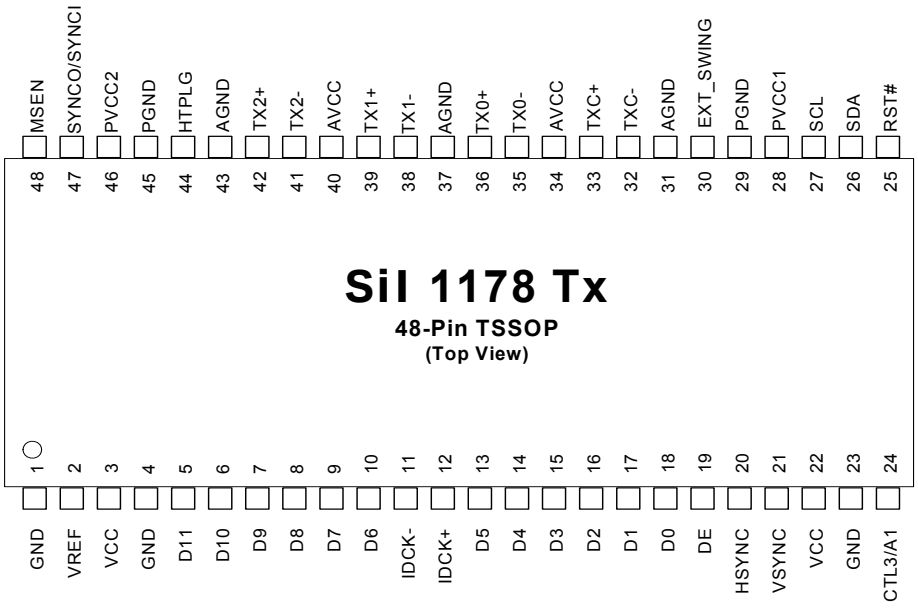


Figure 1. SiI 1178 Tx Pin Diagram

Functional Description

The SiI 1178 Tx is a DVI 1.0 compliant digital-output transmitter with Dual Link capability. Figure 2 shows the functional blocks of the chip.

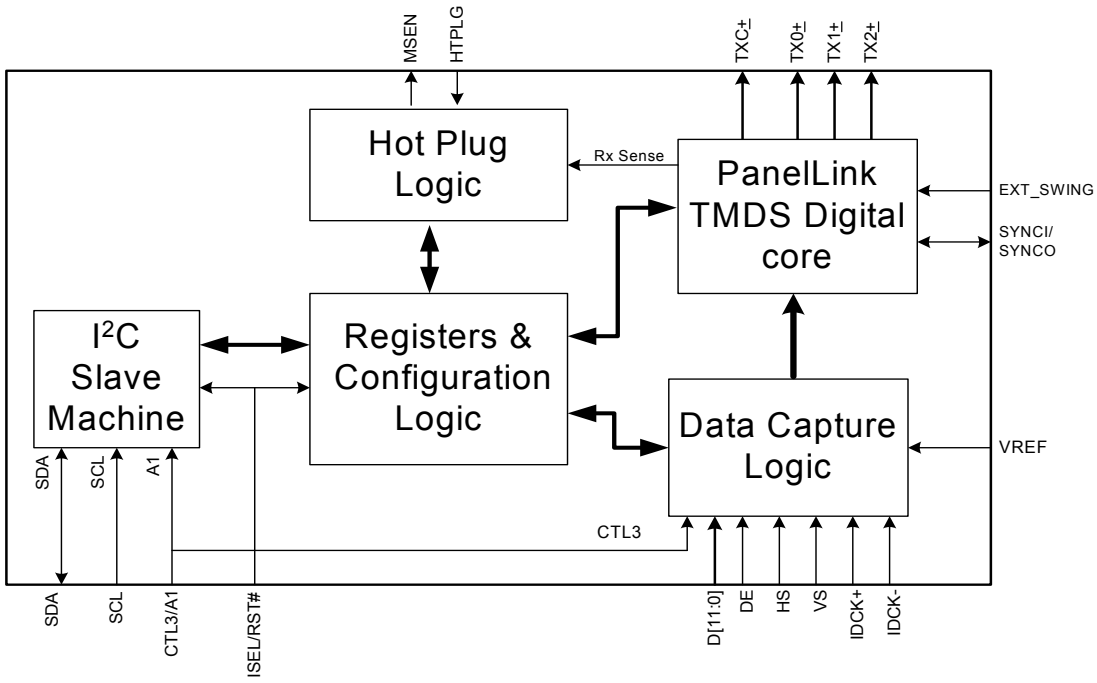


Figure 2. Functional Block Diagram

Data Capture Logic

The Data Capture Logic Block receives video data sent by the host over a 12-bit bus, with ½ pixel arriving at each sampled clock edge. Programming over the I^2C interface selects the edges of the clocks (rising or falling) to be used for first and second phase data sampling. The voltage level on VREF sets the SiI 1178 Tx in high swing or low swing mode. The VREF connection also determines whether one or two input clocks are used. In high swing mode, only a single clock, IDCK+, is used; data is latched on both edges of this clock. IDCK- is ignored in high swing mode and must be tied low. In low swing mode (DVO mode), both IDCK+ and IDCK- clocks are used to sample data. In low swing mode where only IDCK+ is available, IDCK- must be tied to VREF.

PanelLink TMDS Core

The PanelLink TMDS core encodes video information onto three TMDS differential data pairs and a differential clock pair. In dual link mode, where a pair of chips works together as “Master” and “Slave”, both cores are synchronized to each other by way of the SYNCO to SYNCI clock connection. Only the Master transmitter TMDS clock output is connected to the DVI connector. A resistor tied to the EXT_SWING pin is used to control the TMDS swing amplitude.

I²C Slave Machine, Registers, and Configuration Logic

The SiI 1178 Tx uses a slave I²C interface, capable of running up to 50kHz, for communication with the host. For the purposes of configuring the chip, registers are read and written through the slave I²C interface. The SiI 1178 Tx must be programmed via I²C to be operational for correct dual link operation and clock edge selection. The device may be powered down by setting the PD bit.

The slave I²C interface is not 5V tolerant. If the switching levels from the host are not 3.3V, then a voltage level shifter must be used. The RST# input resets the internal registers and is asserted after power up and receipt of a stable input pixel clock.

Hot Plug Logic

Connection of a display to the DVI interface can be detected using the Receiver Sense logic. Either the state of the detection, or an interrupt signal indicating a change of state, may be sent to the MSEN pin. This is useful to the host controller monitoring the SiI 1178 Tx. The HTPLG signal from DVI indicates that a monitor EDID is available for reading by the host via the DDC bus.

Electrical Specifications

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC} [1,2]	Supply Voltage 3.3V	-0.3		4.0	V
V_I [1,2]	Input Voltage	-0.3		V_{CC}+ 0.3	V
V_O [1,2]	Output Voltage	-0.3		V_{CC}+ 0.3	V
T_J [1,2]	Junction Temperature (with power applied)			125	°C
T_{STG} [1,2]	Storage Temperature	-65		150	°C

Notes
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{P-P}
T_A	Ambient Temperature (with power applied[1])	0	25	70	°C
θ_{JA-4LS}	Thermal Resistance (Junction to Ambient)[2]			36	°C/W
$\theta_{JA-4LNS}$	Thermal Resistance (Junction to Ambient)[3,6]			100	°C/W
θ_{JA-2LS}	Thermal Resistance (Junction to Ambient)[4]			63	°C/W
$\theta_{JA-2LNS}$	Thermal Resistance (Junction to Ambient)[5, 6]			109	°C/W

Note
1. Airflow at 0 m/s.
2. Multilayer board, E-pad soldered.
3. Multilayer board, E-pad not soldered.
4. Two-layer board, E-pad soldered.
5. Two-layer board, E-pad not soldered.
6. See page 34 for solder down requirements.

DC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND – 0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			V_{CC} + 0.8	V
V_{REF}	Input Reference Voltage	Low Swing Mode	0.50	0.75	0.95	V
		High Swing Mode	3.00	3.30	3.60	
V_{IH}	High swing high-level input voltage	$V_{REF} = V_{CC}$	2.0		V_{CC} + 0.3	V
V_{IL}	High swing low-level input voltage	$V_{REF} = V_{CC}$	–0.3		0.8	V
V_{SH}	Low swing high-level input voltage	$V_{REF} = V_{DDQ}/2$	$V_{DDQ}/2$ + 100mV			V
V_{SL}	Low swing low-level input voltage	$V_{REF} = V_{DDQ}/2$			$V_{DDQ}/2$ – 100mV	V
I_{IL}	Input Leakage Current	High Impedance	-10		10	µA
V_{OD}	Differential Voltage[2] Single Ended peak-to-peak Amplitude	R_{LOAD}= 50 Ω R_{EXT_SWING} = 390 Ω	510	550	590	mV
V_{DOH}	Differential High Level Output Voltage[2]			AVCC		V
I_{DOS}	Differential Output Short Circuit Current[1]	V_{OUT} = 0V			5	µA
I_{PDQ}	Quiet Power-down Current[3]	PD bit = 0, V_{CC}=3.6V, 0°C ambient			5	mA
I_{PD}	Power-down Current[4]				5	mA
I_{CCT}	Transmitter Supply Current	Typical Pattern[5] at IDCK=165MHz, 25°C ambient, V_{CC}=3.3V, one pixel per clock mode. R_{EXT_SWING} = 390 Ω		135		mA
		Worst Case Pattern[6] at IDCK=165MHz, 0°C ambient, V_{CC}=3.6V, one pixel per clock mode. R_{EXT_SWING} = 390 Ω			170	mA

Notes

1. Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions for a pulse of greater than 3 ns or for more than one third of the clock cycle, whichever is less. Exceeding the Clamp Current I_{CL} listed can result in permanent damage to the chip.
2. Guaranteed by characterization.
3. Quiet Power-down current measured with no transmitter input pins toggling.
4. Power-down current measured with input data bus and control signals toggling.
5. Typical pattern consists of a gray scale area, a checkerboard area, and a text area.
6. Worst-case pattern consists of a black and white checkerboard pattern, with each square being two pixels wide.
7. VDDQ defines the maximum voltage level of Low Swing input. It is not an actual input voltage. Chip characterization for Low Swing operation is performed at 1.5V only. Voltage level of Low Swing input should never exceed absolute maximum rating.

AC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{CIP}	IDCK Period	one pixel per clock	6		40	ns	Figure 3	4
F_{CIP}	IDCK Frequency	one pixel per clock	25		165	MHz	Figure 3	4
T_{CIH}	IDCK High Time	IDCK = 165MHz	2.6			ns	Figure 3	4
T_{CIL}	IDCK Low Time	IDCK = 165MHz	2.9			ns	Figure 3	4
S_{LHT}	Differential Swing Low-to-High Transition Time	R_{LOAD} = 50Ω, R_{EXT_SWING} = 390Ω	170	200	230	ps	Figure 4	6
S_{HLT}	Differential Swing High-to-Low Transition Time	R_{LOAD} = 50Ω, R_{EXT_SWING} = 390Ω	170	200	230	ps	Figure 4	6
T_{IJIT}	Worst Case IDCK Jitter				1	ns		2
T_{SHS}	Data, DE, VSYNC, HSYNC Setup Time to IDCK+ falling/rising edge	V_{REF} = 3.3V (High Swing Input)	0.6			ns	Figure 8	1,5,7
T_{HHS}	Data, DE, VSYNC, HSYNC Hold Time from IDCK + falling/rising edge	V_{REF} = 3.3V (High Swing Input)	0.5			ns	Figure 8	1,5,7
T_{SLS}	Data, DE, VSYNC, HSYNC Setup Time to IDCK± falling/rising edge	V_{REF} = 0.75V (Low Swing Input)	See note 8			ns	Figure 7	1,5
T_{HLS}	Data, DE, VSYNC, HSYNC Hold Time from IDCK± falling/rising edge	V_{REF} = 0.75V (Low Swing Input)	See note 8			ns	Figure 7	1,5
T_{HDE}	DE high time				8191	T_{CIP}	Figure 6	1
T_{LDE}	DE low time		128			T_{CIP}	Figure 6	1,5
T_{DDF}	VSYNC and HSYNC Delay from DE falling edge			1		T_{CIP}	Figure 5	
T_{DDR}	VSYNC and HSYNC Delay to DE rising edge			1		T_{CIP}	Figure 5	
T_{I2CDVD}	SDA Data Valid Delay from SCL high to low transition	C_L = 400pf		3		us	Figure 9	3
T_{RESET}	RST# Signal Low Time required for valid reset		50			µs	Figure 10	
T_{STEP}	De-skew step size increment	See page 18 for range				ps	Figure 14	

Notes:

1. Guaranteed by design.
2. Actual jitter tolerance may be higher depending on the frequency of the jitter.
3. I^2C operation is guaranteed rated at 50kHz and slower speeds.
4. Minimum frequency (maximum IDCK period) defined per DVI 1.0 Specification, section 2.3.1.
5. DE Low time defined as per DVI 1.0 Specification, Section 3.4 Link Timing Requirements.
6. TMDS rise and fall times per DVI 1.0 Specification, Table 4-4, as 0.4*T_{BIT} maximum, where T_{BIT} = 1/10th of T_{CIP}.
7. Typical VCC is defined at 3.3V.
8. The SiI 1178 Transmitter Low Swing timing mode is designed to meet all Intel DVO operational requirements. The DVO interface is proprietary to Intel Corp. and therefore these timings cannot be disclosed here. Refer to the Intel DVO 2.0 specification for details.

Timing Diagrams

Input Timing Diagrams

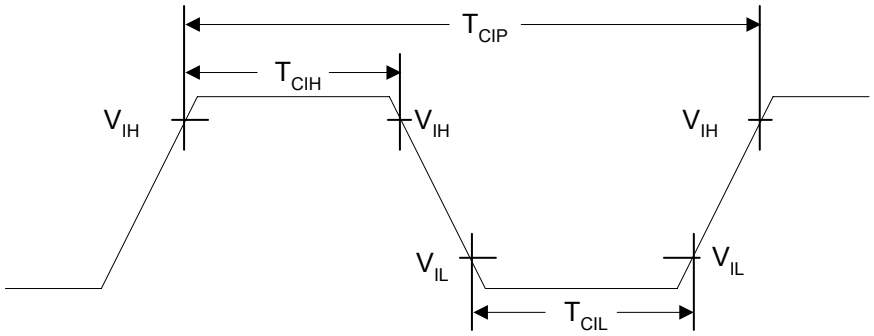


Figure 3. Clock Cycle/High/Low Times in High Swing Mode

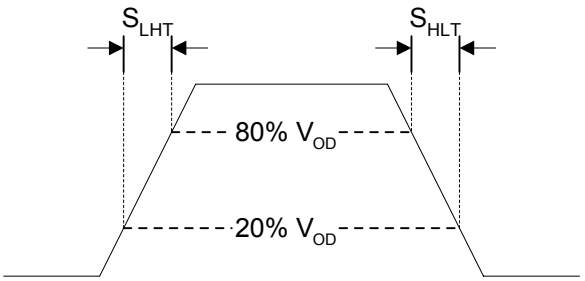


Figure 4. Differential Transition Times

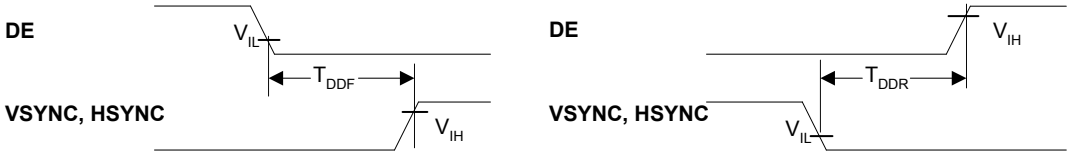


Figure 5. VSYNC, HSYNC Delay Times to DE

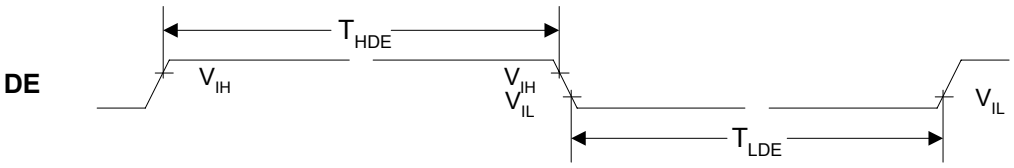


Figure 6. DE High/Low Times

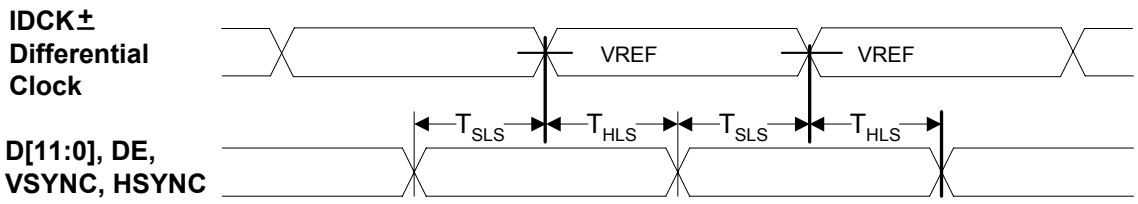


Figure 7. Low Swing Control and Data Setup/Hold Times to IDCK± Differential Clock

Note that VREF is set to $V_{DDQ}/2$ in Low Swing Mode.

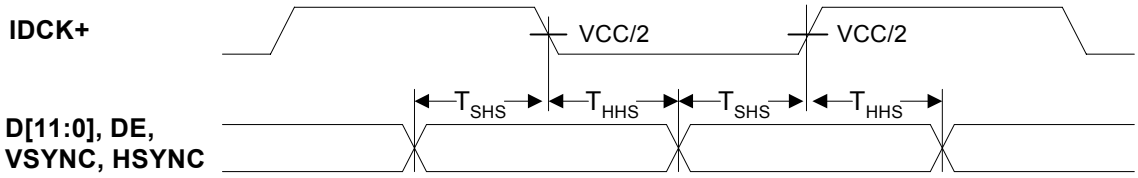


Figure 8. High Swing Control and Data Setup/Hold Times to IDCK+

Note that typical VCC is 3.3V.

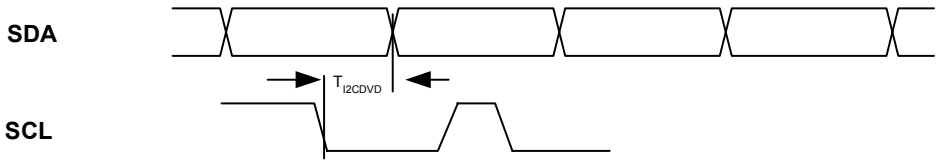


Figure 9. I²C Data Valid Delay (driving Read Cycle data)

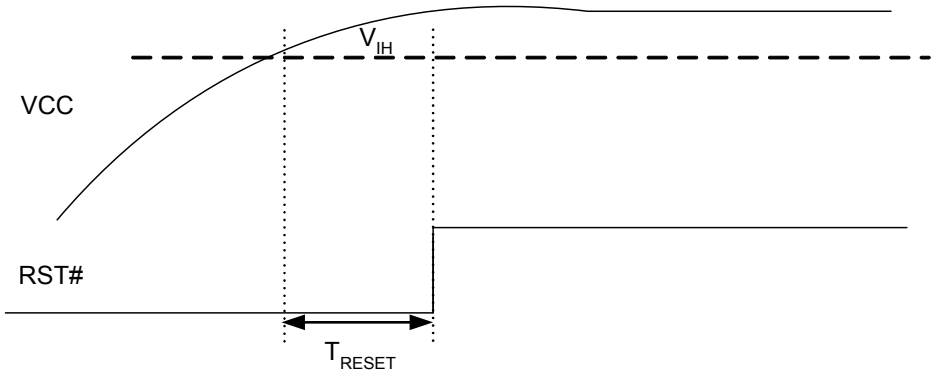


Figure 10. RST# Minimum Timing

Note that VCC must be stable between its limits for Normal Operating Conditions for T_{RESET} before RST# is high. RST# must also be pulled LOW for T_{RESET} before accessing registers.

Pin Descriptions

The SiI 1178 Tx is limited to operation in I²C mode. All required dynamic configuration, including switching between single link and dual link operation, can be achieved via I²C operations to registers

Input Pins

Pin Name	Pin #	Type	Description
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11	18 17 16 15 14 13 10 9 8 7 6 5	In	12-bit pixel bus input. For single link and high-resolution dual link applications, this bus inputs one-half pixel (12 bits) at every clock sampling point. For deep color dual link applications, this bus takes in either the most significant or least significant bits. Refer to Table 5 and Table 6 for exact mapping details.
IDCK+	12	In	Input Data Clock +. In high swing mode, this pin alone is used for data latching on both edges. In low swing mode, the input clock is sensed differentially (IDCK+ minus IDCK-).
IDCK-	11	In	Input Data Clock –. This clock is only used in low swing mode; the input clock is sensed differentially as noted above. In high swing mode, this pin should be tied to GND. However, in the case of low swing mode where only IDCK+ is supplied, tie IDCK- to the same voltage level as the VREF pin.
DE	19	In	Data enable. This signal is high when input pixel data is valid to the transmitter and low otherwise. It is critical that this signal have the same setup/hold timing as the data bus.
HSYNC	20	In	Horizontal Sync input control signal.
VSYNC	21	In	Vertical Sync input control signal.
CTL3 + A1	24	In	Control 3 Input + I²C Address Select. The use of this multi-function input depends on RST#. A1 - The bus device address to which the I²C interface will respond is determined by the state of the A1 pin during the rising edge of RST#. A1 is used to set the second bit of the I²C device address; it also determines whether the part will be Master or Slave when used in dual link applications. A1 = HIGH at reset: I²C Address 0x72; preconfigured for Slave A1 = LOW at reset: I²C Address 0x70; preconfigured for Master The device is only fully configured for dual link after the DLNKEN bit is set via I²C registers. CTL3 - After RST# goes high and the A1 setting has been latched, this pin functions as the CTL3 input unless the CTL23en bit is used to disable it. See page 12 for information.

Status Pin

Pin Name	Pin #	Type	Description
MSEN	48	Out	Monitor Sense. This output is programmable through the I^2C interface either to indicate the Receiver Sense status (available only on DC-coupled systems) or the Hot Plug status, or to generate an interrupt that one of these has changed state. This is an open-collector pin. Therefore, an external pull-up resistor to the host input interface voltage (5KΩ recommended) is required on this pin whenever the pin output function is used. This pin must be connected from the Master to Graphics Host for display detection. However this pin can be no connect for Slave Tx.

Configuration/Programming Pins

Pin Name	Pin #	Type	Description
RST#	25	In	Reset / I^2C Interface Address Select. This pin acts as an asynchronous reset to the I^2C interface controller. It must be set HIGH for normal operation after the Graphics Host has satisfied the minimum T_{RESET} assertion time. Also, a low-to-high edge on this pin latches the state on the CTL3/A1 pin to set the I^2C device access address bit A1.
SCL	27	In	I^2C Clock. This pin is the I^2C Clock input. The incoming clock may be run up to 50kHz. This pin is not 5V-tolerant and will only support 3.3V signaling. When sharing with lower voltage or higher voltage I^2C clocks, a level shifter will be required. See Figure 17 for a circuit example on 1.5V to 3.3V level shifting. This is an open-collector pin. Therefore, a pull-up resistor to 3.3V (2.2KΩ to 4.7KΩ recommended) must be used.
SDA	26	In	I^2C Data. This pin is the I^2C Data input and output. The incoming data may be run up to 50kHz. This pin is not 5V-tolerant and will only support 3.3V signaling. When sharing with lower voltage or higher voltage I^2C clocks, a level shifter will be required. See Figure 17 for a circuit example on 1.5V to 3.3V level shifting. This is an open-collector pin. Therefore, a pull-up resistor to 3.3V (2.2KΩ to 4.7KΩ recommended) must be used.
HTPLG	44	In	Hot Plug input. This pin is used to monitor the “Hot Plug” detect signal from the DVI Connector. This pin is not 5V-tolerant and a 5V to 3.3V level shifting circuit must be used as shown in Figure 26.
EXT_SWING	30	Analog	Voltage Swing Adjust. This resistor sets the amplitude of the voltage swing. Each Master and Slave must have a separate 390Ω ± 5% resistor on this pin pulled up to AVCC. A smaller resistor value sets a larger voltage swing and vice versa.

Input Voltage Reference Pin

Pin Name	Pin #	Type	Description
VREF	2	Analog	Input Reference Voltage. Selects the swing range of the digital parallel data inputs (D [11:0], DE, VSYNC, HSYNC and IDCK±). To enable high swing mode, VREF should be set to 3.3V. When VREF is between 0.5V and 0.95V, the digital parallel data inputs are low swing inputs. In low swing mode, VREF must be set to ½ the value of the maximum low swing input voltage. For DVO mode, VREF should be set to 0.75V. CTL3 is always assumed to be a high swing signal and therefore is not affected by VREF.

Output and Differential Signal Data Pins

Pin Name	Pin #	Type	Description
TX0+	36	Analog	TMDS Low Voltage Differential Signal output data pairs.
TX0-	35	Analog	
TX1+	39	Analog	
TX1-	38	Analog	
TX2+	42	Analog	
TX2-	41	Analog	
TXC+	33	Analog	TMDS Low Voltage Differential Signal output clock pair.
TXC-	32	Analog	

Dual Link Configuration and Control Pin

Pin Name	Pin #	Type	Description
SYNCO/ SYNCI	47	In/Out	Sync Out / Sync In. This pin can be switched between 2 functions during Dual Link mode. This pin is always configured in High Swing mode. SYNCO (A1 = LOW, DLNKEN bit = 1) This pin is an Clock output signal from the dual link Master. This pin should be connected to the Slave SYNCI pin for core clock synchronization with the Slave. SYNCI (A1 = HIGH, DLNKEN bit = 1) This pin is an input to the dual link Slave. This pin should be connected to the Master SYNCO pin for core clock synchronization with the Master. The SYNCO to SYNCI trace should be as short as possible.

Power and Ground Pins

Pin Name	Pin #	Type	Description
VCC	3,22	Power	Digital VCC must be set to 3.3V nominal.
GND	1,4,23	Ground	Digital GND.
AVCC	34,40	Power	Analog VCC must be set to 3.3V nominal.
AGND	31,37,43	Ground	Analog GND.
PVCC1	28	Power	PLL Driver Analog VCC must be set to 3.3V nominal.
PVCC2	46	Power	Filter PLL Analog VCC, must be set to 3.3V nominal.
PGND	29,45	Ground	PLL Analog GND.

Feature Information

I²C Interface

The SiI 1178 Tx slave state machine operates from an internal clock derived from the incoming SCL signal. No video clock and input is required to read and write to the I²C registers from address 0x00 to 0x0F. These accesses can also take place using only the SCL clock in power down mode.

The SiI 1178 Tx responds to the seven-bit binary I²C address of 0x70 in Master Mode and 0x72 in Slave Mode. A read or write transaction is determined by bit 0 of the I²C address. Setting this bit to 1 will enable a write transaction and setting this bit to 0 will enable a read transaction.

The I²C read operation is shown in Figure 11, and the write operation in Figure 12.

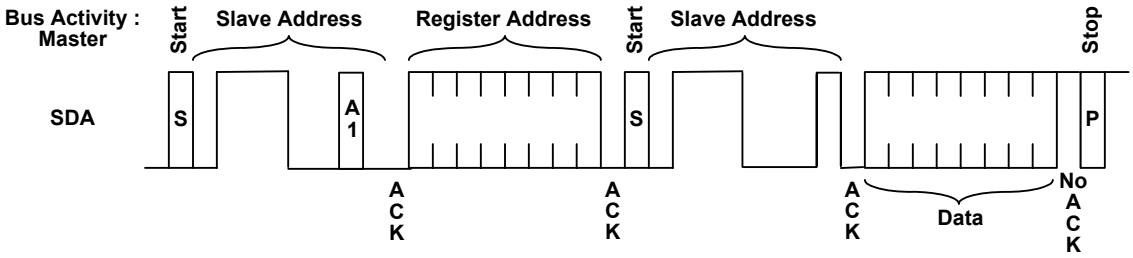


Figure 11. I²C Byte Read

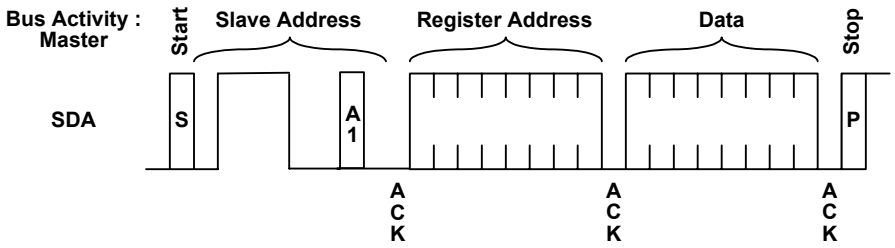


Figure 12. I²C Byte Write

I²C Register Mapping

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initialization Value	Notes
0x0	VND_IDL								0x01	
0x1	VND_IDH								0x00	
0x2	DEV_IDL								0x06	
0x3	DEV_IDH								0x00	
0x4	DEV_REV								0x00	
0x5	RSVD								••	4
0x6	FRQ_LOW								0x19	
0x7	FRQ_HIGH								0xA5	
0x8	RSVD write to 00		VEN	HEN	RSVD write to 01		EDGE	PD	00110100	3, 5
0x9	VLOW	MSEL[2:0]			TSEL	RSEN	HTPLG	MDI	•010••••	3, 5
0xA	RSVD write to 1	DK[1:0]		CTL23_ EN	CTL[3:0]				10010001	4, 5
0xB	RSVD								••	4
0xC	RSVD write to 1	MSTR_ SLV	RSVD write to 001001						1•001001	5
0xD	DCTL[2:0]			DLKEN	RSVD write to 0000				01100000	4, 5
0xE	RSVD write to 00		EZONE	ZONEF	ZONEO	RSVD write to 001			00000001	
0xF	RSVD								0x0C	4

Notes:

1. Legend: Symbol ● indicates either an indeterminate value or a value set dynamically based on pin input level. Hexadecimal values use a prefix of '0x'. All values use bit 7 as most significant, bit 0 as least significant.
2. Read-only or read/write capabilities are noted on the next page.
3. On any RST# assertion event, all registers that have default values lose their previously programmed value and are set back to the default values listed on the next page.
4. Registers listed as RSVD and shaded gray are reserved for factory use and should not be accessed.
5. Write the initialization values indicated.

Table 1. General I²C Register Definitions

Register Name	Access	Description
VND_IDL	RO	Vendor ID Low byte (0x01)
VND_IDH	RO	Vendor ID High byte (0x00)
DEV_IDL	RO	Device ID Low byte (0x06)
DEV_IDH	RO	Device ID High byte (0x00)
DEV_REV	RO	Device Revision (0x00)
FRQ_LOW	RO	IDCK. Low frequency limit is 25MHz. (0x19)
FRQ_HIGH	RO	IDCK High frequency limit is 165MHz. (0xA5)
HEN	RW	Horizontal Sync Enable 0 – HSYNC input is transmitted as fixed LOW 1 – HSYNC input is transmitted as input. → Default
VEN	RW	Vertical Sync Enable 0 – VSYNC input is transmitted as fixed LOW 1 – VSYNC input is transmitted as input. → Default
EDGE	RW	Edge Select 0 – Falling edge latched first in dual edge mode→ Default 1 – Rising edge latched first in dual edge mode
PD	RW	Power Down mode 0 – Power Down. → Default after RESET 1 – Normal operation
VLOW	RO	Voltage Swing Mode 0 – VREF signal indicates low swing inputs 1 – VREF indicates high swing inputs
MSEL[2:0]	RW	Select source of the MSEN output pin 000 – Tri-state MSEN output (will go high due to pullup) 001 – Outputs the MDI bit (interrupt) 010 – Outputs the RSEN bit (receiver detect). → Default 011 – Outputs the HTPLG bit (hot plug detect) 100 to 111 – Do not use
TSEL	RW	Interrupt Generation Method 0 – Interrupt bit (MDI) is generated by monitoring RSEN 1 – Interrupt bit (MDI) is generated by monitoring HTPLG
RSEN	RO	Receiver Sense. This bit is HIGH if a powered on receiver is connected to the transmitter outputs, LOW otherwise. This function is only available for use in DC-coupled systems.
HTPLG	RO	Hot Plug Detect input. The state of HTPLG pin can be read from this bit.
MDI	RW	Monitor Detect Interrupt. Uses signal specified by TSEL to generate an interrupt. Write '1' to this bit to clear the interrupt status. 0 – Detection signal has changed logic level 1 – Detection signal has not changed state
DK[1:0]	RW	De-Skewing Setting. See page 18 for full control detail.
CTL[3:0]	RW	Control 3-0. General Purpose bits to transmit CTL0, CTL1, CTL2, CTL3 when DE is LOW. 0 – Transmit specific CTL as LOW 1 – Transmit specific CTL as HIGH Note that when CTL23_EN bit is set, only CTL 1:0 can be set with these bits.
CTL23_EN	RW	Control 2-3 Enable. This bit determines the source of CTL3 to be sent out over TMDS. 0 – Disable CTL3 input function, send CTL2-3 as defined by bit in CTL[3:0]. 1 – Enable CTL3 input as source for CTL3 over TMDS, CTL2=0. → Default

Notes:

1. RO = Read Only Registers
2. RW = Read/Write Registers
3. 'Default' indicates value set after a reset event. Not all bits default to a defined state after reset.

Table 2. Dual Link I²C Register Definitions

Register Name	Access	Description
DLNKEN	RW	Dual Link enable bit. 0 – Disable Dual Link mode.→ Default Value. 1 – Enable Dual Link mode.
MSTR_SLV	RO	Master/Slave Status. This bit is only valid when DLNKEN bit is 1. 0 – Slave in Dual Link mode. 1 – Master in Dual Link mode.
DCTL[2:0]	RW	Skew control between master and slave in DUAL link mode (see the dual link section for more information). Increment 260psec. 000 : 1 step→ minimum setup / maximum hold 001 : 2 step 010 : 3 step 011 : 4 step→ Default 100 : 5 step 101 : 6 step 110 : 7 step→maximum setup / minimum hold 111 : Not available.

Notes:
1. RO = Read Only Registers
2. RW = Read/Write Registers
3. Default indicates value set after Reset event.

RESET Description

The input pin RST# serves as an asynchronous (active LOW) reset signal for the I²C slave controller. The following lists the behavior of the chip during and after Reset:

- RST# must be driven low for at least 50µs for proper I²C logic reset.
- During reset, the chip I²C registers and logic cannot be accessed. Dual link mode cannot be selected during this period.
- After reset, the chip TMDS outputs will be turned OFF and all registers that are listed with default initialization values will be set to those values. The SiI 1178 Tx can be accessed and enabled via I²C beginning from this event.

Dual Zone PLL

The SiI 1178 Tx offers a dual-zone PLL that changes its operational parameters depending on the frequency zone selected. In the low zone, operation is ideal in the low frequency range, from 20MHz to around 120MHz. High zone operation is optimized in the high frequency range, above 100MHz. In the overlapping range, either low zone or high zone operation can be used.

Operating zone optimization contributes to robust operation over long cables. For example, optimized PLL characteristics account for the ability of the transmitter to send video at UXGA over 20m cables.

PLL zone selection is controlled either manually or automatically. Manual zone control is the preferred mode of operation.

Manual Zone Control

Whenever the application allows it, PLL zone selection should be made manually. The I²C register bits ZONEF and EZONE allow the host graphics controller to set the optimal zone for the current video resolution being transmitted. For frequencies over 100MHz, the controller should select high zone PLL operation. Table 3 describes the relevant register bits.

Automatic Zone Control

For applications that are not able to program the I^2C registers, the chip incorporates an automatic zone control circuit. This circuit determines whether the input pixel clock is operating in the low frequency range or the high frequency range, and sets the PLL zone selection accordingly. The chip defaults to the automatic mode of zone selection after reset.

The zone determination depends primarily on input frequency, but is also affected by operating voltage and chip temperature. Therefore, it is possible for an automatic zone switch to occur while video input is stable, causing momentary (~1μs) unevenness in the video output clock and data streams. This could occur, for example, while the chip is still warming up to its normal operating temperature. However, the automatic selection circuit provides wide hysteresis to ensure that there will not be any oscillation around the zone switch point.

Table 3. Dual Zone PLL I^2C Control Register Bits

Register Name	Access	Description
ZONEF	RW	Zone Force. Enable external selection of main PLL operating zone. When ZONEF=1, the main PLL zone is selected by EZONE. 0 – Automatic zone selection – EZONE bit disabled (default) 1 – Manual zone selection – EZONE bit enabled
EZONE	RW	External Zone Select. Selects operating zone of main PLL, but only when ZONEF=1 (disabled by default). 0 – Low zone (recommended for 20-120MHz) 1 – High zone (recommended for > 100MHz)
ZONEO	RO	Zone Output – indicates current operating zone. When ZONEF=0 (automatic), ZONEO indicates that PLL is operating in zone optimized for: 0 = Lower frequencies 1 = Higher frequencies. When ZONEF=1 (manual), ZONEO indicates the zone that automatic selection would have chosen. 0 – Low frequency operation is sensed 1 – High frequency operation is sensed

Input Signal Swing and Clocking Selection

The SiI 1178 Tx offers two modes of data input signal sampling. Within those modes the input clocking method can also be selected.

- High swing input is defined for signal swings associated with the chip digital VCC voltage, nominally 3.3V. Internal sampling is centered at the VCC/2 point. To select high swing operation, tie VREF to VCC.
  - High swing input automatically selects only a single input clock IDCK+. Tie IDCK- to GND.
- Low swing input is defined for signal swings that are lower than VCC. VREF selects the center point for the sampling, plus or minus 100mV. To select low swing input tie VREF to the max signal swing, divided by two. 1.5V DVO operation, for example, requires VREF to be tied to a 0.75V reference.
  - Two input clocks are used by default with low swing input mode. Connect both IDCK+ and IDCK- to the appropriate source clocks.
  - If only a single input clock is used with low swing input mode, tie the IDCK- pin to VREF.

Note that use of VREF for low swing sample point selection is valid only up to 1.9V. For high swing sample point selection, VREF can fall only in the nominal VCC range (3.0-3.6V). Other values for VREF are undefined.

EDGE Selection

The SiI 1178 Tx provides flexible edge selection.

- In high swing mode, the device supports a single clock input on IDCK+. The EDGE bit selects whether to latch the first data on the rising or the falling edge. In high swing mode, IDCK- must be grounded for proper operation.
- In low swing mode, the device supports dual clock inputs on IDCK+ and IDCK-. The EDGE bit selects whether to latch the data on the rising or the falling edges of the input clocks. If using only IDCK+ in low swing mode, IDCK- must be tied to VREF for proper operation.

Figure 13 details the behavior of the edge selection bit in both high swing and low swing modes

.

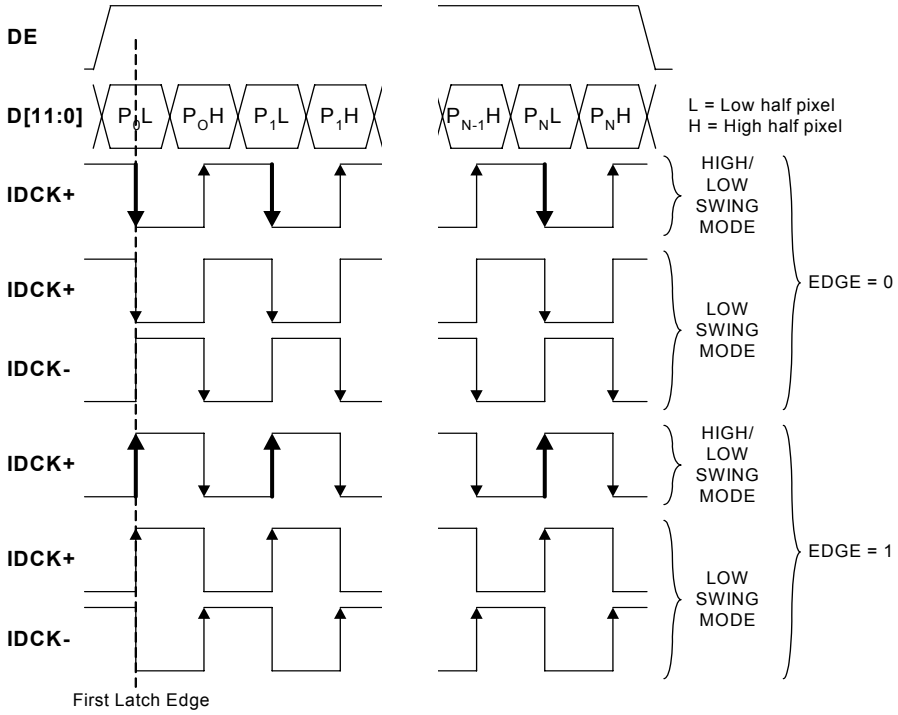


Figure 13. Logical Interface Options for 12-bit Mode

Data De-skew DK[1:0] Feature

Input clock to data setup/hold time can be adjusted through the use of the de-skew feature. It should be noted that it is the clock that is being adjusted internally. The configuration pins DK[1:0] or applicable I^2C registers can be used to vary the input setup/hold time by T_{CD}.

The DK[1:0] bits in the configuration registers can be used to control the T_{CD} value. Table 4 lists the De-skew time increment range and the effect on Setup and Hold.

The de-skew feature should not be used in dual link applications. The variability of the delay from one chip sample to the next would be compounded if two of the chips were used as they must be for dual link.

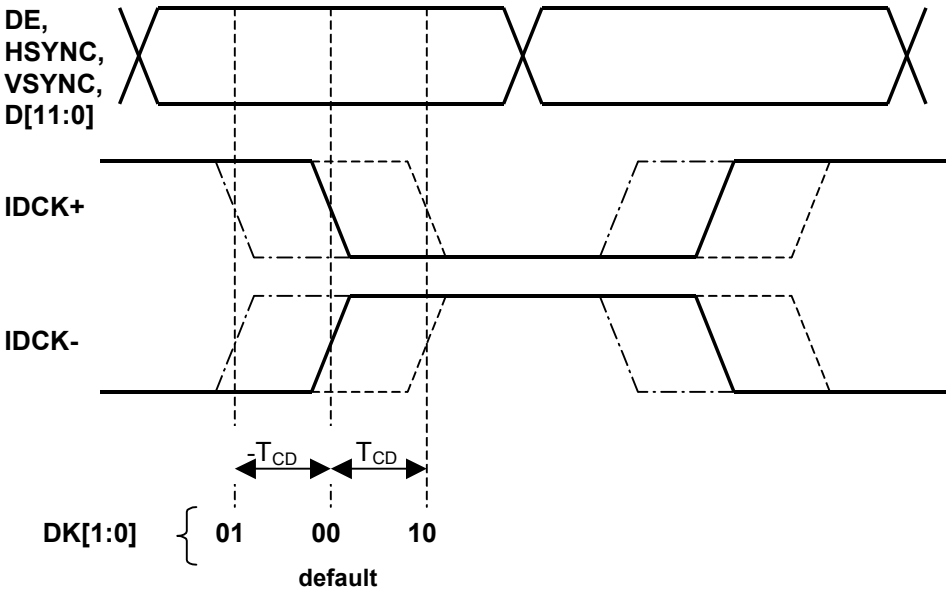


Figure 14. De-skewing Feature Timing

Table 4. DK[1:0] Increments and Effect on Setup and Hold times

DK[1:0]	De-Skew Time (T_{CD})	Setup and Hold Time Effect
01	-100ps to -400ps	Reduces Setup time, increases Hold time.
00	0 ps	No effect. Default and recommended setting.
10	+100ps to +400ps	Reduces Hold time, increases Setup time.
11	-300ps to +300ps	Not recommended.

Dual Link Applications

The SiI 1178 Tx is designed for use in pairs for dual link applications. The primary link or Master transmitter sends synchronization information to the secondary link or Slave transmitter to maintain the correct inter-pair skew among all six data pairs.

The DVI 1.0 specification requires that all pixel clock frequencies above 165MHz be transmitted over dual TMDS links. The specification also allows for extra color depth to be transmitted across the second link. The discussion below refers to the higher pixel rate application, but can also be applied to the extra color depth application as described in the Data Mapping Modes for Dual Link section.

The descriptions below differentiate dual link *mode* and dual link *operation* as follows.

Dual Link Mode: The circuit must be designed to indicate one Master and one Slave device; also the Master-to-Slave synchronization must be established. Finally, the chips must be programmed through the I^2C registers to recognize the dual link application.

Dual Link Operation: Once designed and configured for dual link mode, the chips can operate as either a single link or a dual link interface. The host graphics controller selects between single link and dual link operation through an I^2C register bit depending on pixel rate.

Data must not be supplied to the Master or Slave until both devices have been fully programmed to Dual Link mode.

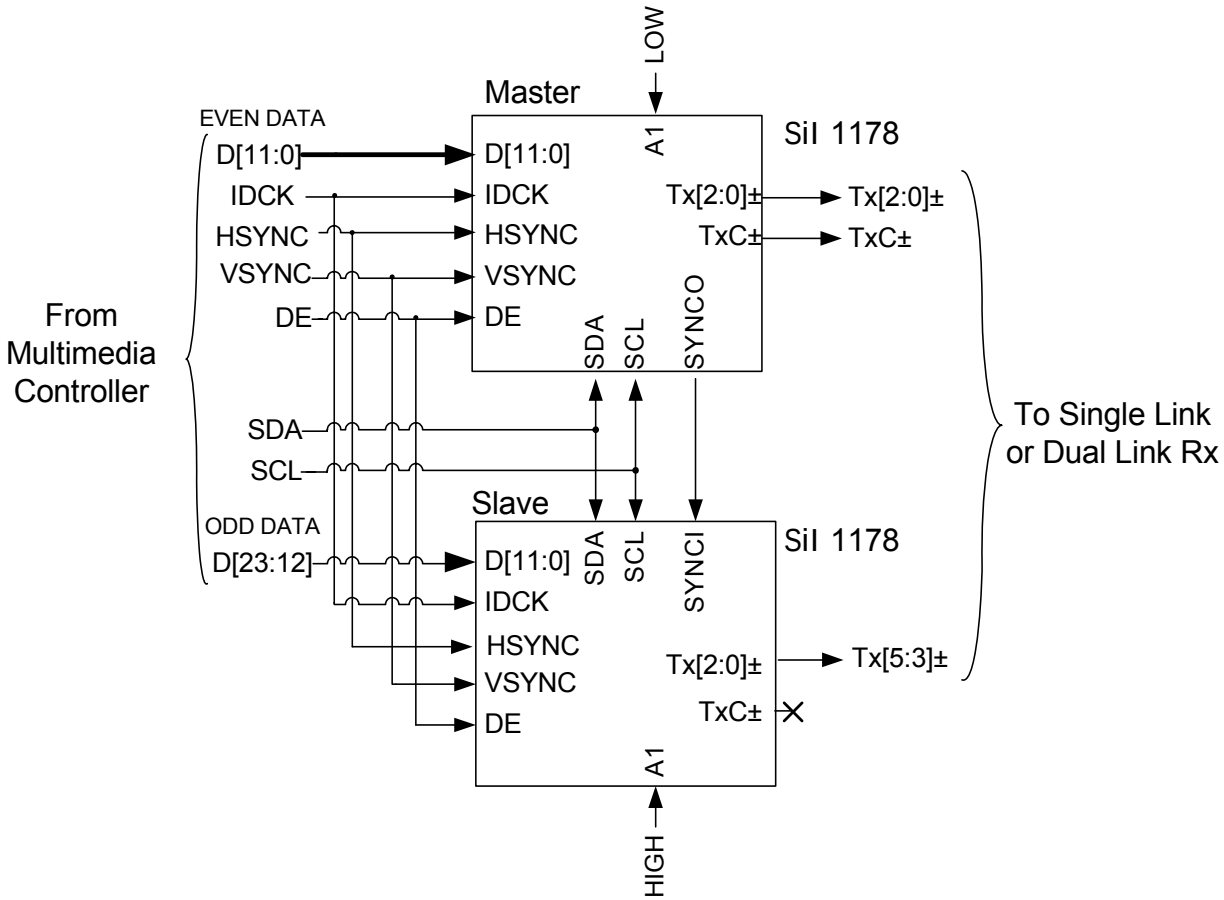


Figure 15. Dual Link Configuration

Master Configuration

The Master transmitter is partially configured for Master mode in a Dual Link operation by setting the A1/CTL3 pin to low before reset, as shown in Figure 15.

The primary 12-bit data from the host graphics controller is connected to the Master transmitter. This bus provides both EVEN and ODD pixels for pixel rates at or below 165MHz, and the EVEN pixel for pixels rates greater than 165MHz.

The Control Signals HSYNC, VSYNC and DE are connected to both the Master and Slave transmitters. Both transmitters require the DE signal (they cannot generate this signal internally). The input clock(s) are connected to both the Master and Slave transmitters.

The SYNCO pin of the Master transmitter is connected to the SYNCI pin of the Slave transmitter. This signal is used to synchronize the two transmitters. This signal has a skew control mechanism to control the skew between the Master and Slave transmitters, which is done through the I^2C register bits DCTL[2:0].

To fully enable the SiI 1178 Tx as Master in dual link mode, the DLNKEN bit must be set to 1. A detailed programming sequence is provided on page 23.

Slave Configuration

The Slave transmitter is partially configured for Slave mode in a Dual Link operation by setting the A1/CTL3 pin to high before reset as shown in Figure 15.

The secondary 12-bit data from the host graphics controller is connected to the Slave transmitter. This bus provides the ODD pixels for pixel rates greater than 165MHz. For rates at or below 165MHz, the host sends no data to the Slave transmitter. Instead, the host powers down the Slave by setting the PD bit in the I^2C registers.

It is important to explicitly power down the Slave transmitter when in single link operation, because the dual link Slave receiver will put the display device into dual link mode if it sees any secondary link activity (even just black video data).

The control signals HSYNC, VSYNC and DE along with input clock(s) are shared with the Master transmitter.

The SYNCI pin of the Slave transmitter is connected to the SYNCO pin of the Master transmitter as noted above.

To fully enable the SiI 1178 Tx as Slave in dual link mode, the DLNKEN bit must be set to 1. A detailed programming sequence is provided on page 23.

Master-Slave Skew Control

Due to the possibility of individual design constraints or mismatches between ODD and EVEN data synchronization, the SiI 1178 Tx has been designed with a dual link skew control feature. This feature allows the skew between the SiI 1178 Tx Master and Slave to be controlled by setting the DCTL[2:0] register. This register allows four steps for adjusting the output of the Master SiI 1178 Tx either ahead of or behind the outputs of the Slave device. This feature should only be used in to control or adjust excessive inter-pair skew between the DVI outputs of the Master and Slave. DCTL[2:0] will not adjust or compensate for input data setup and hold timing deficiencies. Definition of the steps available for DCTL[2:0] is provided in Table 2 on page 15.

Data Mapping Modes for Dual Link

The DVI 1.0 specification offers two uses for dual link. It can support either higher resolution, or else it can support greater color depth.

Table 5 shows how the mapping works for high resolution applications. The input data is divided up into even and odd pixels as shown. Pixels 0, 2, 4, etc. are carried on the Master link. Pixels 1, 3, 5, etc. are carried on the Slave link.

Table 5. Dual Link Data Mapping – High Resolution Application

Device	Pin Name	1st Clock Edge	2nd Clock Edge
Master SiI 1178 Tx EVEN Pixel Data	D11	G0[3]	R0[7]
	D10	G0[2]	R0[6]
	D9	G0[1]	R0[5]
	D8	G0[0]	R0[4]
	D7	B0[7]	R0[3]
	D6	B0[6]	R0[2]
	D5	B0[5]	R0[1]
	D4	B0[4]	R0[0]
	D3	B0[3]	G0[7]
	D2	B0[2]	G0[6]
	D1	B0[1]	G0[5]
	D0	B0[0]	G0[4]
Slave SiI 1178 Tx ODD Pixel Data	D11	G1[3]	R1[7]
	D10	G1[2]	R1[6]
	D9	G1[1]	R1[5]
	D8	G1[0]	R1[4]
	D7	B1[7]	R1[3]
	D6	B1[6]	R1[2]
	D5	B1[5]	R1[1]
	D4	B1[4]	R1[0]
	D3	B1[3]	G1[7]
	D2	B1[2]	G1[6]
	D1	B1[1]	G1[5]
	D0	B1[0]	G1[4]

Notes
1. Color Pixel Components: R = RED, G = GREEN, B = BLUE
2. Bit significance within a color: [7:0] = [Msb:Lsb]

Table 6 shows how the mapping works for deep color applications. The input data is divided up into Most Significant bits (MS bits) of the pixel and Least Significant bits (LS bits) as shown. The MS bits are carried on the Master link. The LS bits are carried on the Slave link, and are left-justified as noted in the DVI spec. Using this scheme ensures that connection of a future source with 12-bit or 16-bit color depth will still map the most significant bits correctly to a 10-bit display.

Table 6. Dual Link Data Mapping – 10-bit Deep Color Application

Device	Pin Name	1st Clock Edge	2nd Clock Edge
Master SiI 1178 Tx MS bits Pixel Data	D11	G0[5]	R0[9]
	D10	G0[4]	R0[8]
	D9	G0[3]	R0[7]
	D8	G0[2]	R0[6]
	D7	B0[9]	R0[5]
	D6	B0[8]	R0[4]
	D5	B0[7]	R0[3]
	D4	B0[6]	R0[2]
	D3	B0[5]	G0[9]
	D2	B0[4]	G0[8]
	D1	B0[3]	G0[7]
	D0	B0[2]	G0[6]
Slave SiI 1178 Tx LS bits Pixel Data	D11	low	R1[1]
	D10	low	R1[0]
	D9	low	low
	D8	low	low
	D7	B1[1]	low
	D6	B1[0]	low
	D5	low	low
	D4	low	low
	D3	low	G1[1]
	D2	low	G1[0]
	D1	low	low
	D0	low	low

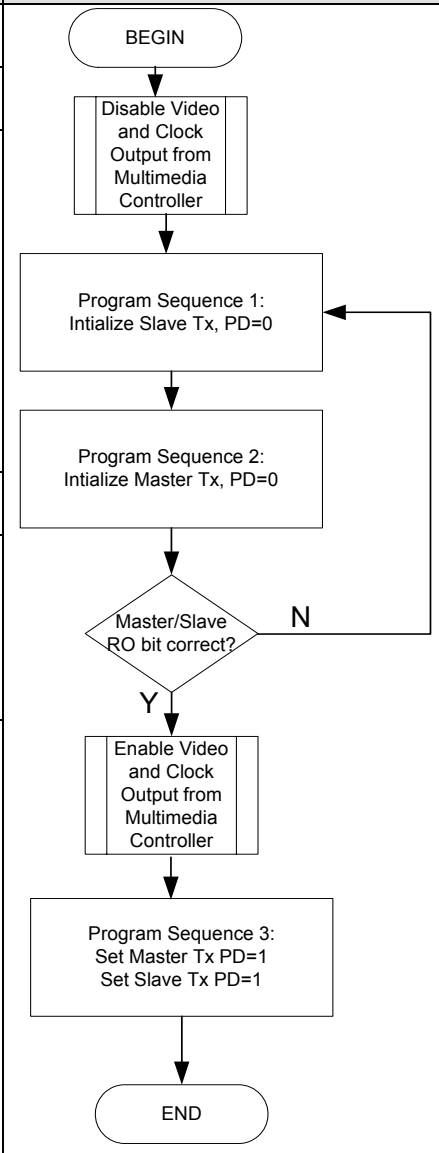
Notes
1. Color Pixel Components: R = RED, G = GREEN, B = BLUE
2. Bit significance within a color: [7:0] = [Msb:Lsb]

Dual Link I²C Programming Sequence Example

To enable the SiI 1178 Tx Master and Slave, the sequence in Table 7 provides a typical program flow. The example uses falling clock edges for input latching.

Table 7. Dual Link Programming Sequence and Flowchart

Step	Details	Flowchart
	Ensure that both Master and Slave have been configured to follow physical configuration shown on Figure 15	
	Disable all video and clock output from the host graphics controller.	
Program Sequence 1[1]	Program Slave (0x72) with the following register values. 0x0F→0x44 0x0F→0x4C [**This register must be set to this value for normal operation after resolution change, exit from power down mode, suspend and hibernation]** 0x0E→34h if > =100MHz(single Link); 10h if <100Mhz 0x0A→0x80 0x09→0x30 [Set MSEN to output Hotplug pin status] 0x0C→0x89 [Initialize reserved register bits] 0x0D→0x70 [Enable dual link function and default DCTL] 0x08→0x32 or 30h [Enable H/V Sync, set correct EDGE, but disable output]	
Program Sequence 2	Program Master (0x70) with the same sequence as above.	
Check Configuration	Check Master/Slave setting option. Read Master (0x70) 0x0C[6] = 1 Read Slave (0x72) 0x0C[6] = 0 Proceed if both bits are read back with the correct values.	
Program Sequence 3	Program Master (0x70) with the following register value. 0x08→0x31(EDGE = Low) or 0x33 (EDGE = High) [Enable output] Program Slave (0x72) with the following register value. 0x08→0x31(EDGE = Low) or 0x33 (EDGE = High) [Enable output]	



Notes
1. Entire programming sequence must be executed after every Reset event, Resolution swtich, Video Clock changes or suspend events.
2. Slave must be programmed before Master during all events listed in note 1.

Timing Diagrams

Figure 16 is an example of the timing for a dual link application. When the bandwidth is less than or equal to 165Mpps, the host graphics controller does not send any data to the Slave transmitter. The Slave transmitter is powered down by setting bit PD=0 in the I²C registers. The host graphics controller is sending both EVEN and ODD data to the Master transmitter via the primary 12-bit bus in single link mode.

When the bandwidth is greater than 165Mpps, the host graphics controller sends the EVEN data to the Master transmitter via the primary 12-bit bus and the ODD data to the slave transmitter via the secondary 12-bit bus. It also powers up the Slave transmitter by setting bit PD=1 in the I^2C registers.

The host graphics controller is always driving the data in 12 bits, in both dual-edge/single-clock and single-edge/dual-clock modes. Only in dual link applications are both the Master and Slave transmitters configured to receive data in that mode.

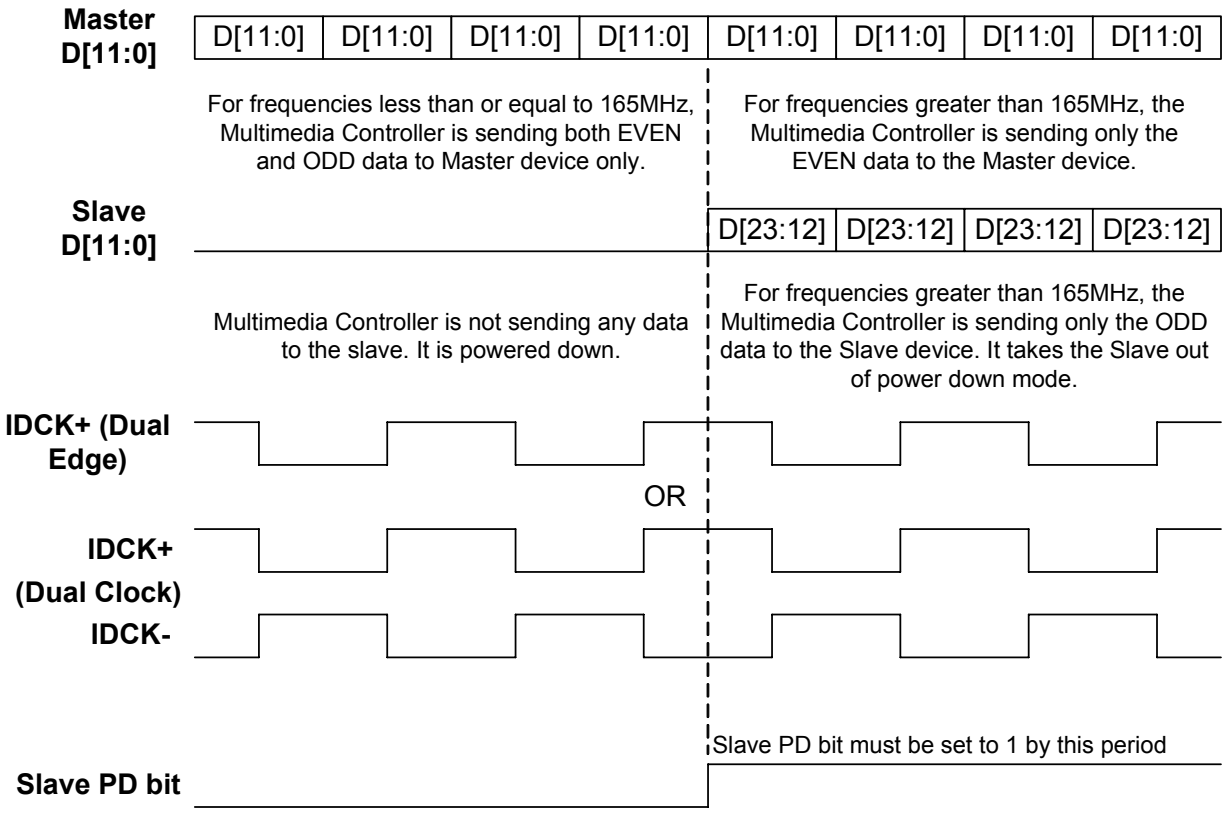


Figure 16. Single/Dual Link Timing Diagram

Enabling Hot Plug Detection Mode

As documented in the VESA Digital Flat Panel Standard, all monitors are required to support Hot Plug Detection but support is optional for the host. The SiI 1178 Tx supports the Hot Plug Detect feature. In I^2C mode, use the HTPLG input. It should be noted that the HTPLG pin on the SiI 1178 Tx is only 3.3V tolerant. Therefore, the HTPLG voltage level from the DVI connector should be level shifted or clamped at 3.3V.

When the voltage level at the HTPLG pin is 3.3V, the HTPLG bit will be set to 1. To output the HTPLG bit via the MSEN pin, register bits MSEL [2:0] should be programmed to 011.

The SiI 1178 Tx can also be programmed to determine Hot Plug detection via the Receiver Sense function. In this mode, input of the HTPLG signal is not required. By programming MSEL[2:0] to 010, the SiI 1178 Tx will output the RSEN bit state though the MSEN pin to indicate whether the SiI 1178 Tx is connected to a powered receiver.

Design Recommendations

The following sections describe recommendations for robust board design with the SiI 1178 Tx. Designers should include provision for these circuits in their design, and adjust the specific passive component values according to the characterization results.

Overview of Pin Differences

When used in an SiI 1162 Tx application, the SiI 1178 Tx is a drop-in replacement that also offers increased input clock jitter tolerance. However, the SiI 1178 Tx part only supports I^2C -controlled mode of operation – it cannot be used in a strap-selected application as the SiI 1162 Tx could. Two pins change function as a result.

ISEL/RST# → RST#: The ISEL function of the SiI 1162 Tx, used to set strap-operated mode, is no longer supported.

PD#: The PD# input pin is no longer available. Power down must instead be controlled by the PD bit in the I^2C register set.

1.5V to 3.3V I^2C Bus Level-Shifting

The SiI 1178 Tx I^2C SDA and SCL swing level must be 3.3V. Intel motherboards with DVO sources provide an I^2C signal with voltage swing of 1.5V. To ensure proper initialization of the SiI 1178 Tx, a bi-directional voltage level-shifting circuit between the SiI 1178 Tx I^2C bus and the Intel Graphics Host should be implemented. Two possible choices that have been tested by Silicon Image for this purpose are a dual N-channel transistor (Fairchild Semiconductor NDC7002N) and a high-speed bus switch (Philips GTL2010).

Figure 17 is a schematic example using the Fairchild dual N-channel transistor to translate I^2C from 1.5V to 3.3V and vice versa.

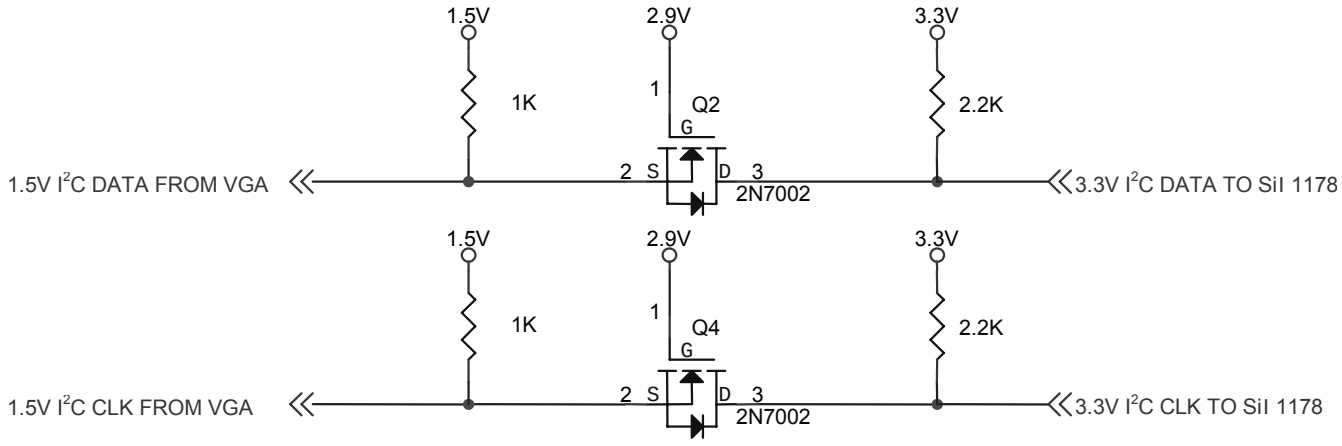


Figure 17. I^2C Bus Voltage Level-Shifting using Fairchild NDC7002N

Figure 18 is a schematic example using the Philips high-speed bus switch to achieve a 1.5V to 3.3V bi-directional level-shift.

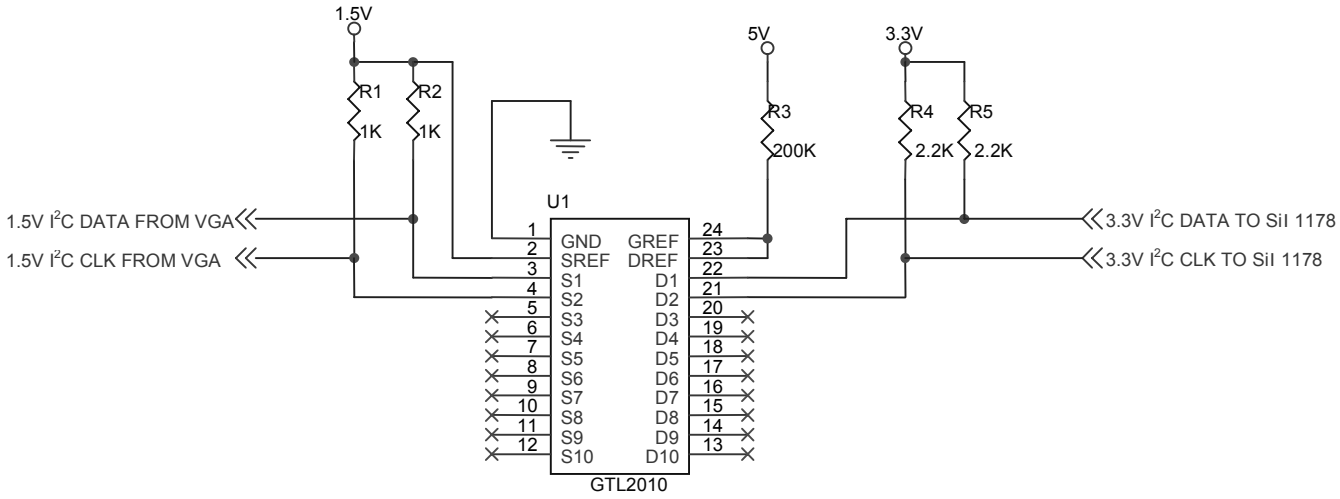


Figure 18. I²C Bus Voltage Level Shifting using Philips GTL 2010

ESD Protection on TMDS Output Pins

Silicon Image does not advise inserting ESD devices onto the differential lines between the SiI 1178 transmitter and the connector in high-speed applications. Capacitance and inductance on these lines from such discrete devices will adversely affect the high-speed performance as it will change the impedance of the lines. However for applications with throughput of less than 108Mbps, a small signal diode such as the BAV99 and 10Ω series resistors may be placed on the differential lines. The diodes should be placed closer to the DVI connector while the 10 Ω resistors should be placed closer to the transmitter output. As noted in the section Transmitter Layout (page 30), 100Ω differential impedance is an important parameter for proper layout. See Figure 19 for an illustration.

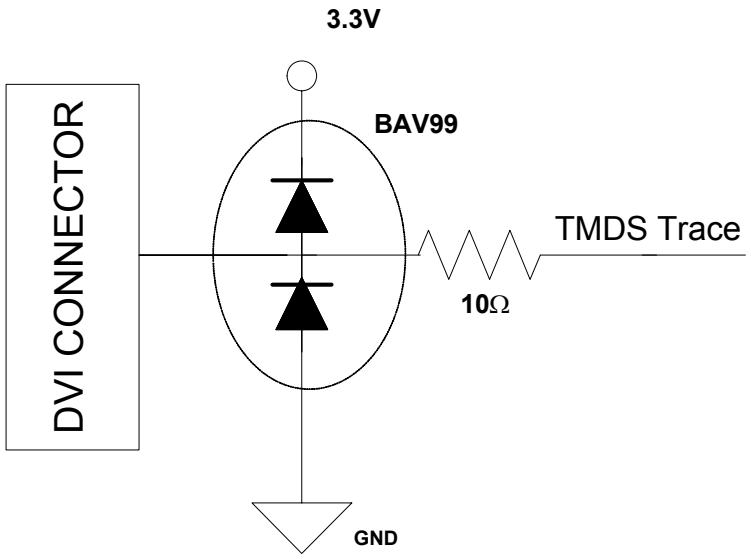


Figure 19. ESD Protection Circuit

Voltage Ripple Regulation

The power supply to VCC pins is very important to the proper operation of the transmitter. An example of a tested regulator circuit is shown in Figure 20. Note that alternative voltage regulator circuits should be considered only if they meet the LM317 standards of line/load regulation. To regulate to 3.3V from a 5V source, choose a voltage regulator capable of 1.7V dropout (such as the LM1117).

Decoupling and bypass capacitors are also involved with power supply connections, as described in detail in Decoupling Capacitors on page 27.

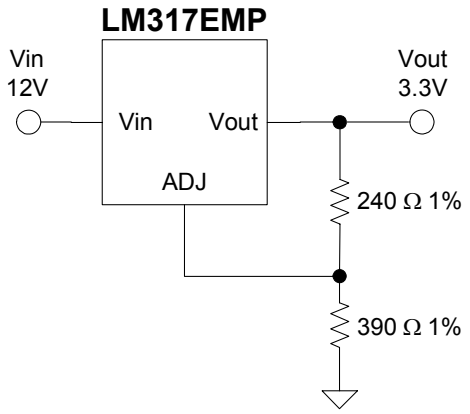


Figure 20. Voltage Regulation using LM317EMP

PCB Ground Planes

All ground pins on the device should be connected to the same, contiguous ground plane in the PCB for dual link applications. This approach helps to avoid ground loops and inductances from one ground plane segment to another. Such low-inductance ground paths are critical for return currents, which affect EMI performance. The entire ground plane surrounding the PanelLink transmitter should be one piece, and include the ground vias for the DVI connector.

Decoupling Capacitors

Designers should include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 22. Place these components as close as possible to the PanelLink device pins, and avoid routing through vias if possible. Figure 21 is representative of the various types of power pins on the transmitter.

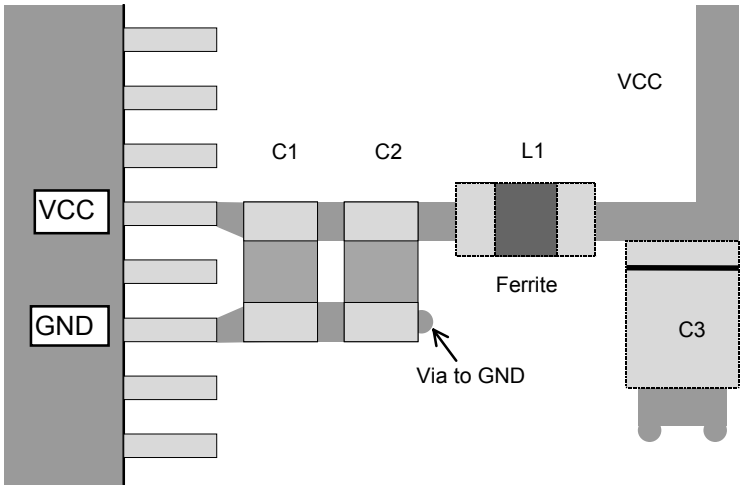


Figure 21. Decoupling and Bypass Capacitor Placement

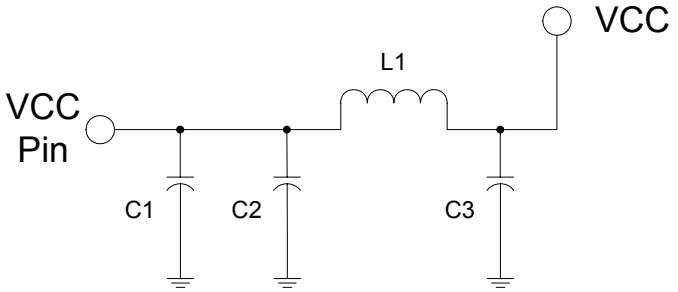


Figure 22. Decoupling and Bypass Schematic

The values shown in Table 8 are recommendations that should be adjusted according to the noise characteristics of the specific board-level design. Pins in one group (such as VCC) for an individual SiI 1178 Tx may share C2, the ferrite and C3. Master and Slave must **not** share the same decoupling capacitors for any pin group: each pin should have a separate C1 placed as close to the pin as possible.

Table 8. Recommended Components for 1-2MHz Noise Suppression

C1	C2	C3	L1
100 – 300 pF	0.1 µF	10 µF	Ferrite, 200+ Ω @ 100MHz

Source Termination Resistors on Differential Outputs

Source termination, consisting of a 300Ω resistor (this value may vary on the physical design and electrical characteristics of the PCB) and a 0.1µF non-polar capacitor, should be used on the differential outputs of the Master and Slave SiI 1178 Tx to improve signal swings. See Figure 23 for an illustration.

Note that the specific value for the source termination resistor and capacitor will depend on the PCB layout and construction. Different values may be needed to create optimum DVI-compliant output waveforms from the transmitter.

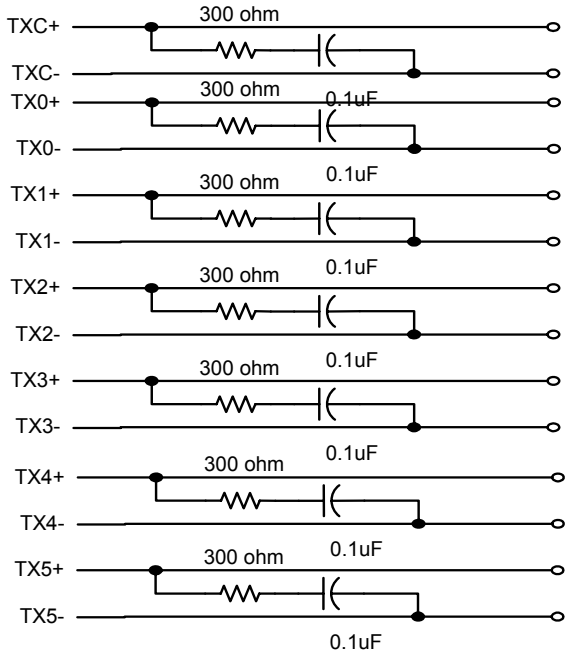


Figure 23. Differential Output Source Terminations

Source termination suppresses signal reflection to prevent non-DVI compliant receivers from mis-sampling the TMDS signals at high frequencies (beyond 135MHz). The impact on DVI compliant receivers is minimal. Therefore, Silicon Image recommends source termination for most applications. Note that the capacitor is required to meet DVI idle mode DC offset requirements and must not be omitted. Note also that the signal suppression requires the R_{EXT_SWING} value to be changed. Refer to recommendations on page 11. Power consumption will be slightly higher when using source termination.

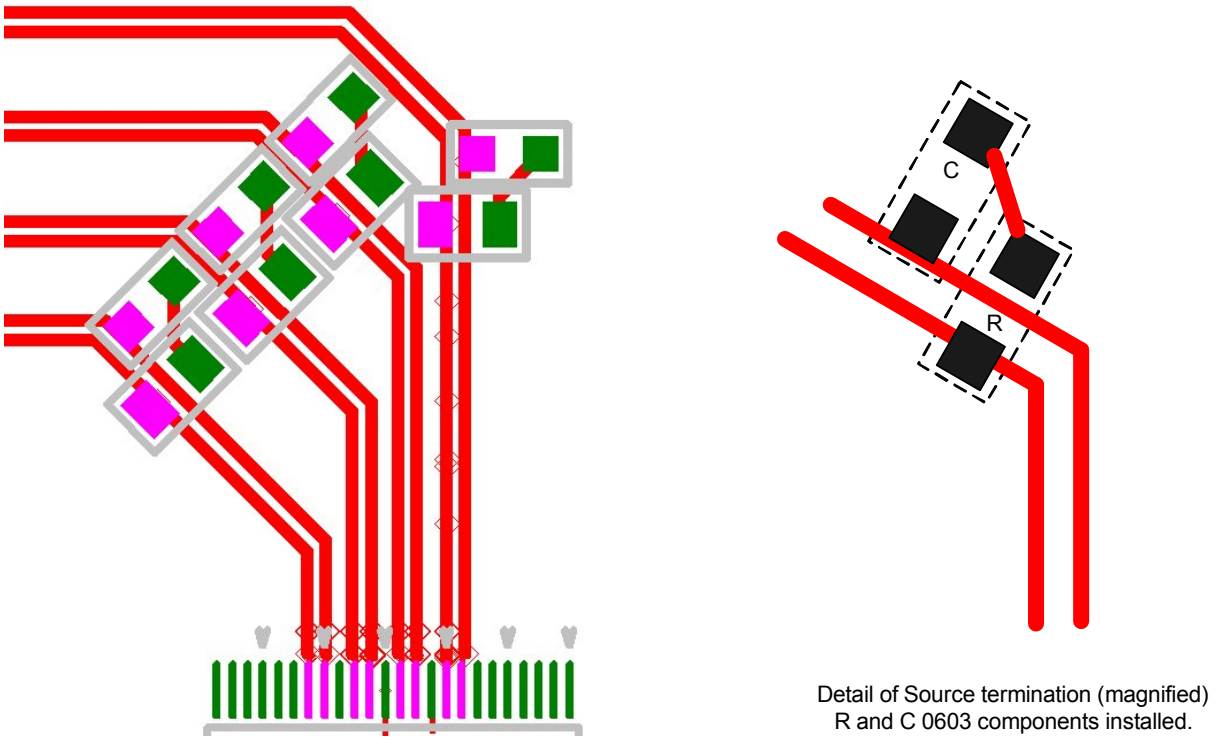


Figure 24. Source Termination Layout Illustration

The layout in Figure 24 has been developed to minimize trace stubs on the differential TMDS lines, while providing pads for the source termination components (left-hand magnified view). Source termination components should be placed close to the transmitter pins. The resistor and capacitor are shown installed on the pads provided (right-hand magnified view).

Transmitter Layout

The transmitter chip should be placed as close as possible to the output connector which carries the TMDS signals. For a system using the industry-standard DVI connector (see http://www.ddwg.org), the differential lines should be routed as directly as possible from transmitter to connector with minimal trace length difference, intra-pair length difference must be within ± 0.75 inch to minimize intra-pair skew. PanelLink devices are tolerant of skews between differential pairs, so spiral skew compensation for path length differences is not required. Each differential pair should be routed together, minimizing the number of vias through which the signal lines are routed. An example of a DVI routing is shown in Figure 25.

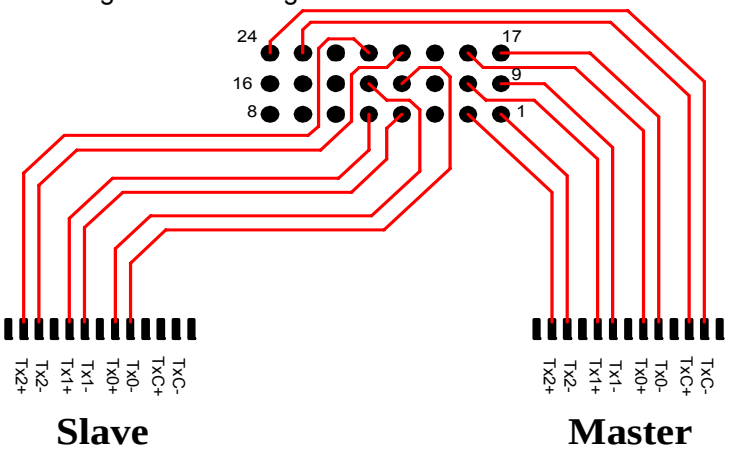


Figure 25. Transmitter to DVI Connector Layout

As defined in the DVI 1.0 Specification, the impedance of the traces between the connector and the transmitter should be 100Ω differentially, and close to 50Ω single-ended. The 100Ω requirement is to best match the differential impedance of the cable and connectors therefore preventing reflections. The common mode currents are very small on the TMDS interface, so differential impedance is more important than single-ended.

Table 9 lists the pin mapping required on the DVI connector for Master and Slave SiI 1178 Tx.

Table 9. DVI Connector to SiI 1178 Tx for Dual Link Pin Connection

DVI Connector		SiI 1178 Tx - Master		SiI 1178 Tx - Slave	
Pin #	**Signal Assignment**	**Pin #**	**Pin Name**	**Pin #**	**Pin Name**
1	TMDS Data2-	30	TMDS Low Voltage Signal Tx2- from Master		
2	TMDS Data2+	31	TMDS Low Voltage Signal Tx2+ from Master		
3	TMDS Data2/4 Shield				
4	TMDS Data4-			27	TMDS Low Voltage Signal Tx1- from Slave
5	TMDS Data4+			28	TMDS Low Voltage Signal Tx1+ from Slave
6	DDC Clock				
7	DDC Data				
8	Analog VSYNC				
9	TMDS Data1-	27	TMDS Low Voltage Signal Tx1- from Master		
10	TMDS Data1+	28	TMDS Low Voltage Signal Tx1+ from Master		
11	TMDS Data1/3 Shield				
12	TMDS Data3-			24	TMDS Low Voltage Signal Tx0- from Slave
13	TMDS Data3+			25	TMDS Low Voltage Signal Tx0+ from Slave
14	+5V Power				
15	Ground				
16	Hot Plug Detect				
17	TMDS Data0-	24	TMDS Low Voltage Signal Tx0- from Master		
18	TMDS Data0+	25	TMDS Low Voltage Signal Tx0+ from Master		
19	TMDS Data0/5 Shield				
20	TMDS Data5-			30	TMDS Low Voltage Signal Tx2- from Slave
21	TMDS Data5+			31	TMDS Low Voltage Signal Tx2+ from Slave
22	TMDS Clock Shield				
23	TMDS Clock+	22	TMDS Low Voltage Signal TxC+ from Master		
24	TMDS Clock-	23	TMDS Low Voltage Signal TxC- from Master		
C1	Analog Red				
C2	Analog Green				
C3	Analog Blue				
C4	Analog HSYNC				
C5	Analog Ground				

Recommended Circuits

The Hot Plug pin on the DVI connector will supply a voltage up to 5V. A level-shifting circuit is needed to connect to the HTPLG pin on the SiI 1178 Tx, as the input pin of the device is not 5V-tolerant. The DVI Specification also makes this recommendation (Sections 2.2.9.1 and 2.2.9.2). See Figure 26.

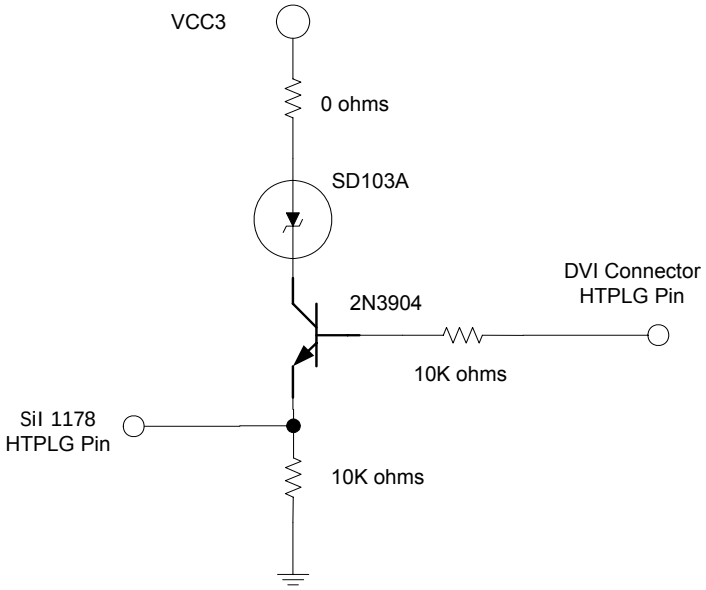
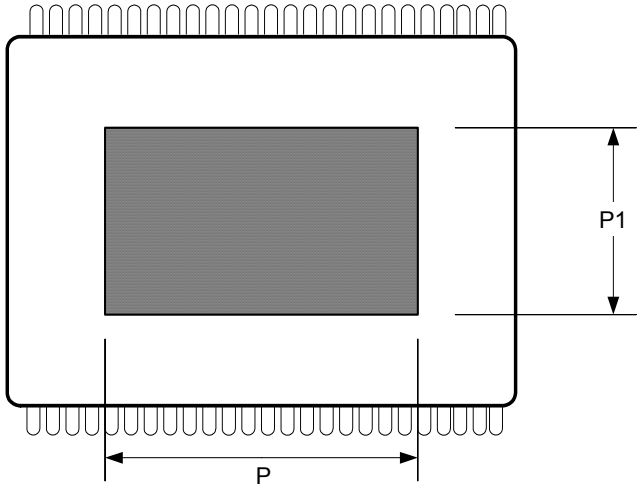


Figure 26. Recommended Hot Plug Connection

Packaging

E-pad Enhancement

The SiI 1178 Tx is packaged in a 48-pin TSSOP package with E-pad. The E-pad dimensions are shown in Figure 27.



E-pad Dimensions

		typ	max
P1	E-pad Height		2.3
P	E-pad Width		5.5

All dimensions are in millimeters.

E-pad is centered on the package center lines.

Figure 27. E-pad Diagram

The E-pad is designed to allow better heat dissipation, and must be soldered down for adequate heat dissipation for all operating frequencies and environments.

Determining Heat Dissipation Requirements

Generally, the thermal performance of a package can be represented by the following parameter (JEDEC standard JESD 51-2, 51-6):

θ_{JA} , Thermal resistance from junction to ambient

$$\theta_{JA} = (T_J - T_A) / P_H$$

Where: T_J is the junction temperature
T_A is the ambient temperature
P_H is the power dissipation

θ_{JA} represents the resistance to the heat flow from the chip to ambient air. It is an index of heat dissipation capability. Lower θ_{JA} means better thermal performance.

Implementation of the thermal landing area, combined with complete soldering of the package to the landing area, results in a θ_{JA} of 36°C/W for a multi-layer PCB (4 or more layers). If the SiI 1178 package is assembled to a two-layer PCB without the thermal landing area, the θ_{JA} increases to 109°C/W; if instead it is assembled to a multi-layer PCB without the thermal landing area, θ_{JA} is only 100°C/W due to the slightly improved ability of the multi-layer PCB to carry away heat.

Table 10 illustrates the power dissipation allowed under different PCB and E-Pad soldered states of SiI 1178.

Table 10. Allowed Power Consumption vs. E-Pad Solder State

	E-Pad not soldered to multi-layer PCB	E-Pad not soldered to 2 layer PCB	E-Pad soldered down to multi-layer PCB	E-Pad soldered down to 2 layer PCB
θ_{JA}	100°C/W	109°C/W	36°C/W	63°C/W
Allowed P_H	0.55W	0.50W	1.53W	0.87W
Max P_H	0.61W	0.61W	0.61W	0.61W

Notes:
1. All calculations based on T_J of 125ºC and T_A of 70ºC.
2. Max P_H is based on peak current consumption listed on page 5 and 3.6V at speed of 165MHz.

- In the case of no thermal landing pad on a two-layer PCB (θ_{JA} = 109°C/W), assuming a worst-case scenario with operation at the maximum ambient temperature (70°C) and maximum voltage of 3.6V, the maximum allowable peak power dissipation is 0.50W at 1.65MHz. This configuration does not allow any headroom for SiI 1178 typical power consumption of 0.50W.
- In the same non-soldered case but on a multi-layer PCB (θ_{JA} = 100°C/W), the maximum allowable peak power dissipation is 0.55W. This configuration is also not recommended since the 0.61W peak power consumption of the SiI 1178 exceeds the allowed power dissipation.
- In both 2 layer and Multi-layer soldered states, each allow a power dissipation of 0.87W and 1.53W respectively. This provides sufficient headroom for operation during sustained typical power dissipation of 0.50W or peak power dissipation of 0.61W by SiI 1178.

All PCBs must be designed with a thermal landing area for use with the SiI 1178 E-pad. Operating outside of chip specifications is not recommended; contact your Silicon Image representative for analysis of non-standard operational requirements.

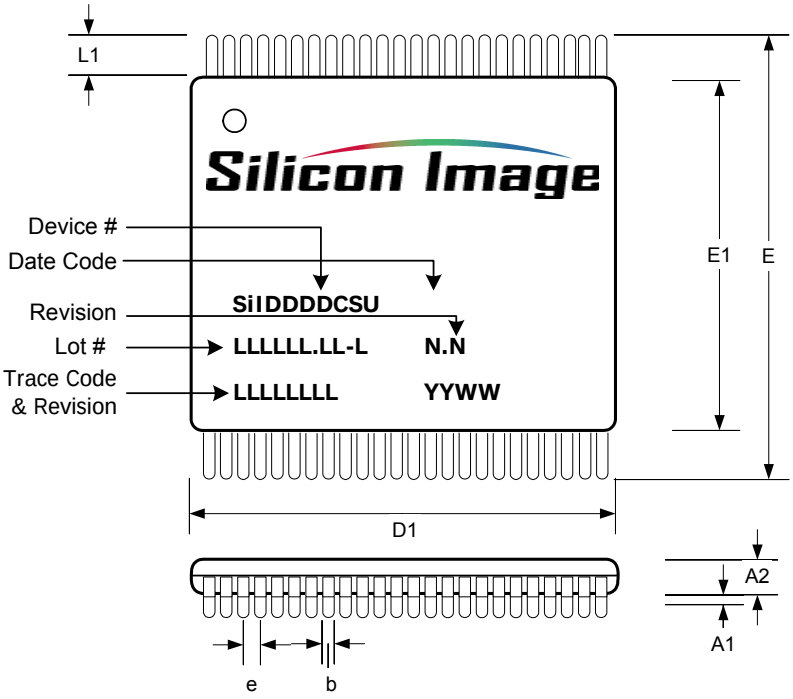
Designing with E-pad Landing Area

When designing the PCB to solder down the E-pad, keep the following in mind.

- The ground connections from die to lead-frame are down-bonded to the E-pad to minimize ground inductance. Therefore, the E-pad must **not** be electrically connected to any other voltage level except ground (GND).
- When providing a thermal landing area for soldering the E-pad, design the PCB with a clearance of at least 0.25mm between the edge of the E-pad and the inner edges of the lead pads to avoid any electrical shorts.
- The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias can double as ground connections, attaching internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package.
- For optimum thermal performance, it is recommended that the via diameter be 12 to 13 mils (0.30 to 0.33mm) and the via barrel be plated with 1 ounce copper to plug the via. This is desirable to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be ‘tented’ with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1mm) larger than the via diameter.
- Package stand-off is also a consideration. For a nominal stand-off of 0.1mm (see Figure 28, dimension ‘A1’), the stencil thickness of 5 to 8 mils should provide a good solder joint between the E-pad and the thermal land. The aperture opening should be subdivided into an array of smaller openings.

48-pin TSSOP Package

48-pin TSSOP Package Dimensions and Marking Specification



JEDEC Package Code MO-153

		typ	max
A	Thickness		1.10
A1	Stand-off		0.15
A2	Body Thickness		0.95
D1	Body Size	9.70	9.80
E1	Body Size	4.40	4.50
E	Footprint		6.40
L1	Lead Length		0.95
b	Lead Width		0.23
c	Lead Thickness		0.20
e	Lead Pitch	0.40	

Dimensions in millimeters.

Overall thickness A=A1+A2.

Lead length L1 = (E-E1)/2.

	Device Number SiIDDDD
Production	SiI1178CSU
Legend	**Description**
DDDD	Part Number
LNNNNN.LLL	Lot Number
YY	Year of Mfr
WW	Week of Mfr
N.N	Revision Number
LLLLLLL	Country of Packaging

Figure 28. Package Diagram

Ordering Information

Production Part Number: SiI1178CSU

Silicon Image, Inc.
1060 E. Arques Avenue
Sunnyvale, CA 94085
USA

Tel: (408) 616-4000
Fax: (408) 830-9530
E-mail: salessupport@siimage.com
Web: www.siliconimage.com