

# DG408/409

## 8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers



### FEATURES

- Low  $r_{DS(ON)}$  (100  $\Omega$  max)
- low Charge Injection (Q < 20 pC typ.)
- Fast Transition Time (250 ns max)
- Low Power ( $I_{SUPPLY}$  < 75  $\mu$ A)
- Single Supply Capability

### BENEFITS

- Reduced Switching Errors
- Reduced Glitching
- Improved Data Throughput
- Reduced Power Consumption
- Increased Ruggedness

### APPLICATIONS

- Data Acquisition Systems
- Audio Signal Routing and Multiplexing/Demultiplexing
- ATE Systems
- Battery Operated Systems
- High Rel Systems
- Single Supply Systems

### DESCRIPTION

The DG408 is an 8-channel single-ended analog multiplexer designed to connect 1 of 8 inputs to a common output as determined by a 3-bit binary address ( $A_0$ ,  $A_1$ ,  $A_2$ ). The DG409 is a 4-channel differential analog multiplexer designed to connect 1 of 4 differential inputs to a common dual output as determined by its 2-bit binary address ( $A_0$ ,  $A_1$ ). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An ON channel conducts current equally well in both directions. In the OFF state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches OFF for stacking several devices. All control inputs, address ( $A_x$ ) and enable (EN) are TTL compatible over the full specified operating temperature range.

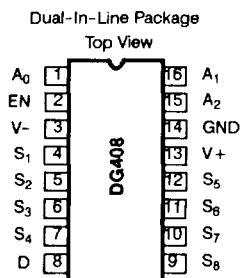
Applications for the DG408/409 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 volts. Additionally, single supply operation is also allowed. An epitaxial layer prevents latchup.

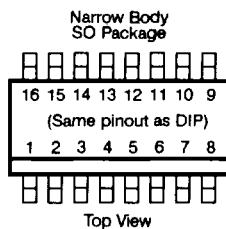
Both DG408 and DG409 are available in dual-in-line ceramic and plastic packages with small outline for surface mount applications, and are specified for operation over the military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

For additional information please see App Note AN89-1 and Technical Article TA89-2.

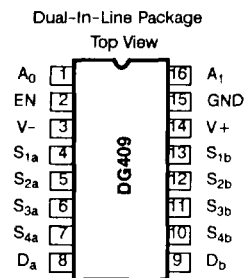
### PIN CONFIGURATION



Order Numbers:  
CerDIP: DG408AK  
DG408AK/883  
Plastic: DG408DJ

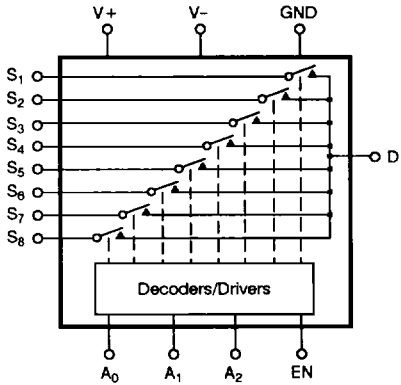


Order Number:  
DG408DY  
DG409DY

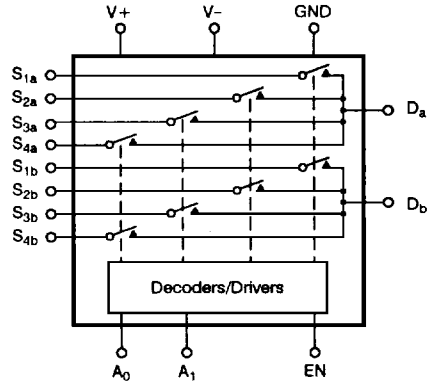


Order Numbers:  
CerDIP: DG409AK  
DG409AK/883  
Plastic: DG409DJ

## FUNCTIONAL BLOCK DIAGRAM



**DG408**  
8-Channel Single Ended Multiplexer



**DG409**  
Differential 4-Channel Multiplexer

## ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-	
V+	44 V
GND	25 V
Digital Inputs <sup>h</sup> , V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first.
Current (Any Terminal, Except S or D)	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	40 mA
Operating Temperature (A Suffix)	-55 to 125°C
(D Suffix)	-40 to 85°C

Storage Temperature (A Suffix)	-65 to 150°C
(D Suffix)	-65 to 125°C

Power Dissipation (Package)*	
16-Pin Ceramic DIP**	900 mW
16-Pin Plastic DIP***	450 mW
16-Pin Narrow Body SO****	600 mW

\*All leads soldered or welded to PC board.

\*\*Derate 12 mW/°C above 75°C.

\*\*\*Derate 6 mW/°C above 75°C.

\*\*\*\*Derate 7.6 mW/°C above 75°C.

## SPECIFICATIONS<sup>a</sup>

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V V <sub>AL</sub> = 0.8 V, V <sub>AH</sub> = 2.4 V			A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT	
			TEMP <sup>l</sup>	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>ANALOG SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V	
Drain-Source ON-Resistance <sup>e</sup>	r <sub>DS(ON)</sub>	V <sub>D</sub> = ±10 V I <sub>S</sub> = -10 mA	Room Full	40	100	125	100	125	Ω	
r <sub>DS(ON)</sub> Matching Between Channels <sup>f</sup>	Δr <sub>DS(ON)</sub>	V <sub>D</sub> = 10 V, -10 V	Room		15		15			
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>EN</sub> = 0 V	Room Full		-0.5	0.5	-0.5	0.5	nA	
Drain OFF Leakage Current	DG408		V <sub>S</sub> = ±10 V V <sub>D</sub> = ∓10 V	Room Full		-1	1	-1		1
	DG409		V <sub>S</sub> = ∓10 V V <sub>D</sub> = ±10 V	Room Full		-1	1	-1		1
Drain ON Leakage Current	DG408	V <sub>S</sub> = V <sub>D</sub> = ±10 V Sequence Each Switch ON	Room Full		-1	1	-1	1		
	DG409		Room Full		-1	1	-1	1		

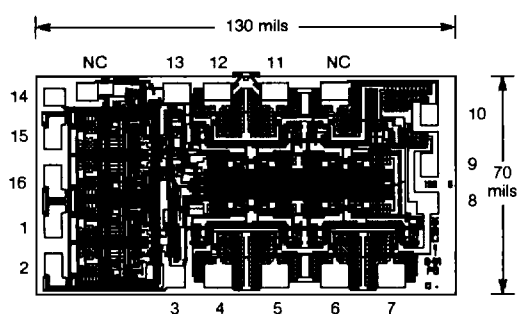
SPECIFICATIONS*										
PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified			A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT	
		V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V V <sub>AL</sub> = 0.8 V, V <sub>AH</sub> = 2.4 V	TEMP <sup>1</sup>	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>c</sup>		
<b>DIGITAL CONTROL</b>										
Logic Input Current Input Voltage High	I <sub>AH</sub>	V <sub>A</sub> = 2.4 V, 15 V	Full		-10	10	-10	10	μA	
Logic Input Current Input Voltage Low	I <sub>AL</sub>	V <sub>EN</sub> = 0 V, 2.4 V, V <sub>A</sub> = 0 V	Full		-10	10	-10	10		
<b>DYNAMIC CHARACTERISTICS</b>										
Transition Time	t <sub>TRANS</sub>	See Figure 1	Full	160		250		250	ns	
Break-Before-Make Interval	t <sub>OPEN</sub>	See Figure 3	Room		10		10			
Enable Turn-ON Time	t <sub>ON(EN)</sub>	See Figure 2	Room Full	115		150 225		150		
Enable Turn-OFF Time	t <sub>OFF(EN)</sub>		Full	105		150		150		
Charge Injection	Q <sub>i</sub>	C <sub>L</sub> = 10 nF, V <sub>S</sub> = 0 V	Room	20					pC	
OFF Isolation <sup>g</sup>		V <sub>EN</sub> = 0 V, R <sub>L</sub> = 1 kΩ f = 100 kHz	Room	-75					dB	
Logic Input Capacitance	C <sub>in</sub>	f = 1 MHz	Room	8						
Source OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V	Room	11						
Drain OFF Capacitance	DG408	C <sub>D(OFF)</sub>	V <sub>EN</sub> = 0 V f = 1 MHz	V <sub>D</sub> = 0 V	Room	40			pF	
	DG409				Room	20				
Drain ON Capacitance	DG408	C <sub>D(ON)</sub>	V <sub>EN</sub> = 0 V f = 1 MHz	V <sub>D</sub> = 0 V	Room	54				
	DG409				Room	34				
<b>POWER SUPPLIES</b>										
Positive Supply Current	I <sub>+</sub>	V <sub>EN</sub> = 0 V, V <sub>A</sub> = 0 V	Full			75		75	μA	
Negative Supply Current	I <sub>-</sub>		Full		-75		-75			
Positive Supply Current	I <sub>+</sub>	V <sub>EN</sub> = 2.4 V, V <sub>A</sub> = 0 V	Room Full			0.5 2		0.5 2	mA	
Negative Supply Current	I <sub>-</sub>		Full		-500		-500			

SPECIFICATIONS <sup>a</sup>						(Single Supply)			
PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified  V <sub>+</sub> = 12 V, V <sub>-</sub> = 0 V V <sub>AL</sub> = 0.8 V, V <sub>AH</sub> = 2.4 V	TEMP <sup>i</sup>	TYP <sup>d</sup>	A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT
					MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>ANALOG SWITCH</b>									
Drain-Source ON Resistance <sup>e</sup>	r <sub>DS(ON)</sub>	V <sub>D</sub> = 3 V, I <sub>S</sub> = -1 mA	Room	90					Ω
<b>DYNAMIC CHARACTERISTICS</b>									
Switching Time of Multiplexer	t <sub>TRANS</sub>	V <sub>S1</sub> = 8 V, V <sub>S8</sub> = 0 V V <sub>IN</sub> = 2.4 V	Room	180					ns
Enable Turn ON Time	t <sub>ON(EN)</sub>	V <sub>INH</sub> = 2.4 V, V <sub>INL</sub> = 0 V	Room	180					
Enable Turn OFF Time	t <sub>ON(EN)</sub>	V <sub>S1</sub> = 5 V	Room	120					
Charge Injection	Q	C <sub>L</sub> = 10 nF V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω	Room	5					pC

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Sequence each switch ON.
- f. Δr<sub>DS(ON)</sub> = r<sub>DS(ON)</sub> MAX - r<sub>DS(ON)</sub> MIN
- g. Worst case isolation occurs on channel 4 due to proximity to the drain pin.
- h. Signals on S<sub>x</sub>, D<sub>x</sub>, on I<sub>Nx</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- i. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

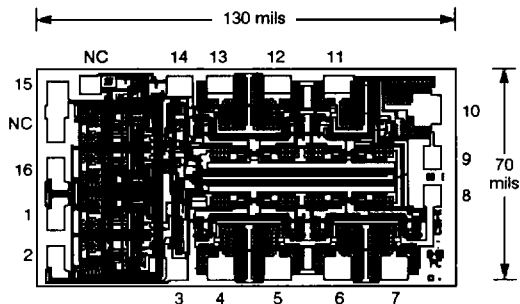
**DIE TOPOGRAPHIES**



Pad No.	Function	Pad No.	Function
1	A <sub>0</sub>	9	S <sub>5</sub>
2	EN	10	S <sub>6</sub>
3	V <sub>-</sub>	11	S <sub>7</sub>
4	S <sub>1</sub>	12	S <sub>8</sub>
5	S <sub>2</sub>	13	V <sub>+</sub> (Substrate)
6	S <sub>3</sub>	14	GND
7	S <sub>4</sub>	15	A <sub>1</sub>
8	D	16	A <sub>2</sub>

**CSHK-A DG408**

9 Diodes  
5 Resistors  
8 p-Channel Enhancement MOSFET's  
103 n-Channel Enhancement MOSFET's  
2 NPN Bipolar Transistors

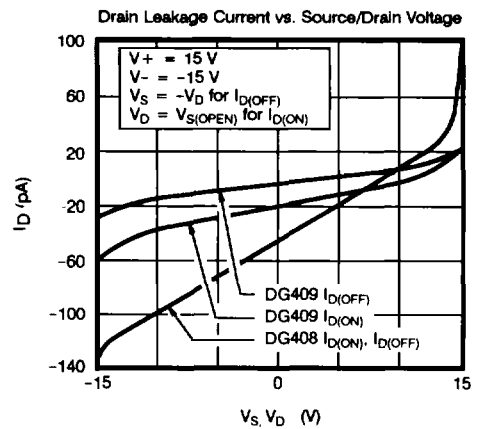
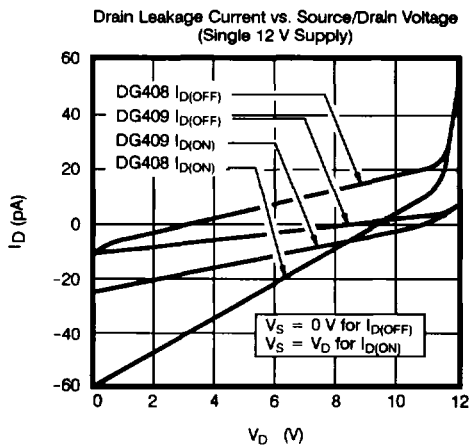
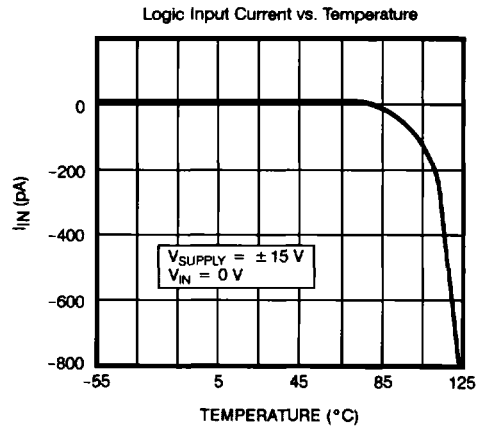
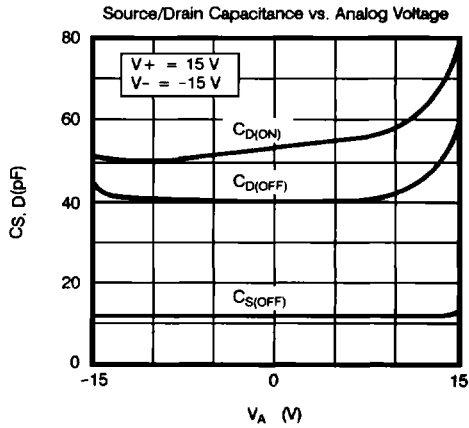
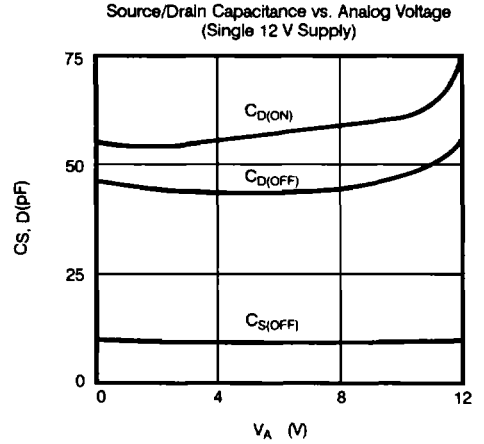
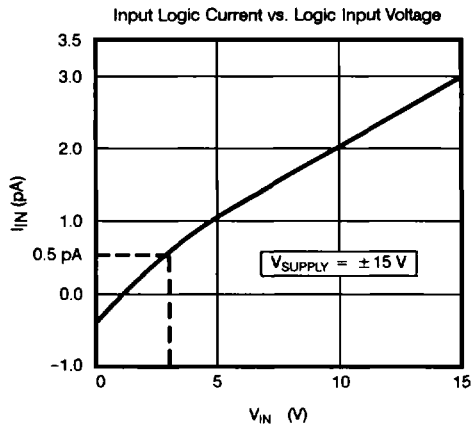


Pad No.	Function	Pad No.	Function
1	A <sub>0</sub>	9	D <sub>b</sub>
2	EN	10	S <sub>1b</sub>
3	V <sub>-</sub>	11	S <sub>2b</sub>
4	S <sub>1a</sub>	12	S <sub>3b</sub>
5	S <sub>2a</sub>	13	S <sub>4b</sub>
6	S <sub>3a</sub>	14	V <sub>+</sub> (Substrate)
7	S <sub>4a</sub>	15	GND
8	D <sub>a</sub>	16	A <sub>1</sub>

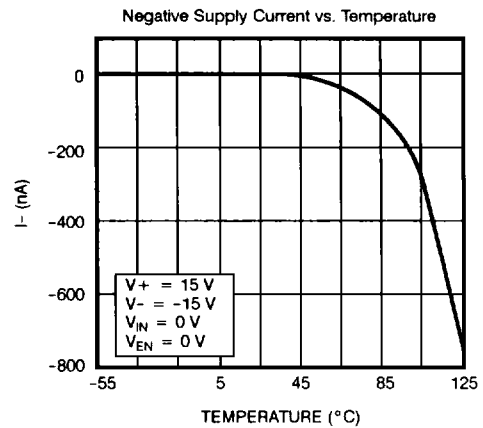
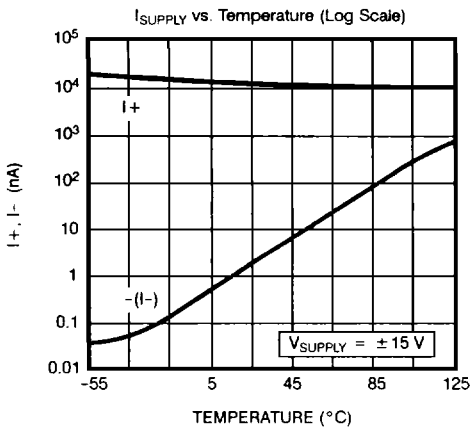
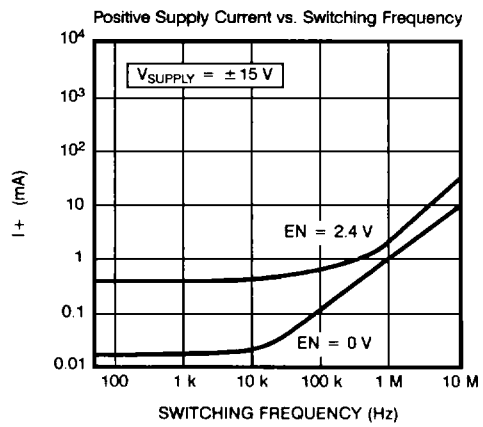
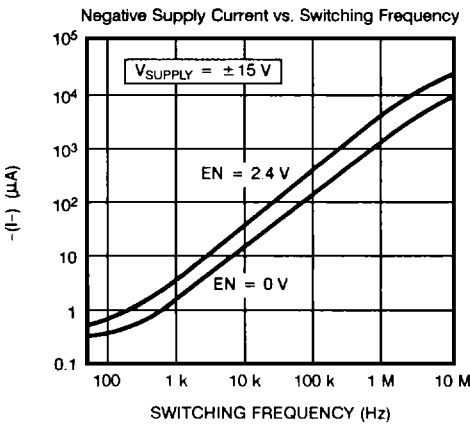
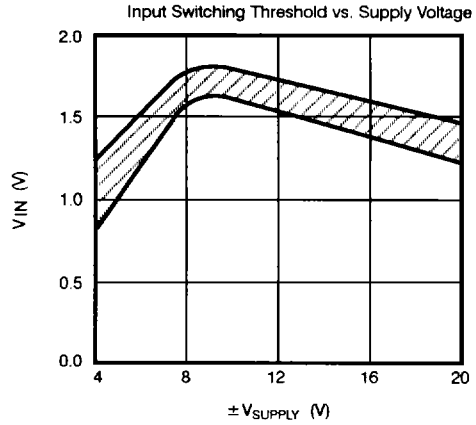
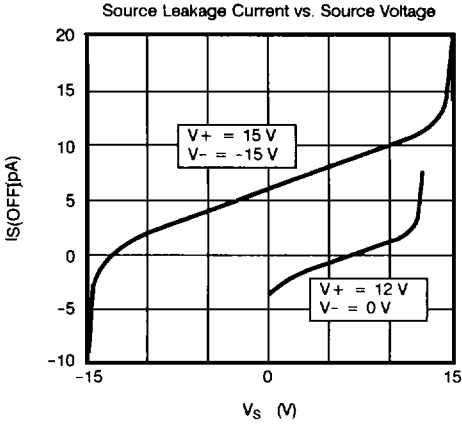
**CSHK-B DG409**

9 Diodes  
5 Resistors  
8 p-Channel Enhancement MOSFET's  
103 n-Channel Enhancement MOSFET's  
2 NPN Bipolar Transistors

## TYPICAL CHARACTERISTICS

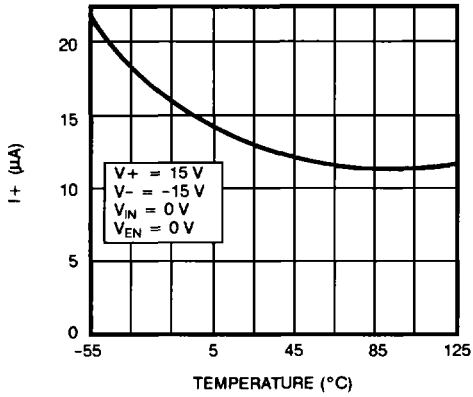


**TYPICAL CHARACTERISTICS (Cont'd)**

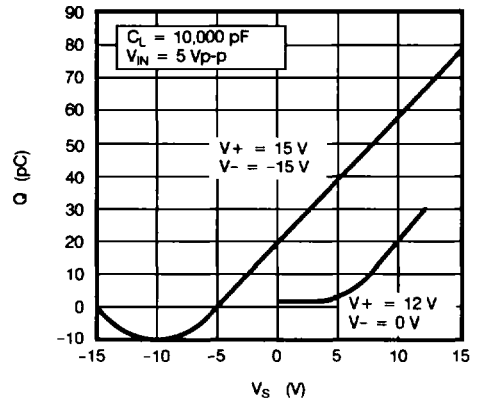


## TYPICAL CHARACTERISTICS (Cont'd)

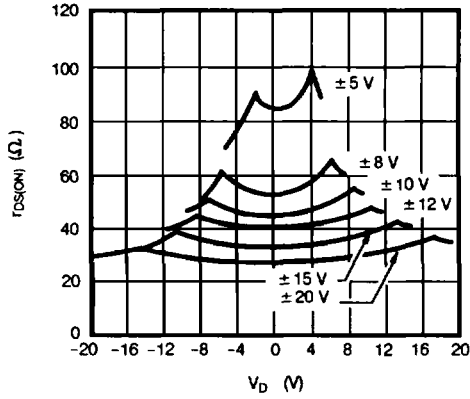
Positive Supply Current vs. Temperature  
DG408



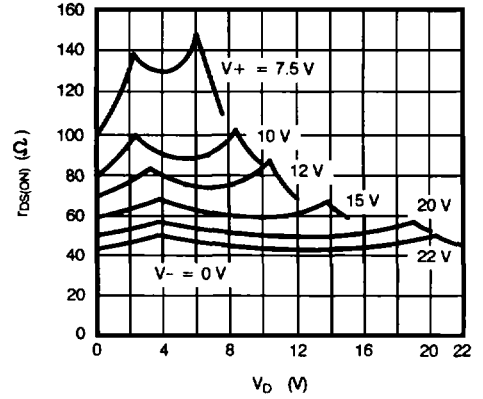
Charge Injection vs. Analog Voltage  $V_S$   
DG408/9



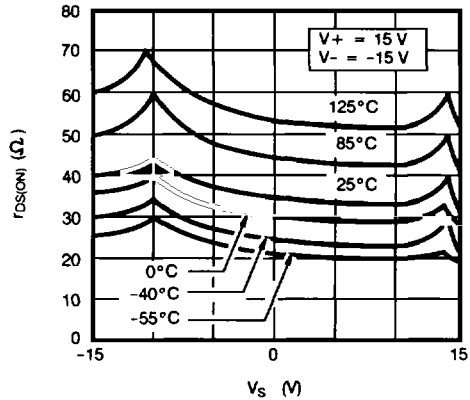
$r_{DS(ON)}$  vs.  $V_D$  and Supply



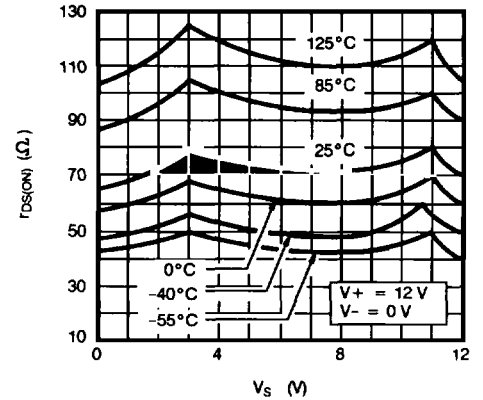
$r_{DS(ON)}$  vs.  $V_D$  (Single Supply)



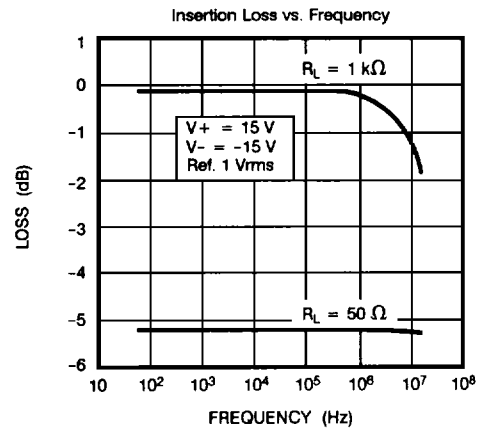
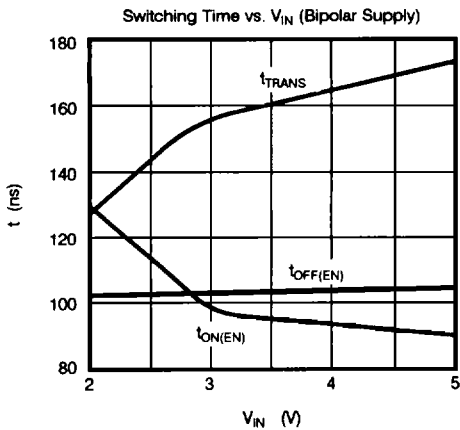
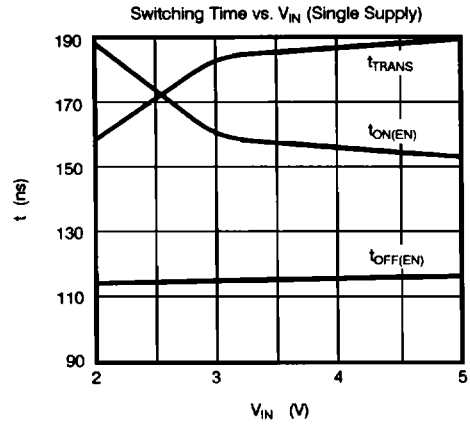
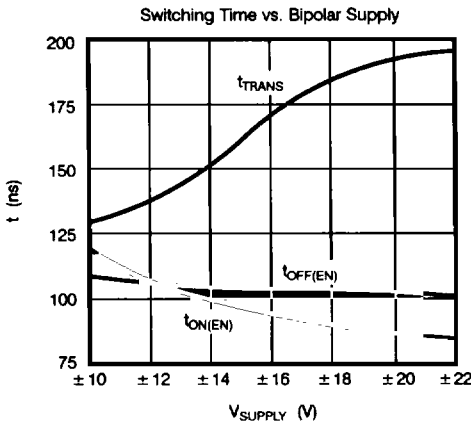
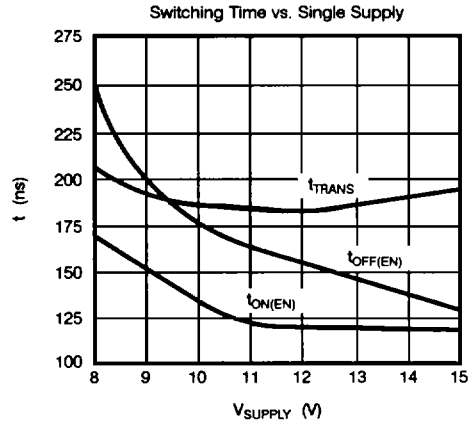
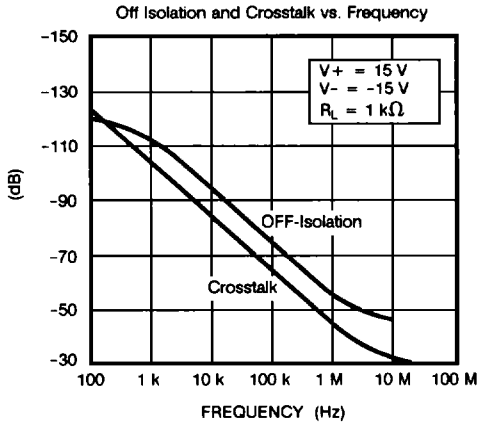
$r_{DS(ON)}$  vs.  $V_S$  and Temperature



$r_{DS(ON)}$  vs.  $V_S$  and Temperature (Single Supply)



**TYPICAL CHARACTERISTICS (Cont'd)**





## TRUTH TABLES

**DG408**

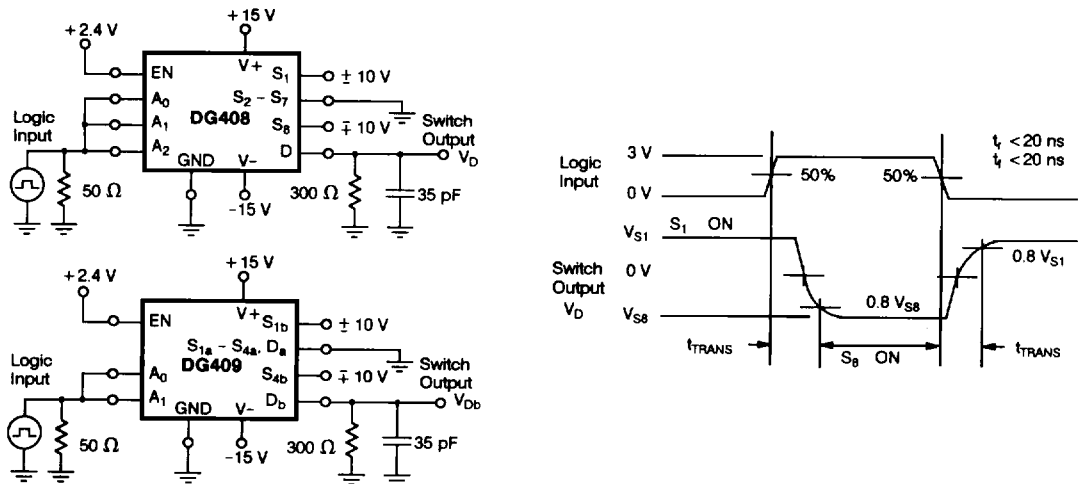
A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

**DG409**

A <sub>1</sub>	A <sub>0</sub>	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0"  $V_{AL} \leq 0.8 \text{ V}$ , Logic "1"  $V_{AH} \geq 2.4 \text{ V}$

## TEST CIRCUITS



**Figure 1.** Transition Time

TEST CIRCUITS (Cont'd)

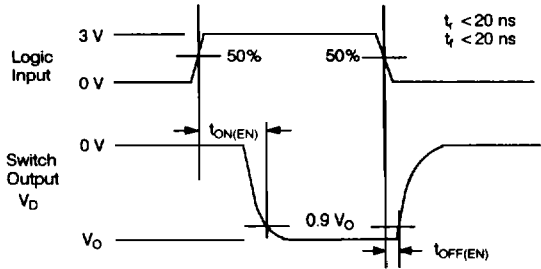
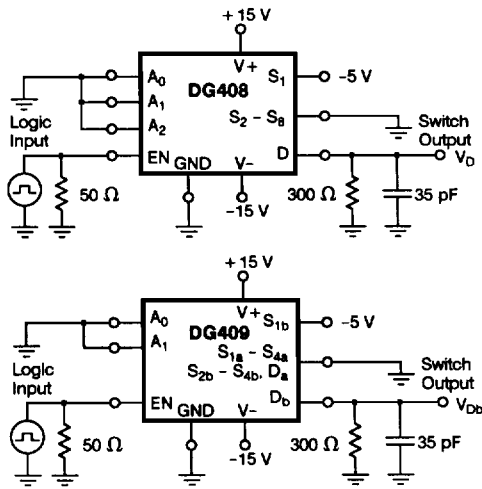


Figure 2.  $t_{ON(EN)}$ ,  $t_{OFF(EN)}$

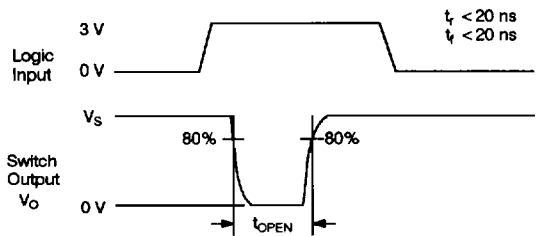
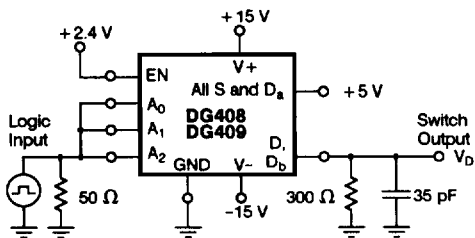
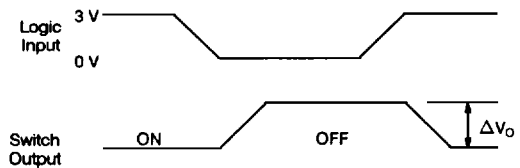
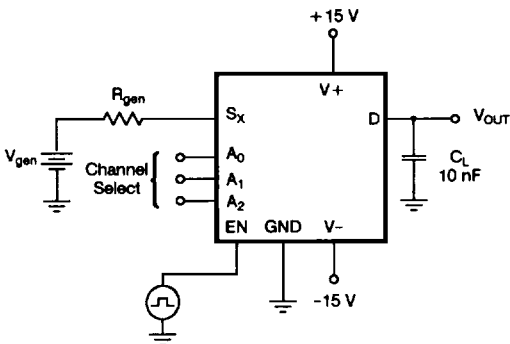


Figure 3. Break-Before-Make Interval



$\Delta V_O$  is the measured voltage due to charge transfer error,  $Q$

$$Q = C_L \times \Delta V_O$$

Figure 4. Charge Injection

## TEST CIRCUITS (Cont'd)

Frequency Tested	Signal Generator	Analyzer
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

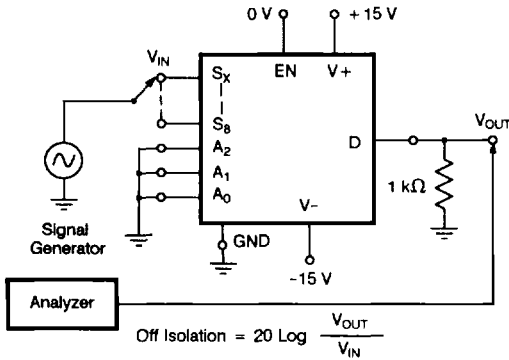


Figure 5. Off Isolation

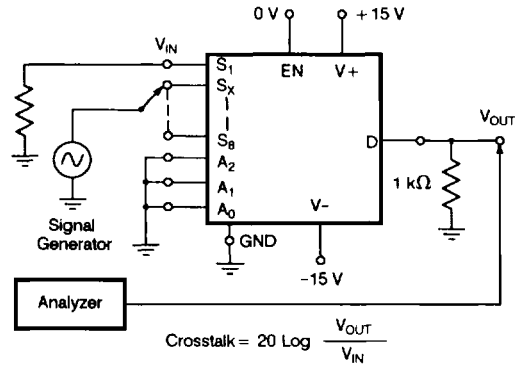


Figure 6. Crosstalk

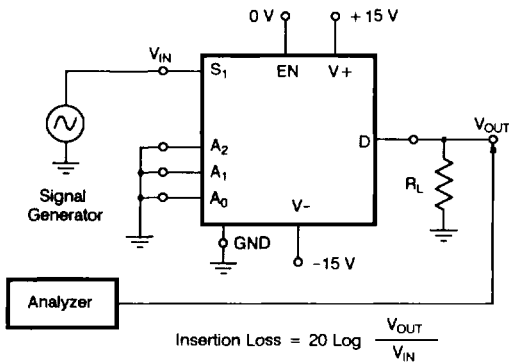


Figure 7. Insertion Loss

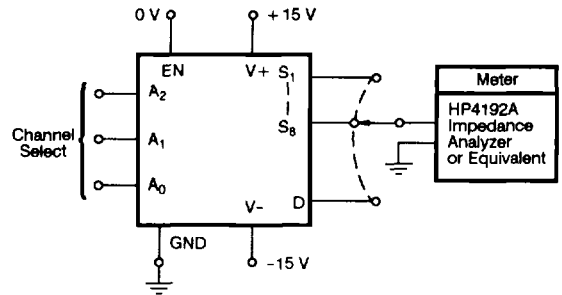


Figure 8. Source/Drain Capacitances

## APPLICATION HINTS\*

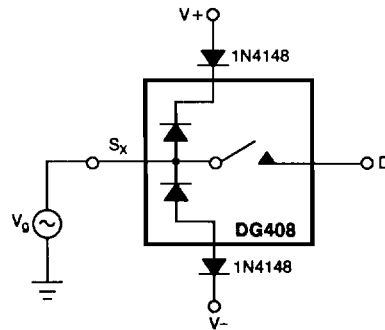
V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/V <sub>INL</sub> Max (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
15**	-15	2.4/0.8	-15 to 15
12	-12	2.4/0.8	-12 to 12
12	0	2.4/0.8	0 to 12
8	-8	2.4/0.4	-8 to 8
5	-5	2.0/0.4	-5 to 5

\* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.  
 \*\* Electrical Characteristics chart based on V+ = 15 V, V- = -15 V.

**APPLICATION HINTS (Cont'd)\***

**Overvoltage Protection**

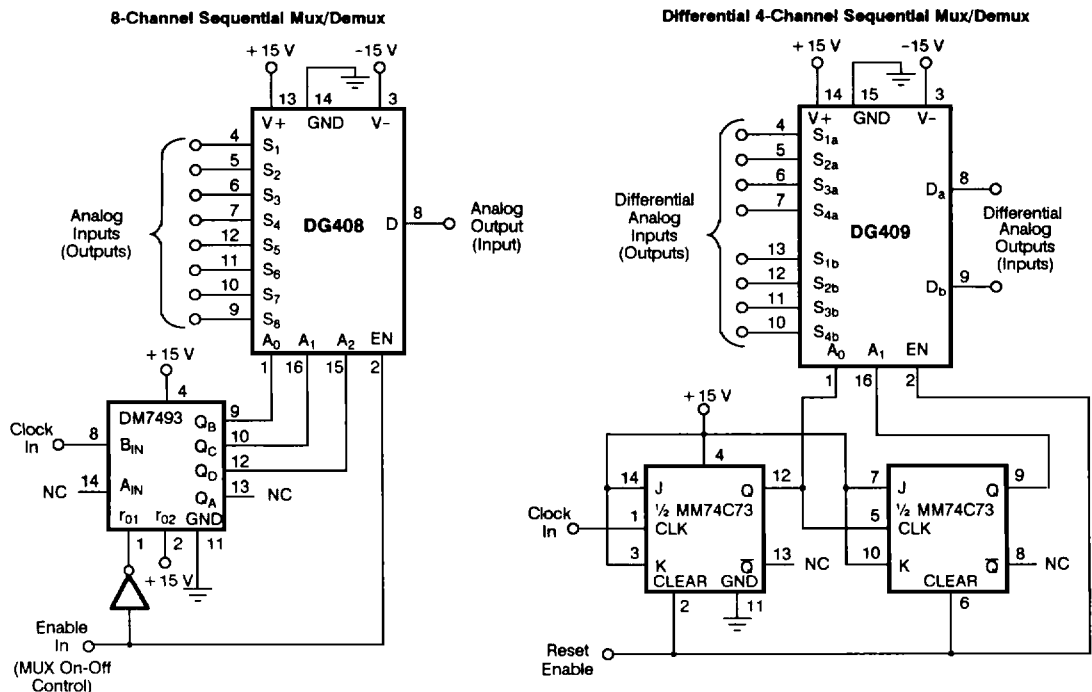
A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see figure). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal  $V+$  or  $V-$  value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference  $V_S - (V-)$  doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below  $V+$  and 1 V above  $V-$ , but it preserves the low channel resistance and low leakage characteristics.



**Figure 9.** Overvoltage Protection Using Blocking Diodes

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**APPLICATIONS**



**Figure 10.**