Low-Charge Coupling JFET Analog Switches *designed for...*

Siliconix

- **Low Error Sample and Hold Circuits**
- **100 MHz Signal Switching with High OFF Isolation**
- **Presettable Integrators with Minimum Offset Error**
- **Low Distortion Click Free Audio Switching**

BENEFITS

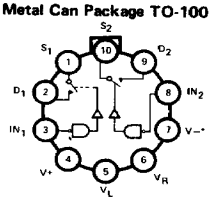
- **Minimum Signal Errors**
  - Low Charge Feedthrough 7 Picocoulombs Typical
  - Low "r_{on} x $I_{D(OFF)}$ Error Factor
  - Low Leakage Less Than 10 Picoamps Typical
  - Low Distortion — Constant ON Resistance
- **Easily Interfaced**
  - TTL and CMOS Logic Compatibility Over Full Temperature Range
- **Compact Circuit Layouts**
  - Several Form Factors Available in Single Packages (eg. 2XSPST, SPDT, 2XSPDT, 2XDPST)

DESCRIPTION

The DG281 series incorporates N-channel junction-type field-effect transistors (JFETs) designed to function as electronic switches. Level-shifting drivers enable TTL or CMOS outputs to control the ON-OFF state of each switch. The driver is designed to provide break-before-make action when switching from one channel to another. The low switch capacitance results in a minimal amount of charge-feedthrough into the analog signal path. In the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block voltages up to 22.5 V peak-to-peak.

PIN CONFIGURATIONS (Top View)

Metal Can Package TO-100

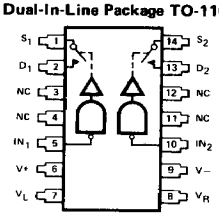


DUAL SPST

LOGIC	SW 1 & 2
0	ON
1	OFF

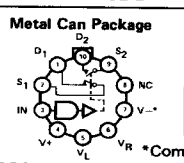
ORDER NUMBERS:
DG281AA OR DG281BA
SEE PACKAGE 2

Dual-In-Line Package TO-116



ORDER NUMBERS:
DG281AP OR DG281BP
SEE PACKAGE 11

Metal Can Package



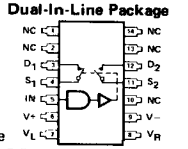
SPDT

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*Common to Substrate and Case

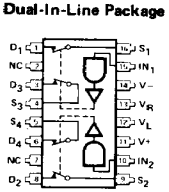
ORDER NUMBERS:
DG287AA OR DG287BA
SEE PACKAGE 2

Dual-In-Line Package



ORDER NUMBERS:
DG287AP OR DG287BP
SEE PACKAGE 11

Dual-In-Line Package



ORDER NUMBERS:
DG284AP OR DG284BP
SEE PACKAGE 12

DUAL DPST

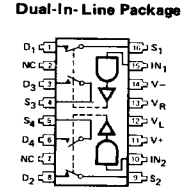
LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

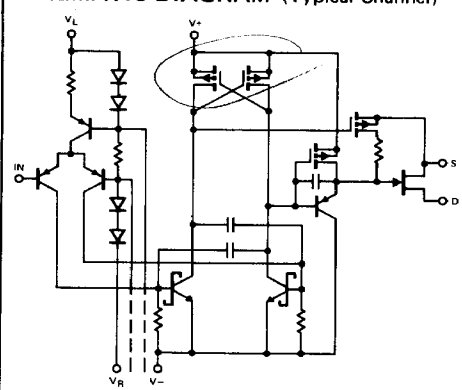
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

Dual-In-Line Package



ORDER NUMBERS:
DG290AP OR DG290BP
SEE PACKAGE 12

SCHEMATIC DIAGRAM (Typical Channel)



APPLICATION HINTS*

V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S Analog Voltage Range (V)
+15**	15	+5	Gnd	2.0/0.8	–7.5 to +15
+10	20	+5	Gnd	2.0/0.8	–12.5 to +10
+12	12	+5	Gnd	2.0/0.8	–4.5 to +12

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Parameter Chart based on V+ = +15 V, V– = –15 V, V_L = 5 V, V_R = Gnd.

ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_D	33 V
V_D to V−	33 V
V_D to V_S	±22 V
V_L to V−	36 V
V_L to V_{IN}	8 V
V_L to V_R	8 V
V_{IN} to V_R	8 V
V_R to V−	27 V
V_R to V_{IN}	8 V
Current (Any Terminal)	20 mA
Storage Temperature	−65 to +150°C
Operating Temperature (A Suffix)	−55 to +125°C
(B Suffix)	−20 to +85°C

Power Dissipation*

Metal Can**	450 mW
14 Pin DIP***	825 mW
16 Pin DIP****	900 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.
****Derate 12 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS DG281A, DG284A, DG287A, DG290A −55°C	25°C	125°C	MAX LIMITS DG281B, DG284B, DG287B, DG290B −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, V_L = 5 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance		300	500		300	500	Ω	V_D = −7.5 V	I_S = −1 mA††
2	SWITCH	$I_{S(off)}$	Source OFF Leakage Current		0.5	100		2	100	nA	V_S = 7.5 V, V_D = −7.5 V	††
3	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current		0.2	100		1	100	nA	V_D = 7.5 V, V_S = −7.5 V	
4	SWITCH	$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−200		−10	−200	nA	V_D = V_S = −7.5 V	††
5	IN	I_{INL}	Input Current, Input Voltage Low	−250	−250	−250	−250	−250	250	µA	V_{IN} = 0	
6	IN	I_{INH}	Input Current, Input Voltage High		10	20		10	20	µA	V_{IN} = 5 V	
7	DYNAMIC	t_{on}	Turn-ON Time		150			180		ns	See Switching Time Test Circuit	
8	DYNAMIC	t_{off}	Turn-OFF Time		130			150		ns	See Switching Time Test Circuit	
9	DYNAMIC	$C_{S(off)}$	Source OFF Capacitance	6 Typical*						pF	V_S = −5 V, I_D = 0	f = 1 MHz
10	DYNAMIC	$C_{D(off)}$	Drain OFF Capacitance	2 Typical*						pF	V_D = −5 V, I_S = 0	f = 1 MHz
11	DYNAMIC	$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	14-17 Typical*						pF	V_D = V_S = 0	f = 1 MHz
12	DYNAMIC	ΔQ	Charge Feedthrough	11 Typical*						pC	V_S = 7.5 V	See Charge-Feedthrough Test Circuit
13	DYNAMIC	ΔQ	Charge Feedthrough	4 Typical						pC	V_S = −7.5 V	See Charge-Feedthrough Test Circuit

POWER SUPPLY CURRENTS

		CHARACTERISTIC 25°C MAX LIMITS		DG281	DG284	DG287	DG290	UNIT	TEST CONDITIONS
14	SUPPLY	I_+	Positive Supply Current	1.5	3	0.8	1.5	mA	V_{IN} = 0†
15	SUPPLY	I_-	Negative Supply Current	−5	−5.5	−3	−5	mA	V_{IN} = 0†
16	SUPPLY	I_L	Logic Supply Current	4.5	4.5	3.2	4.5	mA	V_{IN} = 0†
17	SUPPLY	I_+	Positive Supply Current	1.5	0.1	0.8	1.5	mA	V_{IN} = 5 V†
18	SUPPLY	I_-	Negative Supply Current	5	−4	3	−5	mA	V_{IN} = 5 V†
19	SUPPLY	I_L	Logic Supply Current	4.5	4.5	3.2	4.5	mA	V_{IN} = 5 V†
20	SUPPLY	I_R	Reference Supply Current	2	2	2	−2	mA	Both V_{IN} = 5 V, V_{IN} = 0

†If driver has two channels, both are active.
*Typical values are to DESIGN AID ONLY, not guaranteed and not subject to production testing.
††Switch being tested ON or OFF as indicated. Input Logic Low 0.8 V.
Input Logic High 2V.

DG281	CMJB-NH
DG284	CMJA-NH
DG287	CMJC-NH
DG290	CMJB-NH

TRUTH TABLE

DEVICE	IN 1	SW 1	SW 3	IN 2	SW 2	SW 4
DG281	0.8 V	ON	–	0.8 V	ON	–
	2.0 V	OFF	–	2.0 V	OFF	–
DG284	0.8 V	OFF	OFF	0.8 V	OFF	OFF
	2.0 V	ON	ON	2.0 V	ON	ON
DG287	0.8 V	OFF	–	–	ON	–
	2.0 V	ON	–	–	OFF	–
DG290	0.8 V	OFF	ON	0.8 V	OFF	ON
	2.0 V	ON	OFF	2.0 V	ON	OFF

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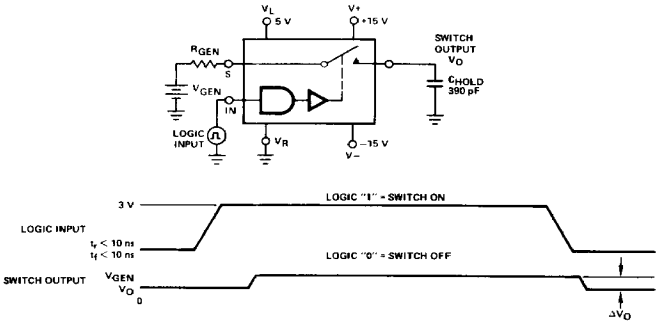
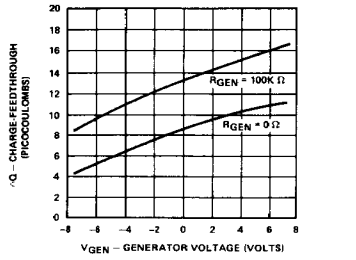
CHARGE INJECTION TEST CIRCUIT



Charge Feedthrough vs R_{GEN} and V_{GEN}

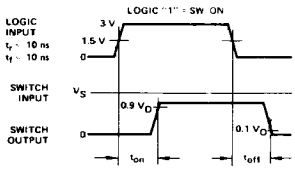


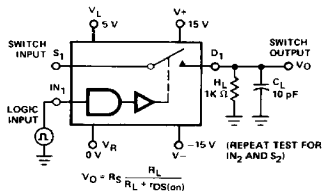
ΔV_O = ERROR VOLTAGE GENERATED ACROSS CAPACITOR

Q = CHARGE INJECTED BY SWITCH DURING TURN-OFF = $\Delta V_O \times C_{HOLD}$

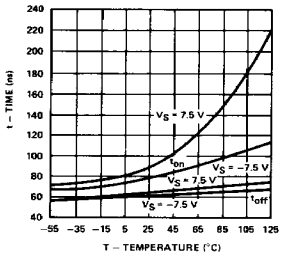
SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



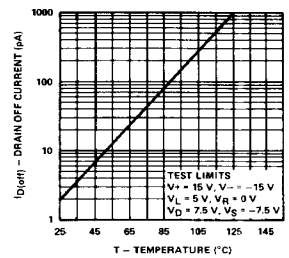


Switching Time vs V_S and Temperature

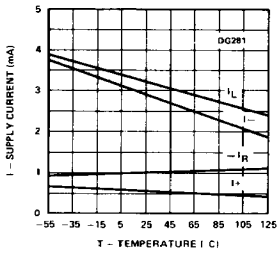


TYPICAL PERFORMANCE CURVES

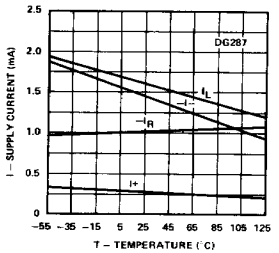
$I_{D(off)}$ vs. Temperature



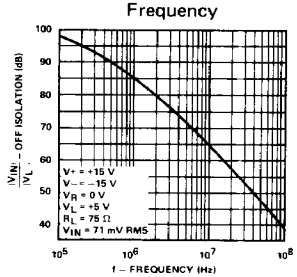
Supply Current vs Temperature



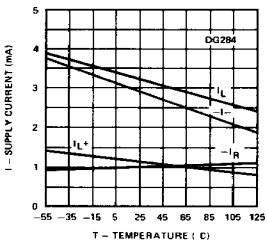
Supply Current vs Temperature



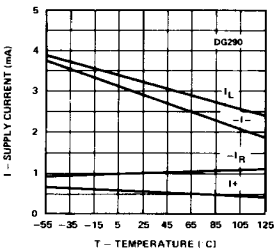
"OFF" Isolation vs Frequency

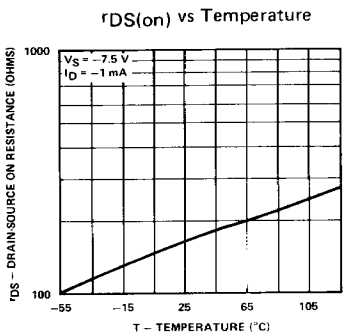


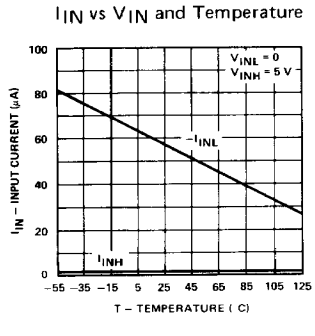
Supply Current vs Temperature

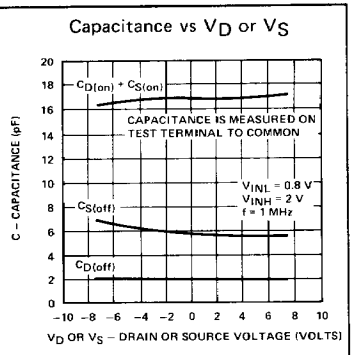


Supply Current vs Temperature

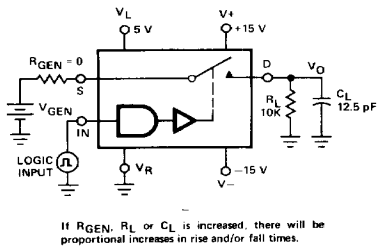






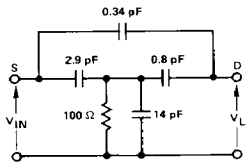


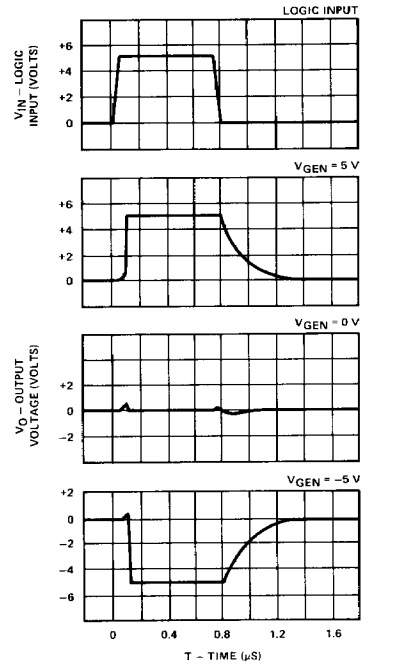
TYPICAL SWITCHING TRANSIENTS



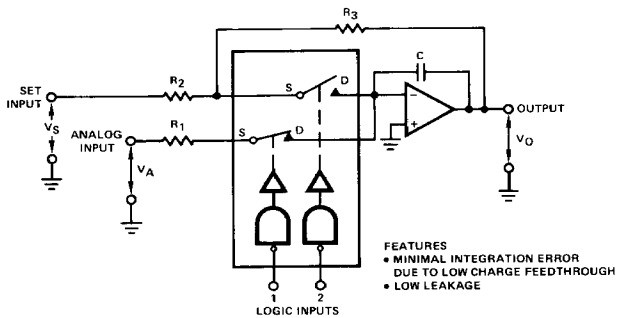
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall times.

Equivalent "OFF" Circuit



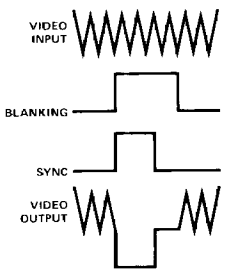


Application: THREE MODE INTEGRATOR

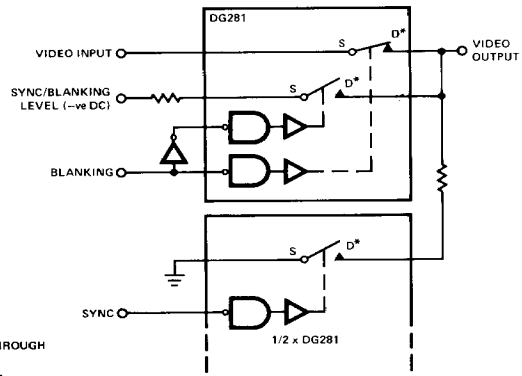


FEATURES
- MINIMAL INTEGRATION ERROR DUE TO LOW CHARGE FEEDTHROUGH
- LOW LEAKAGE

Application: VIDEO/BLANKING/SYNC. SIGNAL COMBINER



FEATURES
- MINIMAL OUTPUT SPIKES DUE TO LOW CHARGE FEEDTHROUGH
- NEGLIGIBLE FEEDTHROUGH DURING BLANKING INTERVAL



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