

## Improved Quad CMOS Analog Switches

### FEATURES

- $\pm 22$ -V Supply Voltage Rating
- TTL and CMOS Compatible Logic
- Low On-Resistance— $r_{DS(on)}$ : 50  $\Omega$
- Low Leakage— $I_{D(on)}$ : 20 pA
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching— $t_{ON}$ : 120 ns
- Low Charge Injection— $Q$ : 1 pC

### BENEFITS

- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Superior to DG211/212
- Space Savings (TSSOP)

### APPLICATIONS

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Disk Drives
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

### DESCRIPTION

The DG211B/212B analog switches are highly improved versions of the industry-standard DG211/212. These devices are fabricated in Vishay Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

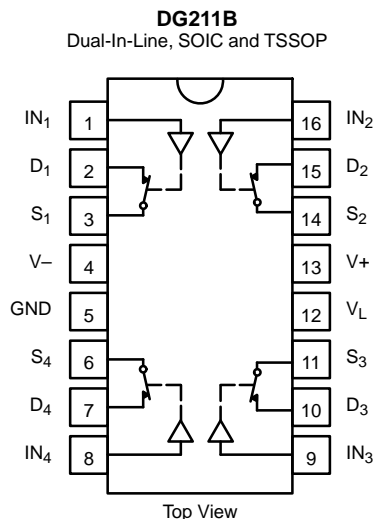
These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. The DG211B and DG212B can handle

up to  $\pm 22$  V, and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

All devices feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

The DG211B is a normally closed switch and the DG212B is a normally open switch. (See Truth Table.)

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	DG211B	DG212B
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85 °C	16-Pin Plastic DIP	DG211BDJ
		DG212BDJ
	16-Pin Narrow SOIC	DG211BDY
		DG212BDY
	16-Pin TSSOP	DG211BDQ
		DG212BDQ

### ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs<sup>a</sup> V<sub>S</sub>, V<sub>D</sub> ..... (V-) -2 V to (V+) +2 V  
or 30 mA, whichever occurs first

Current, Any Terminal ..... 30 mA

Peak Current, S or D

(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature ..... -65 to 125 °C

Power Dissipation (Package)<sup>b</sup>

16-Pin Plastic DIP<sup>c</sup> ..... 470 mW

16-Pin Narrow SOIC and TSSOP<sup>d</sup> ..... 640 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 75 °C
- Derate 7.6 mW/°C above 75 °C

### SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

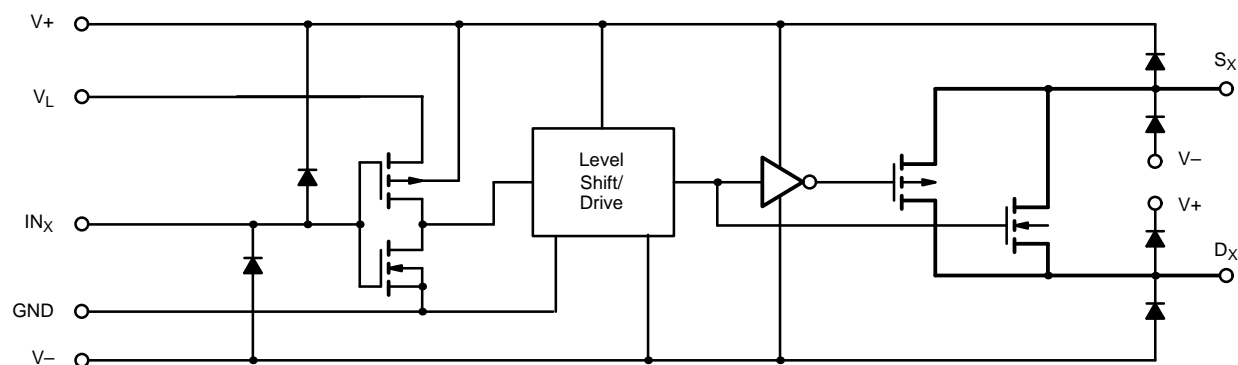


FIGURE 1.



SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_L = 5\text{ V}$ , $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^e$	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	$V_{ANALOG}$		Full	-15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = \pm 10\text{ V}$ , $I_S = 1\text{ mA}$	Room		45	85	$\Omega$
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$		Full		2	100	
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 14\text{ V}$ , $V_D = \mp 14\text{ V}$	Room	-0.5	$\pm 0.01$	0.5	nA
Drain Off Leakage Current	$I_{D(off)}$	$V_D = \pm 14\text{ V}$ , $V_S = \mp 14\text{ V}$	Full	-5	$\pm 0.01$	5	
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = \pm 14\text{ V}$	Room	-0.5	$\pm 0.02$	0.5	
			Full	-10		10	
<b>Digital Control</b>							
Input Voltage High	$V_{INH}$		Full	2.4			V
Input Voltage Low	$V_{INL}$		Full			0.8	
Input Current	$I_{INH}$ or $I_{INL}$	$V_{INH}$ or $V_{INL}$	Full	-1		1	$\mu\text{A}$
Input Capacitance	$C_{IN}$		Room		5		pF
<b>Dynamic Characteristics</b>							
Turn-On Time	$t_{ON}$	$V_S = 10\text{ V}$ See Figure 2	Room			300	ns
Turn-Off Time	$t_{OFF}$		Room			200	
Charge Injection	Q	$C_L = 1000\text{ pF}$ , $V_g = 0\text{ V}$ , $R_g = 0\ \Omega$	Room		1		pC
Source-Off Capacitance	$C_{S(off)}$	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	Room		5		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		5		
Channel On Capacitance	$C_{D(on)}$	$V_D = V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	Room		16		
Off Isolation	OIRR	$C_L = 15\text{ pF}$ , $R_L = 50\ \Omega$ $V_S = 1\text{ V}_{RMS}$ , $f = 100\text{ kHz}$	Room		90		dB
Channel-to-Channel Crosstalk	X <sub>TALK</sub>		Room		95		
<b>Power Supply</b>							
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ or }5\text{ V}$	Room			10	$\mu\text{A}$
Negative Supply Current	$I_-$		Full		-10	50	
Logic Supply Current	$I_L$	Room				10	
Power Supply Range for Continuous Operation	$V_{OP}$		Full	$\pm 4.5$		$\pm 22$	V

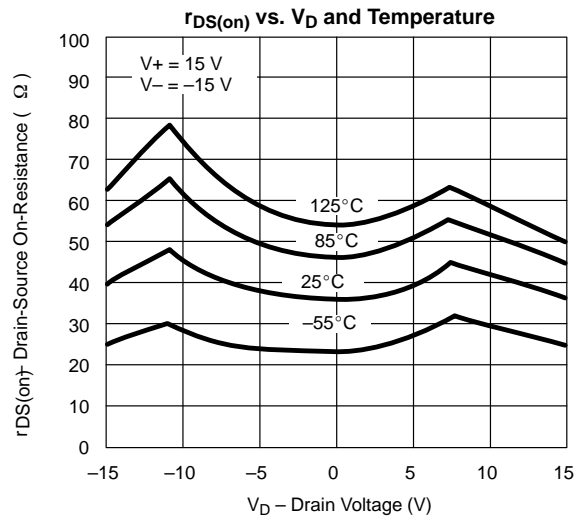
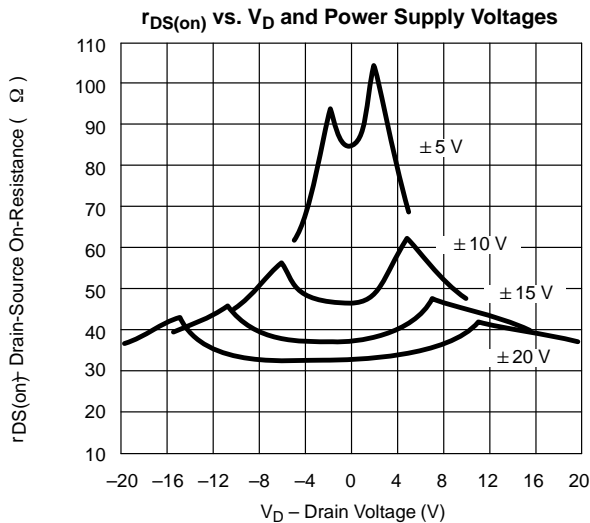


SPECIFICATIONS FOR SINGLE SUPPLY							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^e$	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	$V_{ANALOG}$		Full	0		12	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = 3\text{ V}, 8\text{ V}, I_S = 1\text{ mA}$	Room Full		90	160 200	$\Omega$
<b>Dynamic Characteristics</b>							
Turn-On Time	$t_{ON}$	$V_S = 8\text{ V}$ See Figure 2	Room			300	ns
Turn-Off Time	$t_{OFF}$		Room			200	
Charge Injection	Q	$C_L = 1\text{ nF}, V_{gen} = 6\text{ V}, R_{gen} = 0\ \Omega$	Room		4		pC
<b>Power Supply</b>							
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full			10 50	$\mu\text{A}$
Negative Supply Current	$I_-$		Room Full	-10 -50			
Logic Supply Current	$I_L$		Room Full			10 50	
Power Supply Range for Continuous Operation	$V_{OP}$		Full	+4.5		+25	V

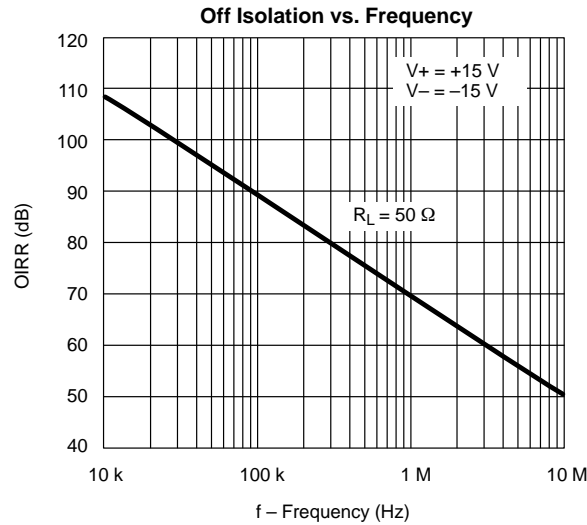
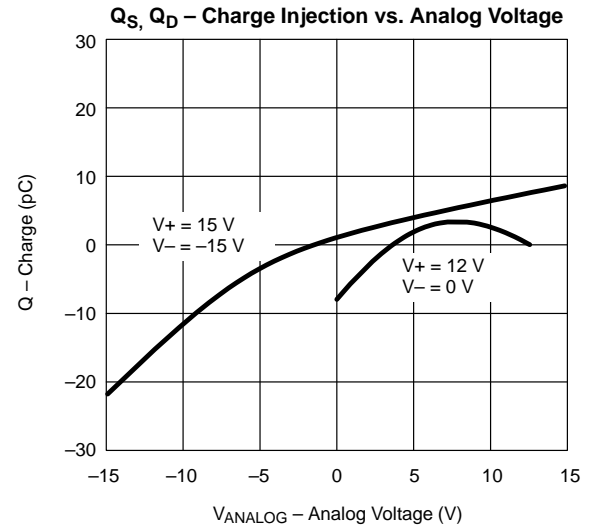
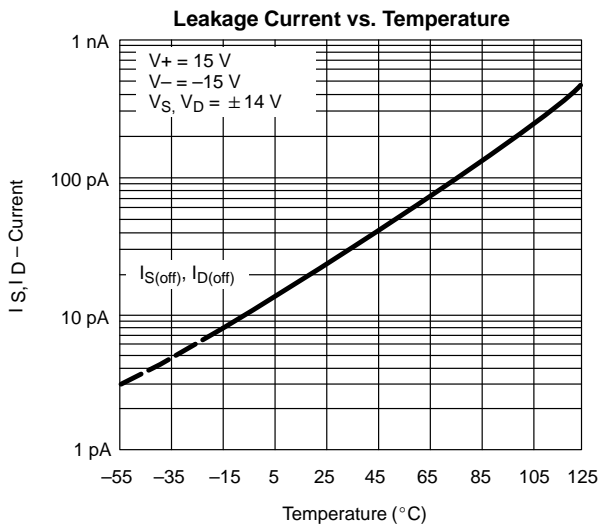
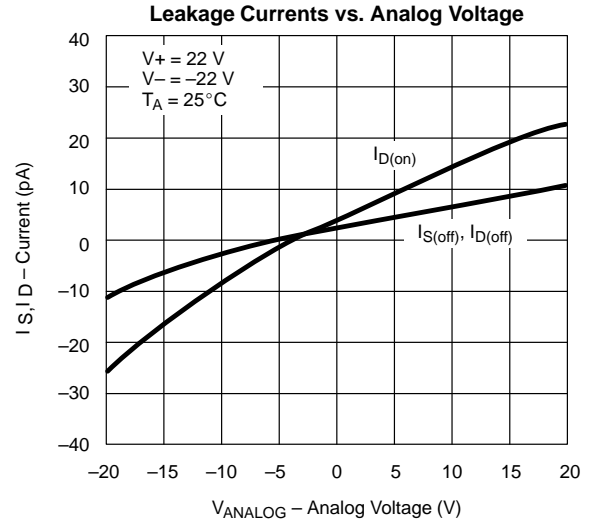
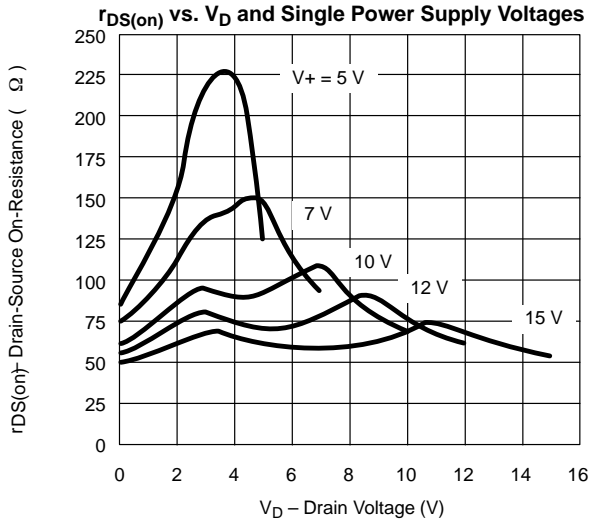
Notes:

- a. Room = 25°C, Full = as determined by the operating temperature suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. Guaranteed by design, not subject to production test.
- e.  $V_{IN}$  = input voltage to perform proper function.

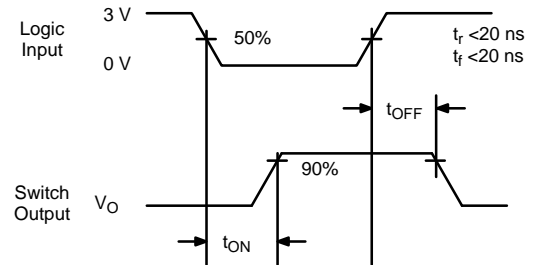
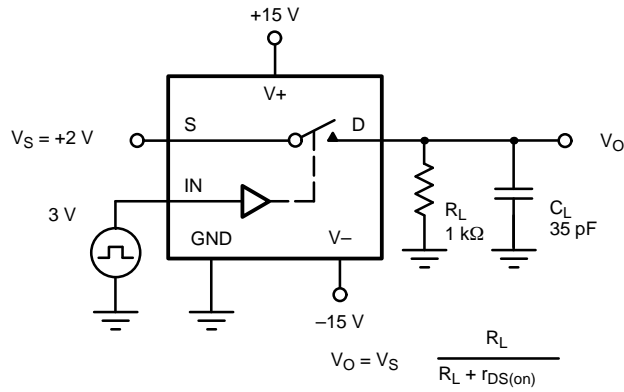
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



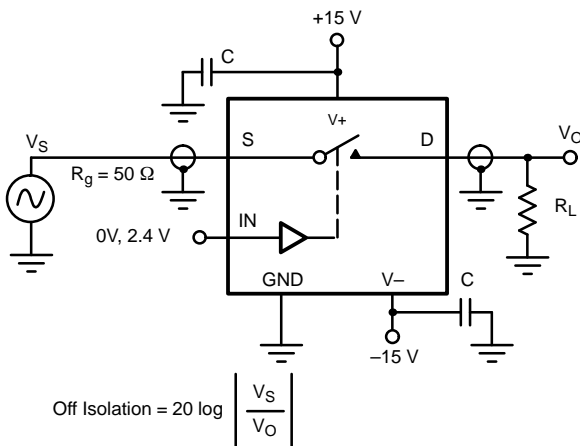
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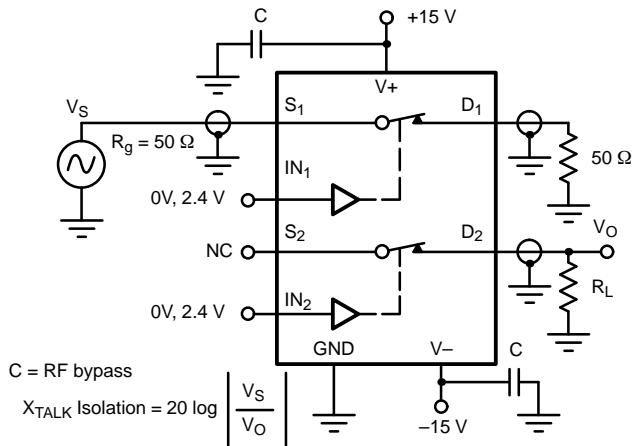
**TEST CIRCUITS**



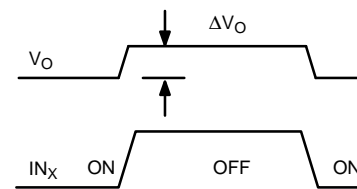
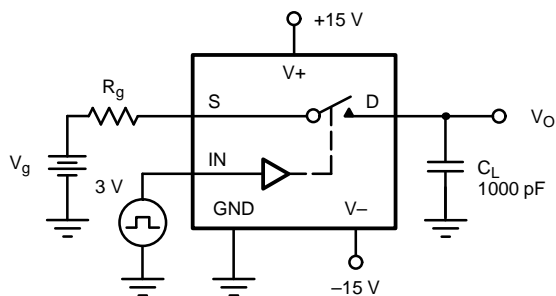
**FIGURE 2.** Switching Time



**FIGURE 3.** Off Isolation

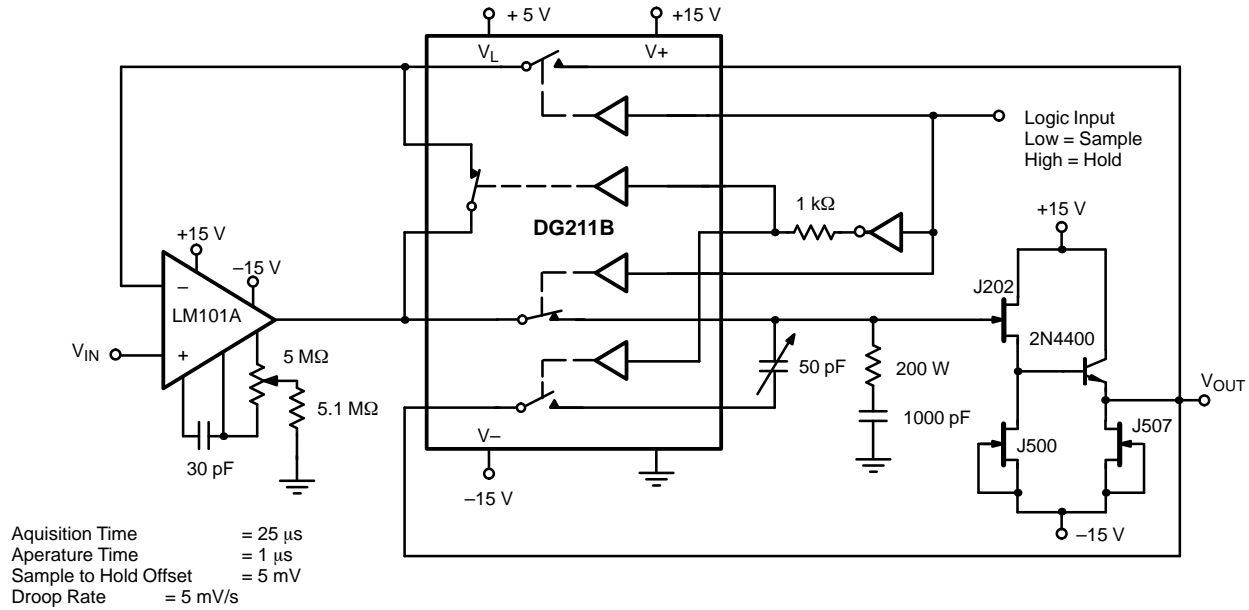
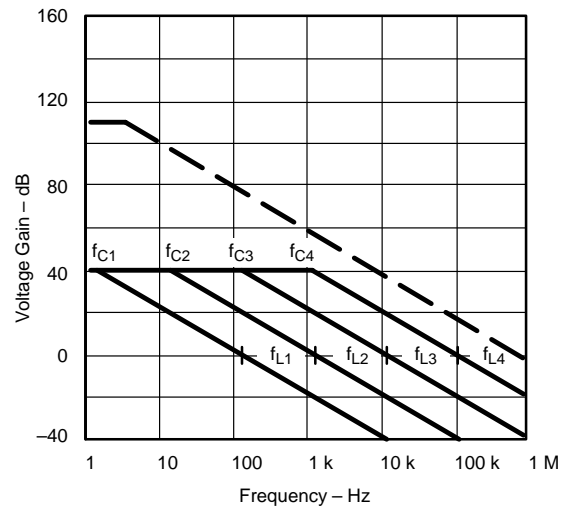
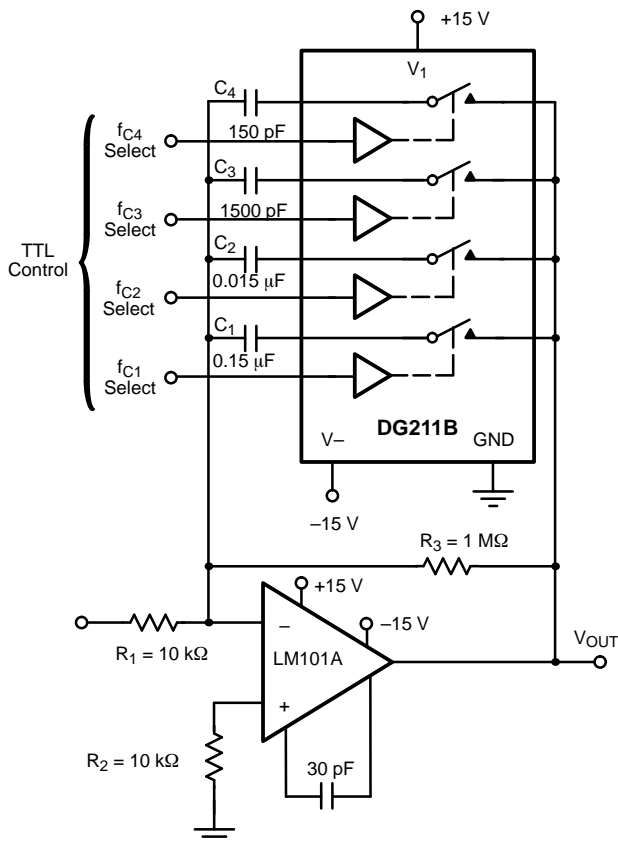


**FIGURE 4.** Channel-to-Channel Crosstalk



$\Delta V_O$  = measured voltage error due to charge injection  
 The charge injection in coulombs is  $Q = C_L \times \Delta V_O$

**FIGURE 5.** Charge Injection

**APPLICATIONS**

**FIGURE 6.** Sample-and-Hold


$$A_L \text{ (Voltage Gain Below Break Frequency)} = \frac{R_3}{R_1} = 100 \text{ (40 dB)}$$

$$f_C \text{ (Break Frequency)} = \frac{1}{2\pi R_3 C_X}$$

$$f_L \text{ (Unity Gain Frequency)} = \frac{1}{2\pi R_1 C_X}$$

$$\text{Max Attenuation} = \frac{\Gamma_{DS(on)}}{10 \text{ k}\Omega} \approx -47 \text{ dB}$$

**FIGURE 7.** Active Low Pass Filter with Digitally Selected Break Frequency

**APPLICATIONS**

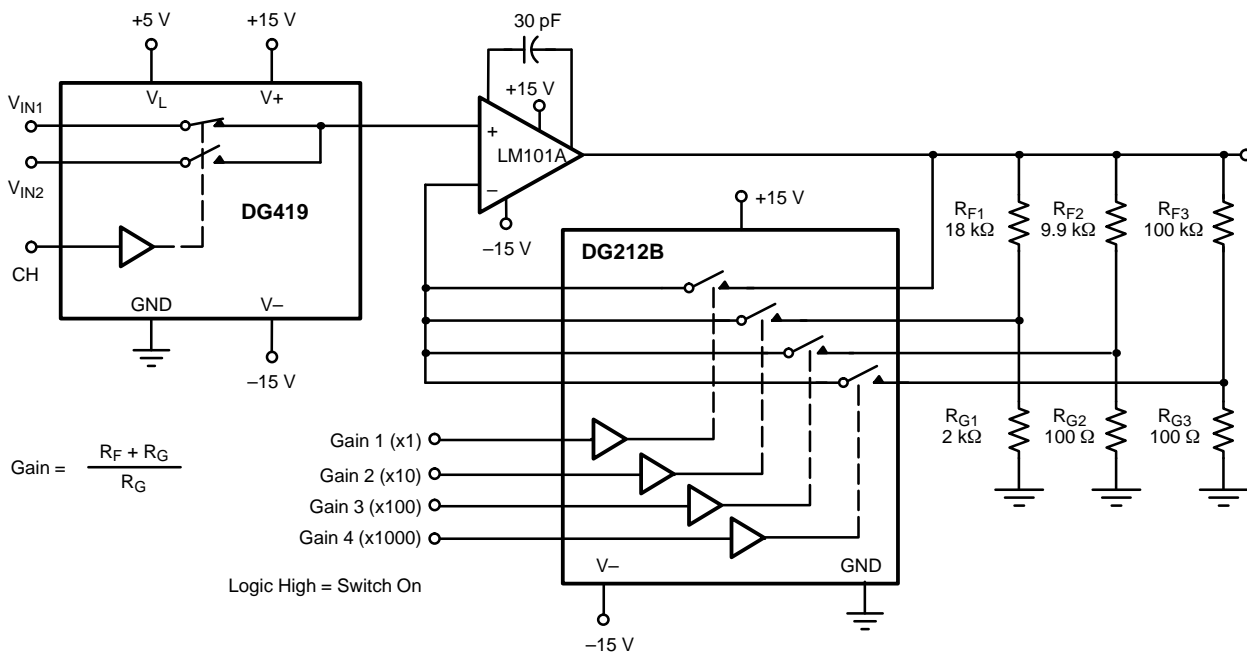


FIGURE 8. A Precision Amplifier with Digitally Programmable Input and Gains





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