74LS Series – Low Power Schottky TTL

INTRODUCTION

Low Power Schottky TTL offers the same speed as Standard TTL at 1/5 the power. The power savings and LSI potential result in Low Power Schottky being the preferred range in most new system designs. The series offers gate propagation delays of typically 10ns at 2 mW (1/5 of standard 74 series power). Flip Flop Toggle rate of 30 MHz and MSI 4-Bit Add Time of 21ns.

Care must be taken however when designing in 74LS as follows:

- Check the fan-out requirements at each output node where a 74LS device may have to drive a 74 device. Do not exceed five 7400 loads.
- Check the system set-up and hold times for sequential functions to ensure that data is available at the correct time for Low-Power Schottky functions. For 74LS these specifications sometimes differ slightly from those of the corresponding 74 type.
- Use standard 74 where necessary to drive capacitive loads greater than about 100 pF.

74LS does offer the following benefits when upgrading standard 74 series to 74LS:

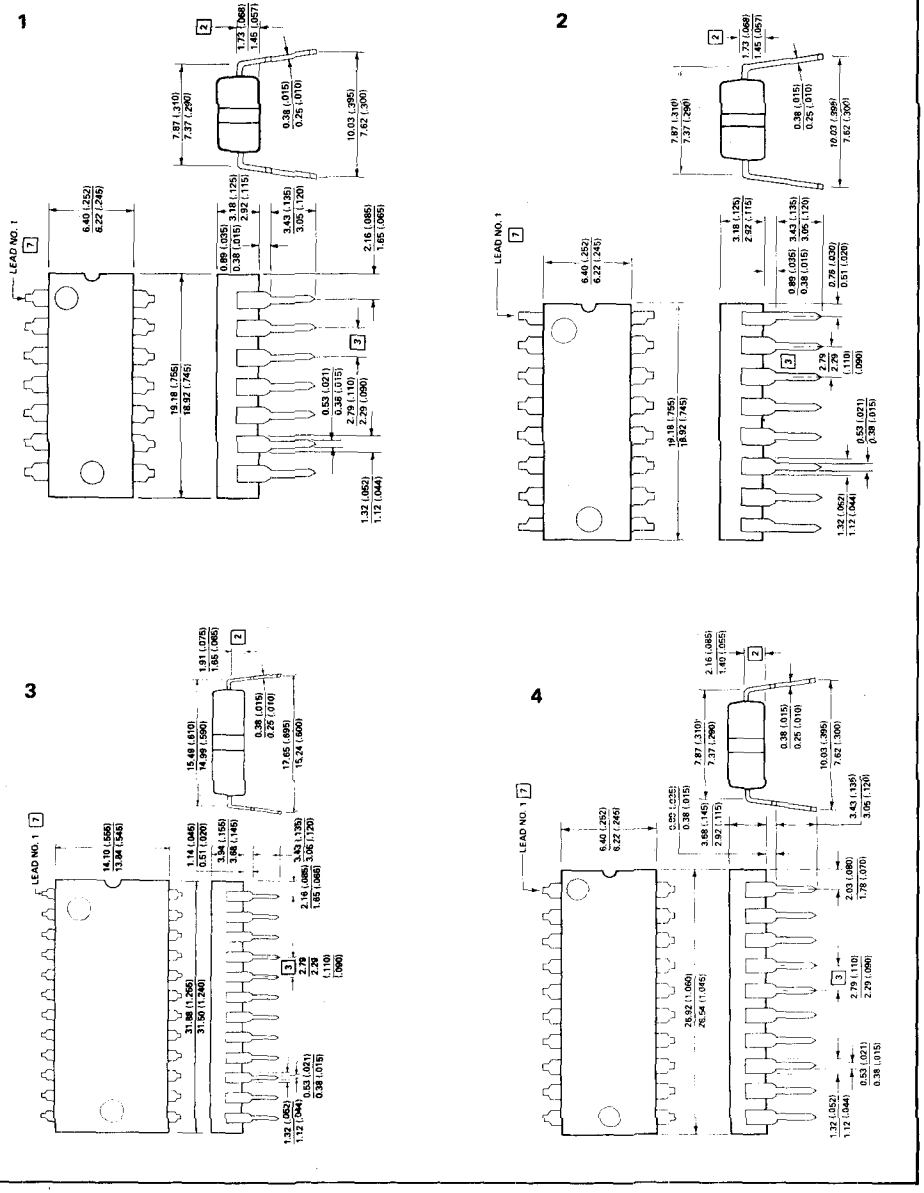
- Elimination of heating problems in systems such as terminals, point-of-sale systems, etc. in which it is necessary to put a lot of logic in a small package. Simply plugging in 74LS cuts heat generation dramatically.
- Reduced power supply cost.
- Possibility of upgrading system capability by adding plug-in logic boards without having to redesign the power supply.

MAXIMUM RATINGS

Supply Voltage, V_{CC} 7.0V
Input Voltage, V_{IN} 7.0V
Inter Emitter Voltage 5.5V
Operating Temperature T_a 0 to +70°C
Storage Temperature T_S −65 to +150°C
Short Circuit Output Current, I_{OS} −15 to −100 mA
DC Noise Margin Logic '1' 0.5V
Logic '0' 0.3V

REFERENCE TABLE

TYPE NO.	DESCRIPTION	STOCK NO.	OUTLINE DRWG. NO.	CONNECTION DIAG. NO.
N74LS00N	Quad 2-Input NAND Gate	**55645E**	1	B1
N74LS01N	Quad 2-Input NAND Gate with o/c	**55646C**	1	B2
N74LS02N	Quad 2-Input NOR Gate	**55647A**	1	B3
N74LS03N	Quad 2-Input NAND Gate with o/c	**55648X**	1	B4
N74LS04N	Hex Inverter	**55649H**	1	B5
N74LS05N	Hex Inverter with o/c	**55650X**	1	B6
N74LS07N	Hex Buffer/Driver with o/c	**55651R**	1	B8
N74LS08N	Quad 2-Input AND Gate	**55652G**	1	B9
N74LS09N	Quad 2-Input AND Gate with o/c	**55653E**	1	B10
N74LS10N	Triple 3-Input NAND Gate	**55654C**	1	B11
N74LS11N	Triple 3-Input NAND Gate	**55655A**	1	B12
N74LS12N	Triple 3-Input NAND Gate with o/c	**55656X**	1	B13
N74LS13N	Dual NAND Schmitt Trigger	**55657H**	1	B14
N74LS14N	Hex Schmitt Trigger	**55658F**	1	B15
N74LS15N	Triple 3-Input AND Gate with o/c	**55659D**	1	B175
N74LS20N	Dual 4-Input NAND Gate	**55660G**	1	B19
N74LS21N	Dual 4-Input AND Gate	**55661E**	1	B20
N74LS22N	Dual 4-Input NAND Gate with o/c	**55662C**	1	B217
N74LS26N	Quad 2-Input NAND Gate with o/c	**55663A**	1	B22
N74LS27N	Triple 3-Input NOR Gate	**55664X**	1	B23
N74LS28N	Quad 2-Input NOR Buffer	**55665H**	1	B24
N74LS30N	8-Input NAND Gate	**55666F**	1	B25
N74LS32N	Quad 2-Input OR Gate	**55667D**	1	B26
N74LS33N	Quad 2-Input NOR Buffer	**55668B**	1	B27
N74LS37N	Quad 2-Input NAND Buffer	**55669X**	1	B28
N74LS38N	Quad 2-Input NAND Buffer with o/c	**55670C**	1	B29
N74LS40N	Dual 4-Input NAND Buffer	**55671A**	1	B30
N74LS42N	BCD-to-Decimal Decoder	**55672X**	2	B31



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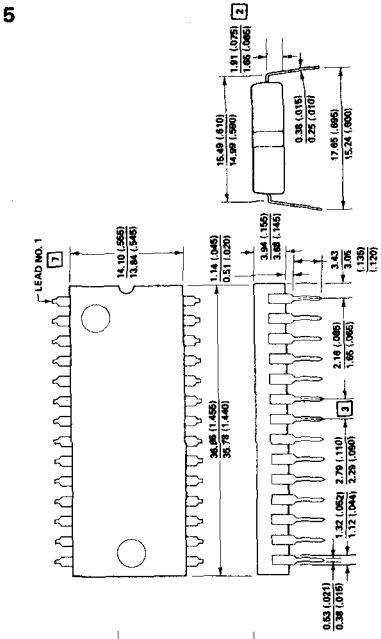
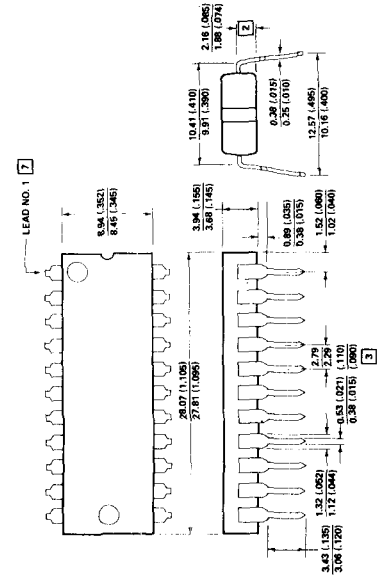
5


LEAD NO. 1
15.49 (.610)
14.99 (.590)
1.91 (.075)
1.65 (.065)
0.38 (.015)
0.25 (.010)
17.65 (.695)
15.24 (.600)
14.10 (.555)
13.84 (.545)
1.14 (.045)
0.51 (.020)
3.94 (.155)
3.68 (.145)
3.43 (.135)
3.05 (.120)
2.16 (.085)
1.65 (.065)
36.85 (1.450)
35.79 (1.440)
2.79 (.110)
2.29 (.090)
1.32 (.052)
1.12 (.044)
0.53 (.021)
0.38 (.015)

6


LEAD NO. 1
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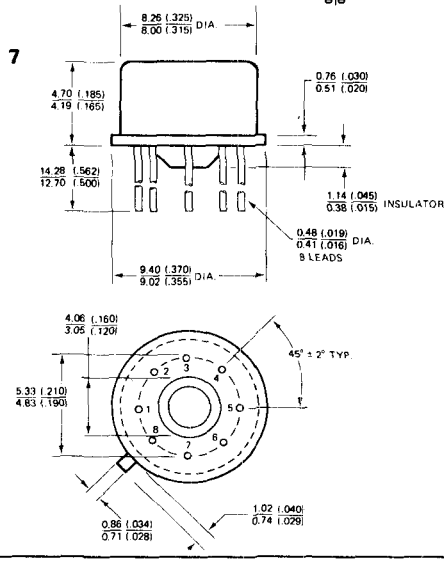
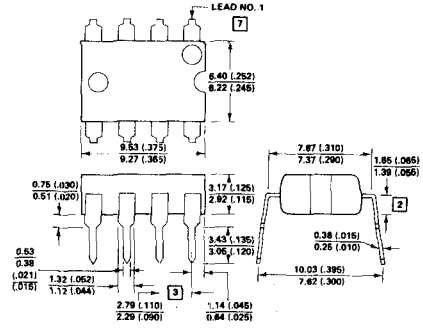
1.88 (.074)
10.41 (.410)
9.91 (.390)
0.38 (.015)
0.25 (.010)
12.57 (.495)
10.16 (.400)
8.94 (.352)
8.45 (.345)
3.94 (.155)
3.68 (.145)
0.89 (.035)
0.38 (.015)
1.52 (.060)
1.02 (.040)
25.07 (1.105)
27.81 (1.095)
2.79
2.29
(.110)
(.090)
0.53 (.021)
0.38 (.015)
1.32 (.052)
1.12 (.044)
3.43 (.135)
3.06 (.120)

7


8.26 (.325)
8.00 (.315) DIA.
4.70 (.185)
4.19 (.165)
0.76 (.030)
0.51 (.020)
14.28 (.562)
12.70 (.500)
1.14 (.045)
0.38 (.015) INSULATOR
0.48 (.019)
0.41 (.016) DIA.
8 LEADS
9.40 (.370)
9.02 (.355) DIA.
4.06 (.160)
3.05 (.120)
45° ± 2° TYP.
5.33 (.210)
4.83 (.190)
0.86 (.034)
0.71 (.028)
1.02 (.040)
0.74 (.029)

8


LEAD NO. 1
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6.22 (.245)
9.53 (.375)
9.27 (.365)
7.87 (.310)
7.37 (.290)
1.85 (.065)
1.39 (.055)
0.75 (.030)
0.51 (.020)
3.17 (.125)
2.92 (.115)
0.38 (.015)
0.25 (.010)
3.43 (.135)
3.06 (.120)
0.53
0.38
(.021)
(.015)
1.32 (.052)
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10.03 (.395)
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1.14 (.045)
0.64 (.025)

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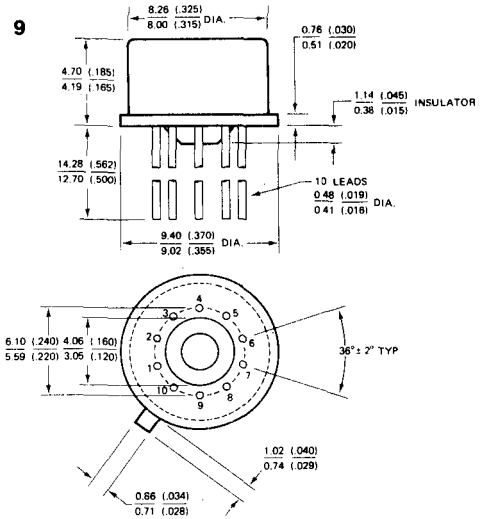

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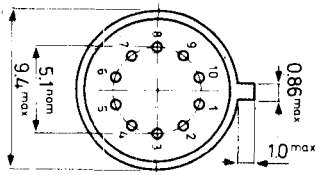

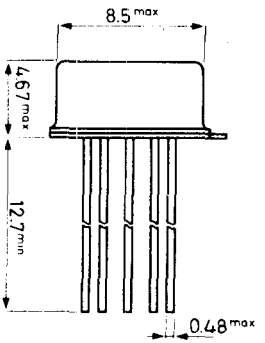

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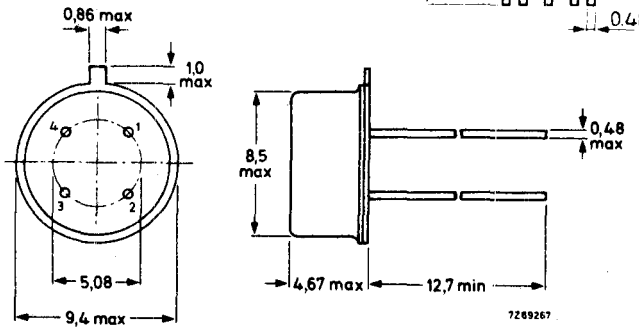

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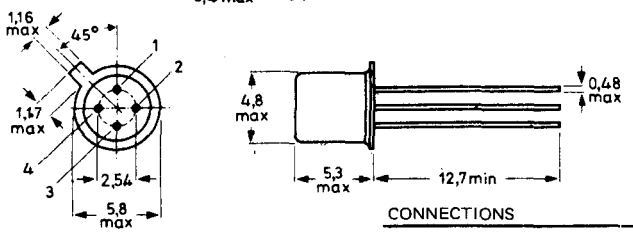
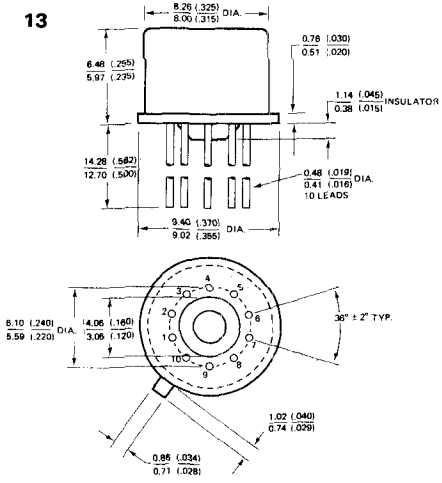


pin 4 connected to case

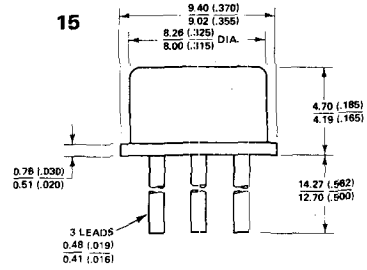
CONNECTIONS

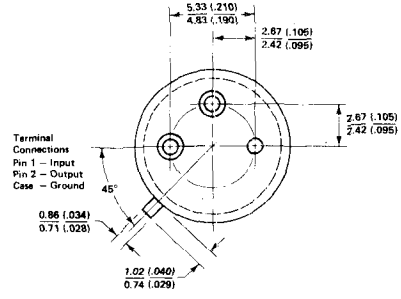
DRWG NO.	1	2	3	4	
12.1	V_O	V_P	V_i	V_N	Substrate connected to envelope
12.2	d	g_2	g_1	S	
12.3	s	d	g	*	

13

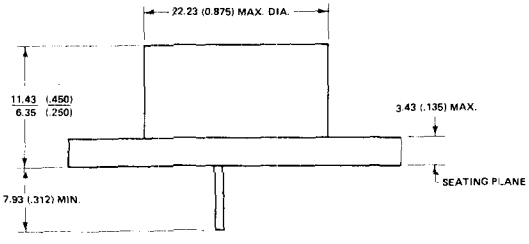

8.26 (.325)
8.00 (.315) DIA.
0.76 (.030)
0.51 (.020)
6.48 (.255)
5.97 (.235)
1.14 (.045)
0.38 (.015) INSULATOR
14.28 (.562)
12.70 (.500)
0.48 (.019)
0.41 (.016) DIA.
10 LEADS
9.40 (.370)
9.02 (.355) DIA.
6.10 (.240)
5.59 (.220) DIA.
4.06 (.160)
3.06 (.120)
36° ± 2° TYP.
1.02 (.040)
0.74 (.029)
0.86 (.034)
0.71 (.028)

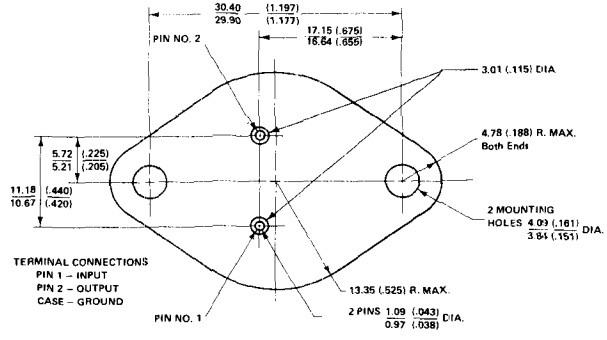
15


9.40 (.370)
9.02 (.355)
8.26 (.325)
8.00 (.315) DIA.
4.70 (.185)
4.19 (.165)
0.76 (.030)
0.51 (.020)
14.27 (.562)
12.70 (.500)
3 LEADS
0.48 (.019)
0.41 (.016)

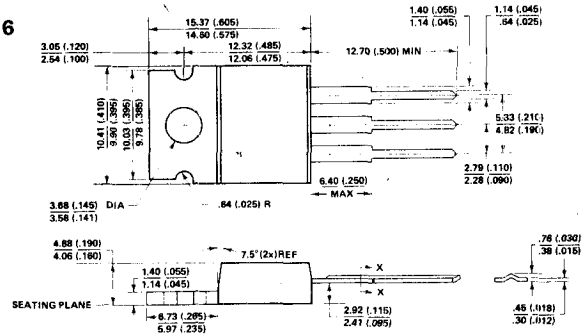

5.33 (.210)
4.83 (.190)
2.67 (.105)
2.42 (.095)
2.67 (.105)
2.42 (.095)
Terminal
Connections
Pin 1 – Input
Pin 2 – Output
Case – Ground
45°
0.86 (.034)
0.71 (.028)
1.02 (.040)
0.74 (.029)

14


22.23 (0.875) MAX. DIA.
11.43 (.450)
6.35 (.250)
3.43 (.135) MAX.
SEATING PLANE
7.93 (.312) MIN.


30.40 (1.197)
29.90 (1.177)
17.15 (.675)
16.64 (.655)
PIN NO. 2
3.01 (.115) DIA.
4.78 (.188) R. MAX.
Both Ends
5.72 (.225)
5.21 (.205)
11.18 (.440)
10.67 (.420)
2 MOUNTING
HOLES 4.09 (.161)
3.84 (.151) DIA.
TERMINAL CONNECTIONS
PIN 1 – INPUT
PIN 2 – OUTPUT
CASE – GROUND
13.35 (.525) R. MAX.
PIN NO. 1
2 PINS 1.09 (.043)
0.97 (.038) DIA.

16



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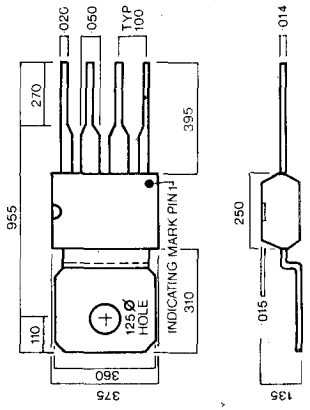

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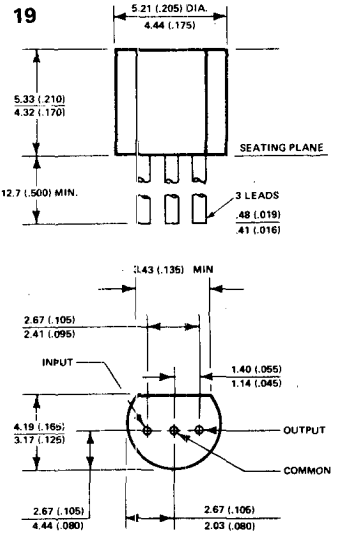

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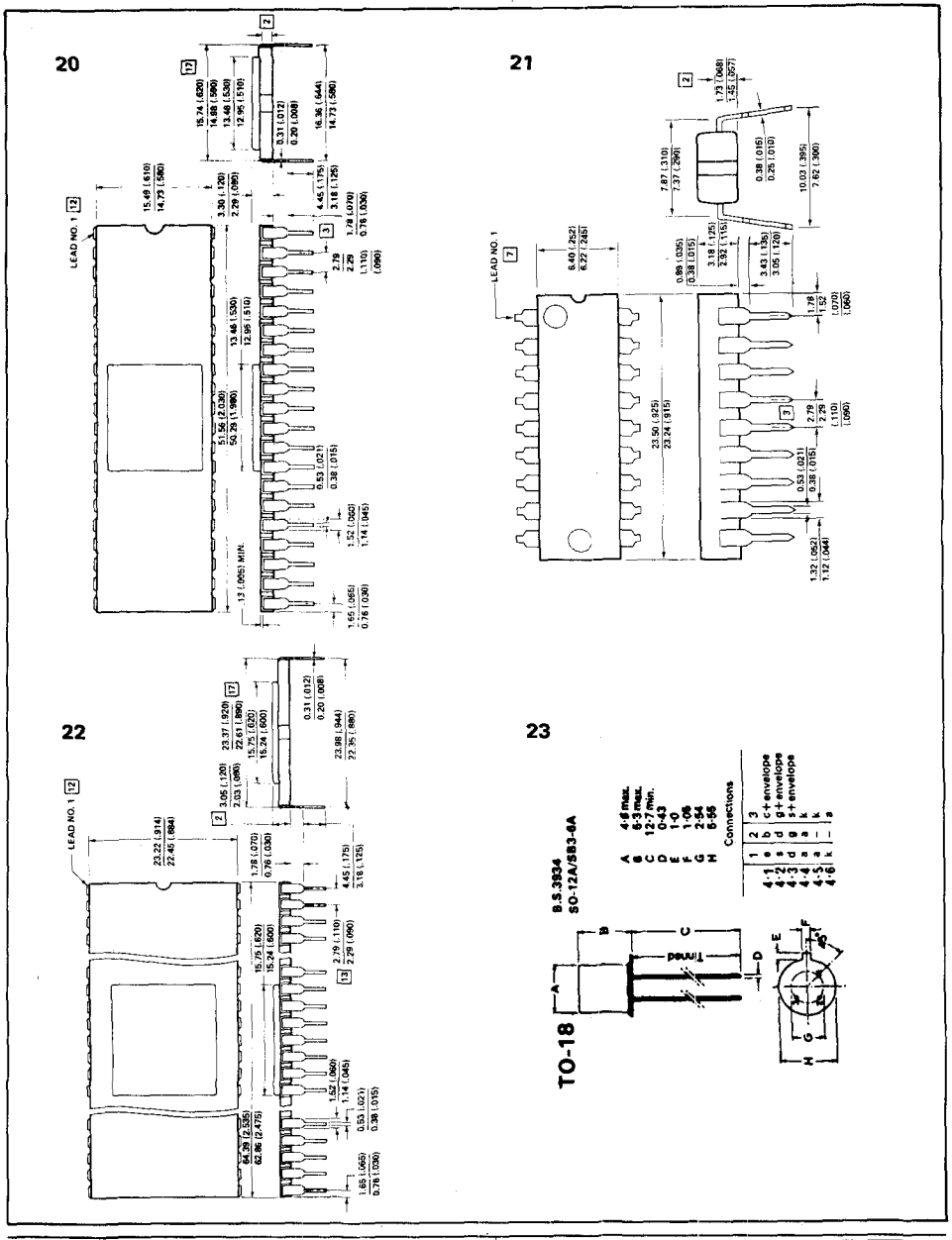
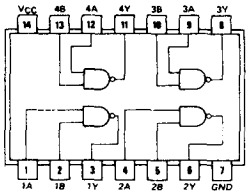

20
21
22
23
LEAD NO. 1
TO-18
SO-12A/SB3-6A
B.S.3934
Connections

B1



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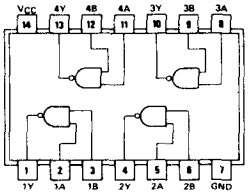

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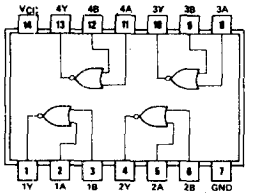

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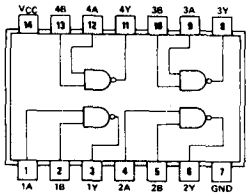

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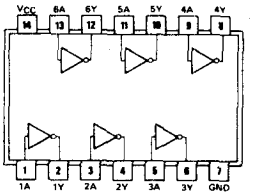

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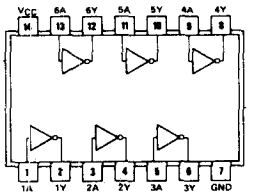

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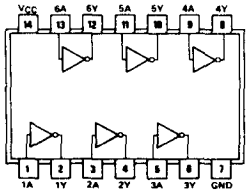

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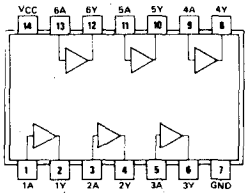

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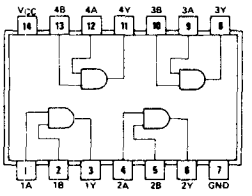

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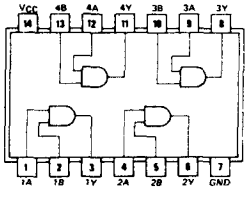

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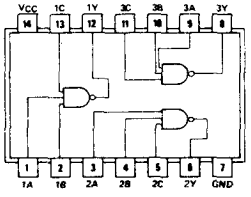

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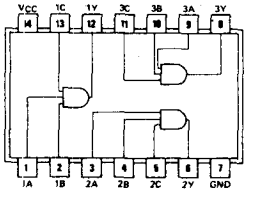

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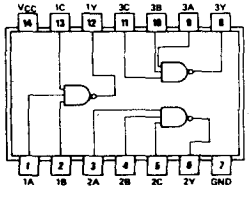

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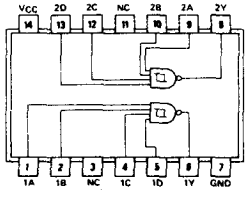

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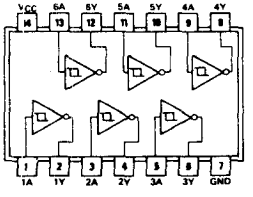

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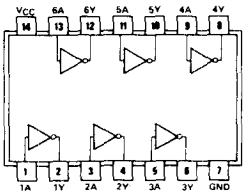
Signetics

Connection Diagram

B17



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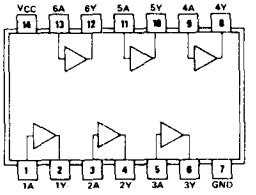

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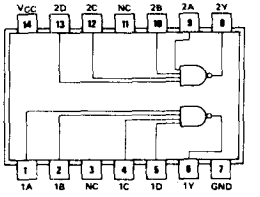

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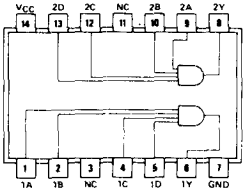

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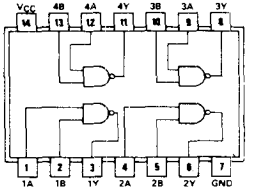

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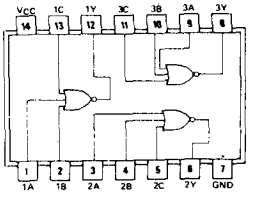

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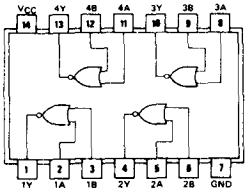

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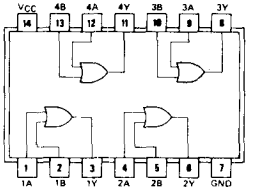

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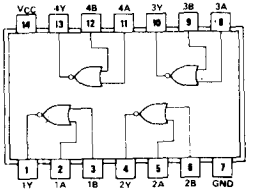

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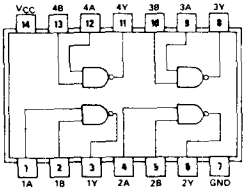

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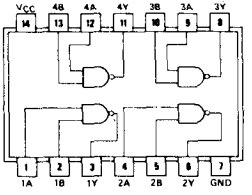

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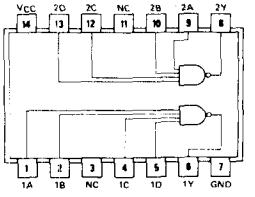

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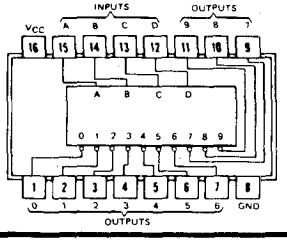

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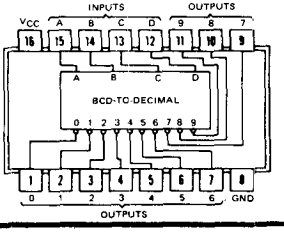

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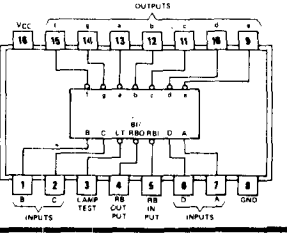

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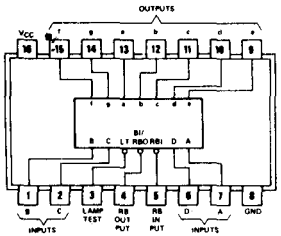

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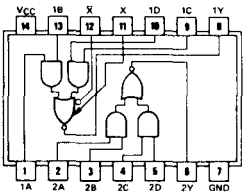

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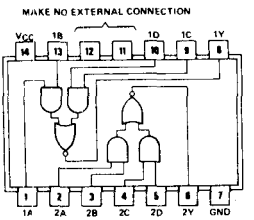

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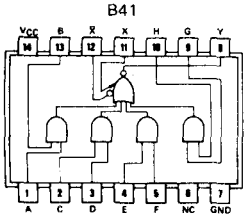

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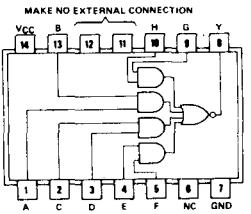

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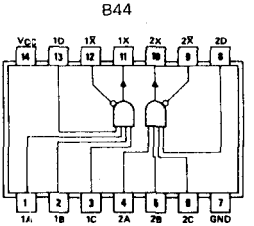

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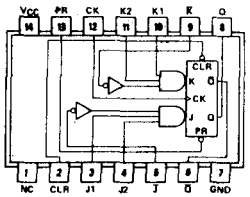

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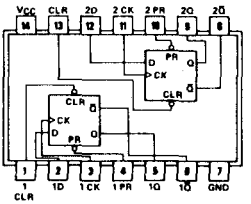

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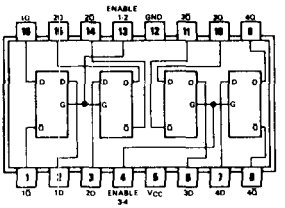

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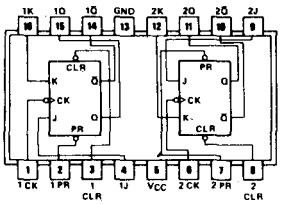

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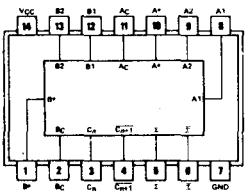

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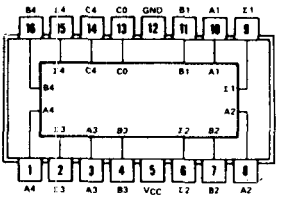

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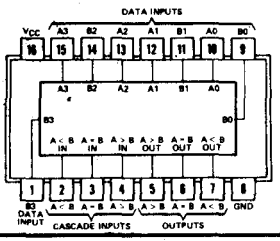

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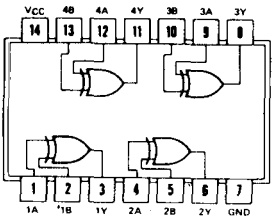

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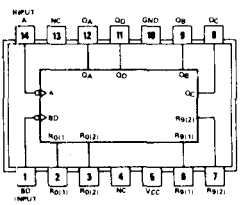

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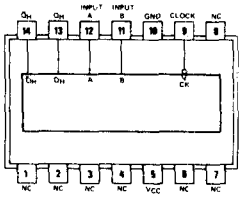

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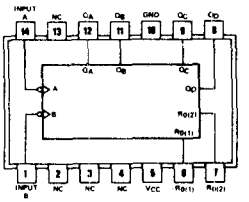

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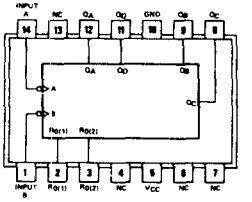

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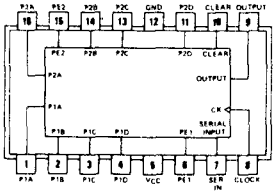

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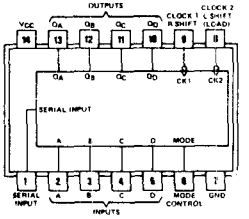

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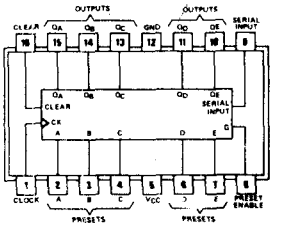

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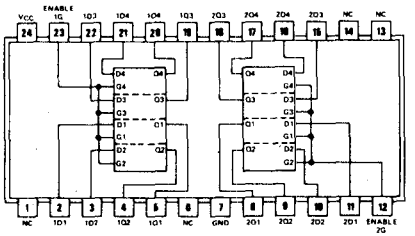

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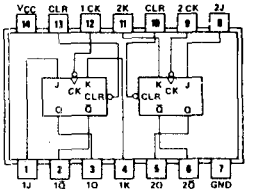

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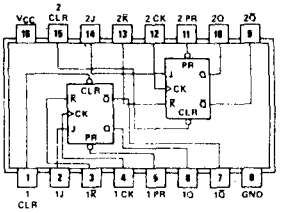

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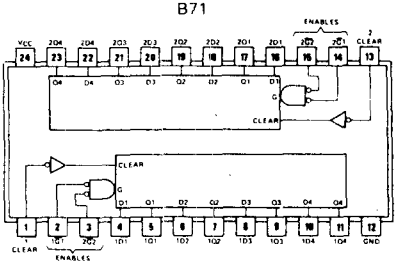

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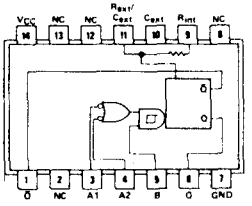

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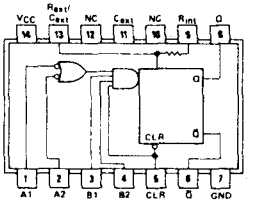

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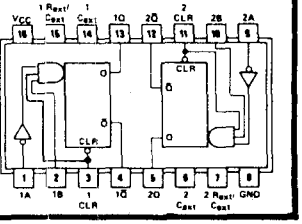

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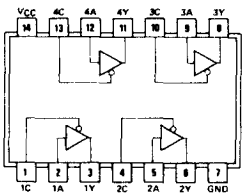

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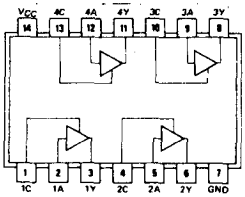

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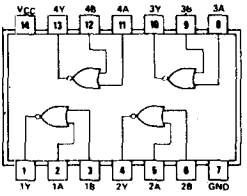

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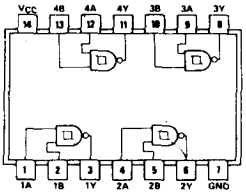

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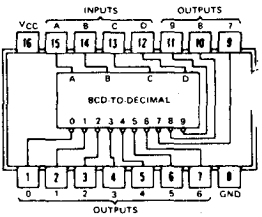

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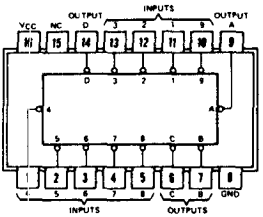

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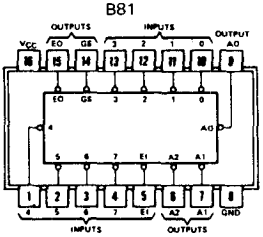

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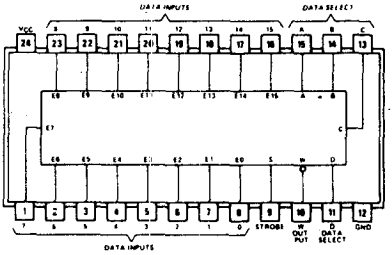

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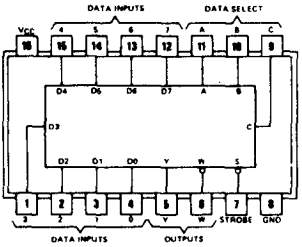

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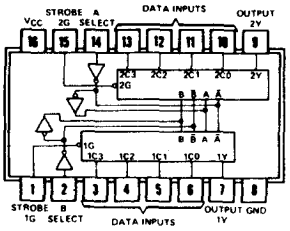

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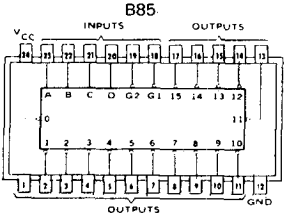

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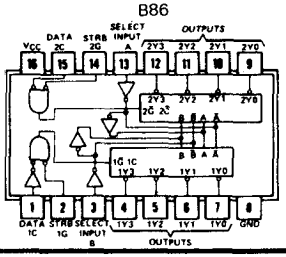

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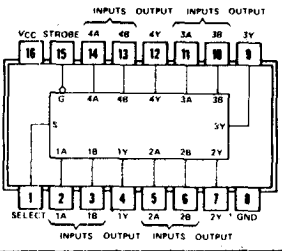

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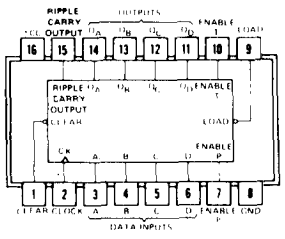

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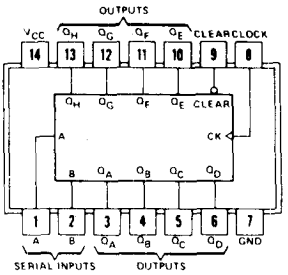

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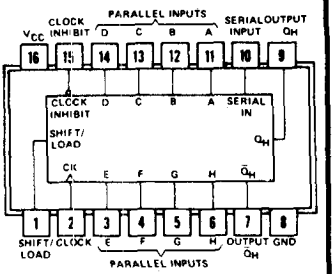

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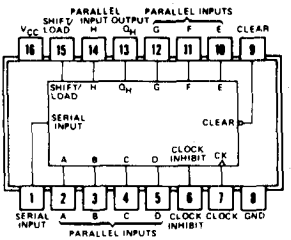

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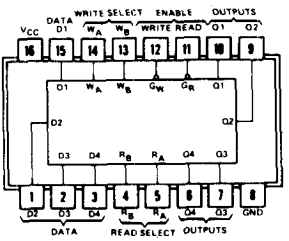

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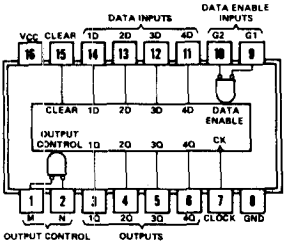

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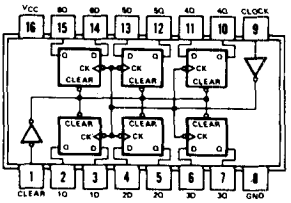

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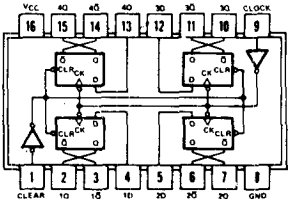

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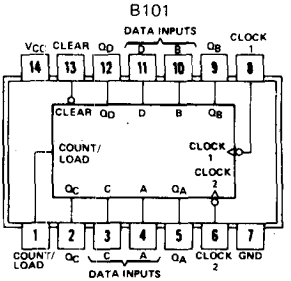

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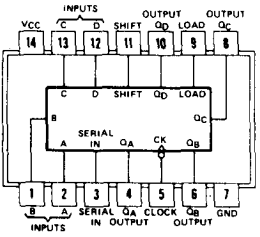

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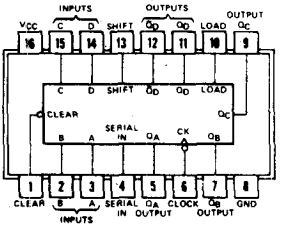

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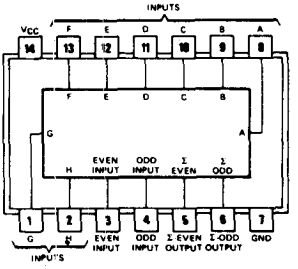

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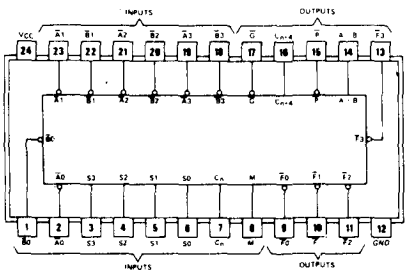

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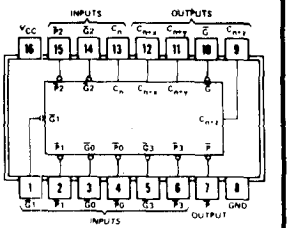

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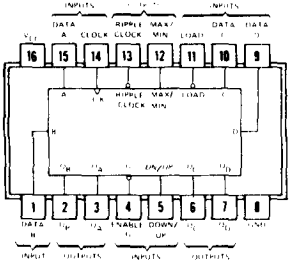

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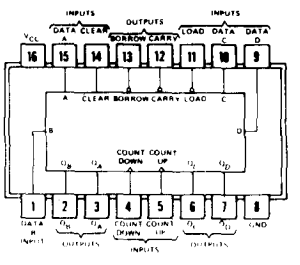

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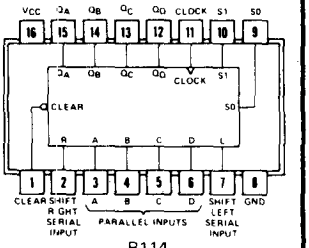

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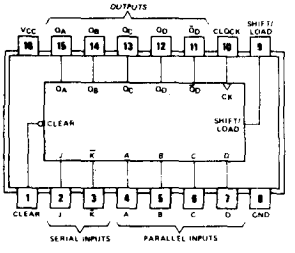

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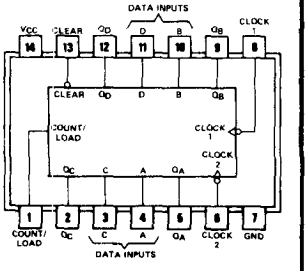

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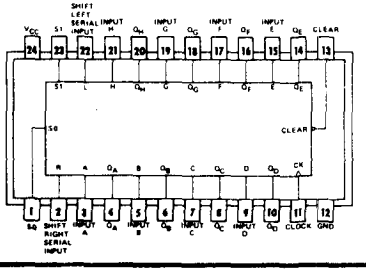

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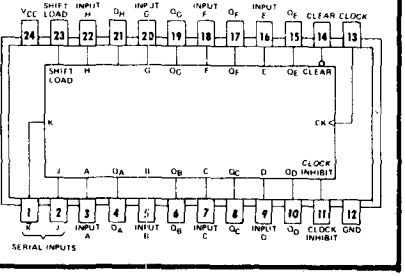

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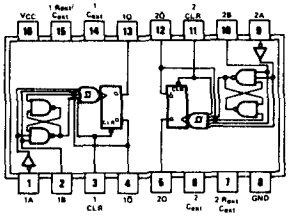

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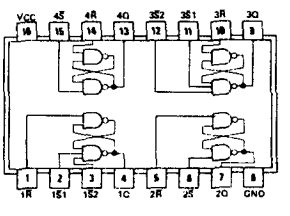

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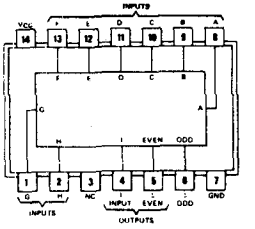

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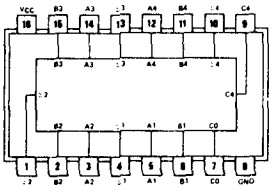

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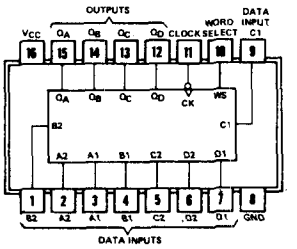

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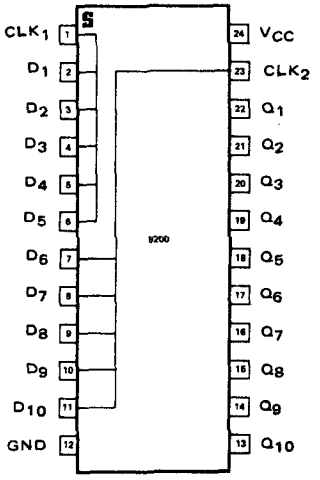

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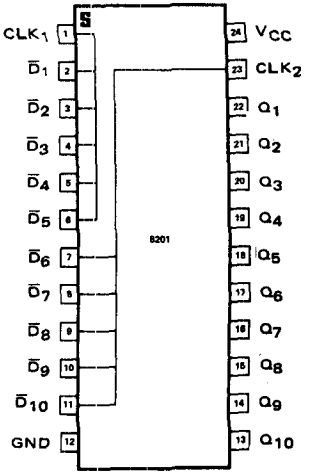

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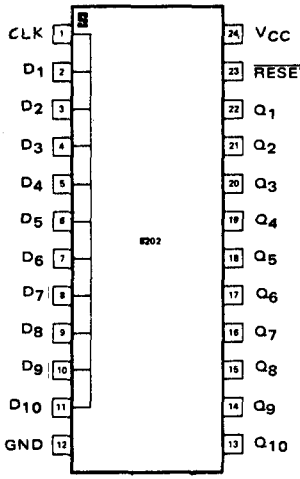

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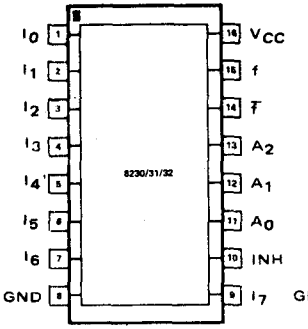

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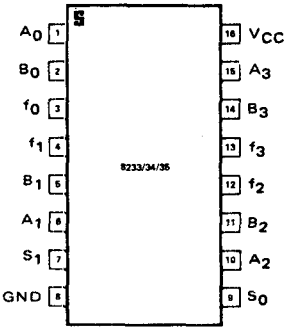

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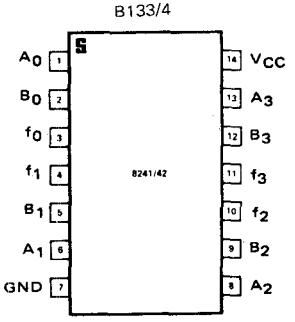

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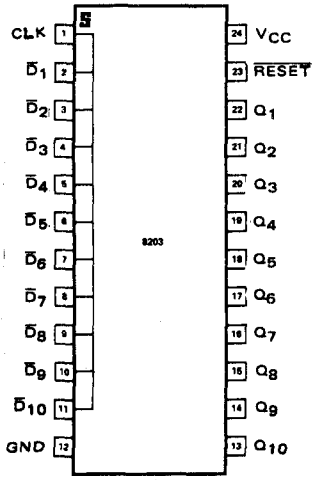

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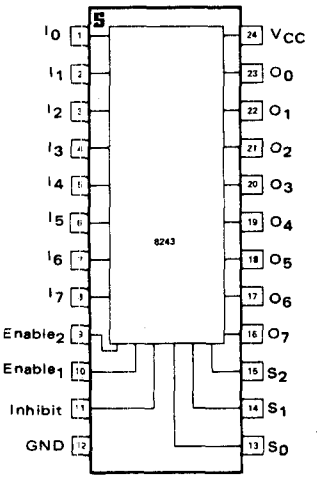

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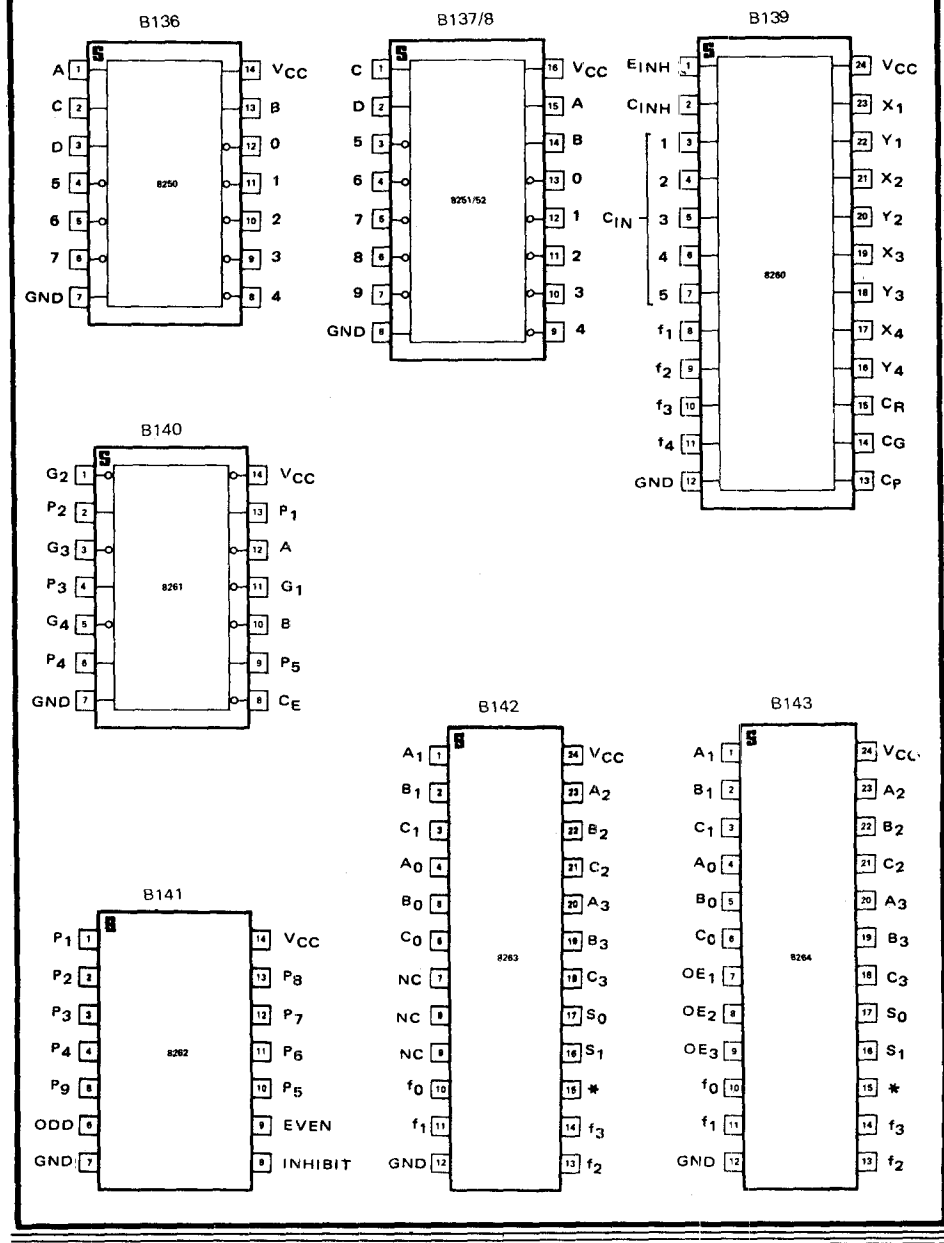

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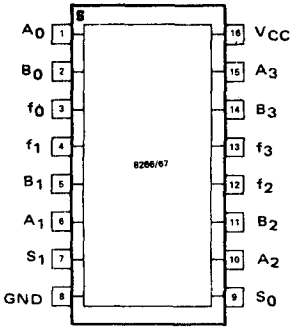

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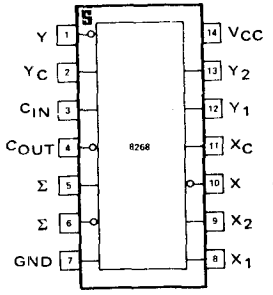

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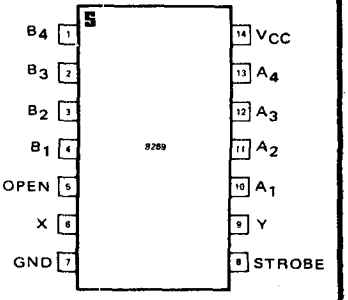

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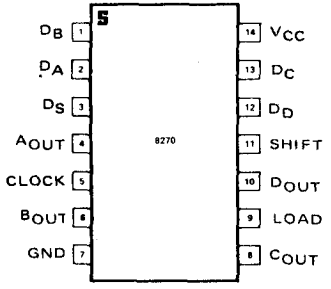

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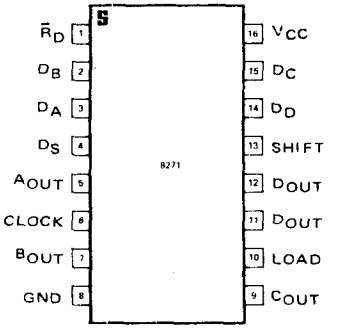

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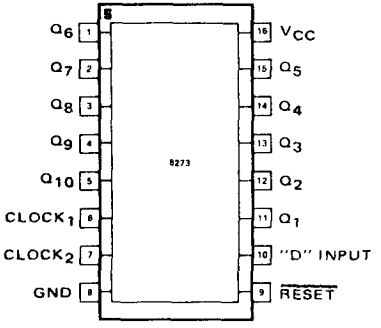

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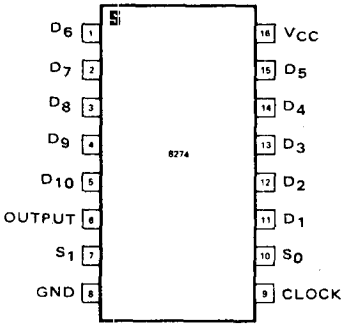

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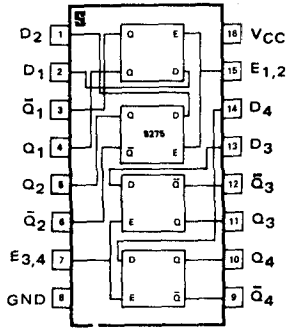

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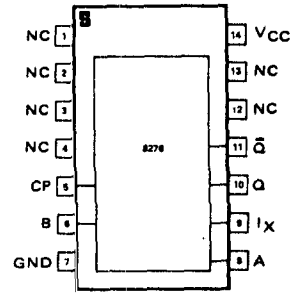

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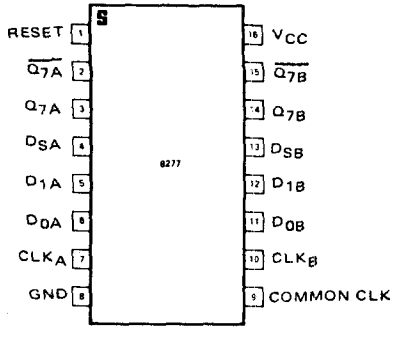

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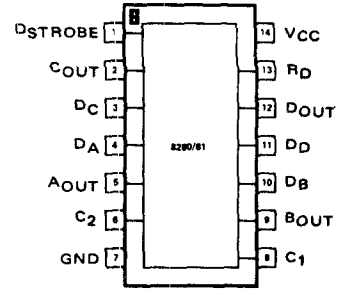

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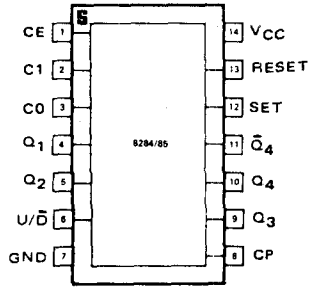

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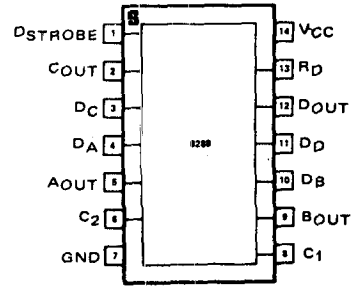

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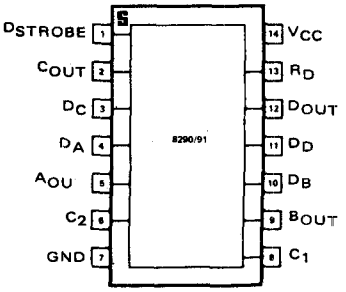

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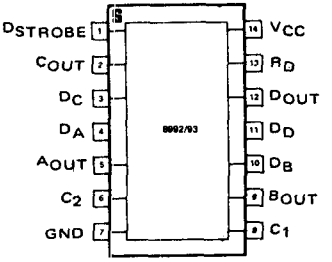

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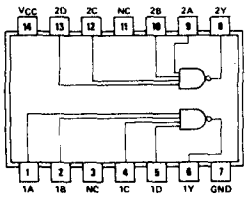

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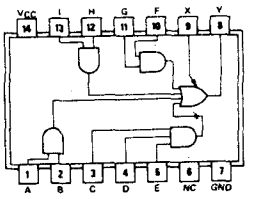

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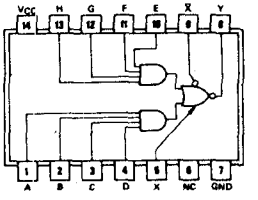

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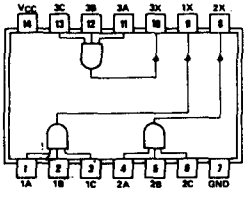

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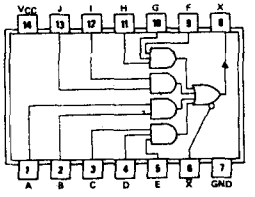

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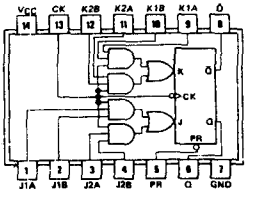

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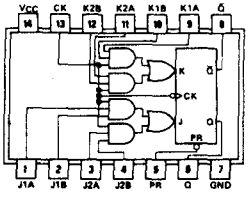

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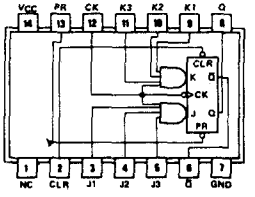

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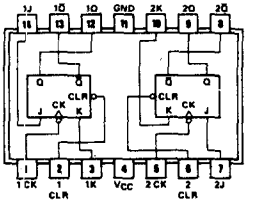

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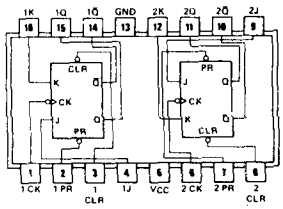

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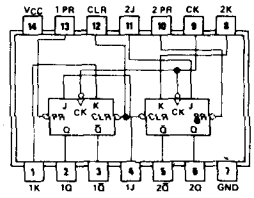

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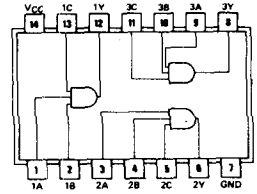

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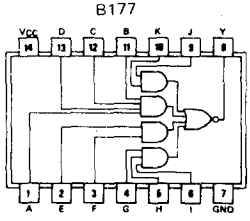

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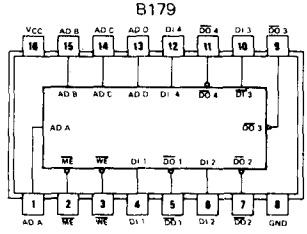

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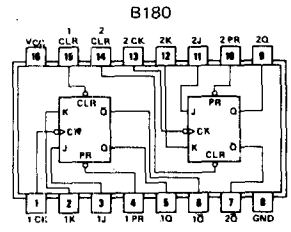

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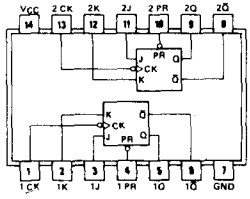

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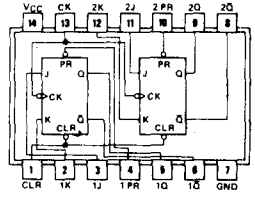

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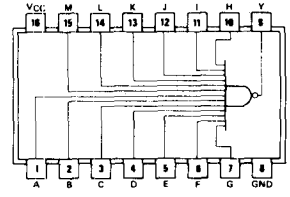

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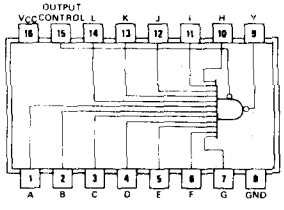

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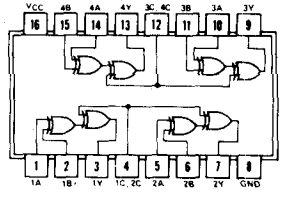

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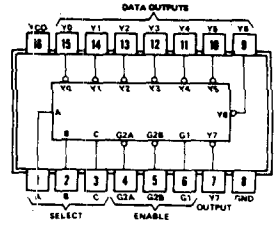

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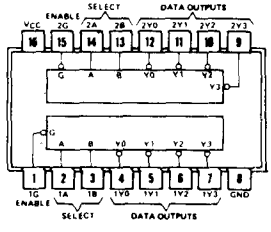

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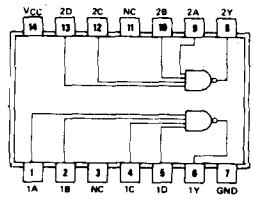

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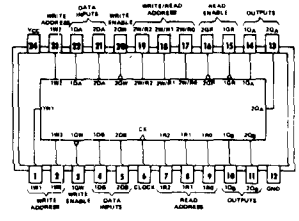

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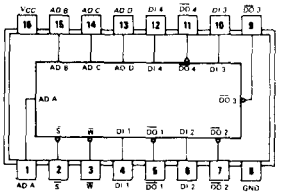

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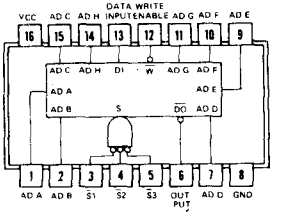

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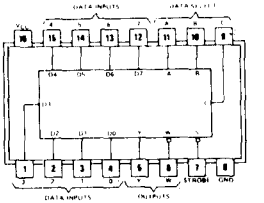

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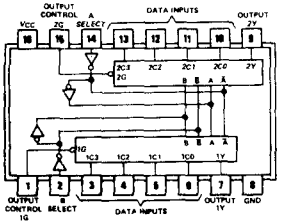

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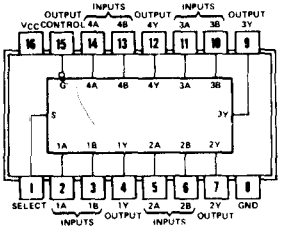

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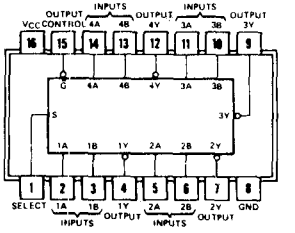

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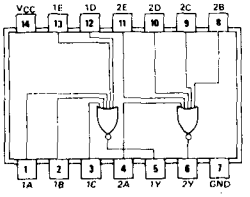

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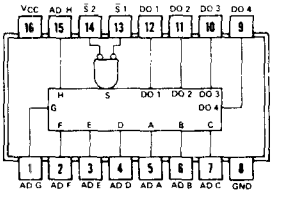

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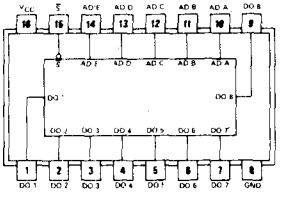

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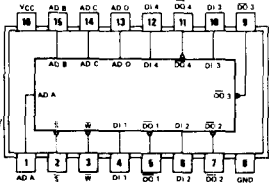

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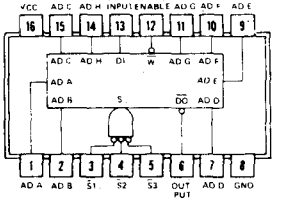

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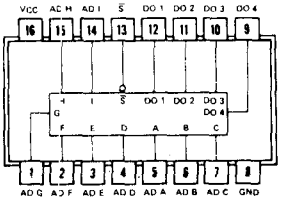

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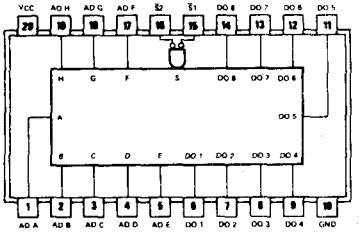

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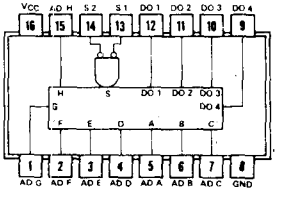

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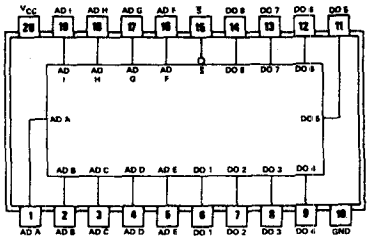

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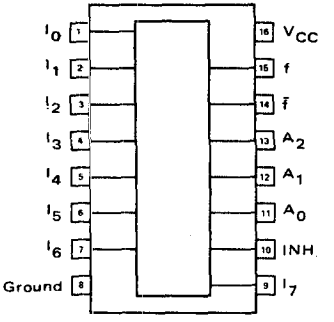

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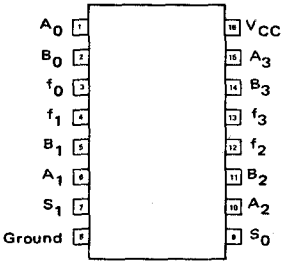

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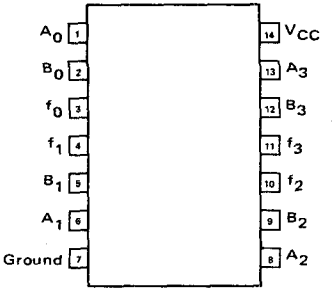

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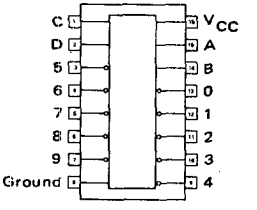

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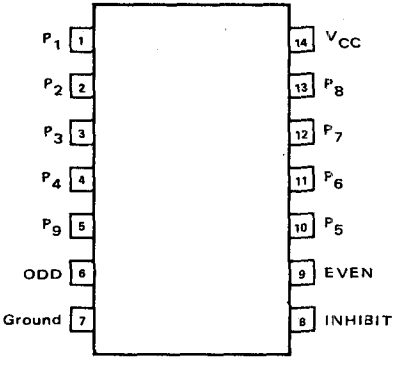

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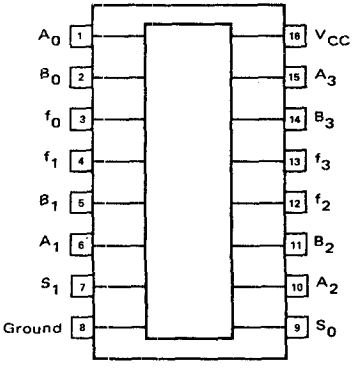

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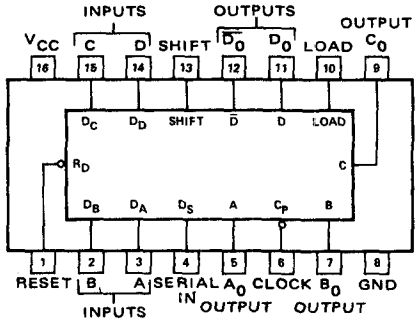

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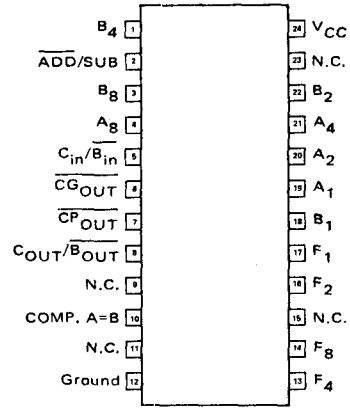

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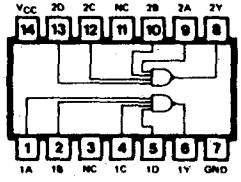

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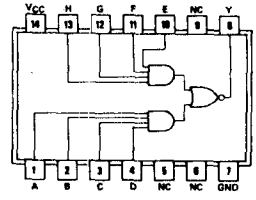

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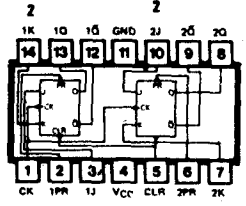

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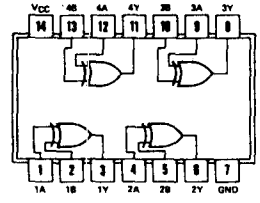

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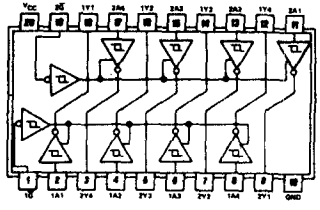

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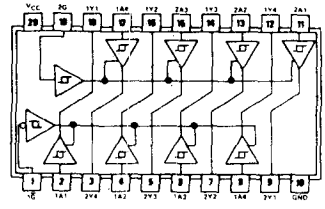

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Connection Diagram

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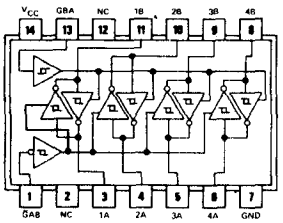

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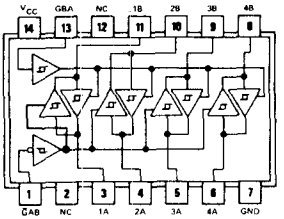

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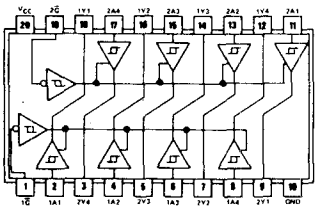

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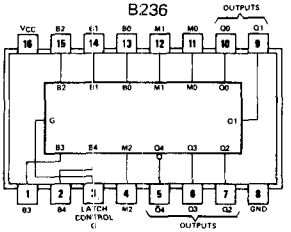

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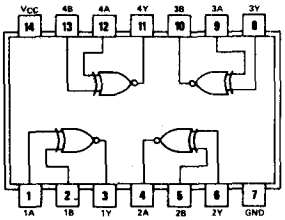

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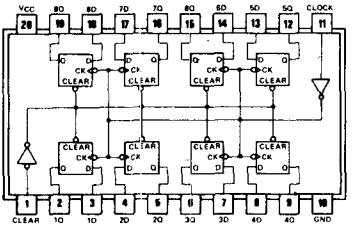

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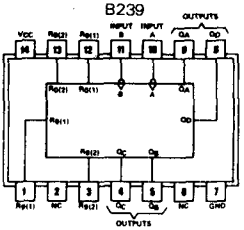

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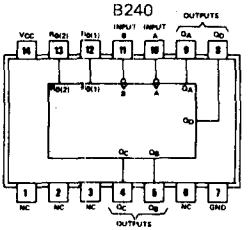

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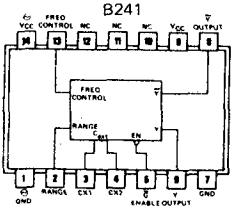

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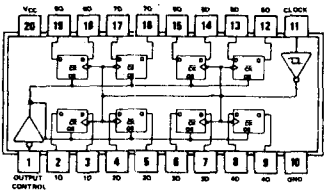

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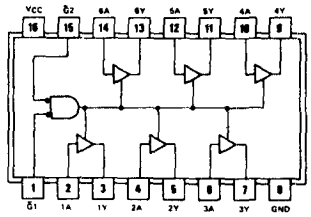

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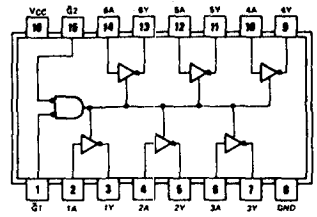

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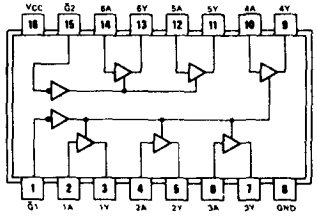

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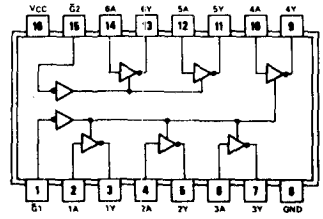

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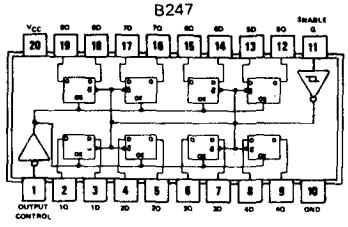

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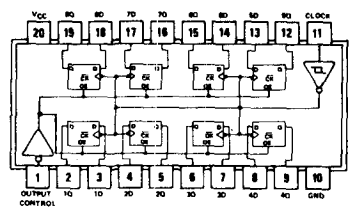

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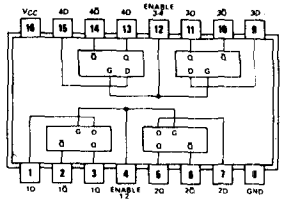

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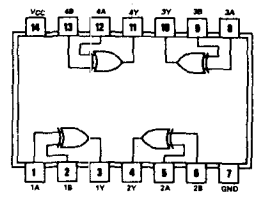

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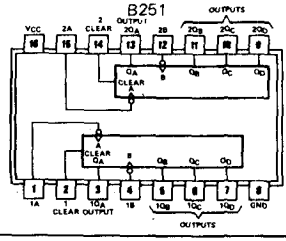

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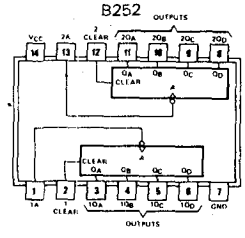

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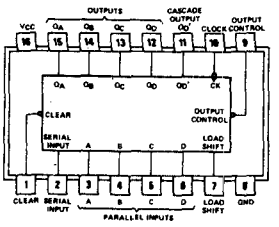

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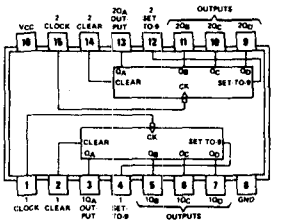
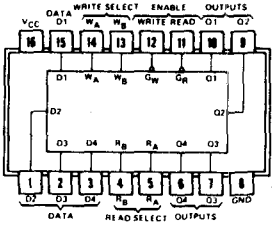


B255



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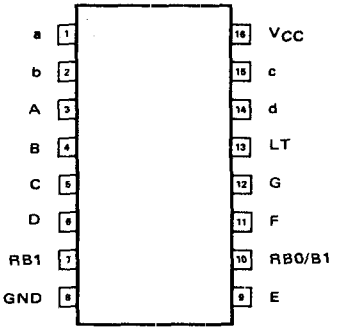
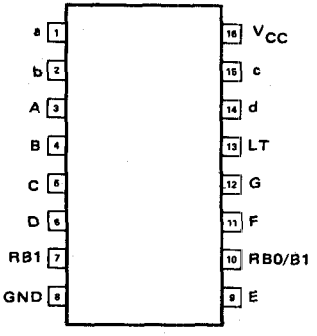
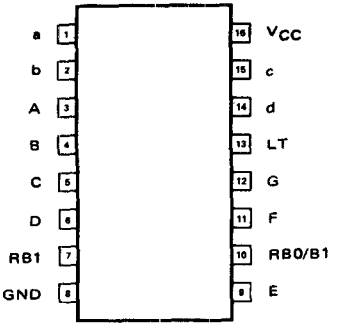


B257



B258



B259