

8K-bit TTL bipolar PROM (1024 x 8)

82S181

FEATURES

- Address access time: 90ns max
- Input loading: -150µA max
- On-chip address decoding
- Four chip enable inputs
- Outputs: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

DESCRIPTION

The 82S181 is field-programmable, which means that custom patterns are immediately available by following the Philips Generic I fusing procedure. The 82S181 is supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

ORDERING INFORMATION

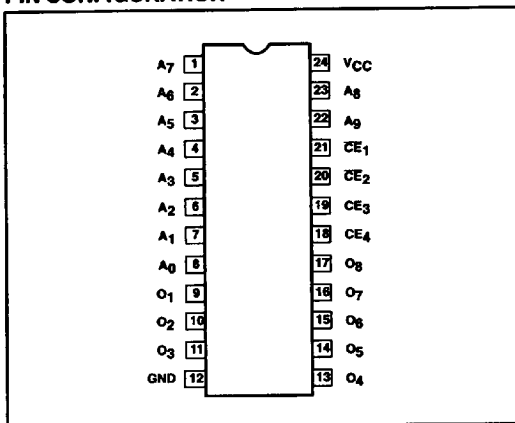
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24-pin Ceramic DIP (600mil-wide)	82S181/BJA	GDIP1-T24
24-pin Ceramic Flat Pack	82S181/BKA	GDFF-F24
28-Pin Ceramic LLCC	82S181/B3A	CQCC2-N28

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

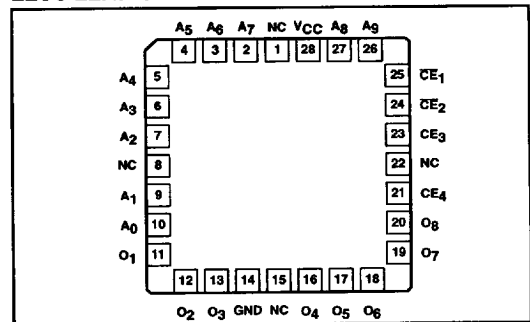
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	+7	V _{DC}
V _I	Input voltage	+5.5	V _{DC}
V _O	Output voltage Off-State	+5.5	V _{DC}
T _A	Operating temperature range	-55 to +125	°C
T _{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



LLCC LEAD CONFIGURATION



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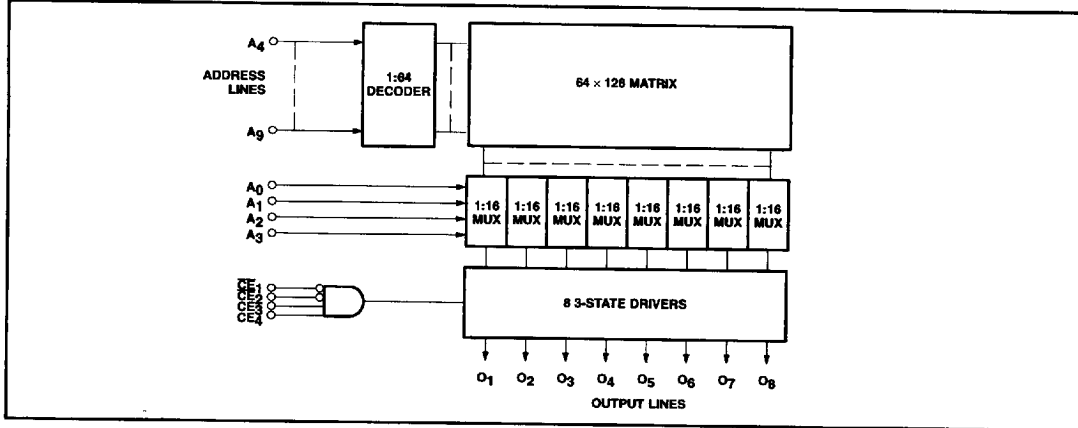
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BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
			Min	Typ ⁵	Max	
Input voltage²						
V _{IL}	Low	V _{CC} = 4.5V, I _I = -18mA	2.0		0.8	V
V _{IH}	High					
V _{IK}	Clamp					
Output voltage²						
V _{OL}	Low	V _{CC} = 4.5V CE _{1,2} = Low, CE _{3,4} = High I _O = 9.6mA	2.4		0.5	V
V _{OH}	High	I _O = -2mA				
Input current¹						
I _{IL}	Low	V _{CC} = 5.5V V _I = 0.45V			-150	μA
I _{IH}	High					
Output current¹						
I _{OZ}	Hi-Z state	V _{CC} = 5.5V CE _{1,2} = High, CE _{3,4} = Low, V _O = 5.5V	-15		40	μA
I _{OS}	Short circuit ³	CE _{1,2} = High, CE _{3,4} = Low, V _O = 0.4V				
		CE _{1,2} = Low, CE _{3,4} = High, V _O = 0V V _{CC} = 5.5V, High stored				
Supply current						
I _{CC}		CE _{1,2} = High, CE _{3,4} = Low, V _{CC} = 5.5V		125	185	mA
Capacitance⁶						
C _{IN}	Input	CE _{1,2} = High, V _{CC} = 5.0V V _I = 2.0V			5	10
C _{OUT}	Output					

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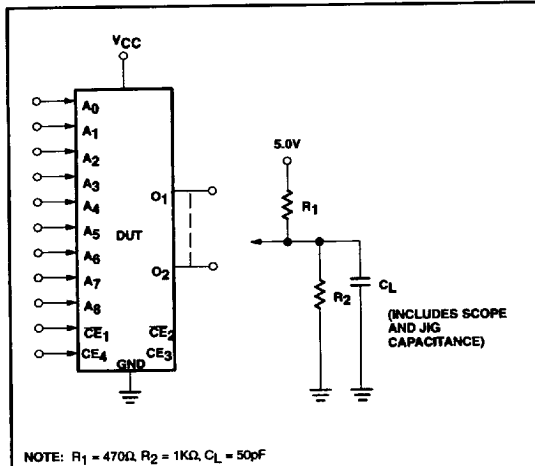
AC ELECTRICAL CHARACTERISTICS $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ ⁵	Max	
t_{AA}	Access time ⁴	Output	Address	50	90		ns
t_{CE}	Access time ⁴	Output	Chip Enable	20	50		ns
t_{CD}	Disable time	Output	Chip Disable	20	50		ns

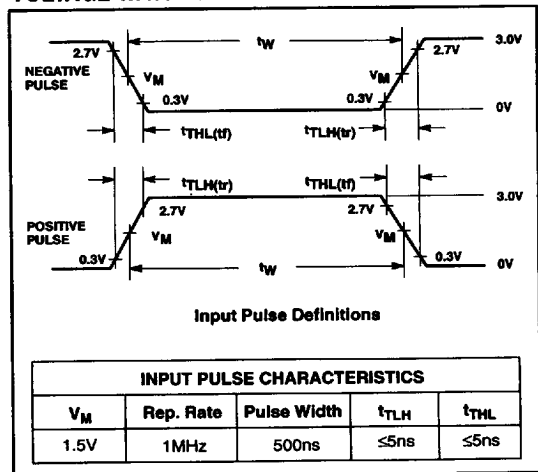
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μ s.
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = +25^{\circ}\text{C}$.
6. Guaranteed, but not tested.

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



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TIMING DIAGRAMS

