

54LS373, 54LS374, 54S373, 54S374

Latches/Flip-Flops

'373 Octal Transparent Latch with 3-State Outputs

'374 Octal D Flip-Flop with 3-State Outputs

Product Specification

Military Logic Products

FEATURES

- 8-bit transparent latch — '373
- 8-bit positive, edge-triggered register — '374
- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

DESCRIPTION

The '373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable (OE) control gates.

ORDERING INFORMATION

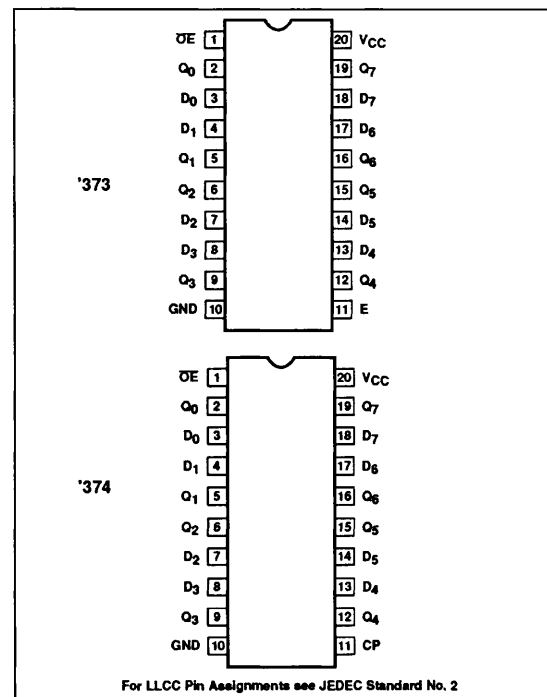
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54LS373/BRA 54S373/BRA 54LS374/BRA 54S374/BRA
20-Pin Ceramic FlatPack	54LS373/BSA 54S373/BSA 54LS374/BSA 54S374/BSA
20-Pin Ceramic LLCC	54LS373/B2A 54S373/B2A 54LS374/B2A 54S374/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

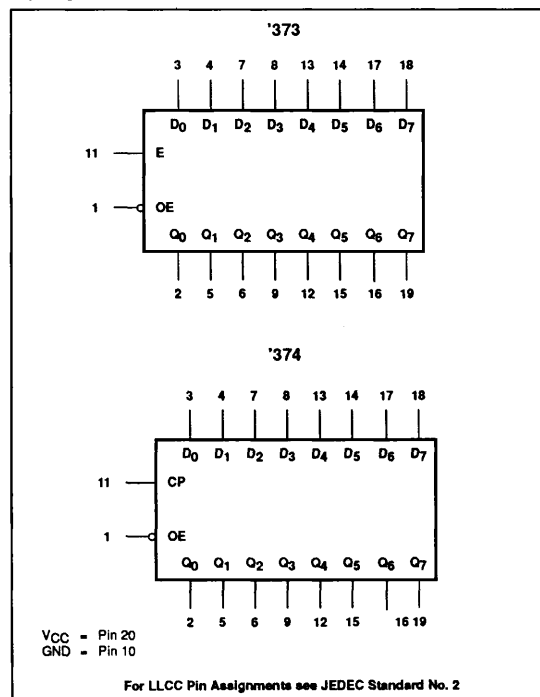
PINS	DESCRIPTION	54S	54LS
All	Inputs	1SUL	1LSUL
All	Outputs	10SUL	30LSUL

NOTE: Where a 54S Unit Load (SUL) is 50 μ A I_{IH} and -2.0mA I_{IL} and a 54LS Unit Load (LSUL) is 20 μ A I_{IH} and -0.4mA I_{IL} .

PIN CONFIGURATION



LOGIC SYMBOL



Latches/Flip-Flops

54LS373, 54LS374, 54S373, 54S374

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data present one setup time before the High-to-Low enable transition. The enable gate has hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When

$\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High impedance "off" state, which means they will neither drive nor load the bus.

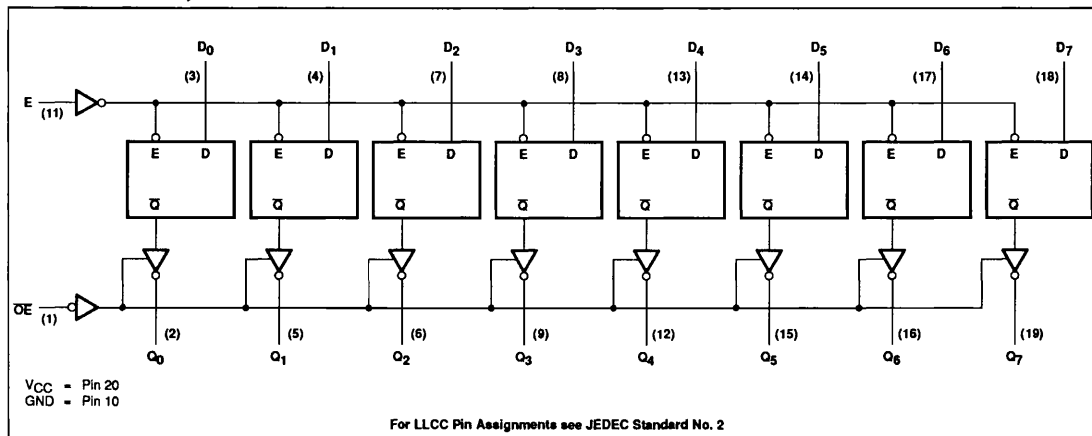
The '374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output. The

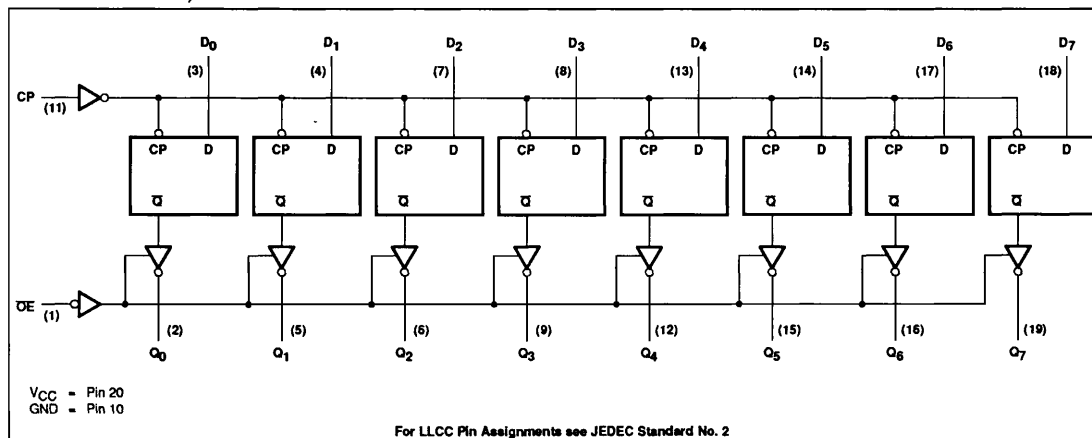
clock buffer has hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is Low, the data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, '373



LOGIC DIAGRAM, '374



Latches/Flip-Flops**54LS373, 54LS374, 54S373, 54S374****MODE SELECT — FUNCTION TABLE '373**

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	OE	E	D _n		Q ₀ - Q ₇
Enable and read register	L L	H H	L H	L H	L H
Latch and read register	L L	L L	L h	L H	L H
Latch register and disable outputs	H H	L L	L h	L H	(Z) (Z)

MODE SELECT — FUNCTION TABLE '374

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	OE	CP	D _n		Q ₀ - Q ₇
Load and read register	L L	↑ ↑	L h	L H	L H
Load register and disable outputs	H H	↑ ↑	L h	L H	(Z) (Z)

H = High voltage level

h = High voltage level one setup time prior to the Low-to-High clock transition or High-to-Low OE transition

L = Low voltage level

X = Don't care

l = Low voltage level one setup time prior to Low-to-High clock transition or High-to-Low OE transition

(Z) = High impedance "off" state

↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54LS	54S	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _I	Input voltage range	-0.5 to +7.0	-0.5 to +7.0	V
I _I	Input current range	-30 to +1	-30 to +5	mA
V _O	Voltage applied to output in High output state range	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			2.0			V
V _{IL}	Low-level input voltage			+0.7			+0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	High-level output current			-1.0			-2.0	mA
I _{OL}	Low-level output current			12			20	mA
T _A	Operating free-air temperature range	-55		+125	-55		+125	°C

Latches/Flip-Flops**54LS373, 54LS374, 54S373, 54S374****DC ELECTRICAL CHARACTERISTICS** (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹		54LS373, 374			54S373, 374			UNIT
				Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH}	High-level output voltage	V _{CC} = Min, V _{IH} = Min, V _{IL} = Max, I _{OH} = Max		2.4	3.1		2.4	3.1		V
V _{OL}	Low-level output voltage	V _{CC} = Min, V _{IH} = Min, V _{IL} = Max, I _{OL} = Max			0.25	0.4			0.5	V
V _{IK}	Input clamp voltage	V _{CC} = Min, I _I = I _{IK}				-1.5			-1.2	V
I _{ZH}	Off-state output current, High-level voltage applied	V _{CC} = Max, V _{IH} = Min	V _O = 2.7V			20				μA
			V _O = 2.4V					50	μA	
I _{ZL}	Off-state output current, Low-level voltage applied	V _{CC} = Max, V _{IH} = Min	V _O = 0.4V			-20				μA
			V _O = 0.5V					-50	μA	
I _{IH2}	Input current at maximum input voltage	V _{CC} = Max	V _I = 7.0V			0.1				mA
			V _I = 5.5V					1.0	mA	
I _{IH1}	High-level input current	V _{CC} = Max, V _I = 2.7V				20			50	μA
I _{IL}	Low level input current	V _{CC} = Max	V _I = 0.4V			-400				μA
			V _I = 0.5V					0.25	mA	
I _{OS}	Short-circuit output current ³	V _{CC} = Max		-30		-130	-40		-100	mA
I _{CC}	Supply current (total)	V _{CC} = Max	I _{CCZ} OE ≥4.0V 'LS373		24	40				mA
			I _{CCL} OE = 0V 'S373					105	160	mA
			I _{CCZ} OE ≥4.0V 'LS374		27	40				mA
			I _{CCL} All inputs grounded 'S374					102	140	mA
			I _{CCZ} CP, OE ≥4.0V 'S374 D inputs = GND						131	180

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54S373, 374		UNIT
			C _L = 15pF		
			Min	Max	
f _{MAX}	Maximum clock frequency	Waveform 6, '374	75		MHz
t _{PLH} t _{PHL}	Propagation delay Latch enable to output	Waveform 1, '373		14 18	ns ns
t _{PLH} t _{PHL}	Propagation delay Data to output	Waveform 4, '373		12 12	ns ns
t _{PLH} t _{PHL}	Propagation delay Clock to output	Waveform 6, '374		15 17	ns ns
t _{PZH}	Enable time to High level	Waveform 2		15	ns
t _{PZL}	Enable time to Low level	Waveform 3, '373, '374		18 18	ns ns
t _{PHZ}	Disable time from High level	Waveform 2, C _L = 5pF ⁴		9	ns
t _{PLZ}	Disable time from Low level	Waveform 3, C _L = 5pF ⁴		12	ns
t _{PHZ}	Disable time from High level	Waveform 2, C _L = 50pF		14	ns
t _{PLZ}	Disable time from Low level	Waveform 3, C _L = 50pF		13.5	ns

Latches/Flip-Flops**54LS373, 54LS374, 54S373, 54S374****AC ELECTRICAL CHARACTERISTICS** $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	54LS373, 374		54S373, 374 ⁵		UNIT
			C _L = 50pF		C _L = 50pF		
			Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency	Waveform 6, '374	35		75		MHz
t _{PLH} t _{PHL}	Propagation delay Latch enable to output	Waveform 1, '373		30 30		16.5 20.5	ns ns
t _{PLH} t _{PHL}	Propagation delay Data to output	Waveform 4, '373		18 18		14.5 14.5	ns ns
t _{PLH} t _{PHL}	Propagation delay Clock to output	Waveform 6, '374		28 28		17.5 19.5	ns ns
t _{PZH}	Enable time to High level	Waveform 2		28		17.5	ns
t _{PZL}	Enable time to Low level	Waveform 3, '373, '374		36 28		20.5 20.5	ns ns
t _{PHZ}	Disable time from High level	Waveform 2, C _L = 5pF ⁴		20		9	ns
t _{PLZ}	Disable time from Low level	Waveform 3, C _L = 5pF ⁴		25		12	ns
t _{PHZ}	Disable time from High level	Waveform 2, C _L = 50pF		36		14	ns
t _{PLZ}	Disable time from Low level	Waveform 3, C _L = 50pF		27		13.5	ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
$t_{\text{W(H)}}$ $t_{\text{W(L)}}$	Latch enable pulse width	Waveform 1, '373	15 15		6 7.3		ns ns
t_s	Setup time, data to latch enable	Waveform 5, '373	5		0		ns
t_h	Hold time, data to latch enable	Waveform 5, '373	20		10		ns
$t_{\text{W(H)}}$ $t_{\text{W(L)}}$	Clock pulse width	Waveform 6, '374	15 15		6 7.3		ns ns
t_s	Setup time, data to clock	Waveform 7, '374	20		5		ns
t_h	Hold time, data to clock	Waveform 7, '374	0		2		ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55^\circ\text{C}$ and $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V}^5$

SYMBOL	PARAMETER	TEST CONDITIONS	54LS373, 374		54S373, 374 ⁵		UNIT
			C _L = 50pF		C _L = 50pF		
			Min	Max	Min	Max	
t _{MAX}	Maximum clock frequency	Waveform 6, '374	26		75		MHz
t _{PLH} t _{PHL}	Propagation delay Latch enable to output	Waveform 1, '373		39 39		21 27	ns ns
t _{PLH} t _{PHL}	Propagation delay Data to output	Waveform 4, '373		23 23		16 16	ns ns
t _{PLH} t _{PHL}	Propagation delay Clock to output	Waveform 6, '374		36 36		23 25	ns ns
t _{PZH}	Enable time to High level	Waveform 2		36		23	ns
t _{PZL}	Enable time to Low level	Waveform 3, '373, '374		47 36		27 27	ns ns
t _{PHZ}	Disable time from High level	Waveform 2, C _L = 5pF ⁴		25		12	ns
t _{PLZ}	Disable time from Low level	Waveform 3, C _L = 5pF ⁴		33		16	ns
t _{PHZ}	Disable time from High level	Waveform 2, C _L = 50pF		47		18.5	ns
t _{PLZ}	Disable time from Low level	Waveform 3, C _L = 50pF		35		18	ns

Latches/Flip-Flops**54LS373, 54LS374, 54S373, 54S374****AC SETUP REQUIREMENTS** $T_A = -55^\circ\text{C}$ and $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V}^5$

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
$t_{W(H)}$ $t_{W(L)}$	Latch enable pulse width	Waveform 1, '373	15 15		6 7.3		ns ns
t_s	Setup time, data to latch enable	Waveform 5, '373	5		0		ns
t_h	Hold time, data to latch enable	Waveform 5, '373	20		15		ns
$t_{W(H)}$ $t_{W(L)}$	Clock pulse width	Waveform 6, '374	15 15		6 7.3		ns ns
t_s	Setup time, data to clock	Waveform 7, '374	20		5		ns
t_h	Hold time, data to clock	Waveform 7, '374	5		2		ns

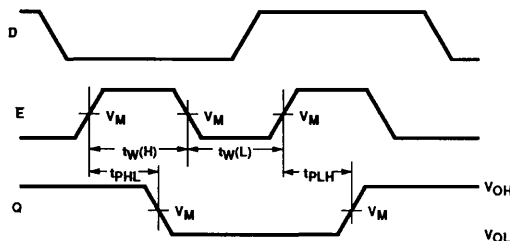
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Guaranteed by the 50pF limits, but not tested.
5. These parameters are guaranteed, but not tested.

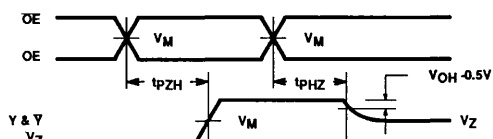
Latches/Flip-Flops

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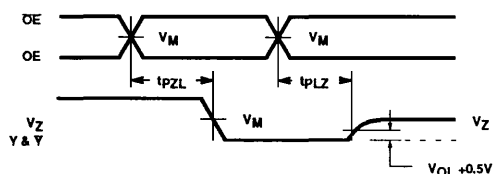
AC WAVEFORMS



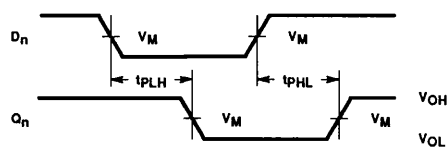
Waveform 1. Latch Enable to Output Delays and Latch Enable Pulse Width



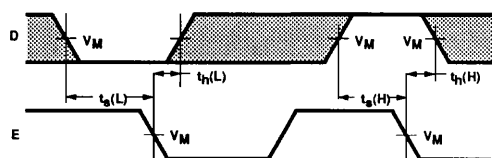
Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



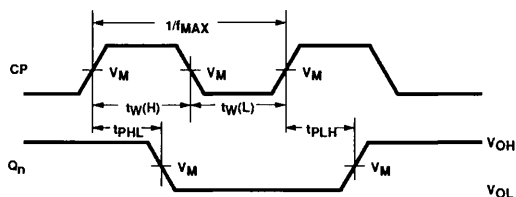
Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level



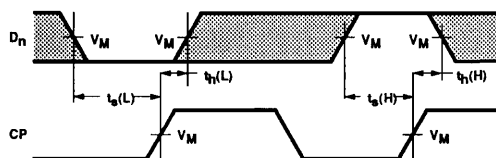
Waveform 4. Propagation Delay Data to Q Outputs



Waveform 5. Data Setup and Hold Times



Waveform 6. Clock to Output Delays and Pulse Width



Waveform 7. Data Setup and Hold Times

FAMILY	V _M	V _{MZL}	V _{MZH}	V _Z
54LSXXX	1.3V	0.7V	1.9V	1.45V
54SXXX	1.5V	0.7V	2.0V	1.65V

Latches/Flip-Flops

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TEST CIRCUIT AND WAVEFORM

