Octal inverting buffer, (3-State)
Octal buffer, (3-State)

54F240
54F241

FEATURES

- 3-state buffer outputs sink 48mA and source 12mA
- Octal bus interface

DESCRIPTION

The 54F240 and 54F241 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 48mA and sourcing up to 12mA, producing very good capacitive drive characteristics. The device features two output enables, ($\overline{OE}$), each controlling four of the 3-state outputs.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
20-Pin Ceramic DIP	54F240/BRA, 54F241/BRA	GDIP1-T20 GDIP1-T20
20-Pin Ceramic Flat Pack	54F240/BSA, 54F241/BSA	GDFP2-F20 GDFP2-F20
20-Pin Ceramic LLCC	54F240/B2A, 54F241/B2A	CQCC2-N20 CQCC2-N20

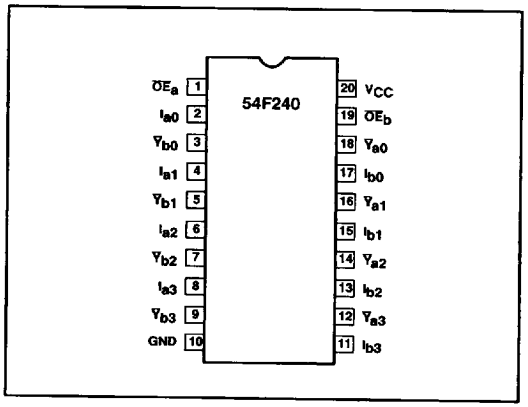
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

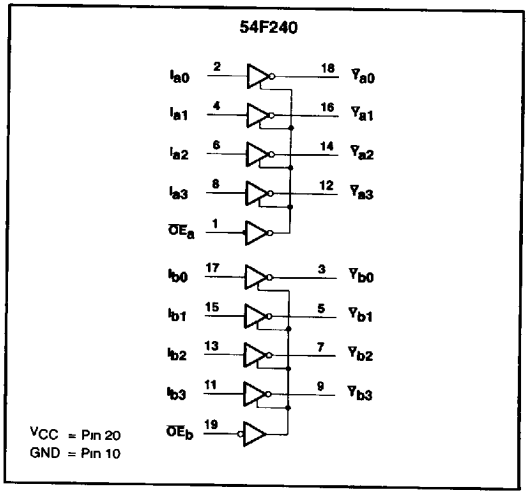
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{aN} - I_{bN}	Data inputs (54F240)	1.0/1.67	20µA/1.0mA
I_{aN} - I_{bN}	Data inputs (54F241)	1.0/2.67	20µA/1.6mA
$\overline{OE}_a$, $\overline{OE}_b$	Output Enable inputs (Active High)	1.0/1.67	20µA/1.0mA
OE_b	3-State Output Enable input (Active Low)	1.0/1.67	20µA/1.0mA
$\overline{Y}_{an}$, $\overline{Y}_{bn}$	Data outputs (54F240)	600/80	12mA/48mA
Y_{an}, Y_{bn}	Data outputs (54F241)	600/80	12mA/48mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

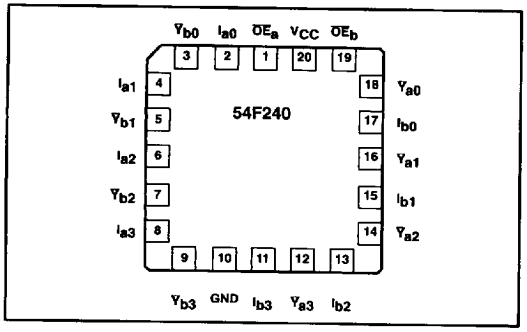
PIN CONFIGURATION



LOGIC SYMBOL



LLCC LEAD CONFIGURATION



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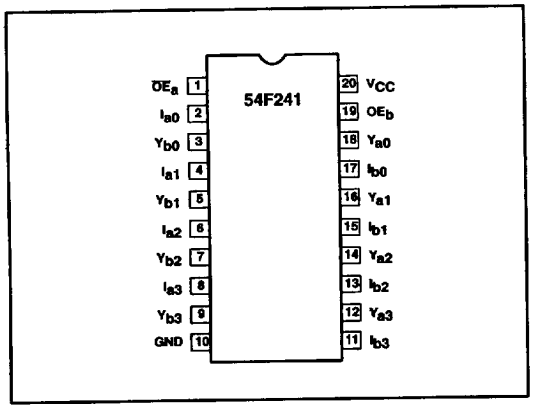
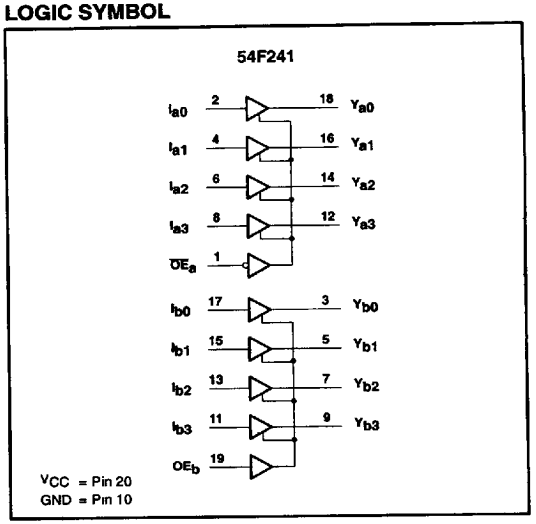
54F240
54F241

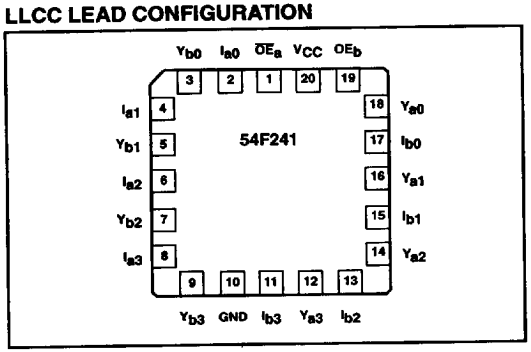
PIN CONFIGURATION



LOGIC SYMBOL



LLCC LEAD CONFIGURATION



FUNCTION TABLE, 54F240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "OFF" state

FUNCTION TABLE, 54F241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "OFF" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	96	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH1}	High-level output current			-1	mA
I_{OH2}	High-level output current			-3	mA
I_{OH3}	High-level output current			-12	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[5]		LIMITS			UNIT
					Min	Typ[6]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH1} = -1mA	2.5			V
				I_{OH2} = -3mA	2.4			V
				I_{OH3} = -12mA	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				0.1	mA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current	'F240 All inputs 'F241 $\overline{OE}_a$, $\overline{OE}_b$	V_{CC} = Max, V_I = 0.5V			-0.6	-1.0	mA
		'F241 I_{an}, I_{bn}				-0.6	-1.6	mA
I_{OZH}	Off-state output current		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			2	50	µA
I_{OZL}	Off-state output current		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V			-2	-50	µA
I_{OS}	Short-circuit output current[7]		V_{CC} = Max, V_O = 0.0V		-100	-150	-225	mA
I_{CC}	Supply current[8] (total)	I_{CCH}	V_{CC} = Max 54F240			12	29	mA
		I_{CCL}				50	75	mA
		I_{CCZ}				35	63	mA
		I_{CCH}	V_{CC} = Max 54F241			40	60	mA
		I_{CCL}				60	90	mA
		I_{CCZ}				60	90	mA

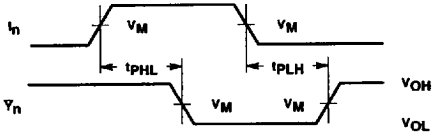
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output (54F240)	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 1.5	9.0 5.5	ns ns
t_{PZH} t_{PZL}	Output Enable time (54F240)	Waveform 3 Waveform 4	3.0 4.5	5.0 6.5	7.5 8.5	2.0 4.0	9.5 10.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time (54F240)	Waveform 3 Waveform 4	3.0 3.0	5.5 5.0	7.0 7.0	2.5 2.5	8.0 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output (54F241)	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.5 2.5	6.5 7.0	ns ns
t_{PZH} t_{PZL}	Output Enable time (54F241)	Waveform 3 Waveform 4	2.0 2.0	4.0 5.0	5.7 7.0	2.0 2.0	7.0 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time (54F241)	Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.5	ns ns

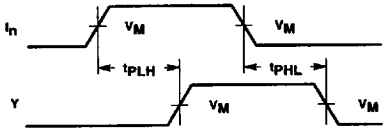
NOTES:

5. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and the functional table for the applicable operating mode.
6. All typical values are at V_{CC} = 5V, T_A = 25°C.
7. Not more than one output should be shorted at a time.
8. I_{CC} is measured with outputs open.

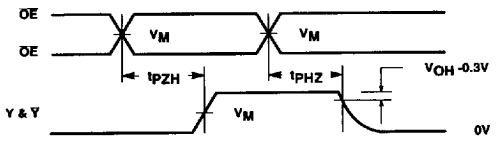
AC WAVEFORMS



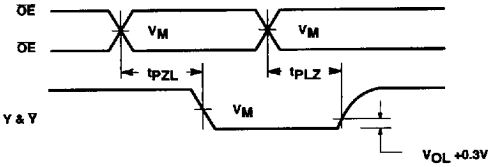
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

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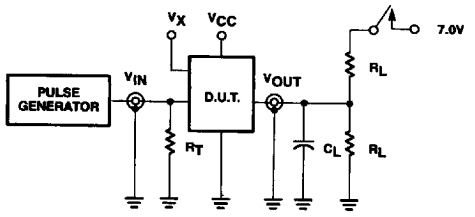
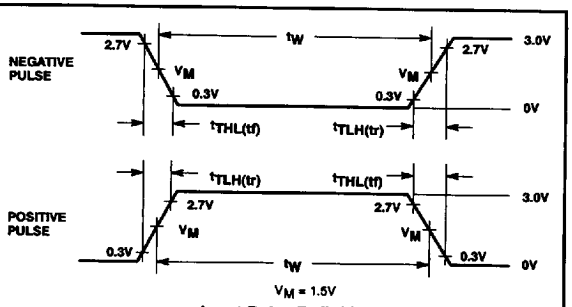
TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed
	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.