Quad 2-input data selector/multiplexer (54F157A non-inverted, 54F158A inverted)

54F157A, 54F158A

DESCRIPTION

The 54F157A is a high-speed quad 2-input multiplexer which selects 4 bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active Low. When $\overline{E}$ is High all of the outputs (Y) are forced Low regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 54F157A. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. Logic equations for the outputs are shown below:

$$Ya = \overline{E} \cdot (I1a \cdot S + I0a \cdot \overline{S})$$
$$Yb = \overline{E} \cdot (I1b \cdot S + I0b \cdot \overline{S})$$
$$Yc = \overline{E} \cdot (I1c \cdot S + I0c \cdot \overline{S})$$
$$Yd = \overline{E} \cdot (I1d \cdot S + I0d \cdot \overline{S})$$

The 54F158A is similar but has inverting outputs:

$$\overline{Ya} = \overline{E} \cdot (I1a \cdot S + I0a \cdot \overline{S})$$
$$\overline{Yb} = \overline{E} \cdot (I1b \cdot S + I0b \cdot \overline{S})$$
$$\overline{Yc} = \overline{E} \cdot (I1c \cdot S + I0c \cdot \overline{S})$$
$$\overline{Yd} = \overline{E} \cdot (I1d \cdot S + I0d \cdot \overline{S})$$

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
16-Pin Ceramic DIP	54F157A/BEA, 54F158A/BEA	GDIP1-T16
16-Pin Ceramic Flat Pack	54F157A/BFA, 54F158A/BFA	GDFP2-F16
20-Pin Ceramic LLCC	54F157A/B2A, 54F158A/B2A	CQCC-N20

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

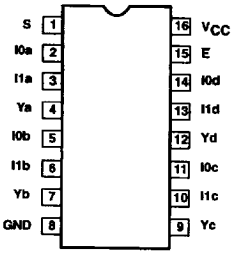
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
All	Inputs	1.0/1.0	20µA/0.6mA
Ya - Yd, $\overline{Ya}$ - $\overline{Yd}$	Outputs	50/33	1.0mA/20mA

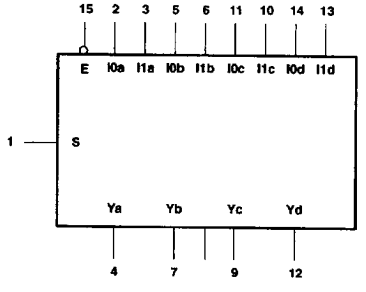
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

54F157A



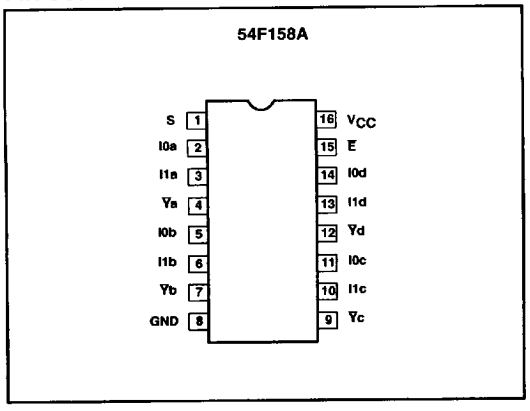
54F157A



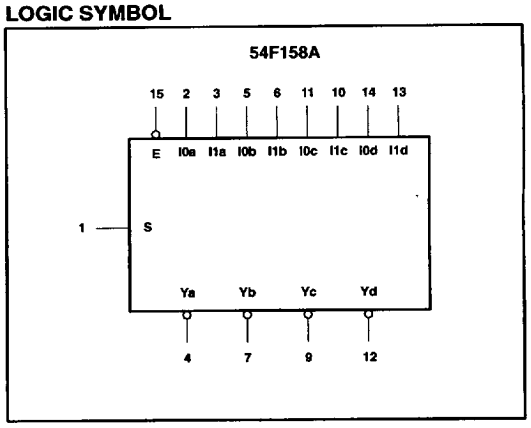
Quad 2-input data selector/multiplexer (54F157A non-inverted, 54F158A inverted)

54F157A, 54F158A

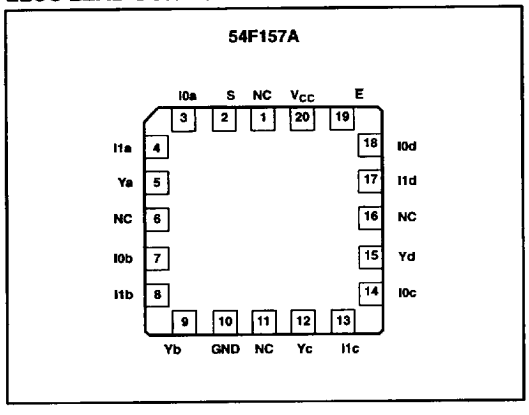
PIN CONFIGURATION



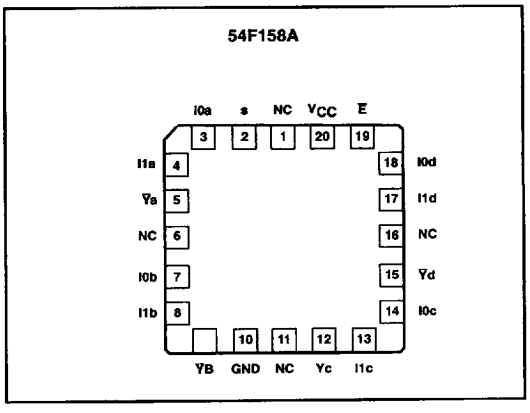
LOGIC SYMBOL



LLCC LEAD CONFIGURATION



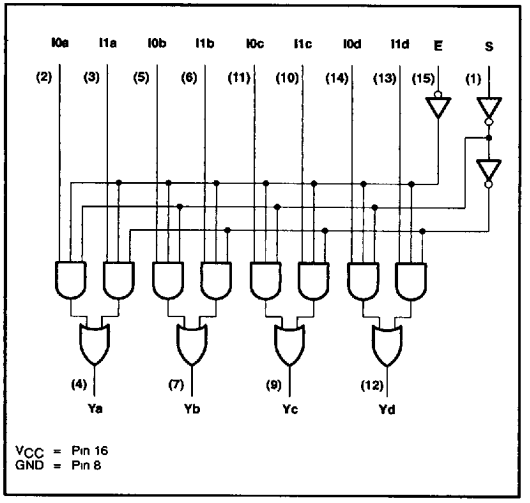
LLCC LEAD CONFIGURATION



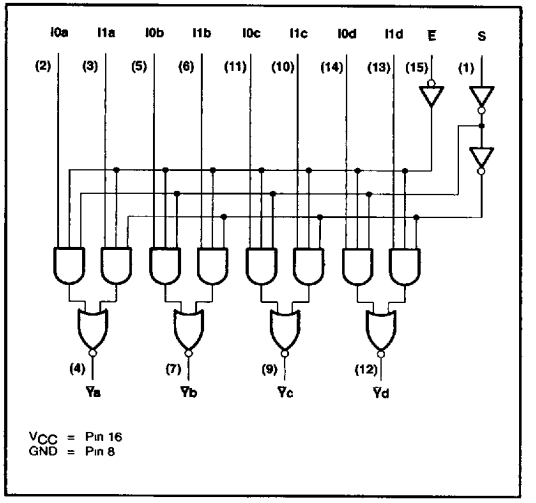
Quad 2-input data selector/multiplexer (54F157A non-inverted, 54F158A inverted)

54F157A, 54F158A

LOGIC DIAGRAM 54F157A



LOGIC DIAGRAM, 54F158A



FUNCTION TABLE, 54F157A

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE, 54F158A

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

Quad 2-input data selector/multiplexer (54F157A non-inverted, 54F158A inverted)

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[4]	LIMITS			UNIT
				Min	Typ[5]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V		5	100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[6]		V_{CC} = Max, V_O = 0.0V	-60	-80	-150	mA
I_{CC}	Supply current[7] (total)	'F157A	V_{CC} = Max		15.0	23.0	mA
		'F158A			10.0	15.0	mA

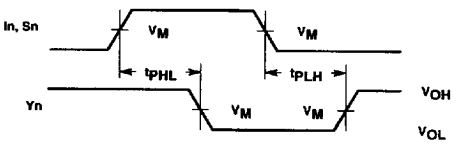
NOTES:

4. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
5. All typical values are at V_{CC} = 5V, T_A = 25°C.
6. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

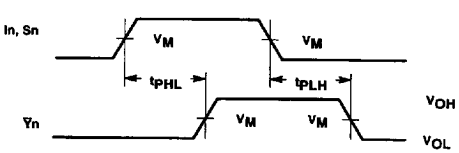
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	'F157A	Waveform 2	3.5 2.5	4.5 3.5	6.5 5.0	2.5 1.5	8.0 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output		Waveform 1	5.0 4.0	7.5 5.0	9.0 6.5	5.0 3.5	12.5 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output		Waveform 2	5.5 4.5	7.5 6.0	10.0 7.5	5.0 4.0	12.0 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	'F158A	Waveform 3	3.0 1.5	4.0 2.5	6.0 4.0	2.5 1.0	9.0 5.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output		Waveform 4	4.0 5.0	5.5 6.0	7.0 7.5	4.0 5.0	8.0 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output		Waveform 3	4.5 4.0	6.5 5.5	8.5 7.5	4.0 3.5	12.0 10.0	ns ns

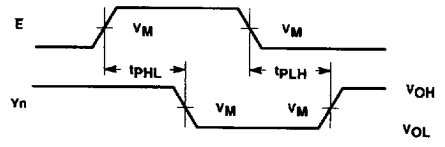
AC WAVEFORMS



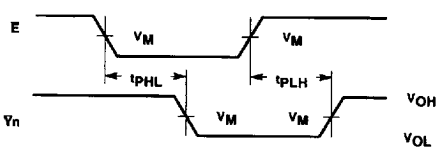
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



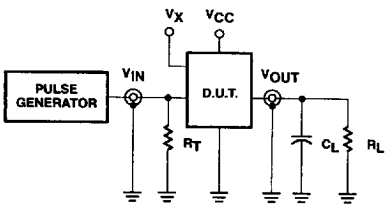
Waveform 3. For Inverting Outputs



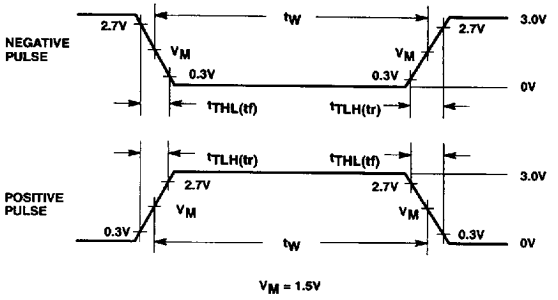
Waveform 4. For Non-Inverting Outputs

NOTE: For all waveforms $V_M = 1.5V$

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns