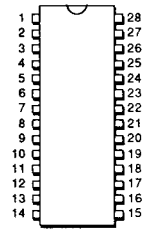
FEATURES

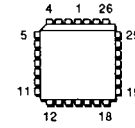
- ☐ Direct interface to SC11004, SC11014 and SC11015 single chip modems
- ☐ Built-in UART
- ☐ Complete "AT" command set in firmware
- ☐ Direct IBM PC bus interface
- ☐ 28-pin DIP or PLCC package

28-PIN DIP PACKAGE



SC11017CN

28-PIN PLCC PACKAGE

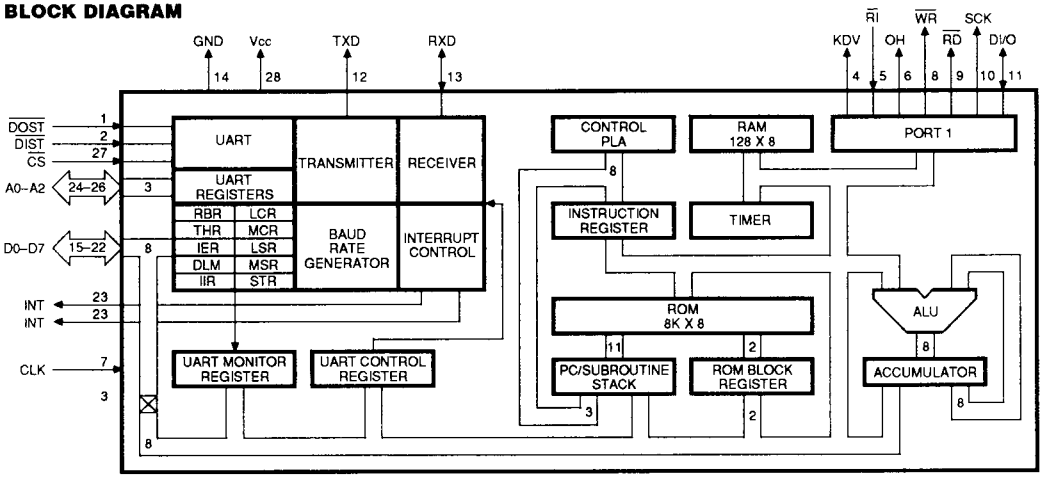


SC11017CV

GENERAL DESCRIPTION

The SC11017 Modem Interface Controller is specifically designed to control Sierra's SC11004, SC11014 and SC11015 single chip, 300/1200 bit per second modems. Built with Sierra's advanced CMOS process, the SC11017 provides a highly cost effective solution for interfacing a modem IC to a system bus. When connected to the SC11004/14/15, with the addition of a data access arrangement (DAA), the SC11017 implements a Hayes-type smart modem for board level, integral modem applications. Because the SC11017 fully emulates the functionality of the 8250B UART with increased speed, and includes data bus transceivers, it can be directly interfaced to a computer's parallel data bus and in particular to the bus of the IBM PC, XT or AT. In particular the SC11017 incorporates IO channel ready control circuitry and provides a RDY signal to inject wait states into the PC thus allowing the SC11017 to work inside any high speed PC compatible computer. All of the popular communications software written for the PC will work with the chip set. Besides including the functionality of the 8250B UART, the SC11017 contains an 8 bit microprocessor, 8k by 8 bytes of ROM and 128 by 8 bytes of RAM. For specific high volume applications, the control program can be modified by Sierra to include additional commands and functions.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES REFER TO PACKAGE PINS. NUMBERS ARE FOR BOTH DIP & PLCC

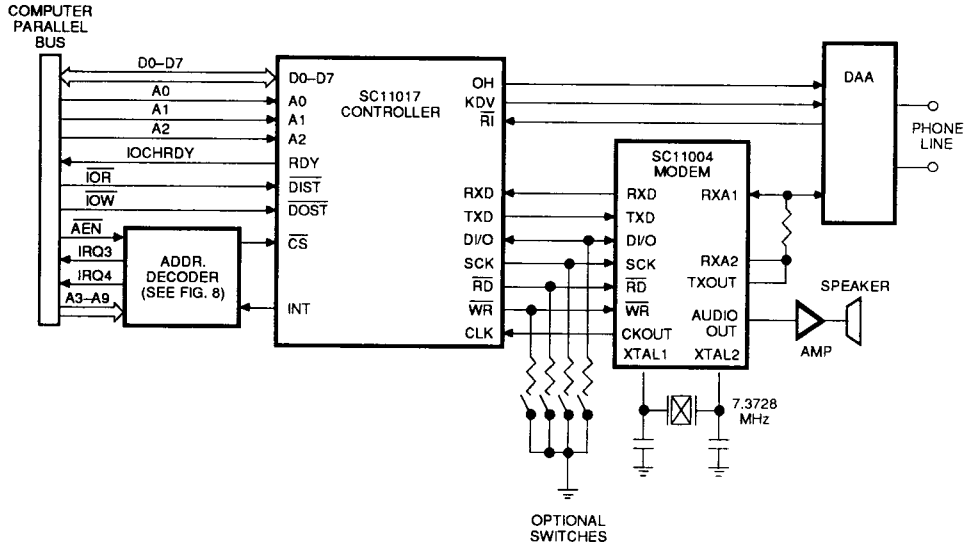


Figure 2. Integral Smart Modem Configuration for PC Bus Applications

PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	$\overline{DOST}$	I	The CPU can write data or control words into a selected register of the SC11017 when $\overline{DOST}$ is low and the chip is selected. Data is latched on the rising edge of the signal.
2	$\overline{DIST}$	I	The CPU can read data or status information from a selected register of the SC11017 when $\overline{DIST}$ is low and the chip is selected.
3	RDY	O	This **open drain output** to low to inject wait state into the computer. Following a self-timed delay (approximately 500 ns) wait state is released.
4	KDV	O	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. During a data call, the SC11017 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads.
5	$\overline{RI}$	I	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the On duration of the ring cycle. This is a Schmidt Trigger input, allowing for slow rising and falling signals on this pin.
6	OH	0	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the SC11017 pulses this output at a rate of 10 pulses per second with appropriate mark/space ratio depending on 212A or V.22 mode.
7	CLK	I	A 7.3728 MHz clock signal must be connected to this input. Normally, the CKOUT pin of the SC11004, SC11014 and SC11015 modem is connected to this pin. All internal timing is derived from this clock.
8	$\overline{WR}$	I/O	This pin is used to initiate writing of data to the SC11004, SC11014 and SC11015 modem. On power-up, it is an input for a brief time in which the SC11017 reads the carrier status switch connected to this pin. If the switch is closed to ground thru an 18 kΩ resistor, the SC11017 sets the Received Line Signal Detect (RLSD) bit in the Modem Status Register. If the switch is open or tied to V_{CC} thru 18 kΩ, the SC11017 resets this bit and writes the actual status of the carrier detector during a data call. However, NO switch is required, since an internal pullup sets the status during power-up to the default state (pullup to V_{CC}) which is to follow the remote modem's carrier.

Pin No.	Pin Name	I/O	Description
9	$\overline{RD}$	I/O	This pin is used to initiate reading of data from the SC11004, SC11014 and SC11015modem. On power-up, this pin is an input for a brief time in which the SC11017 reads the DTR status switch connected to this pin. If this switch is open or tied to V_{CC} thru 18 kΩ, the SC11017 reacts to the status of the DTR bit in the UART Modem Control Register. If the switch is closed to ground thru 18 kΩ, the SC11017 ignores the state of the DTR bit. When the switch is open, writing a 0 to the DTR bit in the Modem Control Register forces the SC11017 into the command state and when on line, causes it to hang up. However, NO switch is required, since an internal pullup to V_{CC} sets the status during power-up to the default state—to follow the DTR status.
10	SCK	I/O	The SC11017 supplies a shift clock on this pin to the SC11004, SC11014 and SC11015 modem for reading or writing data. On power-up, this pin is an input for a brief time in which the SC11017 reads the Bell/CCITT select switch connected to this pin. If this switch is open or tied to V_{CC} thru 18 kΩ, Bell protocol is selected. If this switch is closed to ground 18 kΩ, CCITT V.22 protocol is selected. However, NO switch is required, since an internal pullup sets the status during power-up to the default state—212A mode.
11	DI/O	I/O	The SC11017 shifts data serially out of this pin to SC11004, SC11014 and SC11015 during a write operation and shifts data serially into this pin during a read operation from the SC11004, SC11014 and SC11015. On power-up this pin is an input for a brief time in which the SC11017 reads the Make/Break ratio select switch connected to this pin for selecting the pulse dialing standard. With the switch open or tied to V_{CC} thru 18 kΩ, the Bell standard 39% Make, 61% Break is selected. With the switch closed to ground thru 18 kΩ, the CCITT standard 33% Make, 67% Break is selected. However, NO switch is required, since an internal pullup sets the status during power-up to the default state—Bell standard.
12	TXD	O	During a data call, after the connection is established, the SC11017 converts parallel data received from the computer bus and outputs it in a serial, asynchronous format to the SC11004, SC11014 and SC11015 modem for modulation. At all other times the SC11017 holds this output in the Mark (high) condition.
13	RXD	I	Demodulated data from the SC11004, SC11014 and SC11015 modem is received on this pin during a data call. A high level is considered Mark and a low level is a Space. The SC11017 converts the serial data into a parallel data byte and stores it in the Receiver Buffer Register (RBR). The Data Ready bit in the Line Status Register (LSR) is then set, and an appropriate interrupt indentification code is written in the Interrupt Identification Register (IIR) to signal to the computer, the reception of a new data byte.
14	GND	—	Ground reference (0 Volts).
15–22	D0–D7	I/O	This is the 8 bit data bus comprised of three state input/output lines. This bus provides bidirectional communication between the SC11017 and the CPU. Data, control words and status information are transferred via the D0–D7 data bus. Because on-chip high drive buffers are used, no external transceiver IC, such as the 74LS245, is needed between the computer bus and the SC11017.
23	INT	O	This output goes high whenever any one of the following interrupt types has an active condition and is enabled via the IER: Receiver Line Status Flag, Received Data Available, Transmitter Holding Register Empty and Modem Status. It is reset low upon the appropriate interrupt servicing. **The INT pin is forced to a Hi-Z state** when the OUT2 bit of the Modem Control Register (MCR) is low (power on state).
24–26	A0–A2	I	These three address inputs are used during read or write operation to select a UART register in the SC11017 as shown in Table 1. The Divisor Latch Access Bit (DLAB) must be set high by the system software to access the bit rate divisor latches as shown in Table 2.
27	$\overline{CS}$	I	The SC11017 is selected when this input is low. When high, the SC11017 forces the Data bus lines into a high impedance state.
28	V_{CC}	—	Positive supply (+5 Volts).

SPECIFICATIONS

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read only) (RBR)
0	0	0	0	Transmitter Holding (write only) (THR)
0	0	0	1	Interrupt Enable (IER)
X	0	1	0	Interrupt Identification (read only) (IIR)
X	0	1	1	Line Control (LCR)
X	1	0	0	Modem Control (MCR)
X	1	0	1	Line Status (LSR)
X	1	1	0	Modem Status (read only) (MSR)
X	1	1	1	Speed (STR)
1	0	0	0	Divisor Latch (LSB) (write only) (DLL)
1	0	0	1	Divisor Latch (MSB) (write only) (DLM)

Table 1. SC11017 UART Registers

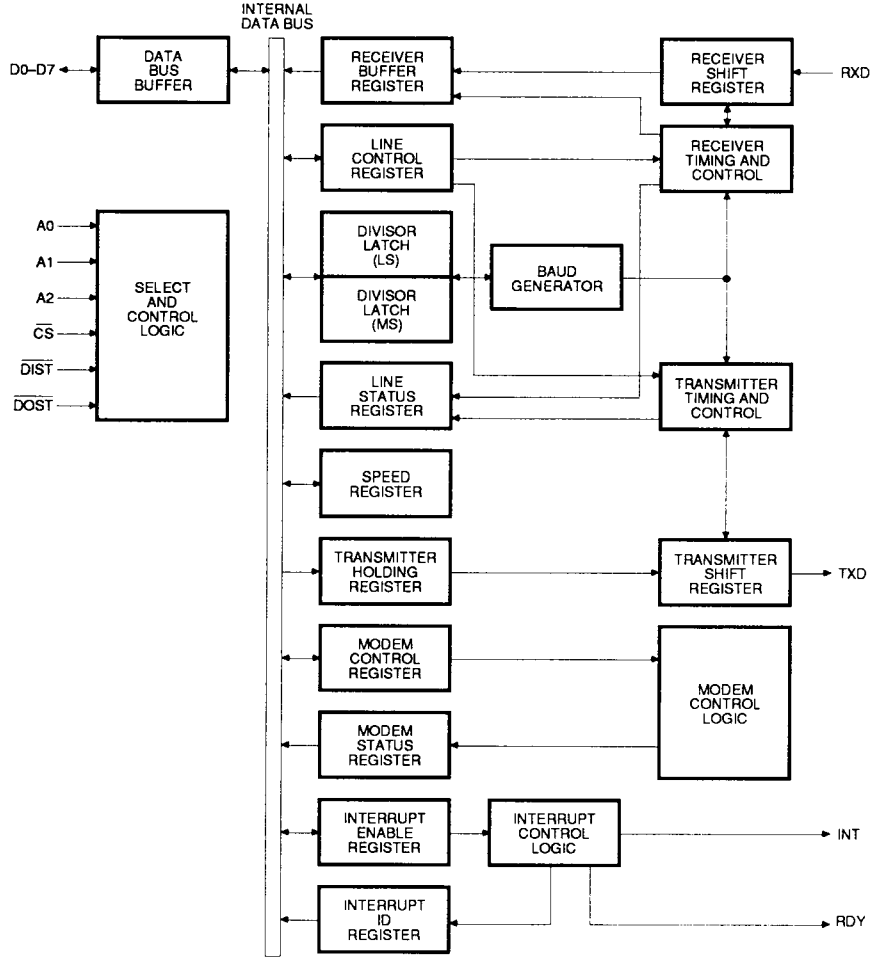


Figure 3. UART Block Diagram

Name	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
RBR	Data	Data	Data	Data	Data	Data	Data	Data
THR	Data	Data	Data	Data	Data	Data	Data	Data
IER	Receive Data Available Interrupt Enable	THRE Interrupt Enable	Receive Line Status Interrupt Enable	Modem Status Interrupt Enable	0	0	0	0
IIR	0 If Interrupt Pending	Interrupt ID Bit 0	Interrupt ID Bit 1	0	0	0	0	0
LCR	0 = 7 Bit Data 1 = 8 Bit Data	1	0 = 1 Stop Bit 1 = 2 Stop Bits	1 = Parity Enable	1 = Even Parity	1 = Stick Parity	1 = Set Break	DLAB
MCR	Data Terminal Ready	Request to Send	OUT1	OUT2 0 = INT Output to HI-Z	No Function	0	0	0
LSR	Data Ready	Overrun Error	Parity Error	Framing Error	Break Interrupt	THRE	TSRE	0
MSR	0	0	Trailing Edge Ring	Delta RLSD	1 (CTS)	1 (DSR)	Ring	RLSD
DLM	Data	Data	Data	Data	Data	Data	Data	Data
STR	Data	Data	Data	Data	Data	Data	Data	Data

Table 2. SC11017 UART Register Function Summary

Register	Range/Units	Description	Default
S0	0–255 rings	Ring to answer telephone on	0
S1	0–255 rings	Number of rings	0
S2	0–127 ASCII	Escape code character	43(+)
S3	0–127 ASCII	Character recognized as carriage return	13(CR)
S4	0–127 ASCII	Character recognized as line feed	10(LF)
S5	0–32, 127 ASCII	Character recognized as back space	8(BS)
S6	2–255 sec.	Wait time for dial tone	2
S7	1–255 sec.	Wait time for carrier	30
S8	0–255 sec.	Pause time (caused by comma)	2
S9	1–255 1/10 sec.	Carrier detect response time	6
S10	1–255 1/10 sec.	Delay between loss of carrier and hang up	7
S11	50–255 millisec.	Duration and spacing of Touch-Tones	70
S12	20–255 1/50 sec.	Escape code guard time	50
S13	bit mapped	UART status register	—
S14	bit mapped	Option register	—
S15	bit mapped	Flag register	—
S16	0,1,2,4	Test modes	0

Table 3. SC11017 S Registers (Software Registers) Used by AT Commands

Command	Desc. (Notes 1 and 2)
Prefix, Repeat and Escape Commands	
AT	Attention prefix: precedes all command lines except + + + (escape) and A/(repeat) commands
A/	Repeat last command line (A/ is not followed by carriage return)
+ + +	Escape code: go from on-line state to command state (one second pause before and after escape code entry; + + + is not followed by carriage return)
Dialing Commands	
D	Dial
P	Pulse*
T	Touch-Tone
,	Pause
!	Flash
/	Wait for 1/8 second
@	Wait for silence
W	Wait for second dial tone
;	Return to command state after dialing
R	Reverse mode (to call originate-only modem)

Command	Desc. (Notes 1 and 2)
Other Commands	
A	Answer call without waiting for ring
B/B0	CCITT V.22 mode (Note3)
B1	Bell 103 and 212A mode*
C/C0	Transmit carrier off
C1	Carrier on*
E/E0	Characters not echoed
E1	Characters echoed*
F/F0	Half duplex
F1	Full duplex*
H/H0	On hook (hang up)
H1	Off hook, line and auxiliary relay
H2	Off hook, line relay only
I/I0	Request product ID code (130)
I1	Firmware revision number
I2	Test internal memory
L/L1	Low speaker volume
L2	Medium speaker volume*
L3	High speaker volume
M/M0	Speaker always off
M1	Speaker on until carrier detected*
M2	Speaker always on

Command	Desc. (Notes 1 and 2)
Other Commands	
O	Go to on-line state
O1	Remote digital loopback off*
O2	Remote digital loopback request
Q/Q0	Result codes displayed*
Q1	Result codes not displayed
Sr?	Requests current value of register r
Sr=n	Sets register r to value of n
V/V0	Digit result codes
V1	Word result codes*
X/X0	Compatible with Hayes-type 300 modems*
X1	Result code CONNECT 1200 enabled
X2	Enables dial tone detection
X3	Enables busy signal detection
X4	Enables dial tone and busy signal detection
Y/Y0	Long space disconnect disabled*
Y1	Long space disconnect enabled
Z	Software reset: restores all default settings

Notes: 1. Default Modes are indicated by *.
2. Commands entered with null parameters assume 0-X is the same as X0.
3. When used with the SC11014 and SC11015 modem IC, which has CCITT V.21 as well as V.22 modes, when the ATB command is used, in the answer mode, the SC11017 will put the SC11014 and SC11015 in either the V.21 mode or the V.22 mode, depending on the response from the remote modem. In the originate mode, the SC11017 will sense if the baud rate is set at 300 or 1200 bits per second and will adjust the SC11014 and SC11015 accordingly.

Table 4. Command Summary

Digit Code	Word Code	Description
0	OK	Command executed
1	CONNECT	Connected at 300 or 1200 bps.
		Connected at 300 bps., if result of X1, X2, X3 or X4 command
2	RING	Ringing signal detected (Note 1)
3	NO CARRIER	Carrier signal not detected or lost
4	ERROR	Illegal command
		Error in command line
		Command line exceeds buffer (40 character, including punctuation)
		Invalid character format at 1200 bps.
5	CONNECT 1200	Connected at 1200 bps. Results from X1, X2, X3, or X4 commands only
6	NO DIALTONE	Dialtone not detected and subsequent commands not processed. Results from X2 or X4 commands only.
7	BUSY	Busy signal detected and subsequent commands not processed. Results from X3 or X4 commands only.
8	NO ANSWER	Silence not detected and subsequent commands not processed. Results from @ command only.

Note 1. When the SC11017 detects a ringing on the telephone line, it sends a RING result code. However, the SC11017 will answer the call only if it is in auto-answer mode or is given an A command.

Table 5. Result Codes

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC}	+ 6 V
Input Voltage	–0.6 V to V_{CC}+0.6
Storage temperature range	–65° to +150°C.
Maximum power dissipation @ 25°C.	500 mW
Lead temperature (soldering, 10 sec)	300°C.
Operating temperature range	0° to 70°C.

Note 1. Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Except for Operating temperature range, the device should not be operated at these limits. The Table of Electrical Characteristics provides actual operating limits.

DC ELECTRICAL CHARACTERISTICS

Param.	Description	Conditions	Min	Typ	Max	Units
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
I_{CC}	Operating Current	@ V_{CC} = 5 V		10.0		mA
V_{ih}	High Level Input Voltage	all pins except $\overline{RI}$	2.0			V
V_{il}	Low Level Input Voltage	all pins except $\overline{RI}$			0.8	V
V_t+	Positive hysterisis threshold	$\overline{RI}$ pin		2.5		V
V_t–	Negative hysterisis threshold	$\overline{RI}$ pin		1.8		V
V_{oh}	High Level Output Voltage	Digital signal pins D0 to D7 & INT @ I_{oh} = 6 mA All other output or I/O pins @ I_{oh} = 2 mA	V_{CC} –1.0 V_{CC} –1.0			V V
V_{ol}	Low Level Output Voltage	Digital signal pins D0 to D7 & INT @ I_{ol} = 6 mA All other output or I/O pins @ I_{ol} = 2 mA			0.4 0.4	V V
I_l	Leakage Current (Note 2)			±1.0		uA
f_{clk}	Clock frequency		7.3721	7.3728	7.3735	MHz

Note 2. This applies to all pins except TEST, which has an internal pull-down, and $\overline{WR}$, $\overline{RD}$, SCK, and the DI/O pins which have internal pullups.

AC ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{DIW}	$\overline{DIST}$ Strobe Width	1TTL Load	570		ns
t_{RC}	Read Cycle Delay	1TTL Load	300		ns
RC	Read Cycle = $t_{DIW} + t_{RC} + 20$ ns	1TTL Load	890		ns
t_{DDD}	Delay from $\overline{DIST}$ to Data	1TTL Load		570	ns
t_{HZ}	$\overline{DIST}$ to Floating Data Delay	1TTL Load	60		ns
t_{DOW}	$\overline{DOST}$ Strobe Width	1TTL Load	570		ns
t_{WC}	Write Cycle Delay	1TTL Load	300		ns
WC	Write Cycle = $t_{DOW} + t_{WC} + 20$ ns	1TTL Load	890		ns
t_{DS}	Data Setup Time	1TTL Load	60		ns
t_{DH}	Data Hold Time	1TTL Load	40		ns
t_{DIC}	$\overline{DIST}$ Delay from Select	1TTL Load	80		ns
t_{DOC}	$\overline{DOST}$ Delay from Select	1TTL Load	50		ns
t_{ACR}	Address and Chip Select Hold Time from $\overline{DIST}$	1TTL Load	10		ns
t_{ACW}	Address and Chip Select Hold Time from $\overline{DOST}$	1TTL Load	70		ns
Receiver					
t_{RINT}	Delay from $\overline{DIST}$ (Read RBR) to Reset Interrupt	100 pF Load		1	µs
Transmitter					
t_{HR}	Delay from $\overline{DOST}$ (Write THR) to Reset Interrupt	100 pF Load		1	µs
t_{IRS}	Delay from Initial INTR Reset to Transmit Start			1	Baud Cycle
t_{SI}	Delay from Initial Write to Interrupt			1	Baud Cycle
t_{SS}	Delay from Stop to Next Start			1	µs
t_{STI}	Delay from Stop to Interrupt (THRE)			1	Baud Cycle
t_{IR}	Delay from $\overline{DIST}$ (Read IIR) to Reset Interrupt (THRE)	100 pF Load		2.2	µs

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Power On Reset	All Bits Low
Interrupt Identification Register	Power On Reset	Bit 0 High; Bits 1–7 Low
Line Control Register	Writing into the LCR	Data
MODEM Control Register	Power On Reset	All Bits Low
Line Status Register	Power On Reset	Bits 0–4, 7 Low; Bits 5 and 6 High
Modem Status Register	Power Reset	Bits 0–3, 6–7 Low; Bits 4–5 High
Divisor Latch (high order bits)	Power On Reset	1200 BPS
TXD	Master Reset	High
INT	Power On Reset	Low (High-Z)

Table 6. Reset Control of Registers and Pinout Signals

AC ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = +5V ± 10%) 1 Clock cycle = 135 ns

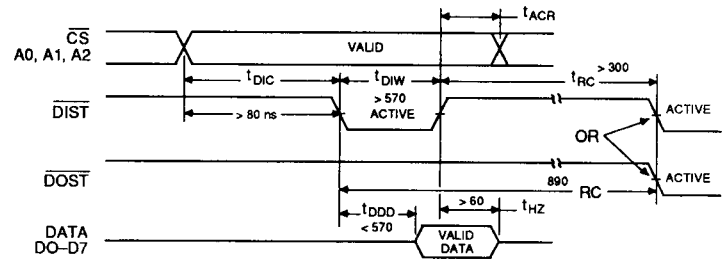


Figure 4. Read Cycle Timing

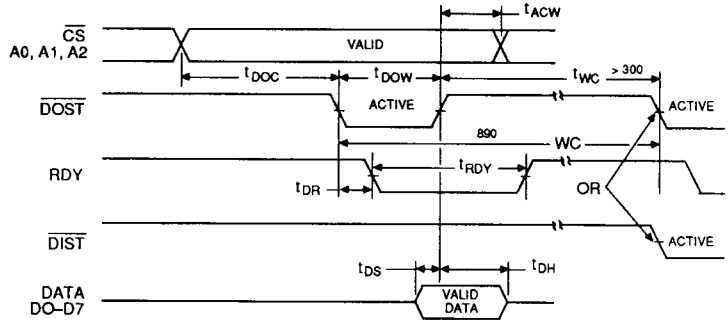


Figure 5. Write Cycle Timing

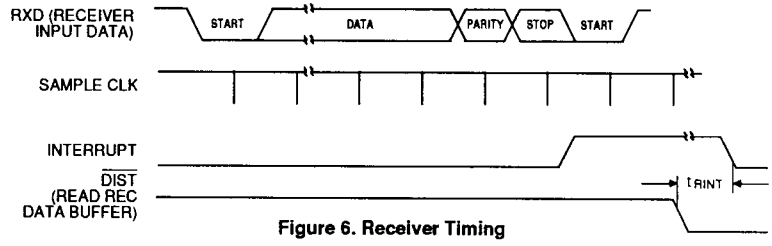


Figure 6. Receiver Timing

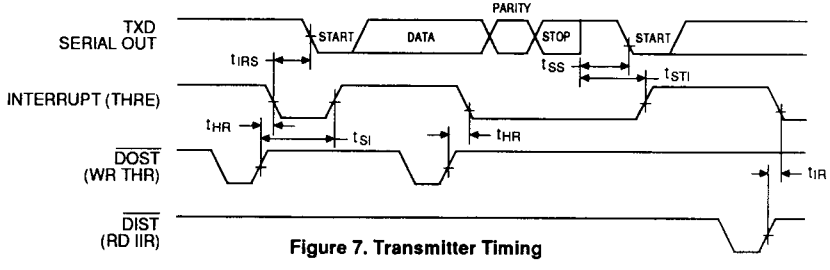


Figure 7. Transmitter Timing

UART REGISTERS

Line Control Register

This register controls the format of the asynchronous data communications.

Bits 0 and 1: Bit 1 is always high. Bit 0 specifies the number of bits in each transmitted or received serial character. The encoding of bit 0 is as follows:

Bit 1	Bit 0	Word Length
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1, when 7-bit word length with no Parity is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 0 is a logic 0 and bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed).

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is logic 1 and bit 5 is logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (TXD) is forced to the Spacing state (logic 0) and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Rate Generator

The SC11017's Baud Rate Generator can be programmed for one of six Baud rates. The desired speed is selected by writing into the Divisor Latch (DLM). On reset, the rate will be 1200 baud.

DLM (HEX Code)	Baud Rate
00	1200
01	300
03	150
04	110
06	75
09	50

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE bit is set to a logic 1 upon detection of parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time—the total time of Start bit + data bits + Parity + Stop bits.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the SC11017 is ready to accept a new character for transmission. In addition, this bit causes the SC11017 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register.

Bit 7: This bit is permanently set to logic 0.

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

UART REGISTERS

Interrupt Identification Register

The SC11017 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors. To provide minimum software overhead during data character transfers, the SC11017 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Table 7). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 7.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the SC11017 to separately activate the Interrupt (INT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Register. The contents of the Interrupt Enable Register are indicated in Table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to a logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

Interrupt Identification Register			Interrupt Set and Reset Functions			
B2	B1	B0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Table 7. Interrupt Control Functions

MODEM Control Register

This 8-bit register controls the interface with the MODEM. The contents of the MODEM Control Register are indicated in Table 2 and are described below.

Bit 0: This bit controls Data Terminal Ready (DTR) signal. If the external switch on the $\overline{RD}$ pin is set to V_{CC} thru an 18 kΩ resistor, setting the DTR low will force the SC11017 into the command state and, if on line, it will hang up.

Bit 1: This bit controls the Request to Send (RTS) signal. This signal is not used by the SC11017.

Bit 2: This bit controls the Output 1 (OUT 1) signal. This signal is not used by the SC11017.

Bit 3: This bit controls the Output 2 (OUT 2) signal. When OUT 2 is a 0, the interrupt output is in High-Z state.

Bit 4: Not used.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, two bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 2 and are described below.

Bit 0 and 1: These bits are always 0.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit indicates that the carrier detector has changed state.

Bit 4: This bit is always 1.

Bit 5: This bit is always 1.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

Bit 7: This bit is the Received Line Signal Detect (RLSD) signal.

Whenever bit 2 is set to logic 1, or bit 3 changes state, a MODEM Status Interrupt is generated if enabled.

Using SC11017's RDY Output

The basic concept behind the RDY circuit is to slow down the computer just during a read or a write cycle to SC11017 to insure (i) the setup time from $\overline{CS}$ to $\overline{DIST}$, $\overline{DOST}$ is met and (ii) the address/data hold time after DOST is satisfied.

SC11017 requires a minimum of 80 ns for (i) and 70 ns for (ii).

When a read/write cycle starts, the circuit applies ground to IOCHRDY signal (Bus pin A10) causing the computer to stretch read/write pulses. IOCHRDY is released when read/write timing requirements are satisfied.

APPLICATIONS

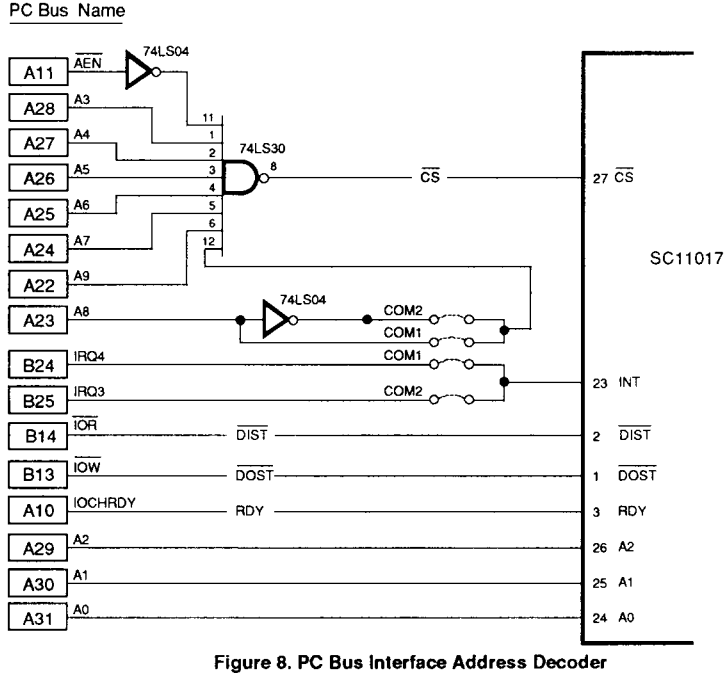


Figure 8. PC Bus Interface Address Decoder