SHARP

Integrated Circuits Group

LH28F640SPHT-PTLZ8
Flash Memory
64Mbit (4Mbitx16)

(Model Number: LHF64PZ8)

SHARP

To; _____

SPECIFICATIONS

Product Type _____ 6 4 M b i t F l a s h M e m o r y _____

L H 2 8 F 6 4 0 S P H T — P T L Z 8

Model No. _____ (L H F 6 4 P Z 8) _____

If you have any objections, please contact us before issuing purchasing order.

* This specifications contains <u>39</u> pages including the cover and appendix.
   Refer to LH28F640SP series Appendix (FUM03201).

CUSTOMERS ACCEPTANCE

DATE: _____

BY: _____

PRESENTED

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    - Office electronics
    - Instrumentation and measuring equipment
    - Machine tools
    - Audiovisual equipment
    - Home appliance
    - Communication equipment other than for trunk lines

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    - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
    - Mainframe computers
    - Traffic control systems
    - Gas leak detectors and automatic cutoff devices
    - Rescue and security equipment
    - Other safety devices and safety equipment, etc.

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    - Aerospace equipment
    - Communications equipment for trunk lines
    - Control equipment for the nuclear power industry
    - Medical equipment related to life support, etc.

  (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

- Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

LH28F640SPHT-PTLZ8
64Mbit (4Mbit×16/8Mbit×8)
Page Mode Flash MEMORY

■ 64-Mbit Density
  • Bit Organization ×8/×16

■ High Performance Page Mode Reads
  for Memory Array
  • 120/25ns 4-Word/ 8-Byte Page Mode

■ V_{CC}=2.7V-3.6V Operation
  • V_{CCQ} for Input/Output Power Supply Isolation
  • Automatic Power Savings Mode reduces I_{CCR}
    in Static Mode

■ OTP (One Time Program) Block
  • 4-Word/ 8-Byte Factory-Programmed Area
  • 3963-Word/ 7926-Byte User-Programmable Area

■ High Performance Program with Page Buffer
  • 16-Word/ 32-Byte Page Buffer
  • Page Buffer Program Time 12.5μs/byte (Typ.)

■ Operating Temperature -40°C to +85°C

■ Symmetrically-Blocked Architecture
  • Sixty-four 64-KWord/ 128-KByte Blocks

■ Enhanced Data Protection Features
  • Individual Block Lock
  • Absolute Protection with $V_{PEN} \leq V_{PENLK}$
  • Block Erase, (Page Buffer) Program Lockout during
    Power Transitions

■ Automated Erase/Program Algorithms
  • Program Time 210μs (Typ.)
  • Block Erase Time 1s (Typ.)

■ Cross-Compatible Command Support
  • Basic Command Set
  • Common Flash Interface (CFI)

■ Extended Cycling Capability
  • Minimum 100,000 Block Erase Cycles

■ 56-Lead TSOP (Normal Bend)

■ CMOS Process (P-type silicon substrate)

■ ETOX^{TM*} Flash Technology

■ Not designed or rated as radiation hardened

The product, which is Page Mode Flash memory, is a high density, low cost, nonvolatile read/write storage solution for a wide range of applications. The product can operate at V_{CC}=2.7V-3.6V and V_{PEN}=2.7V-3.6V

The product supports high performance page mode. It allows code execution directly from Flash, thus eliminating time consuming wait states.

Fast program capability is provided through the use of high speed Page Buffer Program.

The block locking scheme is available for memory array and this scheme provides maximum flexibility for safe nonvolatile code and data storage.

OTP (One Time Program) block provides an area to store security code and to protect its code.

* ETOX is a trademark of Intel Corporation.

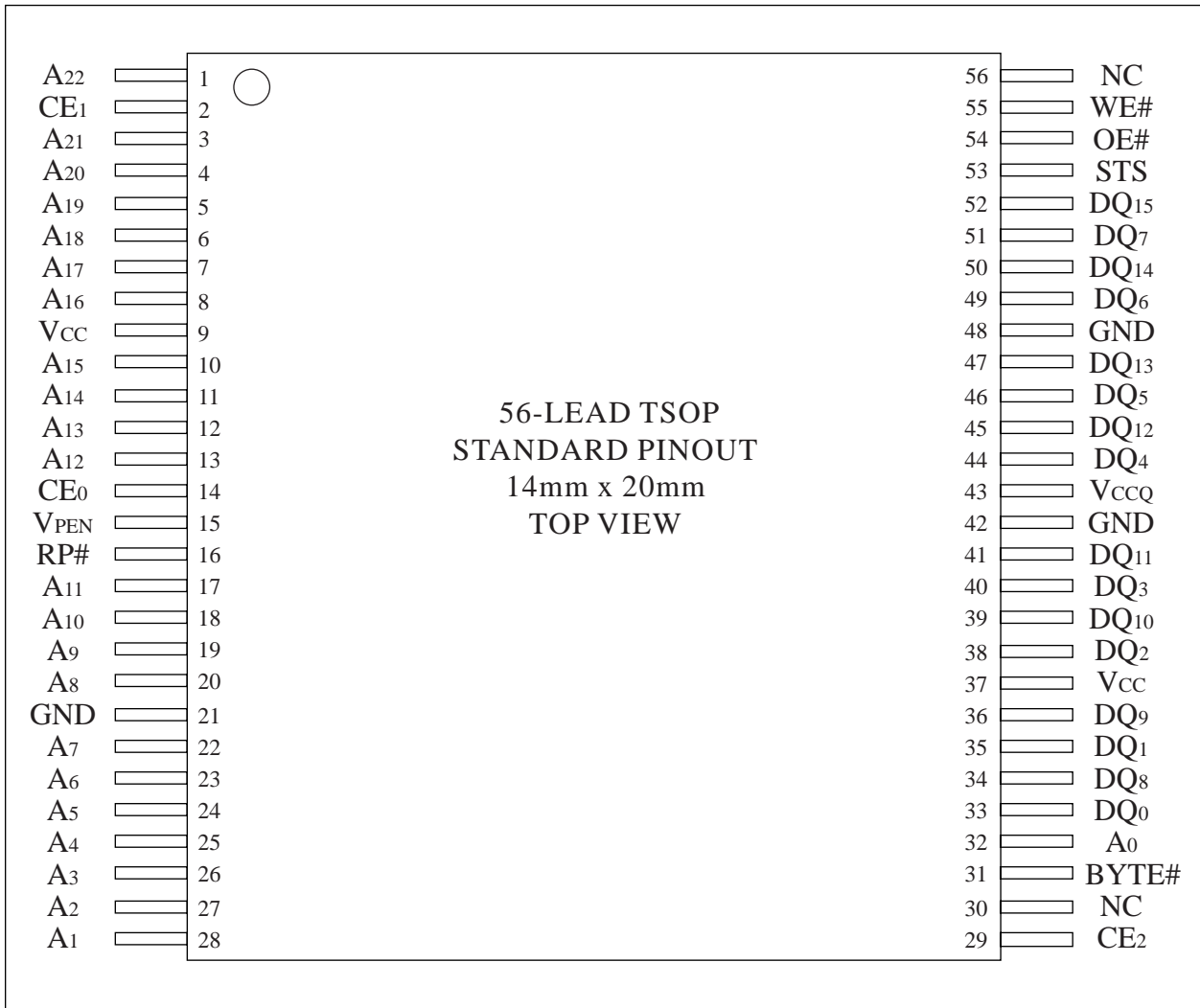|						
A_{22}	1			56		NC
CE_1	2			55		WE#
A_{21}	3			54		OE#
A_{20}	4			53		STS
A_{19}	5			52		DQ_{15}
A_{18}	6			51		DQ_7
A_{17}	7			50		DQ_{14}
A_{16}	8			49		DQ_6
V_{CC}	9			48		GND
A_{15}	10			47		DQ_{13}
A_{14}	11			46		DQ_5
A_{13}	12		56-LEAD TSOP	45		DQ_{12}
A_{12}	13		STANDARD PINOUT	44		DQ_4
CE_0	14		14mm x 20mm	43		V_{CCQ}
V_{PEN}	15		TOP VIEW	42		GND
RP#	16			41		DQ_{11}
A_{11}	17			40		DQ_3
A_{10}	18			39		DQ_{10}
A_9	19			38		DQ_2
A_8	20			37		V_{CC}
GND	21			36		DQ_9
A_7	22			35		DQ_1
A_6	23			34		DQ_8
A_5	24			33		DQ_0
A_4	25			32		A_0
A_3	26			31		BYTE#
A_2	27			30		NC
A_1	28			29		CE_2

Figure 1. 56-Lead TSOP (Normal Bend) Pinout

Table 1. Pin Descriptions

Symbol	Type	Name and Function
A_0	INPUT	ADDRESS INPUTS: Lowest address input in byte mode (BYTE#=V_{IL} : ×8 bit). Address is internally latched during an erase or a program cycle. This pin is not used in word mode (BYTE#=V_{IH} : ×16 bit)
A_{22}-A_1	INPUT	ADDRESS INPUTS: Inputs for addresses during read, erase and program operations. Addresses are internally latched during an erase or a program cycle.
DQ_{15}-DQ_0	INPUT/ OUTPUT	DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code, identifier code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle. DQ_{15}-DQ_8 pins are not used in byte mode (BYTE#=V_{IL} : ×8 bit).
CE_0, CE_1, CE_2	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. When the device is de-selected, power consumption reduces to standby levels. Refer to Table 2 to determine whether the device is selected or de-selected depending on the state of CE_0, CE_1 and CE_2.
RP#	INPUT	RESET: When low (V_{IL}), RP# resets internal automation and inhibits erase and program operations, which provides data protection. RP#-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. RP# must be low during power-up/down.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the first edge of CE_0, CE_1 or CE_2 that disables the device or the rising edge of WE# (whichever occurs first).
STS	OPEN DRAIN OUTPUT	STATUS: Indicates the status of the internal WSM (Write State Machine). When configured in level mode (default mode), STS acts as a RY/BY# pin (STS is V_{OL} when the WSM is executing internal erase or program algorithms). When configured in one of its pulse modes, STS can pulse to indicate erase/program completion. Refer to Table 9 for STS configuration.
BYTE#	INPUT	BYTE ENABLE: BYTE# V_{IL} places the device in byte mode (×8). In this mode, DQ_{15}-DQ_8 is floated (High Z) and A_0 is the lowest address input. BYTE# V_{IH} places the device in word mode (×16) and A_1 is the lowest address input.
V_{PEN}	INPUT	MONITORING POWER SUPPLY VOLTAGE: V_{PEN} is not used for power supply pin. With $V_{PEN} \le V_{PENLK}$, block erase, (page buffer) program, block lock configuration and OTP program cannot be executed and should not be attempted.
V_{CC}	SUPPLY	DEVICE POWER SUPPLY (2.7V-3.6V): With $V_{CC} \le V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (refer to DC Characteristics) produce spurious results and should not be attempted.
V_{CCQ}	SUPPLY	INPUT/OUTPUT POWER SUPPLY (2.7V-3.6V): Power supply for all input/output pins.
GND	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internally connected; it may be driven or floated.

Table 2. CE_0, CE_1, CE_2 Truth Table [1]

CE_2	CE_1	CE_0	Device
V_{IL}	V_{IL}	V_{IL}	Enabled
V_{IL}	V_{IL}	V_{IH}	Disabled
V_{IL}	V_{IH}	V_{IL}	Disabled
V_{IL}	V_{IH}	V_{IH}	Disabled
V_{IH}	V_{IL}	V_{IL}	Enabled
V_{IH}	V_{IL}	V_{IH}	Enabled
V_{IH}	V_{IH}	V_{IL}	Enabled
V_{IH}	V_{IH}	V_{IH}	Disabled

NOTE:
1. For single-chip applications, CE_1 and CE_2 can be connected to GND.

$[A_{22}-A_1]$		$[A_{22}-A_0]$
3FFFFF	64-Kword/128-Kbyte Block 63	7FFFFF
3F0000		7E0000
3EFFFF	64-Kword/128-Kbyte Block 62	7DFFFF
3E0000		7C0000
3DFFFF	64-Kword/128-Kbyte Block 61	7BFFFF
3D0000		7A0000
3CFFFF	64-Kword/128-Kbyte Block 60	79FFFF
3C0000		780000
3BFFFF	64-Kword/128-Kbyte Block 59	77FFFF
3B0000		760000
3AFFFF	64-Kword/128-Kbyte Block 58	75FFFF
3A0000		740000
39FFFF	64-Kword/128-Kbyte Block 57	73FFFF
390000		720000
38FFFF	64-Kword/128-Kbyte Block 56	71FFFF
380000		700000
37FFFF	64-Kword/128-Kbyte Block 55	6FFFFF
370000		6E0000
36FFFF	64-Kword/128-Kbyte Block 54	6DFFFF
360000		6C0000
35FFFF	64-Kword/128-Kbyte Block 53	6BFFFF
350000		6A0000
34FFFF	64-Kword/128-Kbyte Block 52	69FFFF
340000		680000
33FFFF	64-Kword/128-Kbyte Block 51	67FFFF
330000		660000
32FFFF	64-Kword/128-Kbyte Block 50	65FFFF
320000		640000
31FFFF	64-Kword/128-Kbyte Block 49	63FFFF
310000		620000
30FFFF	64-Kword/128-Kbyte Block 48	61FFFF
300000		600000
2FFFFF	64-Kword/128-Kbyte Block 47	5FFFFF
2F0000		5E0000
2EFFFF	64-Kword/128-Kbyte Block 46	5DFFFF
2E0000		5C0000
2DFFFF	64-Kword/128-Kbyte Block 45	5BFFFF
2D0000		5A0000
2CFFFF	64-Kword/128-Kbyte Block 44	59FFFF
2C0000		580000
2BFFFF	64-Kword/128-Kbyte Block 43	57FFFF
2B0000		560000
2AFFFF	64-Kword/128-Kbyte Block 42	55FFFF
2A0000		540000
29FFFF	64-Kword/128-Kbyte Block 41	53FFFF
290000		520000
28FFFF	64-Kword/128-Kbyte Block 40	51FFFF
280000		500000
27FFFF	64-Kword/128-Kbyte Block 39	4FFFFF
270000		4E0000
26FFFF	64-Kword/128-Kbyte Block 38	4DFFFF
260000		4C0000
25FFFF	64-Kword/128-Kbyte Block 37	4BFFFF
250000		4A0000
24FFFF	64-Kword/128-Kbyte Block 36	49FFFF
240000		480000
23FFFF	64-Kword/128-Kbyte Block 35	47FFFF
230000		460000
22FFFF	64-Kword/128-Kbyte Block 34	45FFFF
220000		440000
21FFFF	64-Kword/128-Kbyte Block 33	43FFFF
210000		420000
20FFFF	64-Kword/128-Kbyte Block 32	41FFFF
200000		400000

$[A_{22}-A_1]$		$[A_{22}-A_0]$
1FFFFF	64-Kword/128-Kbyte Block 31	3FFFFF
1F0000		3E0000
1EFFFF	64-Kword/128-Kbyte Block 30	3DFFFF
1E0000		3C0000
1DFFFF	64-Kword/128-Kbyte Block 29	3BFFFF
1D0000		3A0000
1CFFFF	64-Kword/128-Kbyte Block 28	39FFFF
1C0000		380000
1BFFFF	64-Kword/128-Kbyte Block 27	37FFFF
1B0000		360000
1AFFFF	64-Kword/128-Kbyte Block 26	35FFFF
1A0000		340000
19FFFF	64-Kword/128-Kbyte Block 25	33FFFF
190000		320000
18FFFF	64-Kword/128-Kbyte Block 24	31FFFF
180000		300000
17FFFF	64-Kword/128-Kbyte Block 23	2FFFFF
170000		2E0000
16FFFF	64-Kword/128-Kbyte Block 22	2DFFFF
160000		2C0000
15FFFF	64-Kword/128-Kbyte Block 21	2BFFFF
150000		2A0000
14FFFF	64-Kword/128-Kbyte Block 20	29FFFF
140000		280000
13FFFF	64-Kword/128-Kbyte Block 19	27FFFF
130000		260000
12FFFF	64-Kword/128-Kbyte Block 18	25FFFF
120000		240000
11FFFF	64-Kword/128-Kbyte Block 17	23FFFF
110000		220000
10FFFF	64-Kword/128-Kbyte Block 16	21FFFF
100000		200000
0FFFFF	64-Kword/128-Kbyte Block 15	1FFFFF
0F0000		1E0000
0EFFFF	64-Kword/128-Kbyte Block 14	1DFFFF
0E0000		1C0000
0DFFFF	64-Kword/128-Kbyte Block 13	1BFFFF
0D0000		1A0000
0CFFFF	64-Kword/128-Kbyte Block 12	19FFFF
0C0000		180000
0BFFFF	64-Kword/128-Kbyte Block 11	17FFFF
0B0000		160000
0AFFFF	64-Kword/128-Kbyte Block 10	15FFFF
0A0000		140000
09FFFF	64-Kword/128-Kbyte Block 9	13FFFF
090000		120000
08FFFF	64-Kword/128-Kbyte Block 8	11FFFF
080000		100000
07FFFF	64-Kword/128-Kbyte Block 7	0FFFFF
070000		0E0000
06FFFF	64-Kword/128-Kbyte Block 6	0DFFFF
060000		0C0000
05FFFF	64-Kword/128-Kbyte Block 5	0BFFFF
050000		0A0000
04FFFF	64-Kword/128-Kbyte Block 4	09FFFF
040000		080000
03FFFF	64-Kword/128-Kbyte Block 3	07FFFF
030000		060000
02FFFF	64-Kword/128-Kbyte Block 2	05FFFF
020000		040000
01FFFF	64-Kword/128-Kbyte Block 1	03FFFF
010000		020000
00FFFF	64-Kword/128-Kbyte Block 0	01FFFF
000000		000000

Figure 2. Memory Map

Table 3. Identifier Codes Address

	Code	Address [A_{22}-A_1] [1]	Data [DQ_7-DQ_0]	Notes
Manufacturer Code	Manufacturer Code	000000H	B0H	2
Device Code	Device Code	000001H	17H	2
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	$DQ_0 = 0$	3
	Block is Locked		$DQ_0 = 1$	3

NOTES:
1. The address A_0 don't care.
2. "00H" is presented on DQ_{15}-DQ_8 in word mode (BYTE#=V_{IH} : ×16 bit).
3. Block Address = The beginning location of a block address. DQ_{15}-DQ_1 are reserved for future implementation.

[A$_{22}$-A$_1$]		[A$_{22}$-A$_0$]
000FFFFH		001FFFFH
	Customer Programmable Area	
000085H		00010AH
000084H	Factory Programmed Area	000109H
000081H		000102H
000080H	Reserved for Future Implementation (DQ15-DQ2)	000100H

Customer Programmable Area Lock Bit (DQ$_1$)

Factory Programmed Area Lock Bit (DQ$_0$)
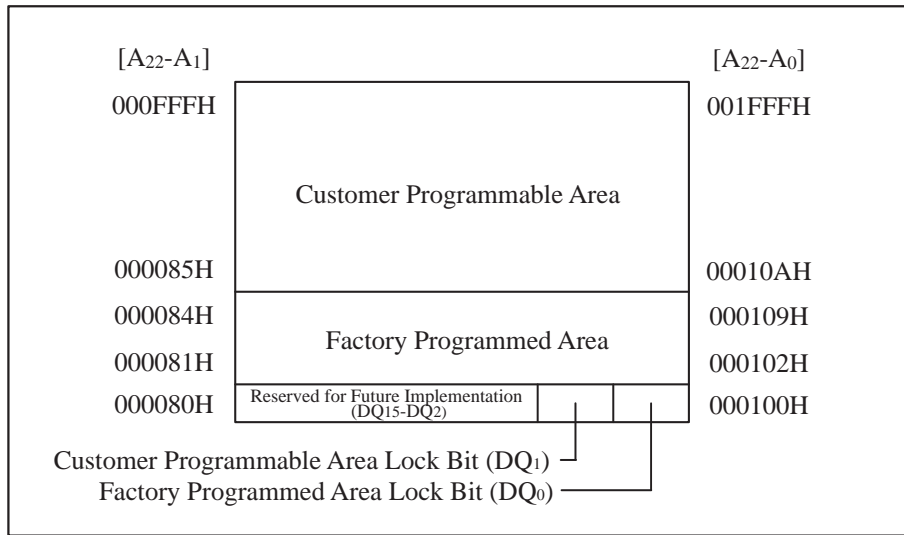
Figure 3. OTP Block Address Map
(The area not specified in the above figure cannot be used.)

Table 4. Bus Operation$^{(1, 2)}$

Mode	Notes	RP#	CE$_{0,1,2}$ $^{(3)}$	OE#	WE#	Address	V$_{PEN}$	DQ $^{(4)}$	STS $^{(10)}$
Read Array	8	V$_{IH}$	Enabled	V$_{IL}$	V$_{IH}$	X	X	D$_{OUT}$	X
Output Disable		V$_{IH}$	Enabled	V$_{IH}$	V$_{IH}$	X	X	High Z	X
Standby		V$_{IH}$	Disabled	X	X	X	X	High Z	X
Reset	5	V$_{IL}$	X	X	X	X	X	High Z	High Z
Read Identifier Codes/OTP	8	V$_{IH}$	Enabled	V$_{IL}$	V$_{IH}$	Refer to Table 3	X	Refer to Table 3	X
Read Query	8,9	V$_{IH}$	Enabled	V$_{IL}$	V$_{IH}$	See Appendix	X	See Appendix	X
Write	6,7,8	V$_{IH}$	Enabled	V$_{IH}$	V$_{IL}$	X	X	D$_{IN}$	X

NOTES:
1. Refer to DC Characteristics. When V$_{PEN}$≤V$_{PENLK}$, memory contents can be read, but cannot be altered.
2. X can be V$_{IL}$ or V$_{IH}$ for control pins and addresses, and V$_{PENLK}$ or V$_{PENH}$ for V$_{PEN}$.
   Refer to DC Characteristics for V$_{PENLK}$ and V$_{PENH}$ voltages.
3. Refer to Table 2 to determine whether the device is selected or de-selected depending on the state of CE$_0$, CE$_1$ and CE$_2$.
4. DQ refers to DQ$_{15}$-DQ$_0$ in word mode (BYTE#=V$_{IH}$: ×16 bit) and DQ$_7$-DQ$_0$ in byte mode (BYTE#=V$_{IL}$: ×8 bit).
5. RP# at GND±0.2V ensures the lowest power consumption.
6. Command writes involving block erase, (page buffer) program, block lock configuration or OTP program are reliably executed when V$_{PEN}$=V$_{PENH}$ and V$_{CC}$=2.7V-3.6V.
7. Refer to Table 5 for valid D$_{IN}$ during a write operation.
8. Never hold OE# low and WE# low at the same timing.
9. Refer to Appendix of LH28F640SP series for more information about query code.
10. STS is V$_{OL}$ when the WSM (Write State Machine) is executing internal block erase, (page buffer) program or OTP program algorithms. It is High Z during when the WSM is not busy, in block erase suspend mode (with program and page buffer program inactive), (page buffer) program suspend mode, or reset mode.

Table 5. Command Definitions [10]

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper[1]	Addr[2]	Data[3]	Oper[1]	Addr[2]	Data[3]
Read Array	1		Write	X	FFH			
Read Identifier Codes/OTP	≥ 2	4	Write	X	90H	Read	IA or OA	ID or OD
Read Query	≥ 2	4	Write	X	98H	Read	QA	QD
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Program	2	5,6	Write	X	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	5,7	Write	BA	E8H	Write	BA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8	Write	X	B0H			
Block Erase and (Page Buffer) Program Resume	1	8	Write	X	D0H			
STS Configuration	2		Write	X	B8H	Write	X	CC
Set Block Lock Bit	2		Write	X	60H	Write	BA	01H
Clear Block Lock Bits	2	9	Write	X	60H	Write	X	D0H
OTP Program	2		Write	X	C0H	Write	OA	OD

NOTES:
1. Bus operations are defined in Table 4.
2. X=Any valid address within the device.
   IA=Identifier codes address (Refer to Table 3).
   QA=Query codes address. Refer to Appendix of LH28F640SP series for details.
   BA=Address within the block for block erase, page buffer program or set block lock bit.
   WA=Address of memory location for the Program command.
   OA=Address of OTP block to be read or programmed (Refer to Figure 3).
3. The upper byte of the data bus (DQ_{15}-DQ_8) during command writes is ignored in word mode (BYTE#=V_{IH} : ×16 bit).
   ID=Data to be read from identifier codes. (Refer to Table 3).
   QD=Data to be read from query database. Refer to Appendix of LH28F640SP series for details.
   SRD=Data to be read from status register. Refer to Table 7 for a description of the status register bits.
   WD=Data to be programmed at location WA. Data is latched on the first edge of CE_0, CE_1 or CE_2 that disables
       the device or the rising edge of WE# (whichever occurs first) during command write cycles.
   N-1=N is the number of the words /bytes to be loaded into a page buffer.
   OD=Data within OTP block. Data is latched on the first edge of CE_0, CE_1 or CE_2 that disables
       the device or the rising edge of WE# (whichever occurs first) during command write cycles.
   CC= STS configuration code (Refer to Table 9).
4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock
   configuration code and the data within OTP block (Refer to Table 3).
   The Read Query command is available for reading CFI (Common Flash Interface) information.
5. Block erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased
   or programmed when RP# is V_{IH}.
6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
7. Following the third bus cycle, write the program sequential address and data of "N" times. Finally, write the any valid
   address within the block to be programmed and the confirm command (D0H).

Refer to Appendix of LH28F640SP series for details.

8. If both block erase operation and (page buffer) program operation are suspended, the suspended (page buffer) program operation is resumed when writing the Block Erase and (Page Buffer) Program Resume (D0H) command.

9. Following the Clear Block Lock Bits command, all the blocks are unlocked at a time.

10. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

Table 6. Functions of Block Lock [1], [2]

DQ$_0$[3]	State Name	Erase/Program Allowed [4]
0	Unlocked	Yes
1	Locked	No

NOTES:
1. Selected block is locked by the Set Block Lock Bit command. Following the Clear Block
   Lock Bits command, all the blocks are unlocked at a time.
2. Locked and unlocked states remain unchanged even after power-up/down and device reset.
3. After writing the Read Identifier Codes/OTP command, read operation outputs the block lock bit
   status on DQ$_0$ (refer to Table 3).
4. Erase and program are general terms, respectively, to express: block erase and
   (page buffer) program operations.

Table 7. Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BECBLS	PBPOPSBLS	VPENS	PBPSS	DPS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)	

SR.7 = WRITE STATE MACHINE STATUS (WSMS)
   1 = Ready
   0 = Busy
	Check SR.7 or STS to determine block erase, (page buffer) program, block lock configuration or OTP program completion. SR.6 - SR.1 are invalid while SR.7="0".

SR.6 = BLOCK ERASE SUSPEND STATUS (BESS)
   1 = Block Erase Suspended
   0 = Block Erase in Progress/Completed	

SR.5 = BLOCK ERASE AND CLEAR BLOCK LOCK BITS STATUS (BECBLS)
   1 = Error in Block Erase or Clear Block Lock Bits
   0 = Successful Block Erase or Clear Block Lock Bits
	If both SR.5 and SR.4 are "1"s after a block erase, page buffer program, block lock configuration, STS configuration attempt, an improper command sequence was entered.

SR.4 = (PAGE BUFFER) PROGRAM, OTP PROGRAM AND SET BLOCK LOCK BIT STATUS (PBPOPSBLS)
   1 = Error in (Page Buffer) Program, OTP Program or Set Block Lock Bit
   0 = Successful (Page Buffer) Program, OTP Program or Set Block Lock Bit	

SR.3 = V_{PEN} STATUS (VPENS)
   1 = V_{PEN} LOW Detect, Operation Abort
   0 = V_{PEN} OK
	SR.3 does not provide a continuous indication of V_{PEN} level. The WSM interrogates and indicates the V_{PEN} level only after Block Erase, (Page Buffer) Program, Set Block Lock Bit, Clear Block Lock Bits or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when $V_{PEN} \neq V_{PENH}$ or V_{PENLK}.

SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS)
   1 = (Page Buffer) Program Suspended
   0 = (Page Buffer) Program in Progress/Completed	

SR.1 = DEVICE PROTECT STATUS (DPS)
   1 = Erase or Program Attempted on a Locked Block, Operation Abort
   0 = Unlocked
	SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/ OTP command indicates block lock bit status.

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.

Table 8. Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R)
 	
XSR.7 = STATE MACHINE STATUS (SMS)
  1 = Page Buffer Program available
  0 = Page Buffer Program not available
 	
XSR.6-0 =RESERVED FOR FUTURE ENHANCEMENTS (R)
	NOTES:
	After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.
	
	XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

SHARP

Table 9. STS Configuration Definition [1]

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
R	R	R	R	R	R	CC	CC
7	6	5	4	3	2	1	0

DQ_{15}-DQ_2 = RESERVED FOR FUTURE
                 ENHANCEMENTS (R)

DQ_1-DQ_0 = STS CONFIGURATION CODE (CC)
    00 = level mode: RY/BY# indication. (Default)
    01 = pulse mode on erase complete.
    10 = pulse mode on program complete.
    11 = pulse mode on erase or program complete.

In STS configuration = "00", STS is V_{OL} when the WSM is executing internal erase or program algorithms.

STS configuration codes "01", "10" and "11" are all pulse modes such that the STS pin pulses low then high when the operation indicated by the configuration code is completed.

NOTES:

After power-up or device reset, STS configuration is set to "00".

STS configuration 00
    The output of the STS pin is the control signal to prevent accessing a flash memory while the internal WSM is busy (SR.7="0").

STS configuration 01
    The output of the STS pin is the control signal to indicate that the erase operation is completed and the flash memory is available for the next operation.

STS configuration 10
    The output of the STS pin is the control signal to indicate that the program operation is completed and the flash memory is available for the next operation.

STS configuration 11
    The output of the STS pin is the control signal to indicate that the erase or program operation is completed and the flash memory is available for the next operation.

NOTE:
1. When the device is configured in one of the pulse modes, the STS pin pulses low with a typical pulse width of 250ns.

1   Electrical Specifications

1.1   Absolute Maximum Ratings*

Operating Temperature

   During Read, Erase and Program ...-40°C to +85°C [1]

Storage Temperature

   During under Bias.............................. -40°C to +85°C
   During non Bias................................ -65°C to +125°C

Voltage On Any Pin (except V_{CC}, V_{CCQ} and V_{PEN})

....-0.5V to V_{CCQ}+0.5V [2]

V_{CC} and V_{CCQ} Supply Voltage .... -0.2V to +3.9V [2]

V_{PEN} Supply Voltage.......................... -0.2V to +3.9V [2]

Output Short Circuit Current ....100mA [3]

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:
1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC}, V_{CCQ} and V_{PEN} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

1.2   Operating Conditions

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
T_A	Operating Temperature		-40	+25	+85	°C	Ambient Temperature
V_{CC}	V_{CC} Supply Voltage	1, 2	2.7	3.0	3.6	V	
V_{CCQ}	I/O Supply Voltage	1, 2	2.7	3.0	3.6	V	
V_{PENH}	V_{PEN} Voltage	1	2.7	3.0	3.6	V	
	Block Erase Cycling: $V_{PEN}=V_{PENH}$		100,000			Cycles	

NOTES:
1. Refer to DC Characteristics tables for voltage range-specific specification.
2. V_{CC} and V_{CCQ} should be the same voltage.

1.2.1   Capacitance [1] (T_A=+25°C, f=1MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
C_{IN}	Input Capacitance		6	8	pF	V_{IN}=0.0V
C_{OUT}	Output Capacitance		8	12	pF	V_{OUT}=0.0V

NOTE:
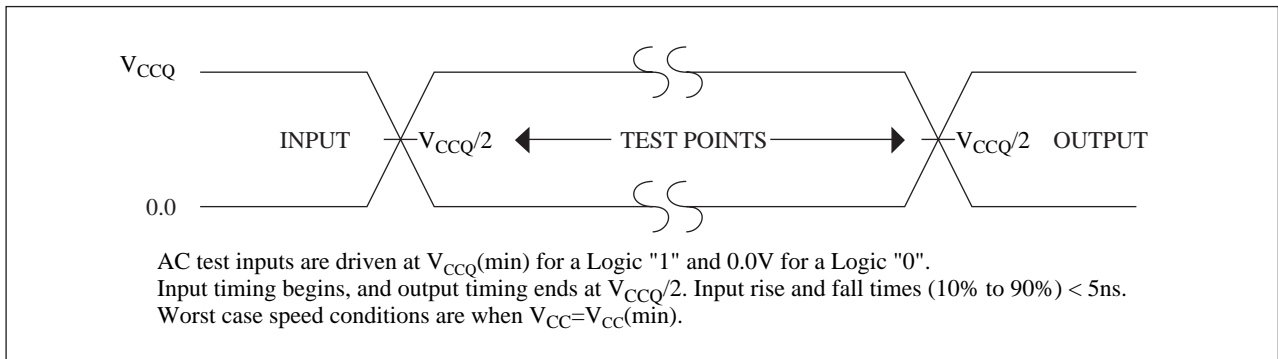1. Sampled, not 100% tested.

1.2.2   AC Input/Output Test Conditions

AC test inputs are driven at V_{CCQ}(min) for a Logic "1" and 0.0V for a Logic "0".
Input timing begins, and output timing ends at V_{CCQ}/2. Input rise and fall times (10% to 90%) < 5ns.
Worst case speed conditions are when V_{CC}=V_{CC}(min).

Figure 4. Transient Input/Output Reference Waveform for V_{CC}=2.7V-3.6V
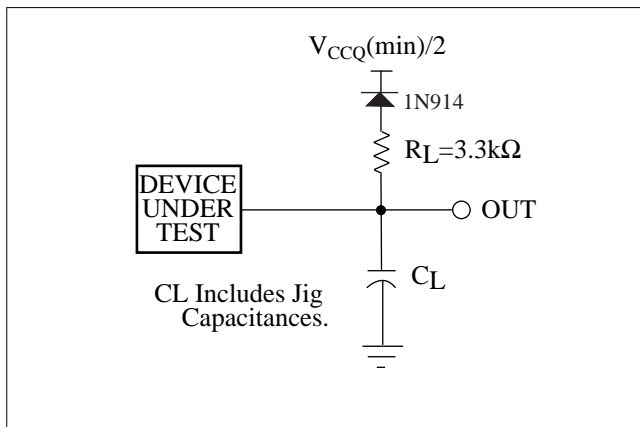
Figure 5. Transient Equivalent Testing Load Circuit

Table 10. Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC}=2.7V-3.6V	30

1.2.3 DC Characteristics

$$V_{CC}=2.7V\text{-}3.6V$$

Symbol	Parameter		Notes	Min.	Typ.	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	-1		+1	μA	$V_{CC}=V_{CC}$Max., $V_{CCQ}=V_{CCQ}$Max., $V_{IN}/V_{OUT}=V_{CCQ}$ or GND
I_{LO}	Output Leakage Current		1	-10		+10	μA	
I_{CCS}	V_{CC} Standby Current		1, 2, 8		50	120	μA	CMOS Inputs, $V_{CC}=V_{CC}$Max., $V_{CCQ}=V_{CCQ}$Max., Device is disabled (refer to Table 2), RP#=$V_{CCQ}\pm0.2V$
					0.71	2	mA	TTL Inputs, $V_{CC}=V_{CC}$Max., $V_{CCQ}=V_{CCQ}$Max., Device is disabled (refer to Table 2), RP#=V_{IH}
I_{CCAS}	V_{CC} Automatic Power Savings Current		1, 2, 5		50	120	μA	CMOS Inputs, $V_{CC}=V_{CC}$Max., $V_{CCQ}=V_{CCQ}$Max., Device is enabled (refer to Table 2)
I_{CCD}	V_{CC} Reset Current		1		50	120	μA	RP#=GND$\pm0.2V$ I_{OUT} (STS)=0mA
I_{CCR}	Average V_{CC} Page Mode Read Current	4 word/ 8 byte read	1, 2		15	20	mA	CMOS Inputs, $V_{CC}=V_{CC}$Max., $V_{CCQ}=V_{CCQ}$Max., Device is enabled (refer to Table 2), f=5MHz, I_{OUT}=0mA
			1, 2		24	29	mA	CMOS Inputs, $V_{CC}=V_{CC}$Max., $V_{CCQ}=V_{CCQ}$Max., Device is enabled (refer to Table 2), f=33MHz, I_{OUT}=0mA
	Average V_{CC} Read Current	1 word/ 1 byte read	1, 2		40	50	mA	CMOS Inputs, $V_{CC}=V_{CC}$Max., $V_{CCQ}=V_{CCQ}$Max., Device is enabled (refer to Table 2), f=5MHz, I_{OUT}=0mA
I_{CCW}	V_{CC} (Page Buffer) Program, Set Block Lock Bit Current		1, 2, 6		35	60	mA	CMOS Inputs, $V_{PEN}=V_{PENH}$
			1, 2, 6		40	70	mA	TTL Inputs, $V_{PEN}=V_{PENH}$

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DC Characteristics (Continued)

$V_{CC}=2.7V-3.6V$

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
I_{CCE}	V_{CC} Block Erase, Clear Block Lock Bits Current	1, 2, 6		35	70	mA	CMOS Inputs, $V_{PEN}=V_{PENH}$
		1, 2, 6		40	80	mA	TTL Inputs, $V_{PEN}=V_{PENH}$
I_{CCWS} I_{CCES}	V_{CC} (Page Buffer) Program or Block Erase Suspend Current	1, 3			10	mA	Device is disabled (refer to Table 2).
V_{IL}	Input Low Voltage	6	-0.5		0.8	V	
V_{IH}	Input High Voltage	6	2.0		V_{CCQ} + 0.5	V	
V_{OL}	Output Low Voltage	6, 8			0.4	V	$V_{CC}=V_{CC}$Min., $V_{CCQ}=V_{CCQ}$Min., $I_{OL}=2mA$
					0.2	V	$V_{CC}=V_{CC}$Min., $V_{CCQ}=V_{CCQ}$Min., $I_{OL}=100\mu A$
V_{OH}	Output High Voltage	6, 8	$0.85\times V_{CCQ}$			V	$V_{CC}=V_{CC}$Min., $V_{CCQ}=V_{CCQ}$Min., $I_{OH}=-1.5mA$
			V_{CCQ} -0.2			V	$V_{CC}=V_{CC}$Min., $V_{CCQ}=V_{CCQ}$Min., $I_{OH}=-100\mu A$
V_{PENLK}	V_{PEN} Lockout Voltage during Normal Operations	4, 6, 7			1.0	V	
V_{PENH}	V_{PEN} Voltage during Block Erase, (Page Buffer) Program, Set Block Lock Bit, Clear Block Lock Bits or OTP Program Operations	4, 7	2.7	3.0	3.6	V	
V_{LKO}	V_{CC} Lockout Voltage	4	2.0			V	

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values are the reference values at $V_{CC}=3.0V$, $V_{CCQ}=3.0V$ and $T_A=+25°C$ unless V_{CC} is specified.
2. CMOS inputs are either $V_{CCQ}\pm0.2V$ or GND$\pm0.2V$. TTL inputs are either V_{IL} or V_{IH}.
3. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of I_{CCES} and I_{CCR} or I_{CCW}. If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of I_{CCWS} and I_{CCR}.
4. Block erase, (page buffer) program, block lock configuration and OTP program operations are inhibited when $V_{PEN}\leq V_{PENLK}$ or $V_{CC}\leq V_{LKO}$. These operations are not guaranteed outside the specified voltage ($V_{CC}=2.7V-3.6V$ and $V_{PEN}=2.7V-3.6V$).
5. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVQV}) provide new data when addresses are changed.
6. Sampled, not 100% tested.
7. V_{PEN} is not used for power supply pin. With $V_{PEN}\leq V_{PENLK}$, block erase, (page buffer) program, block lock configuration and OTP program operations are inhibited.
8. Includes STS.

1.2.4 AC Characteristics - Read-Only Operations [1]

T_A=-40°C to +85°C

Symbol	Parameter	Notes	V_{CC} 3.0V-3.6V		2.7V-3.6V		
			V_{CCQ} 3.0V-3.6V		2.7V-3.6V		
			Min.	Max.	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		120		120		ns
t_{AVQV}	Address to Output Delay			120		120	ns
t_{ELQV}	CE_X to Output Delay	3, 4		120		120	ns
t_{APA}	Page Address Access Time			25		30	ns
t_{GLQV}	OE# to Output Delay	3		25		30	ns
t_{PHQV}	RP# High to Output Delay			180		180	ns
t_{ELQX}	CE_X to Output in Low Z	2, 4	0		0		ns
t_{GLQX}	OE# to Output in Low Z	2	0		0		ns
t_{EHQZ}	CE_X to Output in High Z	2, 5		35		35	ns
t_{GHQZ}	OE# to Output in High Z	2		15		15	ns
t_{OH}	Output Hold from First Occurring Address, CE_X or OE# change	2, 5	0		0		ns
t_{ELFL}/t_{ELFH}	CEx Setup to BYTE# Going Low or High	2, 4		10		10	ns
t_{FLQV}/t_{FHQV}	BYTE# to Output Delay			1000		1000	ns
t_{FLQZ}/t_{FHQZ}	BYTE# to Output in High Z	2		1000		1000	ns

NOTES:

1. Refer to AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. Sampled, not 100% tested.
3. OE# may be delayed up to t_{ELQV} — t_{GLQV} after the first edge of CE_0, CE_1 or CE_2 that enables the device (refer to Table 2) without impact to t_{ELQV}.
4. The timing is defined from the first edge of CE_0, CE_1 or CE_2 that enables the device.
5. The timing is defined from the first edge of CE_0, CE_1 or CE_2 that disables the device.
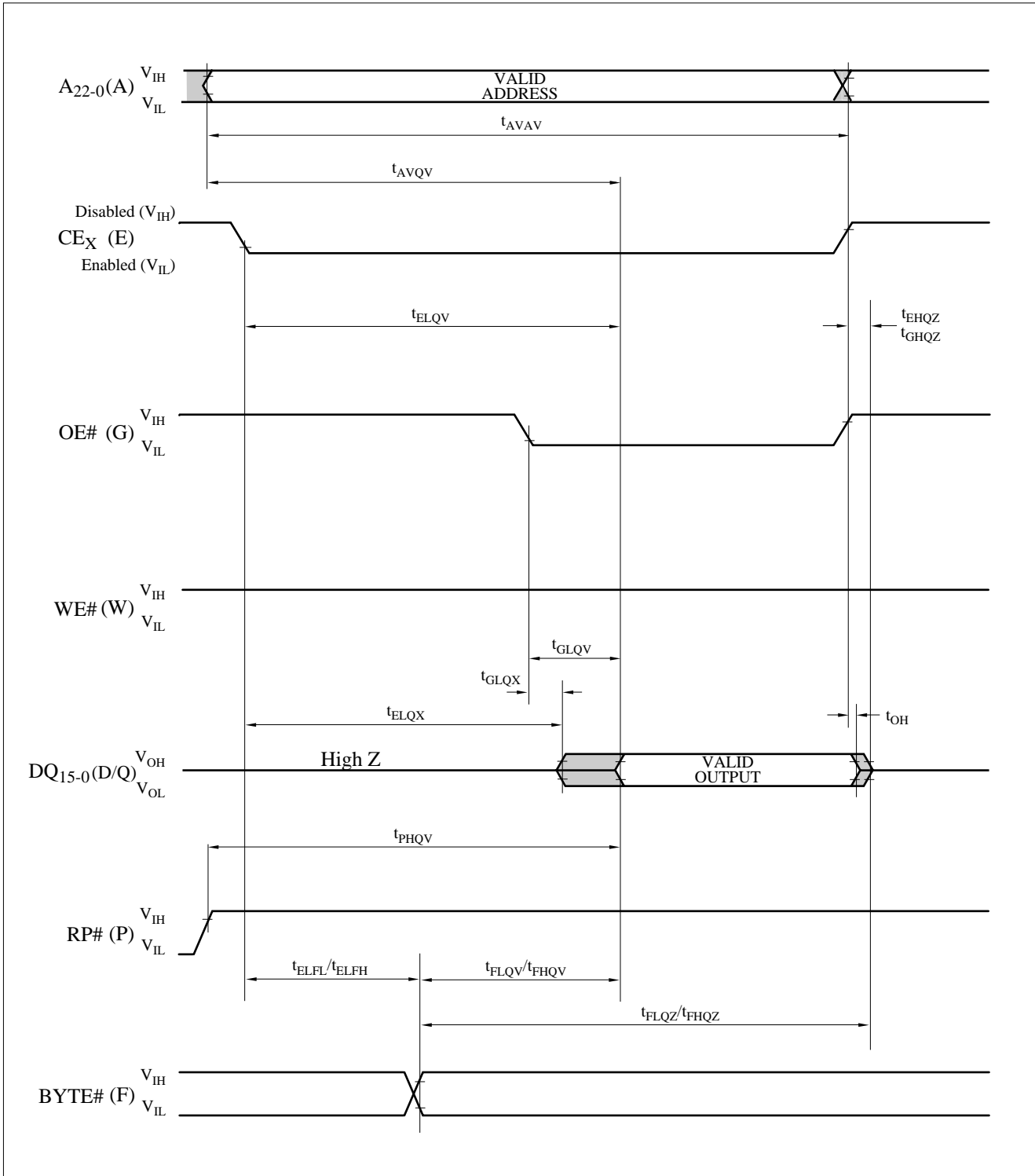
Figure 6. AC Waveform for 1-Word/ 1-Byte Read Operations
(Status Register, Identifier Codes, OTP Block or Query Code)

NOTE:
1. Status register, identifier codes, OTP block and query code can only be read in 1-word/ 1-byte
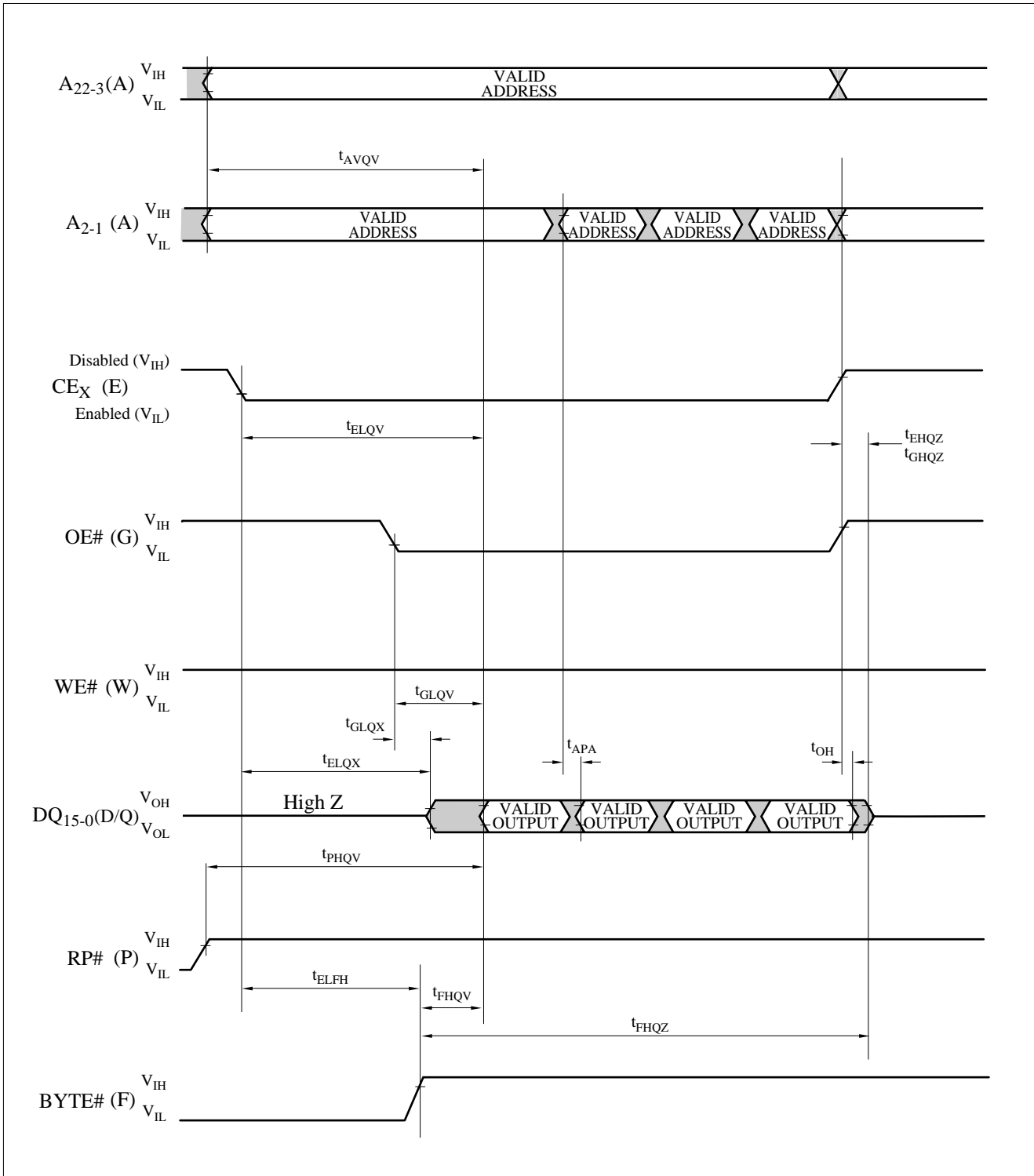   read operations.

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Figure 7. AC Waveform for 4-Word Page Mode Read Operations
(Memory Array)

NOTE:
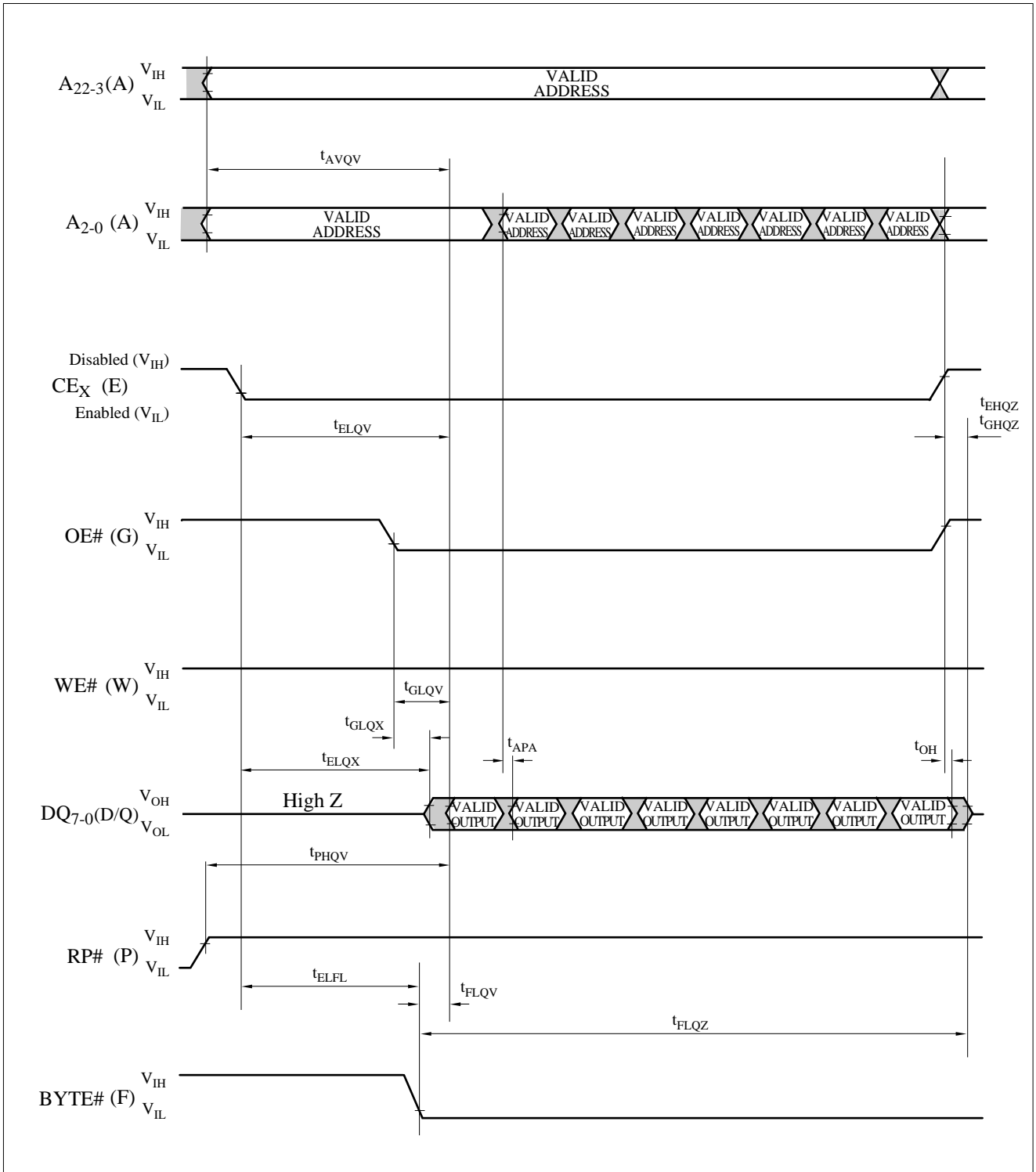1. Memory array supports page mode read operations.

Figure 8. AC Waveform for 8-Byte Page Mode Read Operations
(Memory Array)

NOTE:
1. Memory array supports page mode read operations.

1.2.5 AC Characteristics - Write Operations [(1), (2)]

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		120		ns
t_{PHWL} (t_{PHEL})	RP# High Recovery to WE# (CE_X) Going Low	3, 9	1		μs
t_{ELWL} (t_{WLEL})	CE_X (WE#) Setup to WE# (CE_X) Going Low	9	0		ns
t_{WLWH} (t_{ELEH})	WE# (CE_X) Pulse Width Low	4, 9, 10	70		ns
t_{DVWH} (t_{DVEH})	Data Setup to WE# (CE_X) Going High	7, 10	50		ns
t_{AVWH} (t_{AVEH})	Address Setup to WE# (CE_X) Going High	7, 10	55		ns
t_{WHEH} (t_{EHWH})	CE_X (WE#) Hold from WE# (CE_X) High	10	0		ns
t_{WHDX} (t_{EHDX})	Data Hold from WE# (CE_X) High	10	0		ns
t_{WHAX} (t_{EHAX})	Address Hold from WE# (CE_X) High	10	0		ns
t_{WHWL} (t_{EHEL})	WE# (CE_X) Pulse Width High	5, 9, 10	30		ns
t_{VVWH} (t_{VVEH})	V_{PEN} Setup to WE# (CE_X) Going High	3, 10	0		ns
t_{WHGL} (t_{EHGL})	Write Recovery before Read	8	35		ns
t_{WHR0} (t_{EHR0}) t_{WHRL} (t_{EHRL})	WE# (CE_X) High to SR.7 Going "0", STS Going Low	10, 11		500	ns
t_{QVVL}	V_{PEN} Hold from Valid SRD, STS High Z	3, 6, 11	0		ns
t_{FLWH}/t_{FHWH} (t_{FLEH}/t_{FHEH})	BYTE# Setup to WE# (CE_X) Going High	10	50		ns
t_{WHFL}/t_{WHFH} (t_{EHFL}/t_{EHFH})	BYTE# Hold from WE# (CE_X) High	10	90		ns

NOTES:
1. The timing characteristics for reading the status register during block erase, (page buffer) program, block lock configuration and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. A write operation can be initiated and terminated with either CE_0, CE_1, CE_2 or WE#.
3. Sampled, not 100% tested.
4. Write pulse width low (t_{WP}) is defined from the first edge of CE_0, CE_1 or CE_2 that enables the device or the falling edge of WE# (whichever occurs last) to the first edge of CE_0, CE_1 or CE_2 that disables the device or the rising edge of WE# (whichever occurs first). Hence, t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}.
5. Write pulse width high (t_{WPH}) is defined from the first edge of CE_0, CE_1 or CE_2 that disables the device or the rising edge of WE# (whichever occurs first) to the first edge of CE_0, CE_1 or CE_2 that enables the device or the falling edge of WE# (whichever occurs last). Hence, t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}.
6. V_{PEN} should be held at V_{PEN}=V_{PENH} until determination of block erase, (page buffer) program, block lock configuration or OTP program success (SR.1/3/4/5=0).
7. Refer to Table 5 for valid address and data for block erase, (page buffer) program, block lock configuration and OTP program.
8. The output delay time t_{AVQV} or t_{ELQV} is required in addition to t_{WHGL} (t_{EHGL}) for read operations after command writes.
9. The timing is defined from the first edge of CE_0, CE_1 or CE_2 that enables the device.
10. The timing is defined from the first edge of CE_0, CE_1 or CE_2 that disables the device.
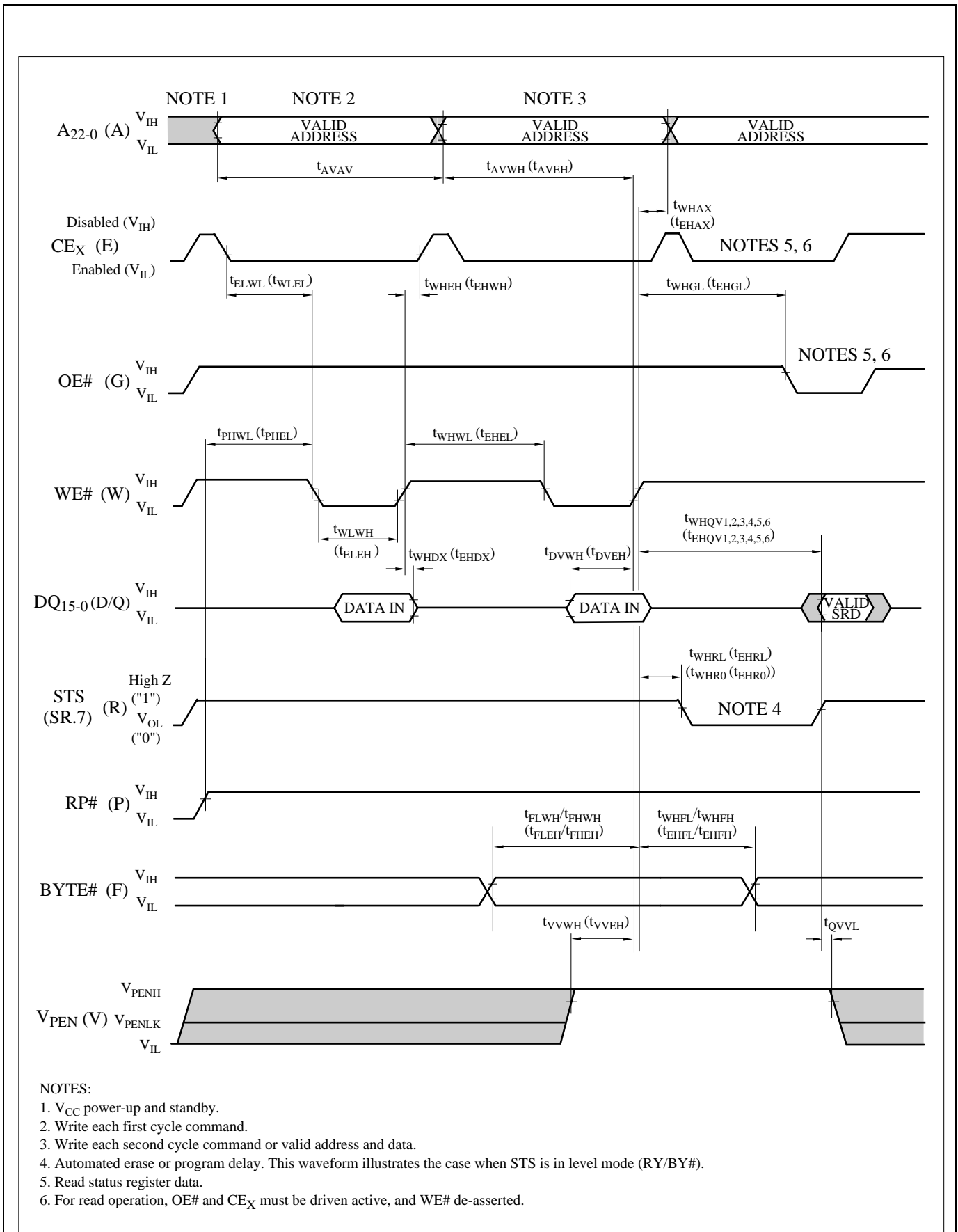11. STS timings depend on STS configuration.

Figure 9. AC Waveform for Write Operations

NOTES:
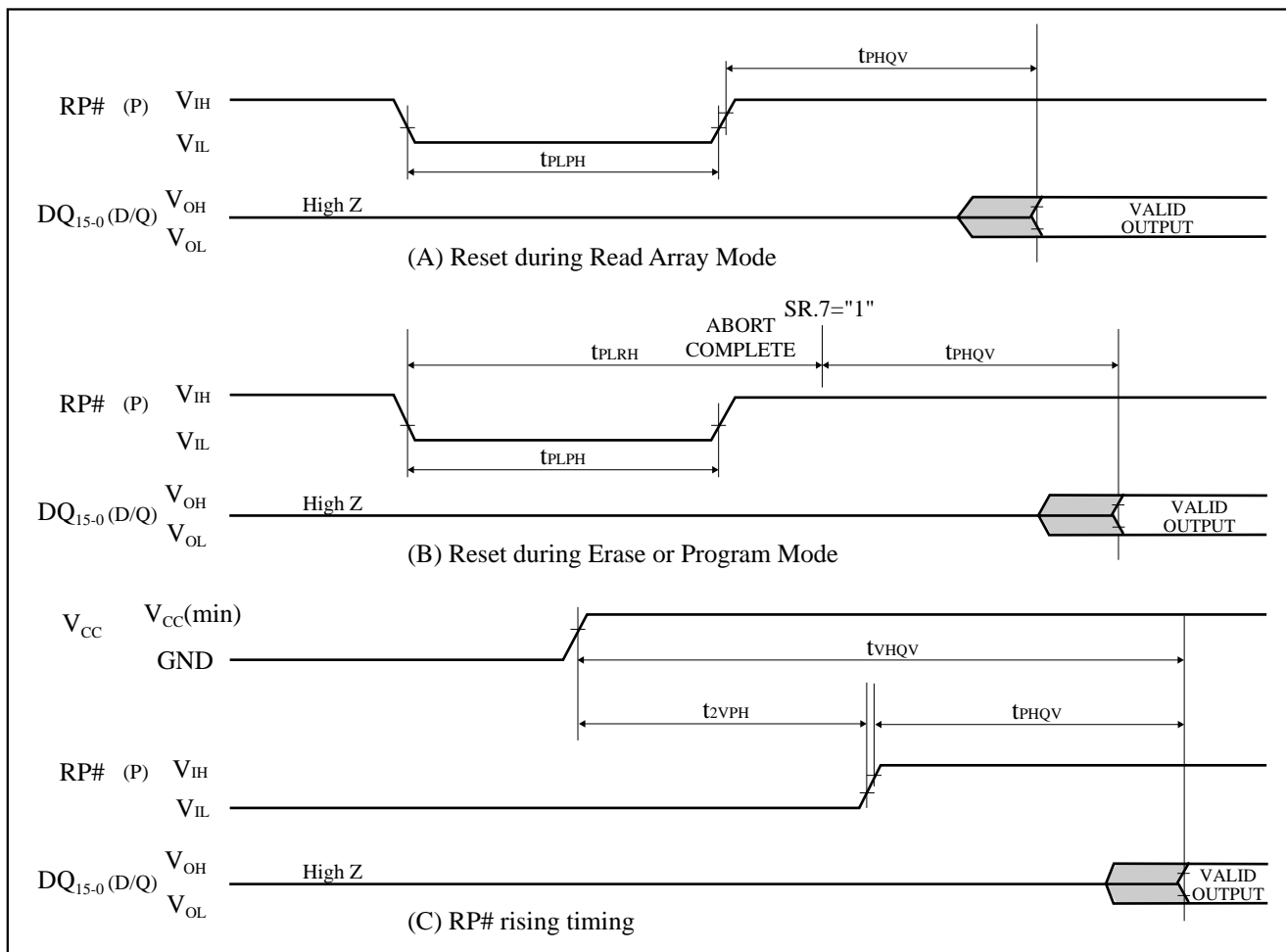1. V_{CC} power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay. This waveform illustrates the case when STS is in level mode (RY/BY#).
5. Read status register data.
6. For read operation, OE# and CE_X must be driven active, and WE# de-asserted.

1.2.6 Reset Operations

Figure 10. AC Waveform for Reset Operations

Reset AC Specifications (V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	RP# Low to Reset during Read (RP# must be low during power-up.)	1, 2, 3	100		ns
t_{PLRH}	RP# Low to Reset during Erase or Program	1, 3, 4		30	µs
t_{2VPH}	V_{CC} 2.7V to RP# High	1, 3, 5	100		ns
t_{VHQV}	V_{CC} 2.7V to Output Delay	3		1	ms

NOTES:

1. A reset time, t_{PHQV}, is required from the later of SR.7 (STS) going "1" (High Z) or RP# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV}.
2. The device may reset if t_{PLPH} is <100ns, but this is not guaranteed.
3. Sampled, not 100% tested.
4. If RP# asserted while a block erase, (page buffer) program, block lock configuration or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding RP# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

1.2.7 Block Erase, (Page Buffer) Program and Block Lock Configuration Performance[3]

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Symbol	Parameter	Notes	$V_{PEN}=V_{PENH}$			Unit
			Min.	Typ.[1]	Max.	
	Page Buffer Program Time (Time to Program 16 words/ 32 bytes)	2, 6, 7		400	1200	μs
$t_{WHQV3}/$ t_{EHQV3}	Program Time	2		210	630	μs
	Block Program Time (Using Page Buffer Program Command)	2		1.6	4.8	s
$t_{WHQV4}/$ t_{EHQV4}	Block Erase Time	2		1	5	s
$t_{WHQV5}/$ t_{EHQV5}	Set Block Lock Bit Time	2		64	85	μs
$t_{WHQV6}/$ t_{EHQV6}	Clear Block Lock Bits Time	2		0.5	0.7	s
$t_{WHRH1}/$ t_{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	4		25	90	μs
$t_{WHRH2}/$ t_{EHRH2}	Block Erase Suspend Latency Time to Read	4		26	40	μs
t_{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	600			μs

NOTES:
1. Typical values measured at V_{CC}=3.0V, V_{PEN}=3.0V and T_A=+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (the first edge of CE_0, CE_1 or CE_2 that disables the device or the rising edge of WE#) until SR.7 going "1" or STS going High Z.
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.
6. These values are valid when the page buffer is full, and the start address is aligned on a 16-word/ 32-byte boundary.
7. Program time per byte ($t_{WHQV1}/$ t_{EHQV1}) is 12.5μs/byte (typical).
   Program time per word ($t_{WHQV2}/$ t_{EHQV2}) is 25.0μs/word (typical).

2 Related Document Information[1]

Document No.	Document Name
FUM03201	LH28F640SP series Appendix

NOTE:

1. International customers should contact their local SHARP or distribution sales offices.

3   Package and packing specification

[Applicability]
   This specification applies to IC package of the LEAD-FREE delivered as a standard specification.

1.Storage Conditions.
   1-1.Storage conditions required before opening the dry packing.
         ・ Normal temperature : 5～40℃
         ・ Normal humidity : 80%(Relative humidity) max.
           *"Humidity" means "Relative humidity"

   1-2.Storage conditions required after opening the dry packing.
         In order to prevent moisture absorption after opening, ensure the following storage
         conditions apply:
         （1） Storage conditions for one-time soldering. (Convection reflow[*1], IR/Convection reflow.[*1],
               or Manual soldering.)
               ・ Temperature : 5～25℃
               ・ Humidity : 60% max.
               ・ Period : 96 hours max. after opening.
         （2） Storage conditions for two-time soldering. (Convection reflow[*1], IR/Convection reflow.[*1])
               a. Storage conditions following opening and prior to performing the 1st reflow.
               ・ Temperature : 5～25℃
               ・ Humidity : 60% max.
               ・ Period : 96 hours max. after opening.
               b. Storage conditions following completion of the 1st reflow and prior to performing
                  the 2nd reflow.
               ・ Temperature : 5～25℃
               ・ Humidity : 60% max.
               ・ Period : 96 hours max. after completion of the 1st reflow.
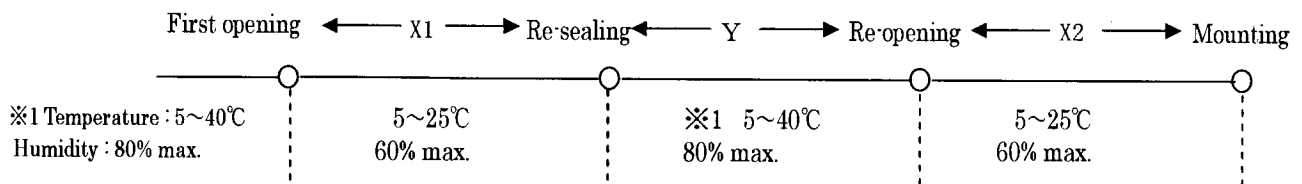   [*1]:Air or nitrogen environment.

   1-3.Temporary storage after opening.
         To re-store the devices before soldering, do so only once and use a dry box or place desiccant
         (with a blue humidity indicator) with the devices and perform dry packing again using
         heat-sealing.
         The storage period, temperature and humidity must be as follows :
         （1） Storage temperature and humidity.
                 ※1 : External atmosphere temperature and humidity of the dry packing.


```
First opening  ◄─── X1 ───►  Re-sealing ◄─── Y ───►  Re-opening ◄─── X2 ───►  Mounting
       ────────○──────────────────────○──────────────────────○──────────────────────○───
※1 Temperature : 5～40℃        5～25℃          ※1  5～40℃          5～25℃
Humidity : 80% max.           60% max.           80% max.            60% max.
```

         （2） Storage period.
               ・ X1＋X2 : Refer to Section 1-2(1) and (2)a , depending on the mounting method.
               ・ Y   : Two weeks max.

2. Baking Condition.
　(1)　Situations requiring baking before mounting.
　　　　　・ Storage conditions exceed the limits specified in Section 1-2 or 1-3.
　　　　　・ Humidity indicator in the desiccant was already red (pink) when opened.
　　　　　　　(Also for re-opening.)
　(2)　Recommended baking conditions.
　　　　　・ Baking temperature and period :
　　　　　　　120℃ for 16～24 hours.
　　　　　・　The above baking conditions apply since the trays are heat-resistant.
　(3)　Storage after baking.
　　　　　・ After baking, store the devices in the environment specified in Section 1-2 and mount
　　　　　　immediately.

3. Surface mount conditions.
　The following soldering condition are recommended to ensure device quality.
　3-1.Soldering.
　(1)　Convection reflow or IR/Convection. (one-time soldering or two-time soldering in air or
　　　　nitrogen environment)
　　　　　・ Temperature and period :
　　　　　　　A)　Peak temperature.　　　　　　　250℃ max.
　　　　　　　B)　Heating temperature.　　　　　　40 to 60 seconds as 220℃
　　　　　　　C)　Preheat temperature.　　　　　　It is 150 to 200℃, and is 120±30 seconds
　　　　　　　D)　Temperature increase rate.　　　It is 1 to 3℃/seconds
　　　　　・ Measuring point : IC package surface.
　　　　　・ Temperature profile:
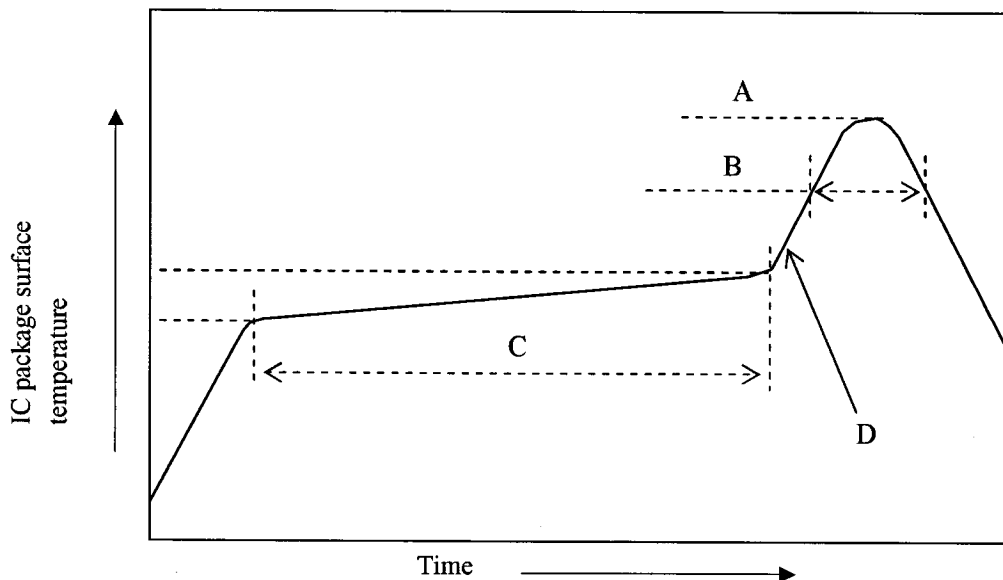
(2)   Manual soldering (soldering iron) (one-time soldering only)
        Soldering iron should only touch the IC's outer leads.
                · Temperature and period :
                        350℃ max. for 3 seconds / pin max.
                        (Soldering iron should only touch the IC's outer leads.)
                · Measuring point : Soldering iron tip.

4. Condition for removal of residual flux.
  (1) Ultrasonic washing power : 25 watts / liter max.
  (2) Washing time : Total 1 minute max.
  (3) Solvent temperature : 15~40℃

5. Package outline specification.
      Refer to the attached drawing.
      (Plastic body dimensions do not include burr of resin.)
      The contents of LEAD-FREE TYPE application of the specifications. (*2)

6. Markings.
    6-1.Marking details. (The information on the package should be given as follows.)
        (1) Product name   :   LH28F640SPHT-PTLZ8
        (2) Company name   :   SHARP
        (3) Date code   :   (Example) YYWW XXX
                YY   →   Denotes the production year. (Last two digits of the year.)
                WW   →   Denotes the production week. (01 · 02 · ~ · 52 · 53)
                XXX   →   Denotes the production ref. code (1~3 digits).
        (4) "JAPAN" indicates the country of origin.

    6-2.Marking layout.
        The layout is shown in the attached drawing.
        (However, this layout does not specify the size of the marking character and marking position.)

            *2   The contents of LEAD-FREE TYPE application of the specifications.

LEAD FINISH or BALL TYPE	LEAD-FREE TYPE (Sn-Bi)
DATE CODE	They are those with an underline.
The word of " LEAD FREE" is printed on the packing label	Printed

(Note)It is those with an underline printing in a date code because of a LEAD-FREE type.

LH28F640SPHT-PTLZ8
SHARP
JAPAN
YYWW XXX

P=0.5TYP.

14.0±0.2

□ 0.10

56-0.2±0.08

⊕ 0.08 Ⓜ

56

28   29

20.0±0.3
18.4±0.2

0.125±0.05

SEE DETAIL A

0.125

0.435±0.05

0.995±0.1

1.19MAX

PKG.BASE PLANE

0.435±0.05

0.115±0.1

18.4±0.2
19.0±0.3

TSOP056-P-1420-AA1115

DETAIL A

0.435±0.05

0.995±0.1

0.435

0.115±0.1

PKG. BASE PLANE

0~10°

LEAD TYPE	LEAD FINISH	LEAD MATERIAL
	Sn-Bi PLATING	42Alloy

NAME	TSOP056-P-1420		NOTE : Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1115	UNIT mm	

20040720

7.Packing Specifications (Dry packing for surface mount packages.)
    7-1.Packing materials.

Material name	Material specifications	Purpose
Inner carton	Cardboard　(910 devices / inner carton max.)	Packing the devices. (10 trays / inner carton)
Tray	Conductive plastic　(91 devices / tray)	Securing the devices.
Upper cover tray	Conductive plastic　(1 tray / inner carton)	Securing the devices.
Laminated aluminum bag	Aluminum polyethylene	Keeping the devices dry.
Desiccant	Silica gel	Keeping the devices dry.
Label	Paper	Indicates part number, quantity, and packed date.
PP band	Polypropylene　(3 pcs. / inner carton)	Securing the devices.
Outer carton	Cardboard　(3640 devices / outer carton max.)	Outer packing.

(Devices must be placed on the tray in the same direction.)

    7-2.Outline dimension of tray.
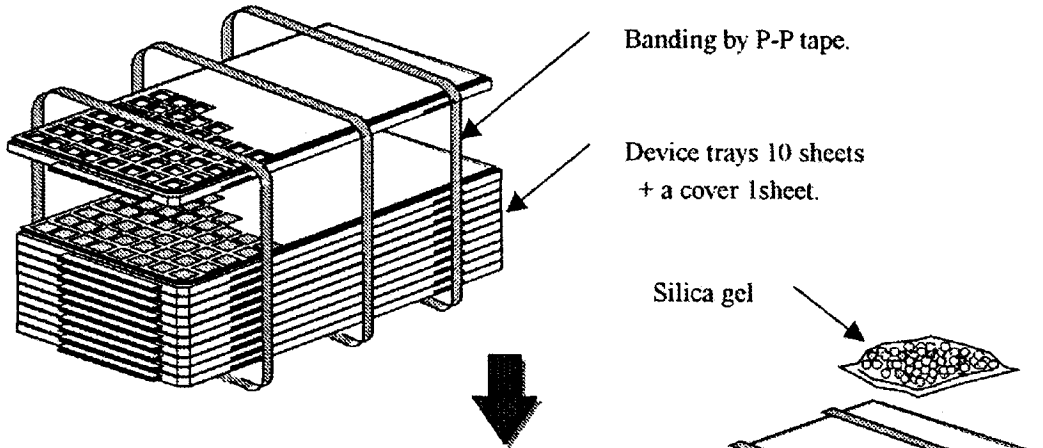   Refer to the attached drawing.
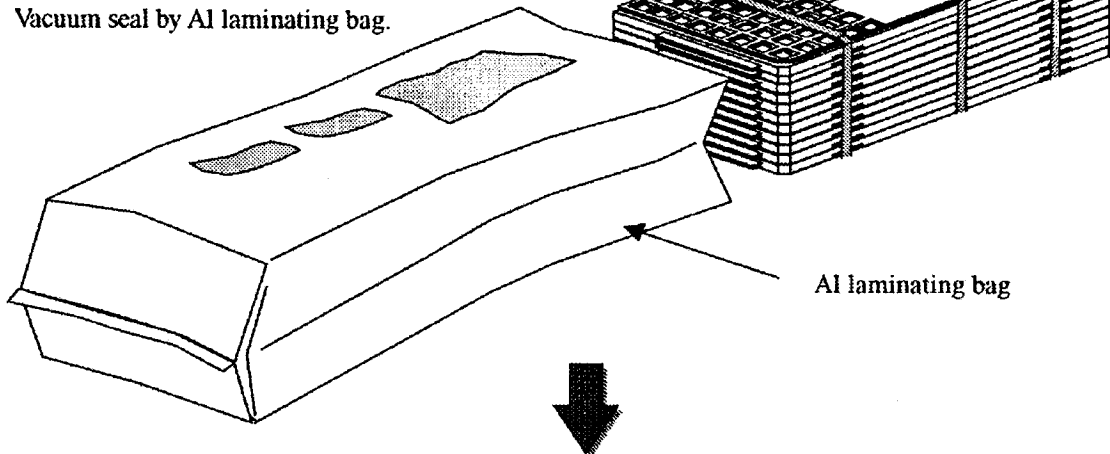   7-3.Outline dimension of carton.
       Refer to the attached drawing.

8. Precautions for use.
    (1)   Opening must be done on an anti-ESD treated workbench.
          All workers must also have undergone anti-ESD treatment.
    (2)   The trays have undergone either conductive or anti-ESD treatment.
          If another tray is used, make sure it has also undergone conductive or anti-ESD treatment.
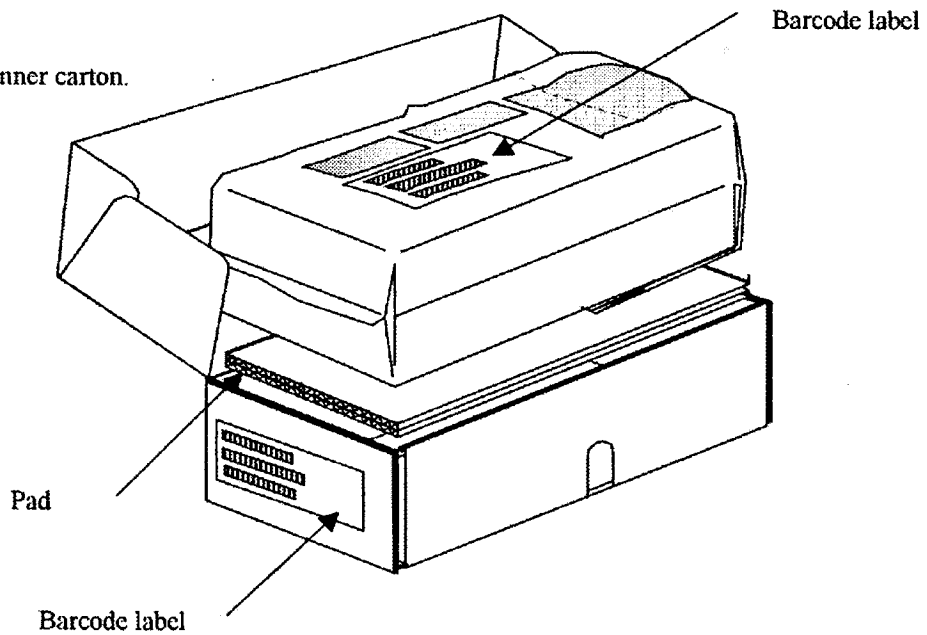   (3)   The devices should be mounted the devices within one year of the date of delivery.

名称 NAME		TSOP56-1420-JCM-RH-N	備考 NOTE	
DRAWING NO.	CV912	単位 UNIT mm		

(1) Banding device tray together.

Banding by P-P tape.

Device trays 10 sheets
+ a cover 1sheet.

Silica gel

(2) Vacuum seal by Al laminating bag.

Al laminating bag

Barcode label

(3) Packing by Inner carton.

Pad

Barcode label

NAME	Packing specifications		NOTE There is a possibility different from this specification when the number of shipments is fractions.
DRAWING NO.	BJ433c	UNIT mm	

20040720

Inner carton

Inner carton barcode label

Adhesive tape ("H" taping)

Outer carton

Outer carton barcode label
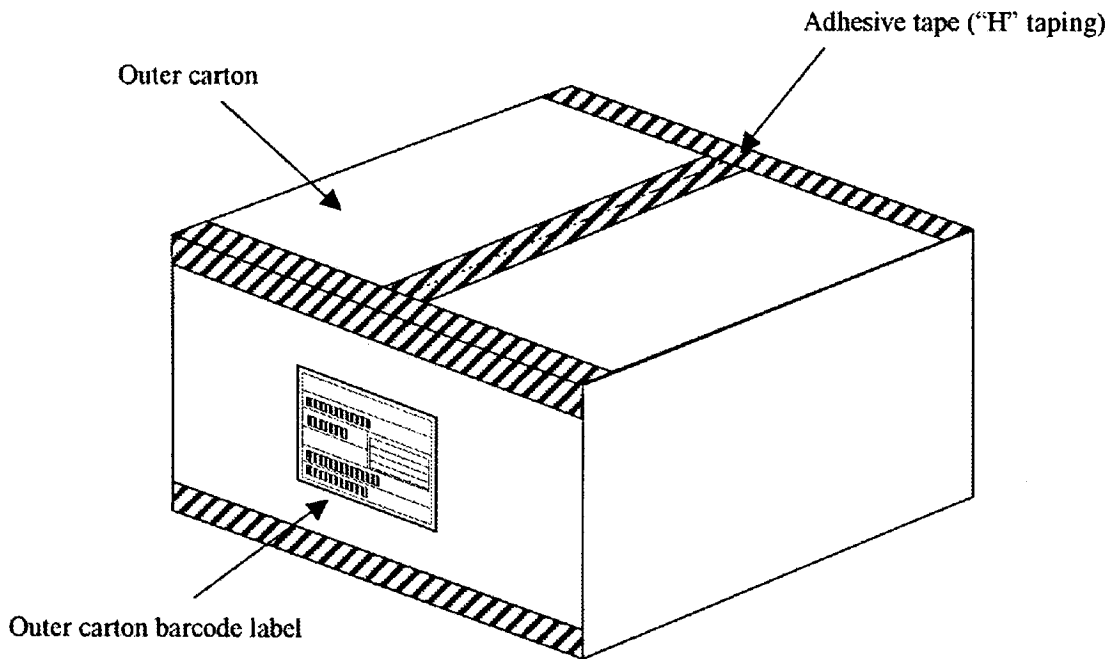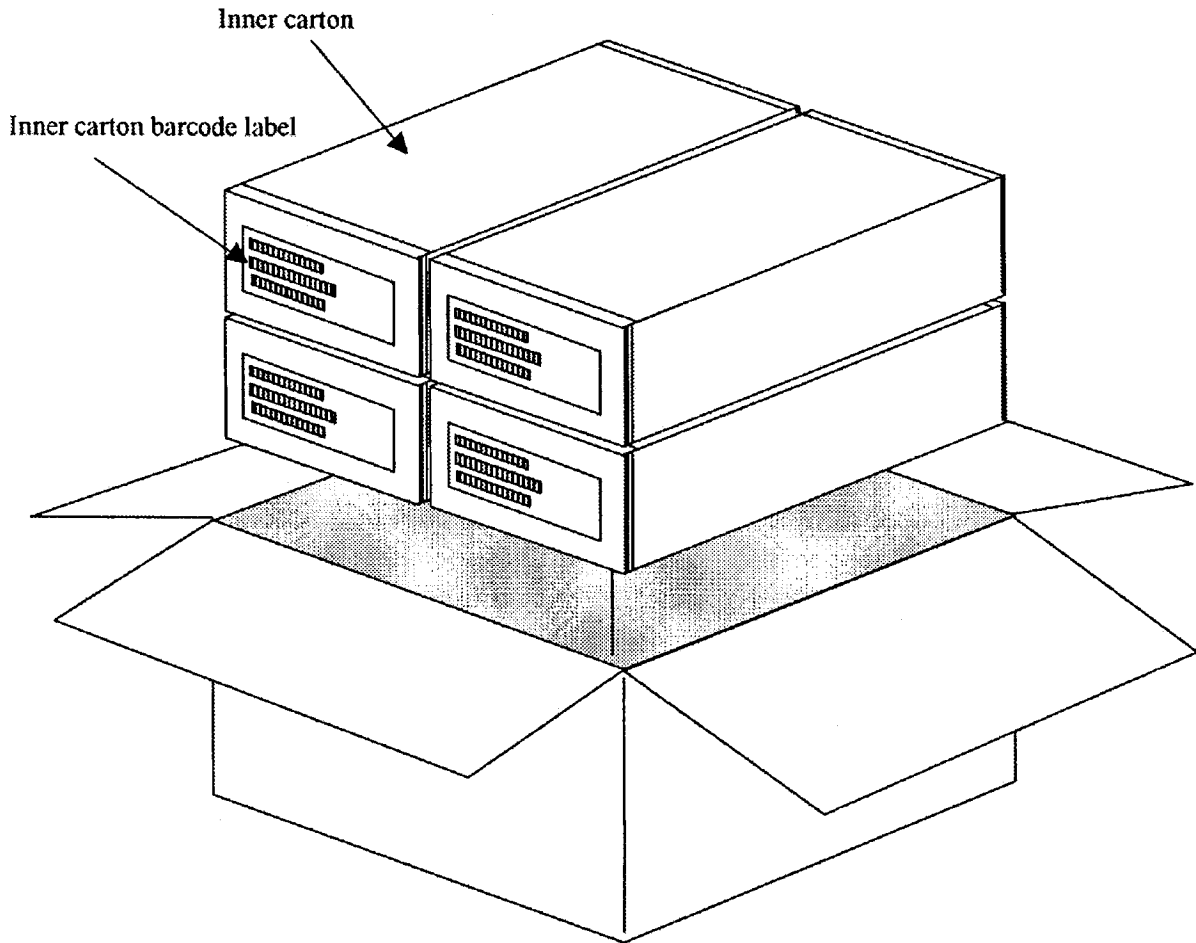
L × W× H
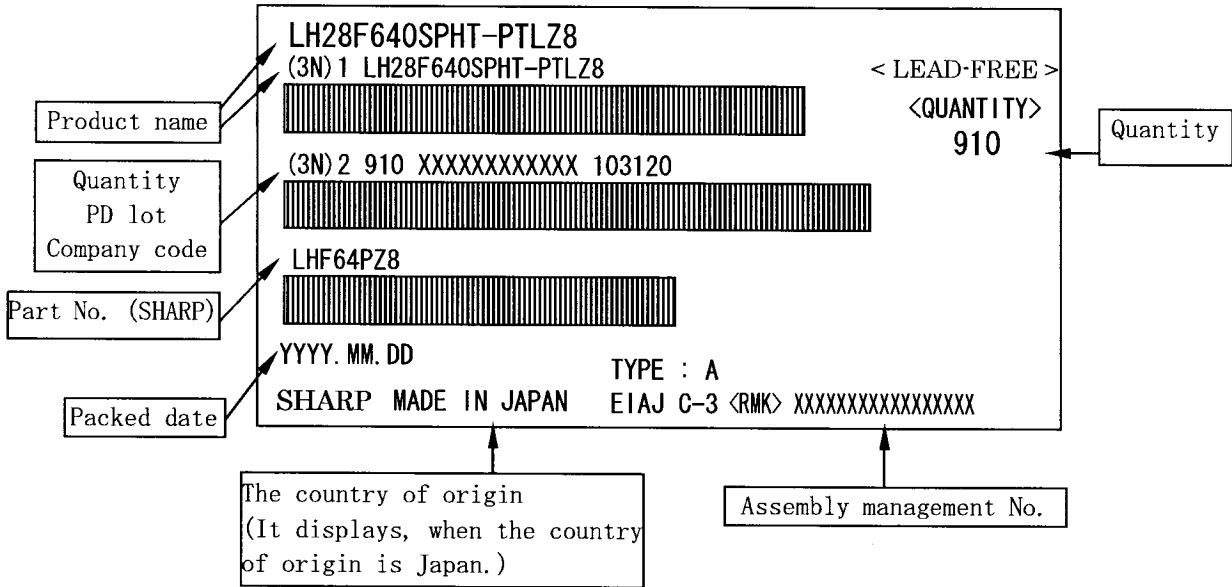Inner carton – Outer dimensions : 360×150×95
Outer carton – Outer dimensions : 390×335×230

NOTE There is a possibility different from this
      specification when the number of shipments
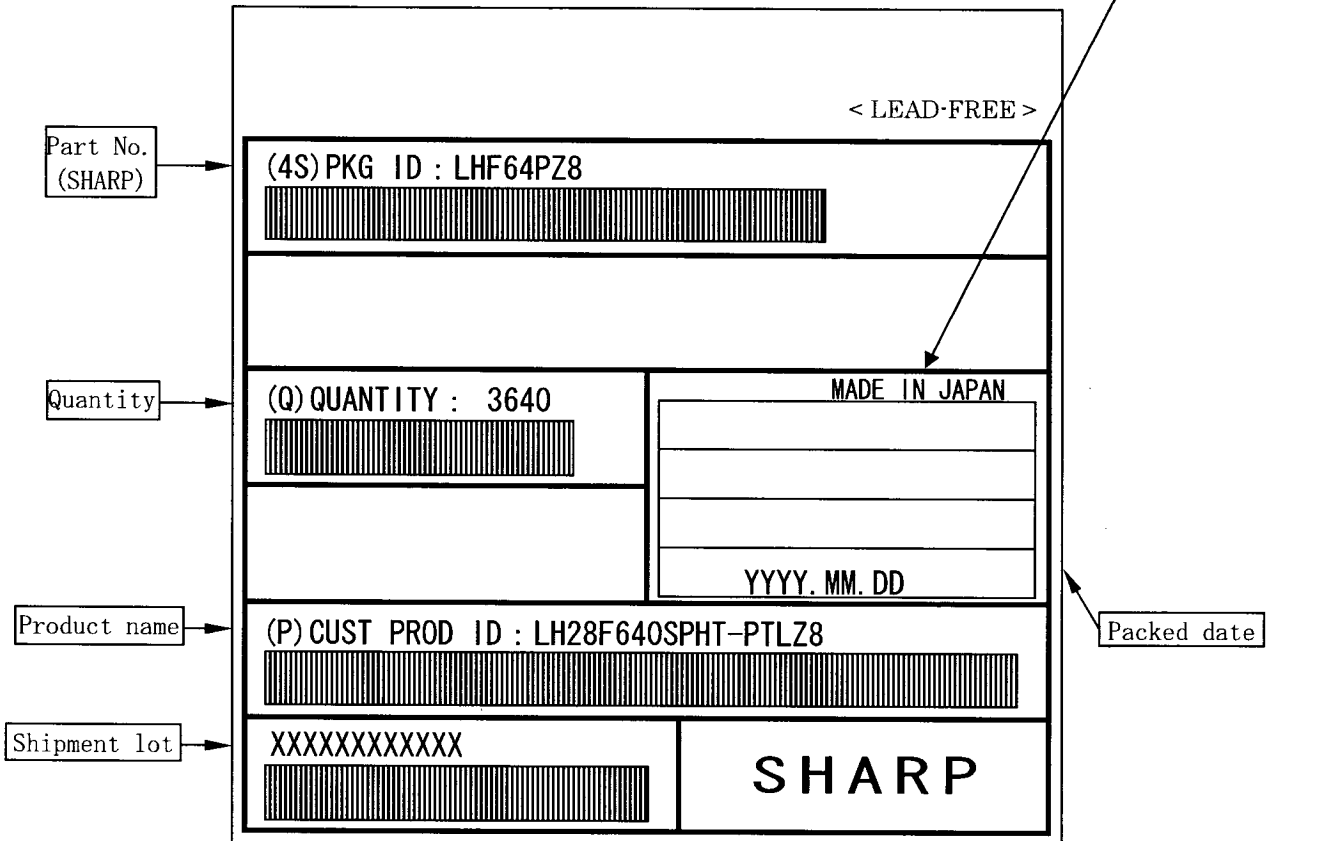   is fractions.

NAME	Packing specifications		
DRAWING NO.	BJ433d	UNIT	mm

(Note) The <LEAD-FREE> display shows a lead-free article.

Inner carton label

LH28F640SPHT-PTLZ8
(3N)1 LH28F640SPHT-PTLZ8

< LEAD-FREE >
<QUANTITY>
910

(3N)2 910 XXXXXXXXXXXX 103120

LHF64PZ8

YYYY. MM. DD

TYPE : A

SHARP MADE IN JAPAN   EIAJ C-3 <RMK> XXXXXXXXXXXXXXXXX

Product name → Product name
Quantity PD lot Company code
Part No. (SHARP)
Packed date
Quantity → 910

The country of origin
(It displays, when the country of origin is Japan.)

Assembly management No.

The country of origin
(It displays, when the country of origin is Japan.)

Outer carton label

< LEAD-FREE >

(4S)PKG ID : LHF64PZ8

(Q)QUANTITY : 3640

MADE IN JAPAN

YYYY. MM. DD

(P)CUST PROD ID : LH28F640SPHT-PTLZ8

XXXXXXXXXXXX

SHARP

Part No. (SHARP)
Quantity
Product name
Shipment lot
Packed date

(Former) EIAJ B Standard conforming

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.
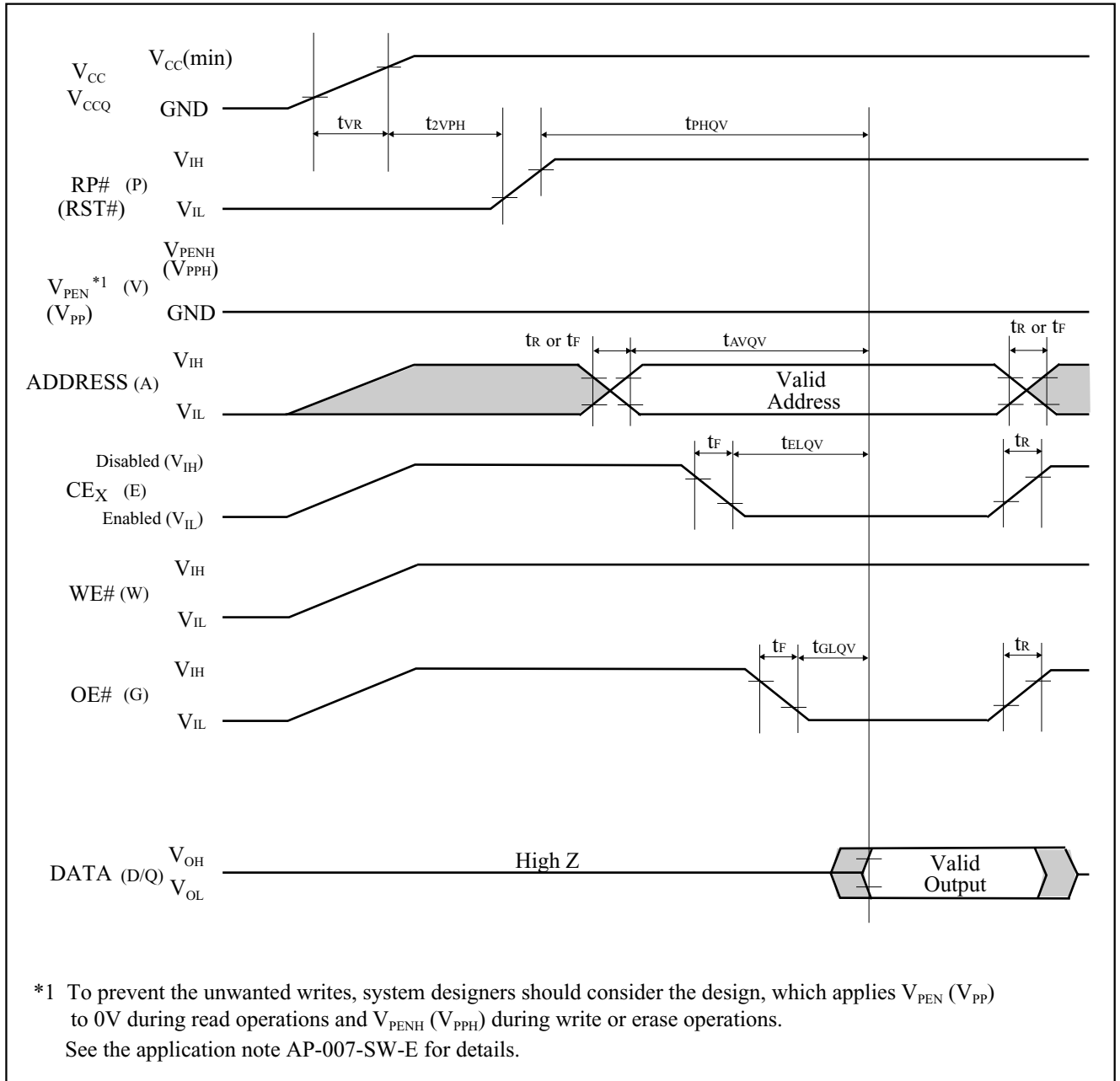

*1 To prevent the unwanted writes, system designers should consider the design, which applies V_{PEN} (V_{PP}) to 0V during read operations and V_{PENH} (V_{PPH}) during write or erase operations. See the application note AP-007-SW-E for details.

Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the "ELECTRICAL SPECIFICATIONS" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	V_{CC} Rise Time	1	0.5	30000	µs/V
t_R	Input Signal Rise Time	1, 2		1	µs/V
t_F	Input Signal Fall Time	1, 2		1	µs/V

NOTES:
1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

A-1.2   Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).
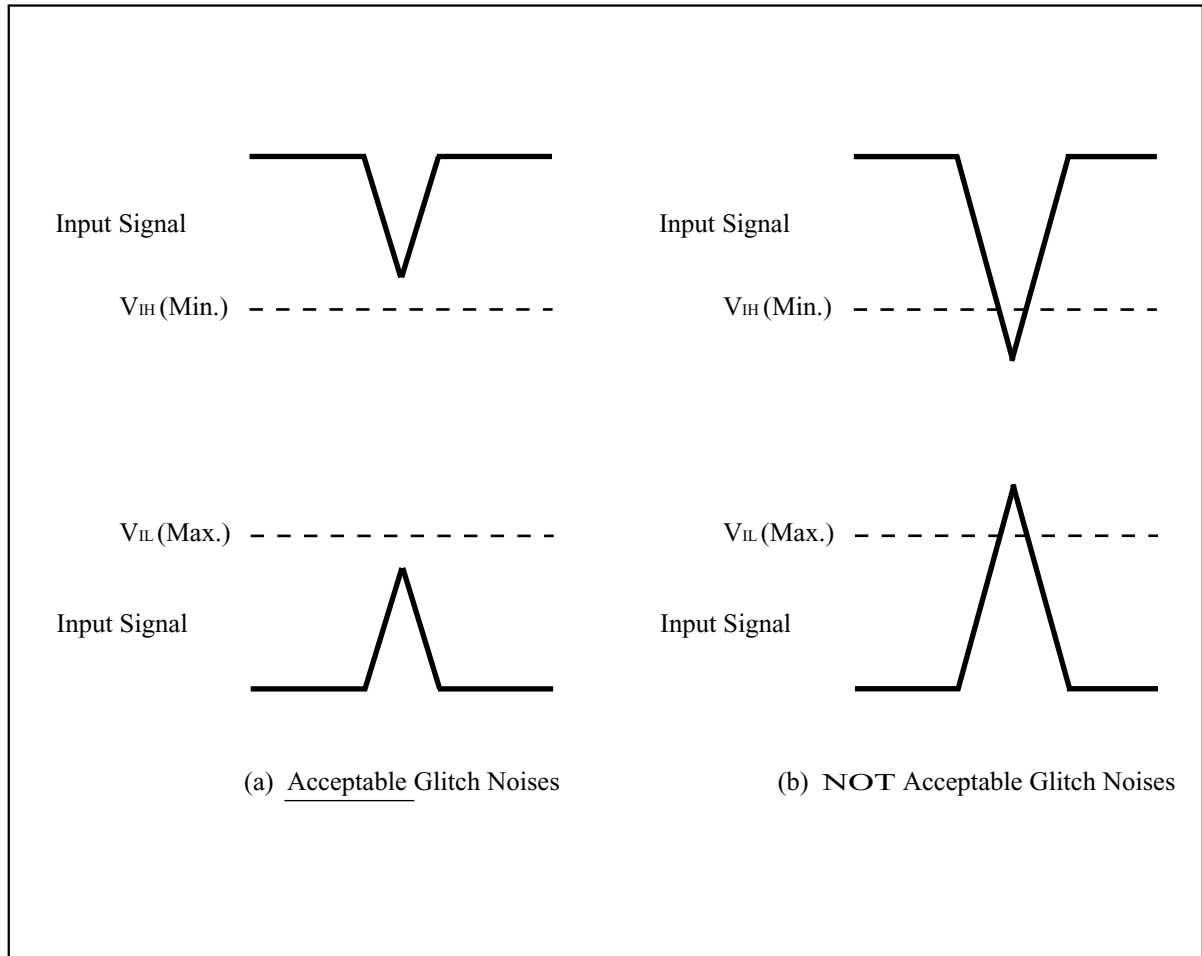

Input Signal

V_{IH} (Min.)

V_{IL} (Max.)

Input Signal

Input Signal

V_{IH} (Min.)

V_{IL} (Max.)

Input Signal

(a) Acceptable Glitch Noises

(b) NOT Acceptable Glitch Noises

Figure A-2. Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

SHARP

A-2 RELATED DOCUMENT INFORMATION[1]

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE:
1. International customers should contact their local SHARP or distribution sales office.

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