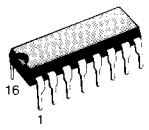
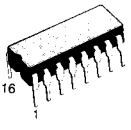
3-STATE HEX BUFFERS

DESCRIPTION

These devices are high-speed Hex Buffers with 3-state outputs. They are organized as single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable ($\overline{E}$) is LOW.
When the output Enable input ($\overline{E}$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedence state to avoid high currents that woud exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices, whose outputs are tied together, are disigned so there is no overlap.



B1
Plastic Package



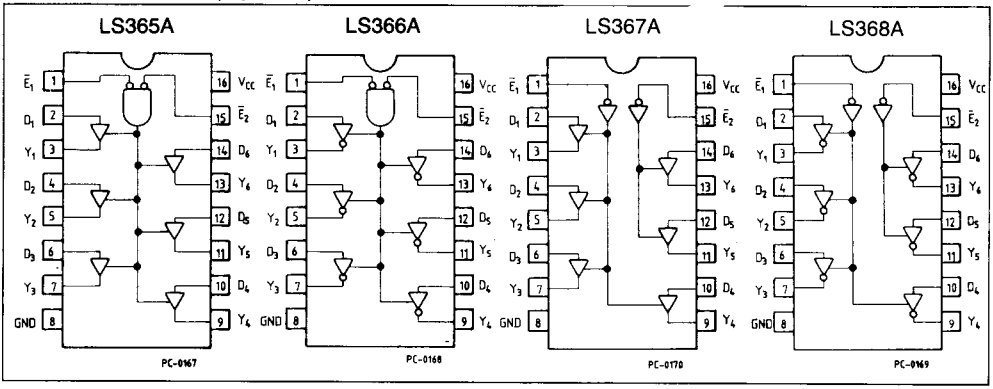
D1/D2
Ceramic Package

M1
Micro Package

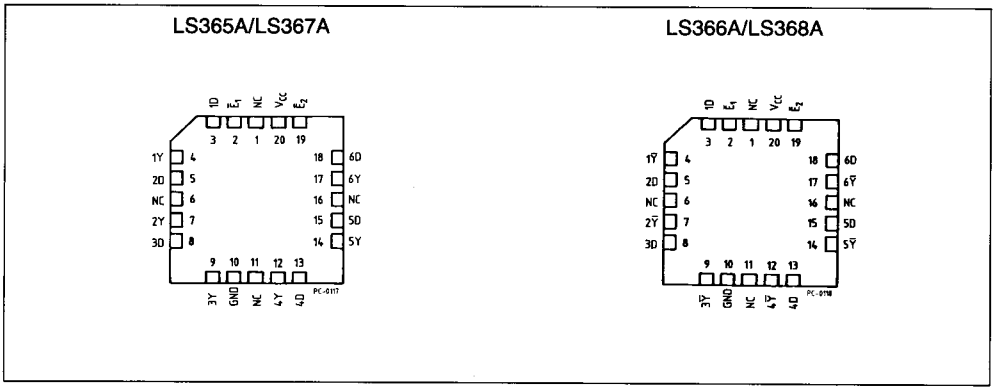
C1
Plastic Chip Carrier

ORDERING NUMBERS:
T54LSXXXX D2
T74LSXXXX D1
T74LSXXXX B1
T74LSXXXX C1
T74LSXXXXM1

PIN CONNECTION (top view) DUAL IN LINE



CHIP CARRIER



TRUTH TABLES

LS365A

INPUTS			OUTPUT
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	L
L	L	H	H
H	X	X	(Z)
X	H	X	(Z)

LS366A

INPUTS			OUTPUT
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)

LS367A

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

LS368A

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	H
L	H	L
H	X	(Z)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS365A/366A/367A/368AD2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS365A/366A/367A/368AXX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Typ.	Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.4	3.4		I_{OH} = −1.0mA, V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.4	3.1		I_{OH} = −2.6mA, V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 12mA, V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 24mA, V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{OZH}	Output Off Current HIGH				20	V_{CC} = MAX, V_{OUT} = 2.7V, $V_{\overline{E}}$ = 2.0V	μA
I_{OZL}	Output Off Current LOW				−20	V_{CC} = MAX, V_{OUT} = 0.4V, $V_{\overline{E}}$ = 2.0V	μA
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V	μA
I_{IL}	Input LOW Current	D Inputs			−20	V_{CC} = MAX, V_{IN} = 0.5V Either E Input at 2V	μA
					−0.4	V_{CC} = MAX, V_{IN} = 0.4V Both E Inputs at 0.4V	mA
		E Inputs			−0.4		mA
I_{OS}	Output Short Circuit Current (Note 2)		−40		−225	V_{CC} = MAX, V_{OUT} = 0V	mA
I_{CC}	Power Supply Current LS365A/367A			13.5	24	V_{CC} = MAX, V_{IN} = 0V, $V_{\overline{E}}$ = 4.5V	mA
	LS366A/368A			11.8	21		

Notes:
1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the device type.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter	Limits LS365A/367A Min.	Typ.	Max.	LS366A/368A Min.	Typ.	Max.	Test Conditions	Units
t_{PLH} t_{PHL}	Propagation Delay,		10 9.0	16 22		7.0 12	15 18	V_{CC} = 5.0V C_L = 45pF R_L 667Ω	ns
t_{PLH} t_{PHL}	Output Enable Time		19 24	35 40		18 28	35 45		ns
t_{PLH} t_{PHL}	Output Disable Time			30 35			32 35	V_{CC} = 5.0V C_L = 5.0pF	ns

AC WAVEFORMS

Fig. 1

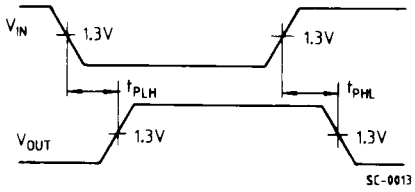


Fig. 2

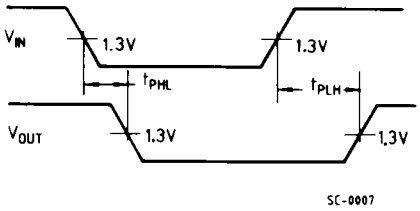


Fig. 3

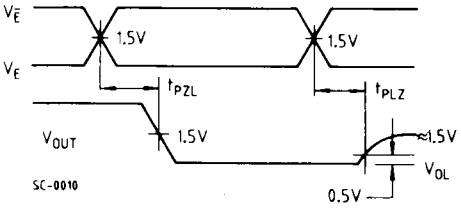
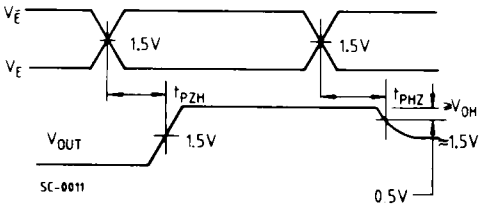
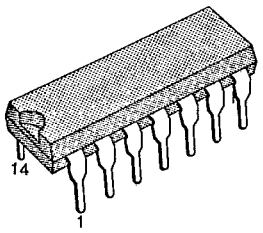
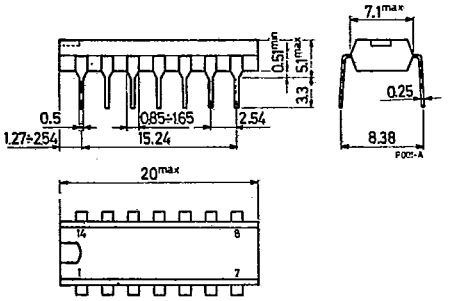


Fig. 4

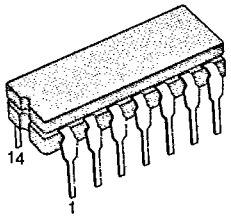


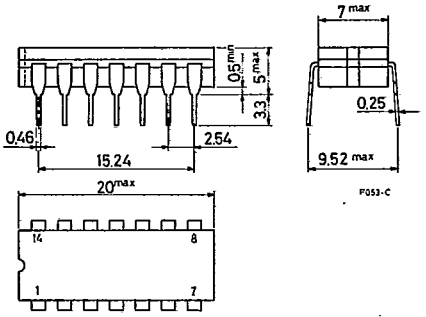
14-LEAD PLASTIC DIP



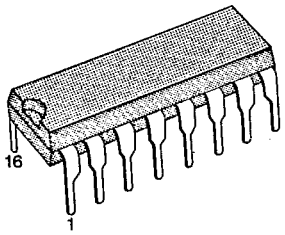


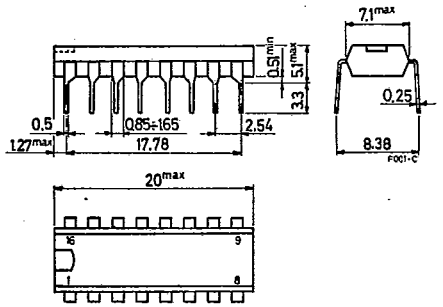
14-LEAD CERAMIC DIP





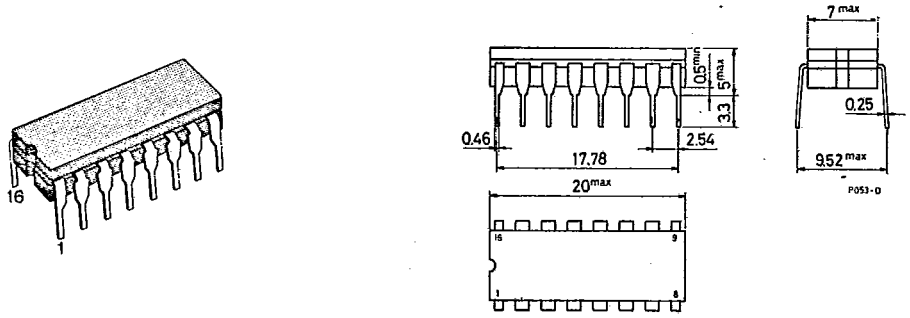
16-LEAD PLASTIC DIP



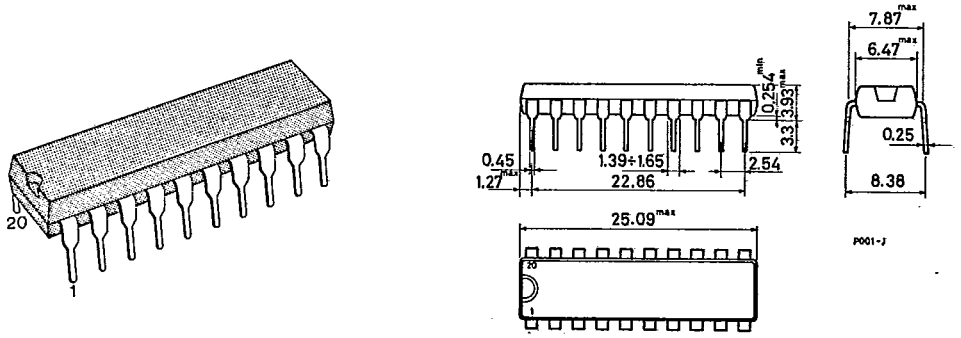


Packages

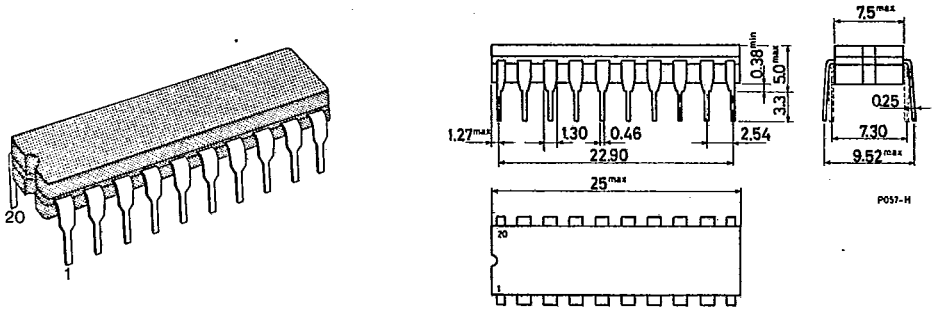
16-LEAD CERAMIC DIP



20-LEAD PLASTIC DIP

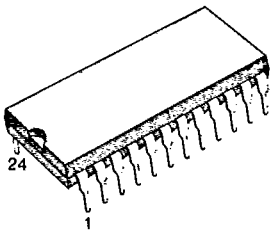


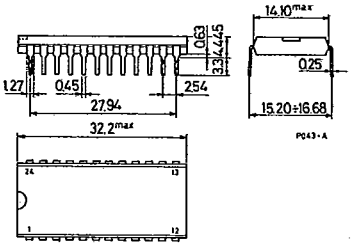
20-LEAD CERAMIC DIP



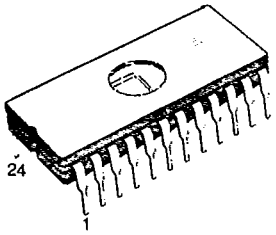
Packages

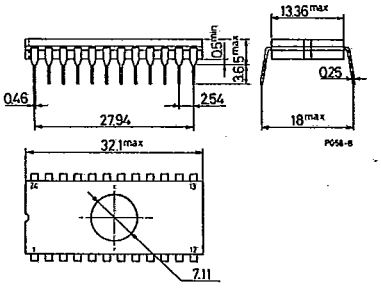
24-LEAD PLASTIC DIP



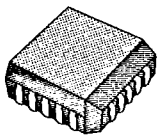


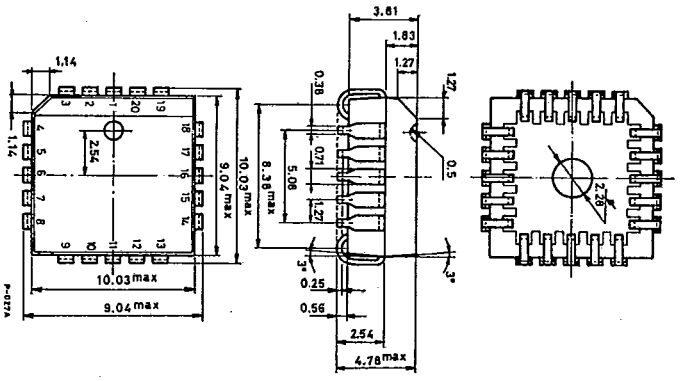
24-LEAD CERAMIC DIP





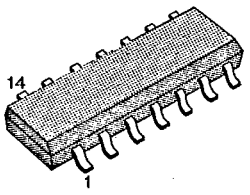
CHIP CARRIER 20 LEAD PLASTIC

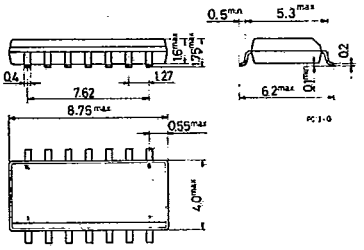




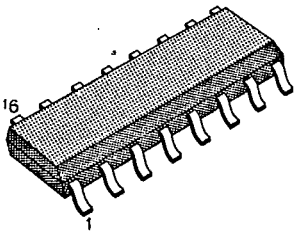
Packages

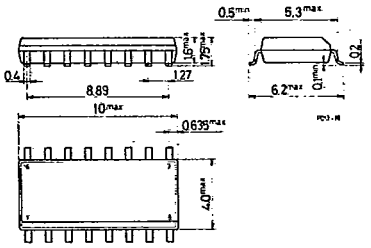
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.