

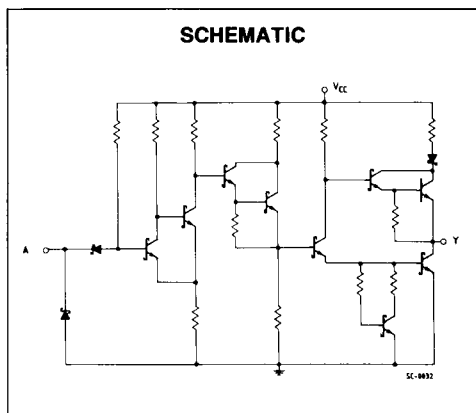


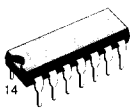
HEX SCHMITT TRIGGER INVERTER

DESCRIPTION

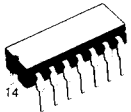
The T54LS14/T74LS14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater a noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter that drives a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.







B1
Plastic Package



D1/D2
Ceramic Package



M1
Micro Package



C1
Plastic Chip Carrier

ORDERING NUMBERS:

T54LS14 D2	T74LS14 C1
T74LS14 D1	T74LS14 M1
T74LS14 B1	

PIN CONNECTION
(top view)

DUAL IN LINE

PC-0028

CHIP CARRIER

PC-0081

NC = No Internal Connection



LOGIC DIAGRAM AND TRUTH TABLE



A	Y
L	H
H	L

L = LOW Voltage Level
H = HIGH Voltage Level

ABSOLUTE MAXIMUM RATINGS

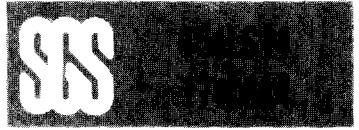
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	Input Voltage, Applied to Input	- 0.5 to 15	V
V_O	Output Voltage, Applied to Output	- 0.5 to 10	V
I_I	Input Current, Into Inputs	- 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS14D2	4.5 V	5.0 V	5.5 V	- 55°C to + 125°C
T74LS14XX	4.75 V	5.0 V	5.25 V	0°C to + 70°C

XX = package type.



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Conditions (Note 1)	Units
		Min.	Typ.	Max.		
V_{T+}	Positive-Going Threshold Voltage	1.4	1.6	1.9	$V_{CC} = 5.0V$	V
V_{T-}	Negative-Going Threshold Voltage	0.5	0.8	1.0	$V_{CC} = 5.0V$	V
$V_{T+} - V_{T-}$	Hysteresis	0.4	0.8		$V_{CC} = 5.0V$	V
V_{CD}	Input Clamp Diode Voltage		-0.65	-1.5	$V_{CC} = \text{MIN}, I_{IN} = -18\text{mA}$	V
V_{OH}	Output HIGH Voltage	54	2.5	3.4	$V_{CC} = \text{MIN}, I_{OH} = -400\mu\text{A}, V_{IN} = 0.5V$	V
		74	2.7	3.4		
V_{OL}	Output LOW Voltage	54,74	0.25	0.4	$I_{OL} = 4.0\text{mA}$ $V_{CC} = \text{MIN}, V_{IN} = 1.9V$	V
		74	0.35	0.5		
I_{T+}	Input Current at Positive-Going Threshold		-0.14		$V_{CC} = 5.0V, V_{IN} = V_{T+}$	mA
I_{T-}	Input Current at Negative-Going Threshold		-0.18		$V_{CC} = 5.0V, V_{IN} = V_{T-}$	mA
I_{IH}	Input HIGH Current		1.0	20 0.1	$V_{CC} = \text{MAX}, V_{IN} = 2.7V$ $V_{CC} = \text{MAX}, V_{IN} = 7.0V$	μA mA
I_{IL}	Input LOW Current			-0.4	$V_{CC} = \text{MAX}, V_{IN} = 0.4V$	mA
I_{OS}	Output Short Circuit Current (Note 2)	-20		-100	$V_{CC} = \text{MAX}, V_{OUT} = 0V$	mA
I_{CCH}	Supply Current HIGH		8.6	16	$V_{CC} = \text{MAX}, V_{IN} = 0V$	mA
I_{CCL}	Supply Current LOW		12	21	$V_{CC} = \text{MAX}, V_{IN} = 4.5V$	mA

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_{PLH}	Turn Off Delay, Input to Output		15	22	$V_{CC} = 5.0V$ $C_L = 15\text{pF}$	ns
t_{PHL}	Turn On Delay, Input to Output		15	22		ns

Notes:

- 1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2) Not more than one output should be shorted at a time.
- 3) Typical values are at $V_{CC} = 5.0V, T_A = 25^\circ\text{C}$.



T54LS14
T74LS14

Fig. 1

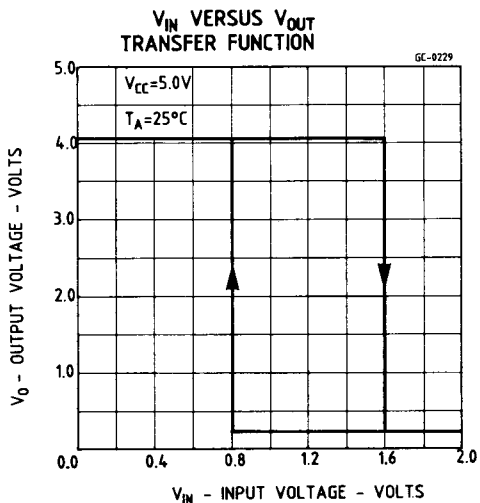


Fig. 3

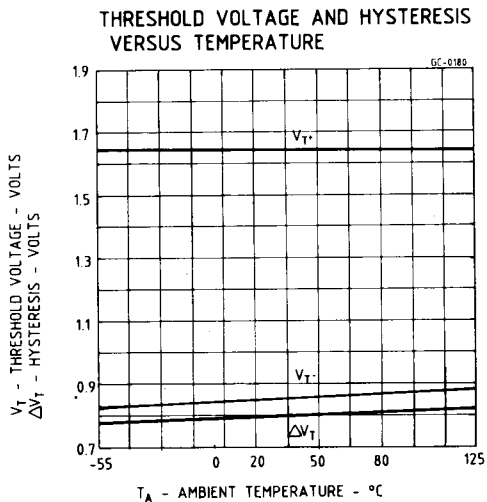


Fig. 2

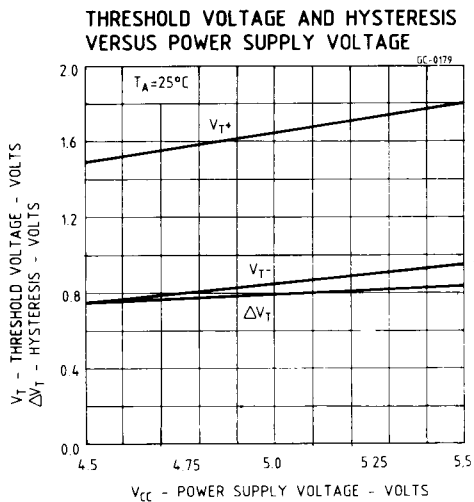


Fig. 4

