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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

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# MOS FIELD EFFECT TRANSISTOR NP20P06SLG

# SWITCHING P-CHANNEL POWER MOSFET

#### DESCRIPTION

The NP20P06SLG is P-channel MOS Field Effect Transistor designed for high current switching applications.

#### ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE		
NP20P06SLG-E1-AY Note					
NP20P06SLG-E2-AY Note	Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZK)		

Note Pb-free (This product does not contain Pb in external electrode.)

#### FEATURES

Super low on-state resistance

 $R_{DS(on)1} = 48 \text{ m}\Omega \text{ MAX.}$  (V<sub>GS</sub> = -10 V, I<sub>D</sub> = -10 A)

 $R_{DS(on)2}$  = 64 m $\Omega$  MAX. (VGs = -4.5 V, ID = -10 A)

- Low input capacitance
  - Ciss = 1650 pF TYP.
- Built-in gate protection diode

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	VDSS	-60	V
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V
Drain Current (DC) (Tc = 25°C)	D(DC)	∓20	А
Drain Current (pulse) <sup>Note1</sup>	D(pulse)	∓60	Α
Total Power Dissipation (Tc = $25^{\circ}$ C)	<b>P</b> T1	38	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	Pt2	1.2	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Single Avalanche Current Note2	las	17	Α
Single Avalanche Energy <sup>Note2</sup>	Eas	28	mJ

#### **Notes 1.** PW $\leq$ 10 $\mu$ s, Duty Cycle $\leq$ 1%

**2.** Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = -30 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = -20  $\rightarrow$  0 V

#### THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	3.9	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	125	°C/W

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(TO-252)

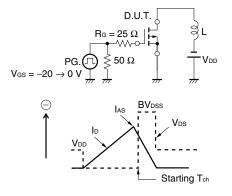
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V			-10	μA
Gate Leakage Current	lgss	V <sub>GS</sub> = ∓20 V, V <sub>DS</sub> = 0 V			∓10	μA
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS}$ = $V_{GS}$ , $I_D$ = -250 $\mu$ A	-1.0	-1.6	-2.5	V
Forward Transfer Admittance Note	<b>y</b> fs	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -10 A	7	14		S
Drain to Source On-state Resistance <sup>Note</sup>	RDS(on)1	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -10 A		36	48	mΩ
	RDS(on)2	V <sub>GS</sub> = −4.5 V, I <sub>D</sub> = −10 A		42	64	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = -10 V,		1650		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V,		200		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		130		pF
Turn-on Delay Time	td(on)	$V_{DD} = -30 V, I_D = -10 A,$		8		ns
Rise Time	tr	V <sub>GS</sub> = -10 V,		8		ns
Turn-off Delay Time	td(off)	R <sub>G</sub> = 0 Ω		160		ns
Fall Time	tr			80		ns
Total Gate Charge	QG	V <sub>DD</sub> = -48 V,		34		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = -10 V,		4		nC
Gate to Drain Charge	Qgd	I <sub>D</sub> = -20 A		9		nC
Body Diode Forward Voltage Note	V <sub>F(S-D)</sub>	IF = -20 A, V <sub>GS</sub> = 0 V		0.95	1.5	V
Reverse Recovery Time	trr	IF = -20 A, VGS = 0 V,		38		ns
Reverse Recovery Charge	Qrr	di/dt = −100 A/µs		51		nC

#### ELECTRICAL CHARACTERISTICS (TA = 25°C)

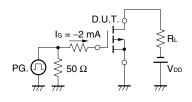
**Note** Pulsed test PW  $\leq$  350  $\mu$ s, Duty Cycle  $\leq$  2%

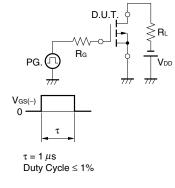
#### TEST CIRCUIT 1 AVALANCHE CAPABILITY

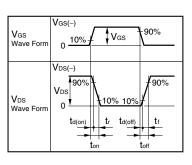
#### **TEST CIRCUIT 2 SWITCHING TIME**



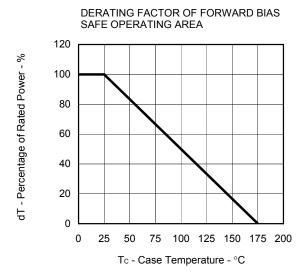
# TEST CIRCUIT 3 GATE CHARGE



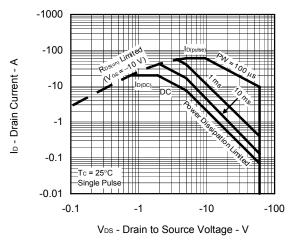


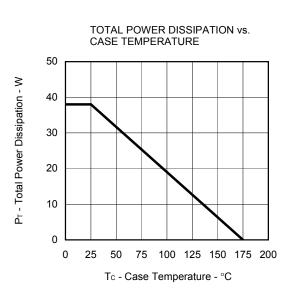


# TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

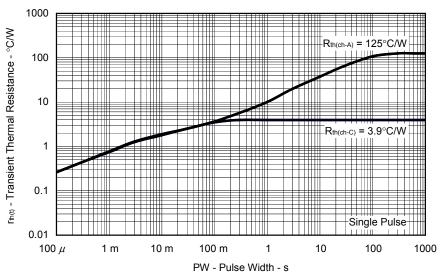




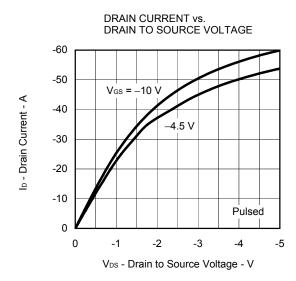




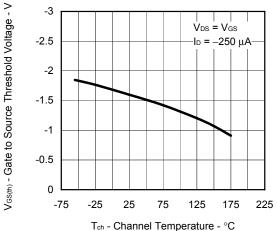


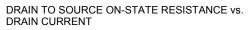


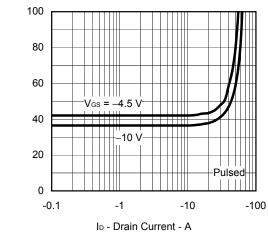
Data Sheet D19076EJ1V0DS

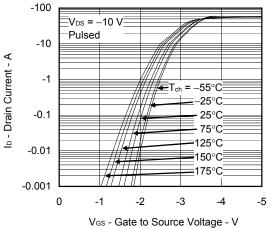




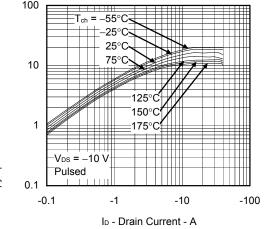


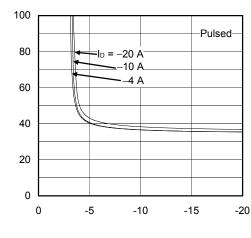






FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT





DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



Data Sheet D19076EJ1V0DS

 $R_{DS(cn)}$  - Drain to Source On-state Resistance -  $m\Omega$ 

 $\mathsf{R}_{\mathsf{DS}(m)}$  - Drain to Source On-state Resistance -  $m\Omega$ 

100

| yfs | - Forward Transfer Admittance - S

FORWARD TRANSFER CHARACTERISTICS

1000

100

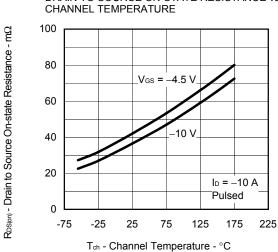
10

-0.01

0

0.5

 $V_{\text{F(S-D)}}$  - Source to Drain Voltage - V



SWITCHING CHARACTERISTICS

td(off)

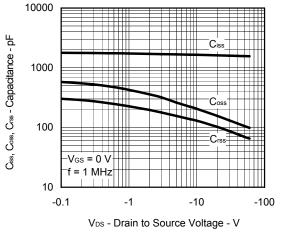
tſ

tr

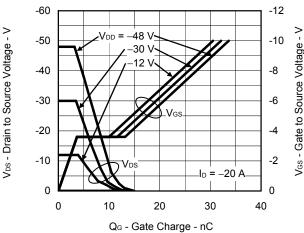
td(on

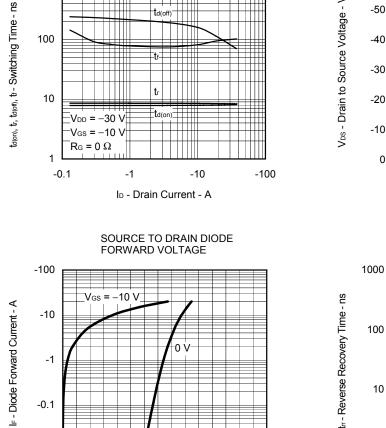
DRAIN TO SOURCE ON-STATE RESISTANCE vs.

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



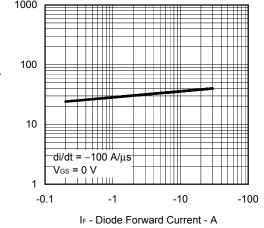


1

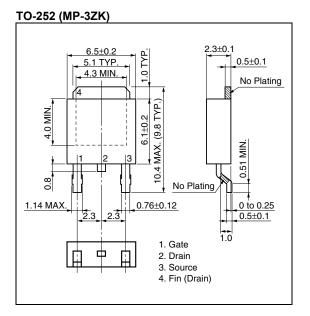
Pulsed

1.5

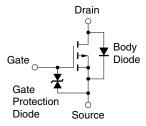
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



### PACKAGE DRAWING (Unit: mm)



#### EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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