

CMOS 7-Stage Binary Counter

With Buffered Reset

The RCA-CD4024A consists of an INPUT PULSE shaping circuit, RESET line driver circuitry, and seven binary counter stages. The counter is reset to "zero" by a high level on the RESET input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each INPUT PULSE.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 12-lead hermetic TO-5-style package (T suffix) 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- Frequency-dividing circuits
- Time-delay circuits
- Counter control
- D/A counter and switch on one chip

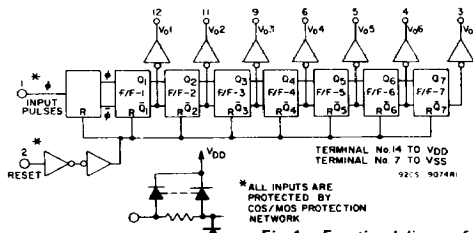


Fig. 1 - Functional diagram for CD4024AD, AE, AF.

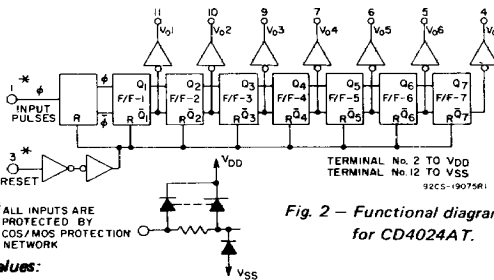
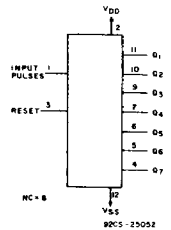
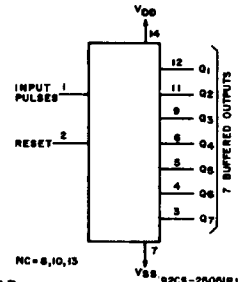


Fig. 2 - Functional diagram for CD4024AT.



MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T _{stg})	-65 to +150 °C
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPES (D, F, K, T, H)	-55 to +125 °C
PACKAGE TYPE E	-40 to +85 °C
DC SUPPLY-VOLTAGE RANGE, (V _{DD})	
(Voltages referenced to V _{SS} Terminal):	-0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P _D)	
FOR T _A = -40 to +60 °C (PACKAGE TYPE E)	500 mW
FOR T _A = +60 to +85 °C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T _A = -55 to +100 °C (PACKAGE TYPES D, F, K, T)	500 mW
FOR T _A = +100 to +125 °C (PACKAGE TYPES D, F, K, T)	Derate, Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V _{DD} + 0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

RECOMMENDED OPERATING CONDITIONS at T_A = 25 °C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V _{DD} (V)	LIMITS				UNITS
		D, F, K, T, H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range)		3	12	3	12	V
Clock Pulse Width, t _W	5 10	330 125	—	500 165	—	ns
Clock Input Frequency, f _{CL}	5 10	dc dc	1.5 4	dc 3	1	MHz
Clock Rise or Fall Time, t _{rCL} , t _{fCL}	5 10	15 15	— —	15 15	—	μs
Reset Pulse Width, t _W	5 10	500 300	—	600 350	—	ns

Features:

- Medium-speed operation
- . . 7-MHz (typ.) input pulse rate at V_{DD} - V_{SS} = 10 V
- Low high-and-low level output impedance
- . . 700Ω and 500Ω (typ.), respectively at V_{DD} - V_{SS} = 10 V
- Fully static operation
- Common reset
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

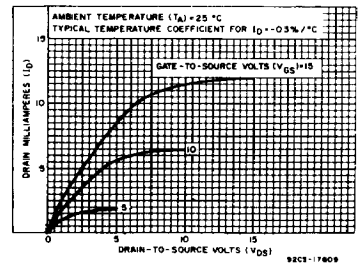


Fig. 3 - Typical output n-channel drain characteristics.

CD4024A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, T, H Packages				E Package				
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	+25		+125	-40	+25		+85	
Quiescent Device Current, I _Q Max.	-	-	5	5	0.3	5	300	50	0.5	50	700	μA
	-	-	10	10	0.5	10	600	100	1	100	1400	
	-	-	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V _{OL}	-	5	5	0 Typ.; 0.05 Max.								V
	-	10	10	0 Typ.; 0.05 Max.								
High Level, V _{OH}	-	0	5	4.95 Min.; 5 Typ.								V
	-	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V _{NL}	4.2	-	5	1.5 Min.; 2.25 Typ.								V
	9	-	10	3 Min.; 4.5 Typ.								
Inputs High, V _{NH}	0.8	-	5	1.5 Min.; 2.25 Typ.								V
	1	-	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V _{NML}	4.5	-	5	1 Min.								V
	9	-	10	1 Min.								
Inputs High, V _{NMH}	0.5	-	5	1 Min.								V
	1	-	10	1 Min.								
Output Drive Current: n-Channel (Sink), I _{DN} Min.	0.5	-	5	0.31	0.5	0.25	0.175	0.15	0.5	0.12	0.095	mA
	0.5	-	10	0.62	1	0.5	0.35	0.31	1	0.25	0.2	
p-Channel (Source) I _{DP} Min.	4.5	-	5	-0.19	-0.3	-0.15	-0.105	-0.145	-0.3	-0.12	-0.095	mA
	9.5	-	10	-0.45	-0.7	-0.35	-0.25	-0.31	-0.7	-0.25	-0.2	
Input Leakage Current, I _{IL} , I _{IH}	Any Input			±10 ⁻⁵ Typ.; ±1 Max.								μA
	-	-	15									

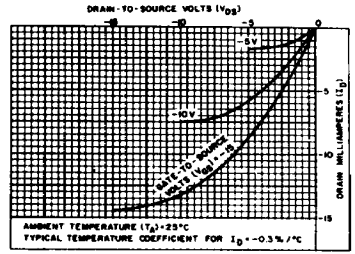


Fig. 4 - Typical output p-channel drain characteristics.

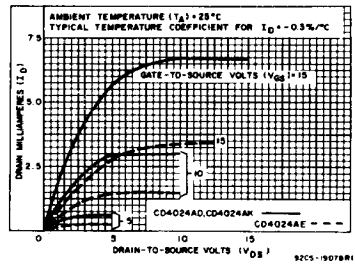


Fig. 5 - Minimum output n-channel drain characteristics.

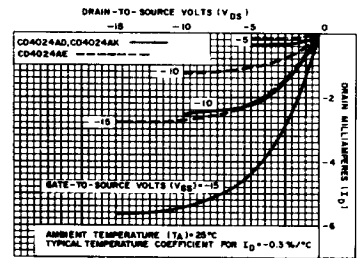
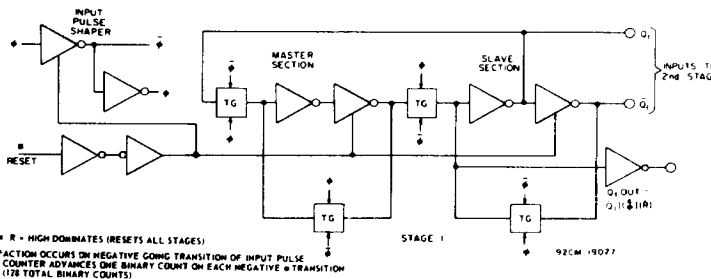


Fig. 6 - Minimum output p-channel drain characteristics.



* R = HIGH DOMINATES (RESETS ALL STAGES)
 * ACTION OCCURS ON NEGATIVE GOING TRANSITION OF INPUT PULSE
 COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE GOING TRANSITION
 (128 TOTAL BINARY COUNTS)

EQUATIONS FOR STAGES 2 TO 7

$$\begin{aligned}
 Q_{2OUT} &= (\bar{I}_2)(Q_1)(\bar{R}) & Q_{5OUT} &= (\bar{I}_5)(Q_1)(Q_2)(Q_3)(Q_4)(\bar{R}) \\
 Q_{3OUT} &= (\bar{I}_3)(Q_1)(Q_2)(\bar{R}) & Q_{6OUT} &= (\bar{I}_6)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(\bar{R}) \\
 Q_{4OUT} &= (\bar{I}_4)(Q_1)(Q_2)(Q_3)(\bar{R}) & Q_{7OUT} &= (\bar{I}_7)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(Q_6)(\bar{R})
 \end{aligned}$$

Fig. 7 - Logic block diagram (pulse shaper and 1 binary stage).

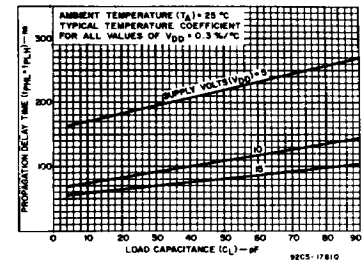


Fig. 8 - Typical propagation delay time vs. C_L.

CD4024A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 15\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, T, H Packages			E Package			
		VDD (V)	Min.	Typ.	Max.	Min.	Typ.	
φ INPUT OPERATION								
Propagation Delay Time; t_{PLH}, t_{PHL}	5	—	175	350	—	175	400	ns
	10	—	80	125	—	80	150	
Transition Time; t_{THL}, t_{TLH}	5	—	175	225	—	175	250	ns
	10	—	80	125	—	80	150	
Maximum Pulse Input Frequency, f_ϕ	5	1.5	2.5	—	1	2.5	—	MHz
	10	4	7	—	3	7	—	
Minimum Input Pulse Width, t_W	5	—	200	330	—	200	500	ns
	10	—	140	125	—	140	165	
Input Pulse Rise & Fall Time, t_r, t_f	5	—	—	15	—	—	15	μs
	10	—	—	10	—	—	10	
Average Input Capacitance, C_i	Any Input	—	5	—	—	5	—	pF
RESET OPERATION								
Propagation Delay Time; T_{PLH}, T_{PHL}	5	—	500	700	—	500	800	ns
	10	—	250	350	—	250	400	
Minimum Reset Pulse Width; t_W	5	—	375	500	—	375	600	ns
	10	—	200	300	—	200	350	

* Propagation delay time is from input pulse to Q_1 output.

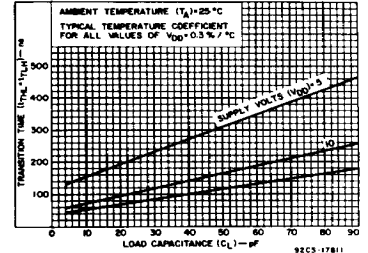


Fig. 9 — Typical transition time vs. C_L .

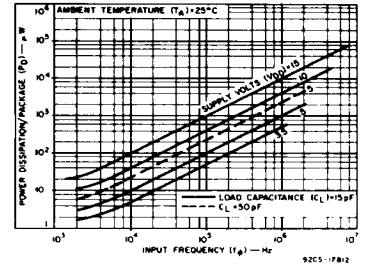


Fig. 10 — Typical dissipation characteristics.

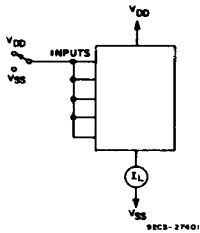


Fig. 12 — Quiescent-device-current test circuit.

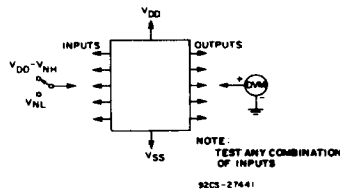


Fig. 13 — Noise-immunity test circuit.

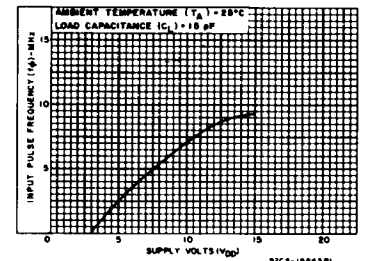


Fig. 11 — Typical input pulse frequency vs. V_{DD} .

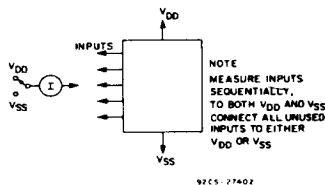


Fig. 14 — Input-leakage-current test circuit.