

CD4013B Types

CMOS Dual 'D'-Type Flip-Flop

High-Voltage Types (20-Volt Rating)

The RCA-CD4013B consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and \bar{Q} outputs. These devices can be used for shift register applications, and, by connecting \bar{Q} output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

The CD4013B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Set-Reset capability
- Static flip-flop operation — retains state indefinitely with clock level either "high" or "low"
- Medium-speed operation — 16 MHz (typ.) clock toggle rate at 10V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range): 1 V at $V_{DD}=5$ V
2 V at $V_{DD}=10$ V
2.5 V at $V_{DD}=15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Registers, counters, control circuits

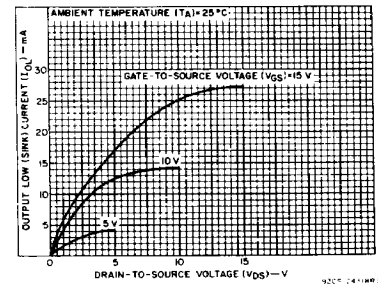
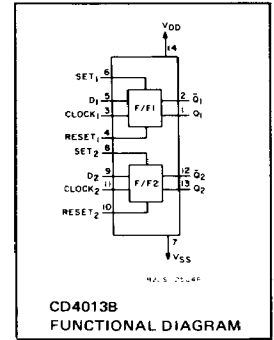


Fig. 1 — Typical output low (sink) current characteristics.

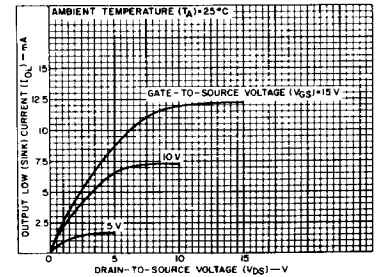


Fig. 2 — Minimum output low (sink) current characteristics.

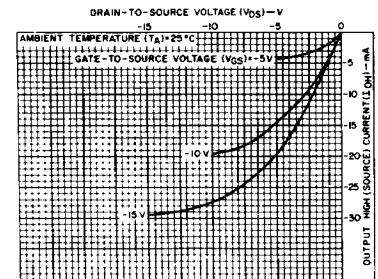


Fig. 3 — Typical output high (source) current characteristics.

RECOMMENDED OPERATING CONDITIONS

At $T_A = 25^\circ\text{C}$, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply Voltage Range (For $T_A =$ Full Package Temperature Range)	—	3	18	V
Data Setup Time t_S	5	40	—	ns
	10	20	—	
Clock Pulse Width t_W	15	15	—	ns
	5	140	—	
Clock Input Frequency f_{CL}	10	60	—	MHz
	15	40	—	
Clock Rise or Fall Time $t_{rCL}, * t_{fCL}$	5	—	3.5	μ s
	10	—	70	
Set or Reset Pulse Width t_W	15	—	6	ns
	5	180	—	
	10	80	—	ns
	15	50	—	

*If more than one unit is cascaded in a parallel clocked operation, t_{fCL} should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	Values at -55,+25,+125 Apply to D,F,K,H Pkgs.				Values at -40,+25,+85 Apply to E Pkgs.			
				-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current I _{DD} Max.	-	0,5	5	1	1	30	30	-	0.02	1	μA
	-	0,10	10	2	2	60	60	-	0.02	2	
	-	0,15	15	4	4	120	120	-	0.02	4	
Output Low (Sink) Current, I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05				-	0	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5	4.95				4.95	5	-	V
	-	0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage, V _{IL} Max.	0.5,4.5	-	5	1.5				-	-	1.5	V
	1.9	-	10	3				-	-	3	
	1.5,13.5	-	15	4				-	-	4	
Input High Voltage, V _{IH} Min.	0.5,4.5	-	5	3.5				3.5	-	-	V
	1.9	-	10	7				7	-	-	
	1.5,13.5	-	15	11				11	-	-	
Input Current, I _{IN} Max.	-	0,18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

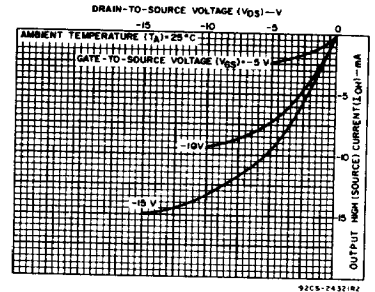


Fig. 4 - Minimum output high (source) current characteristics.

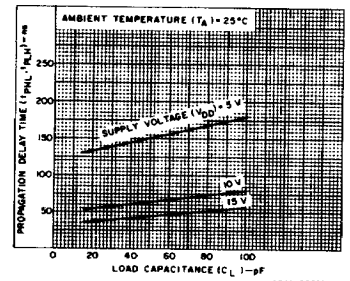


Fig. 5 - Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to Q).

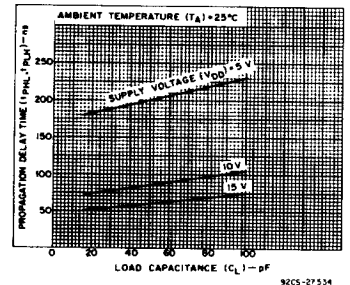


Fig. 6 - Typical propagation delay time vs. load capacitance (SET to Q or RESET to Q).

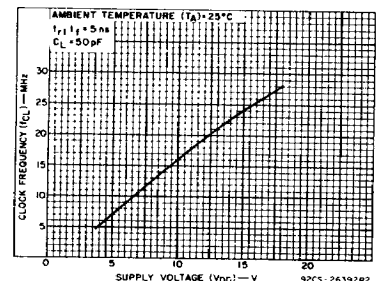


Fig. 8 - Typical maximum clock frequency vs. supply voltage.

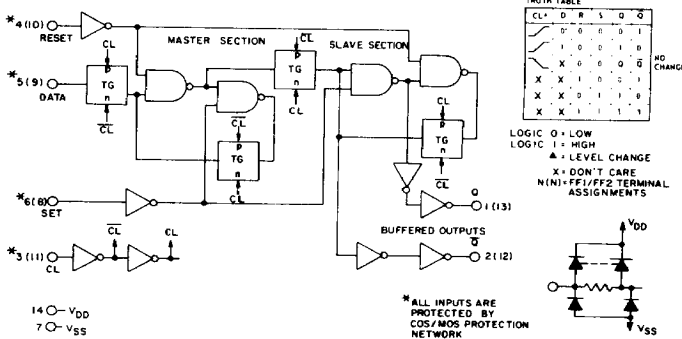


Fig. 7 - Logic diagram and truth table for CD4013B (one of two identical flip-flops).

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MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F, K)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$

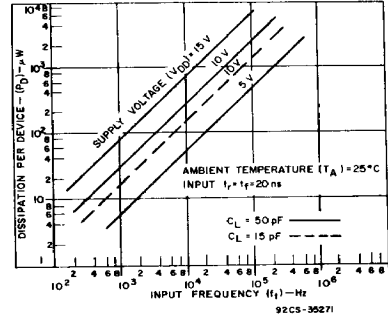


Fig. 9 - Typical power dissipation vs. frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ k Ω

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		V_{DD} (V)	MIN.	TYP.		MAX.
Propagation Delay Time: Clock to Q or \bar{Q} Outputs t_{PHL}, t_{PLH}		5	-	150	300	ns
		10	-	65	130	
		15	-	45	90	
Set to Q or Reset to \bar{Q} t_{PLH}		5	-	150	300	ns
		10	-	65	130	
		15	-	45	90	
Set to \bar{Q} or Reset to Q t_{PHL}		5	-	200	400	ns
		10	-	85	170	
		15	-	60	120	
Transition Time t_{THL}, t_{TLH}		5	-	100	200	ns
		10	-	50	100	
		15	-	40	80	
Maximum Clock Input Frequency Frequency # f_{CL}		5	3.5	7	-	MHz
		10	8	16	-	
		15	12	24	-	
Minimum Clock Pulse Width t_W		5	-	70	140	ns
		10	-	30	60	
		15	-	20	40	
Minimum Set or Reset Pulse Width t_W		5	-	90	180	ns
		10	-	40	80	
		15	-	25	50	
Minimum Data Setup Time t_S		5	-	20	40	ns
		10	-	10	20	
		15	-	7	15	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}		5	-	-	70	μs
		10	-	-	6	
		15	-	-	2	
Input Capacitance C_{IN}	Any Input		-	5	7.5	pF

#Input $t_r, t_f = 5$ ns.

TEST CIRCUITS

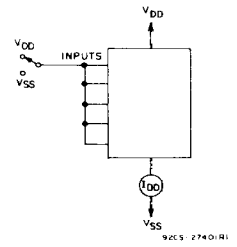


Fig. 10 - Quiescent device current.

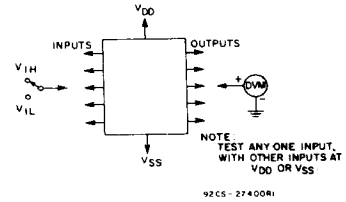


Fig. 11 - Input voltage.

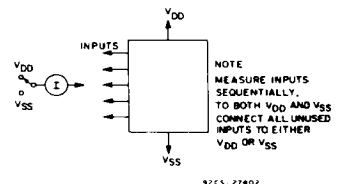


Fig. 12 - Input current.

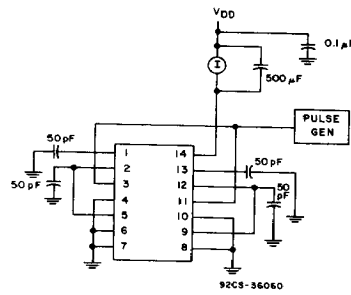
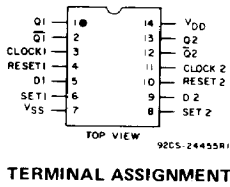
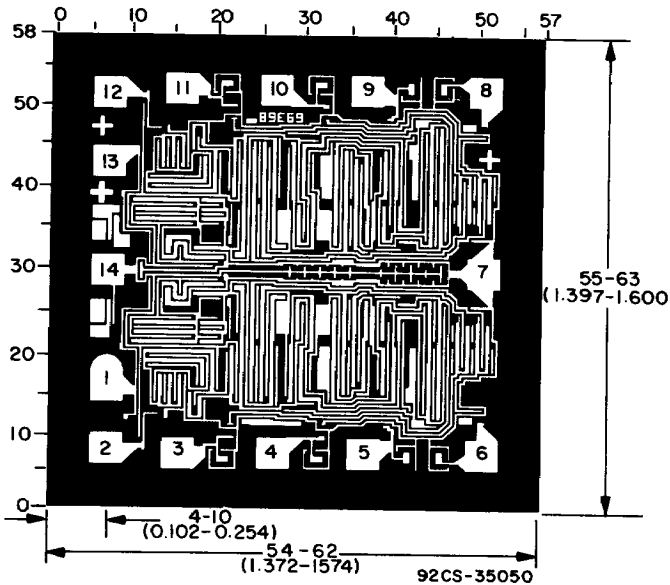


Fig. 13—Dynamic power dissipation test circuit.

DIMENSIONS AND PAD LAYOUT FOR CD4013BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to $+16$ mils applicable to the nominal dimensions shown.