QUALITY SEMICONDUCTOR, INC.

High-Performance CMOS Two Channel 4PST Switch

QS4A105Q

FEATURES

- Low on-resistance: $r_{DS(on)} = 5\Omega$
- Wide bandwidth: 1.3GHz (–3dB point)
- Crosstalk:
  –100dB @ 50KHz, –70dB @ 5MHz,
  –50dB @ 30MHz
- Off-isolation:
  –90dB @ 50KHz, –60dB @ 5MHz,
  –55dB @ 30MHz,
- Single 5V supply
- Bidirectional signal flow
- TTL compatible control inputs
- Ultra-low quiescent current: 3µA
- Switch turn on time of 6.5ns

APPLICATIONS

- High-speed video signal switching/routing
- HDTV-quality video signal routing
- Audio signal switching/routing
- Data acquisition
- ATE systems
- Telecomm routing
- Token Ring transceivers
- High-speed networking

GENERAL DESCRIPTION

The QS4A105Q is a high-performance CMOS Two-Channel 4PST switch with 3-state outputs. The low on-resistance of the QS4A105Q allows inputs to be connected to outputs with low insertion loss and high bandwidth.

The QS4A105Q with 1.3GHz bandwidth, makes it ideal for high-performance video signal switching, audio signal switching, and telecomm routing applications. Low power dissipation makes this device ideal for battery operated and remote instrumentation applications.

The QS4A105Q is offered in the QSOP package which has several advantages over conventional packages such as PDIP and SOIC including:

- Reduced signal delays due to denser component packaging on circuit boards
- Reduced system noise due to less pin inductance

Figure 1. Functional Block Diagram

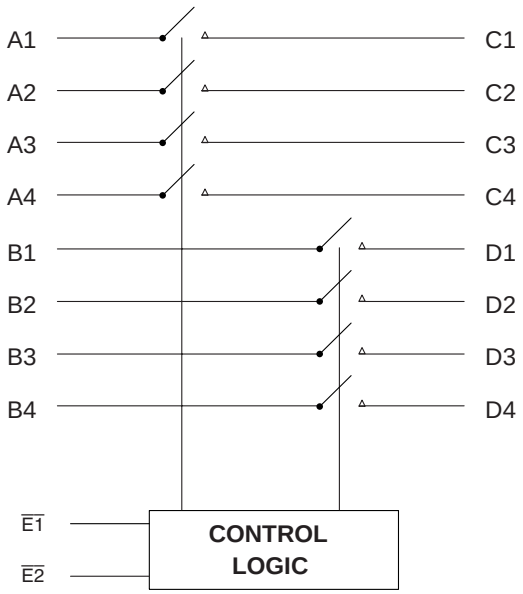


Figure 2. Pin Configuration

(All Pins Top View)

QSOP

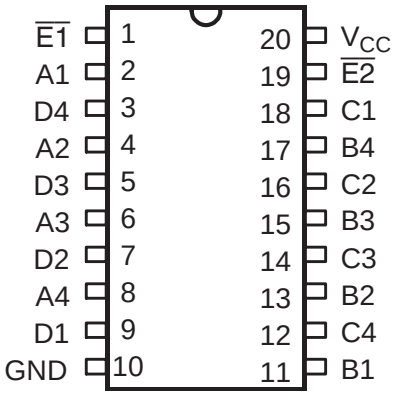


Table 1. Pin Definitions

Name	I/O	Description
$\overline{E1}$, $\overline{E2}$	I	Enable
A_N, B_N	I/O	Port A, Port B
C_N, D_N	I/O	Port C, Port D

Table 2. Function Table

$\overline{E1}$	$\overline{E2}$	A_N, C_N I/Os	B_N, D_N I/Os
H	H	Disconnected	Disconnected
L	H	$A_N = C_N$	Disconnected
H	L	Disconnected	$B_N = D_N$
L	L	$A_N = C_N$	$B_N = D_N$

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to +7.0V
DC Switch Voltage V_S	0V to +7.0V
Analog Input Voltage	0V to +7.0V
DC Input Voltage V_{IN}	0V to +7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.7 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: ABSOLUTE MAXIMUM RATINGS are those conditions beyond which damage to the device may occur. Exposure to these conditions or beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rating conditions is not implied.

Table 4. Power Supply Characteristics

Symbol	Parameter	Test Conditions	Max	Unit
I_{CC}	Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	3	µA

Table 5. Electrical Characteristics Over Operating Range

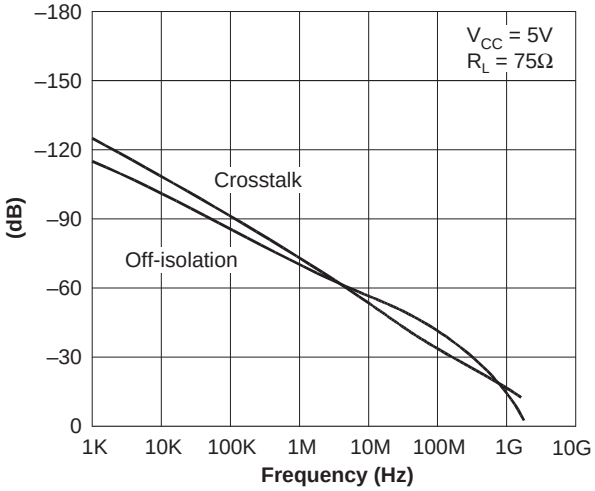
Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
Analog Switch						
V_{IN}	Analog Signal Range(2)		0	—	V_{CC}– 1	V
$r_{DS(on)}$	Drain-source On-resistance(2,3)	V_{CC} = Min., V_{IN} = 0.0V, I_{ON} = 30mA	—	5	7	Ω
		V_{CC} = Min., V_{IN} = 1.5V,	—	5.5	8	Ω
$\Delta r_{DS(on)}$	$r_{DS(on)}$ Matching Between Channels(2,3,4)	V_{CC} = Min., V_{IN} = 0.0V, I_{ON} = 30mA	—	1	4	Ω
		V_{CC} = Min., V_{IN} = 1.5V, I_{ON} = 15mA	—	1	—	Ω
$I_{C (OFF)}$	Channel Off Leakage Current	A_N, B_N = V_{CC} or 0V, C_N, D_N = 0V or V_{CC}, $\overline{E}$ = V_{CC}	—	1	—	nA
$I_{C (ON)}$	Channel On Leakage Current	A_N = B_N = C_N = D_N = 0V, Each Channel is Turned On Sequentially	—	1	—	nA
Digital Control						
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Pins	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Pins	—	—	0.8	V
Dynamic Characteristics						
$t_{ON(\overline{E})}$	Enable Turn-on Time $\overline{E}$ to A_N, B_N, C_N or D_N	R_L = 1KΩ, C_L = 100pF (See Figure 9)	0.5	—	6.5	ns
$t_{OFF(\overline{E})}$	Enable Turn-off Time $\overline{E}$ to A_N, B_N, C_N or D_N	R_L = 1KΩ, C_L = 100pF (See Figure 9)	0.5	—	6.0	ns
t_{PD}	Group Delay(2,5)	R_L = 1KΩ, C_L = 100pF	—	—	250	ps
f_{3dB}	–3 dB Bandwidth	V_{IN} = 0 to 1V, 1V p-p, R_L = 75Ω	—	1.3	—	GHz
	Off Isolation	V_{IN} = 0 to 1V, 1V p-p, R_L = 75Ω, f = 5.5MHz	—	–60	—	dB
X_{TALK}	Crosstalk	V_{IN} = 1V p-p, R_L = 75Ω, f = 5.5MHz	—	–70	—	dB
$C_{(OFF)}$	MUX Off Capacitance	$\overline{E}$ = V_{CC}, V_{IN} = V_{OUT} = 0V	—	5	—	pF
$C_{(ON)}$	MUX On Capacitance	$\overline{E}$ = GND, V_{IN} = V_{OUT} = 0V	—	10	—	pF
Q_{CI}	Charge Injection	C_L = 1000pF	—	1.5	—	pC

Notes:
1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. Guaranteed by design, not subject to production test.
3. Measured by voltage drop between A and C or B and D pins at indicated current through the switch. On-resistance is determined by the lower of the voltages on the two (A,C or B,D) pins.
4. $\Delta r_{DS(on)}$ compares on-resistance at the specified V_{IN} Values.
5. The bus switch contributes no group delay other than the RC delay of the on-resistance of the switch and load capacitance. Group delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

TYPICAL CHARACTERISTICS

Figure 5. Off-isolation and Crosstalk vs. Frequency



Note: 1. Crosstalk = 20 log | V_O/V_S|
2. Off-isolation = 20 log | V_O/V_S|

Figure 4. Off-isolation and Crosstalk vs. Frequency

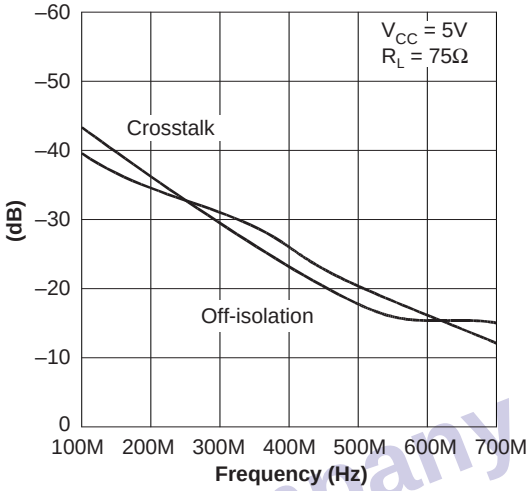


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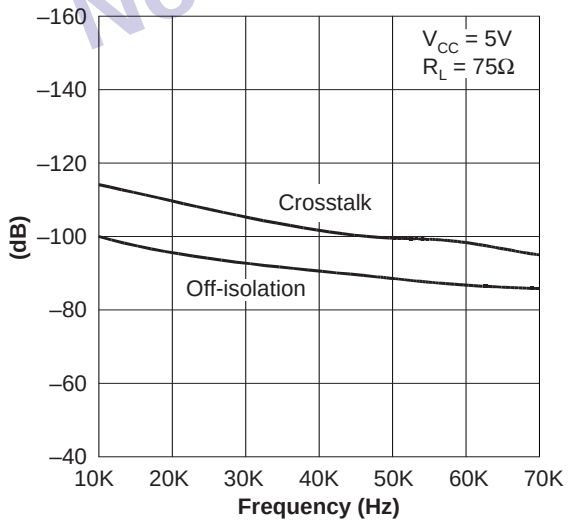
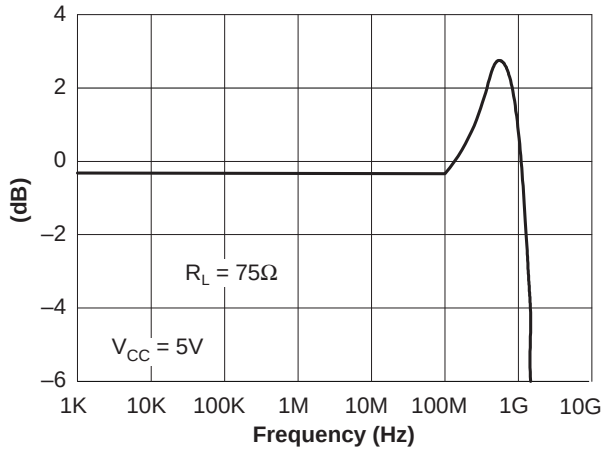
Figure 5. OFF Isolation and Crosstalk vs. Frequency



Note: 1. Crosstalk = 20 log | V_O/V_S|
2. Off-isolation = 20 log | V_O/V_S|

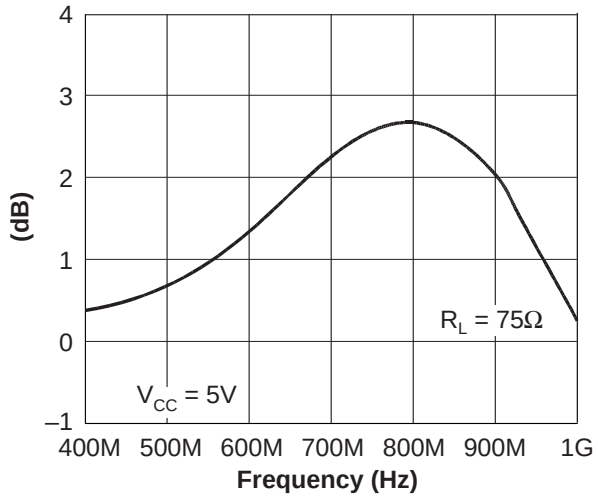
Figure 6. Insertion Loss vs. Frequency



Note: 1. Insertion Loss = 20 log | V_O/V_S|

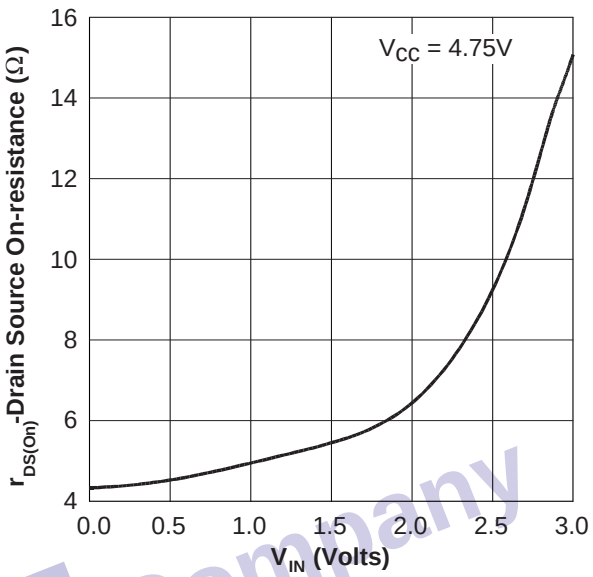
TYPICAL CHARACTERISTICS (continued)

Figure 7. Insertion Loss vs. Frequency



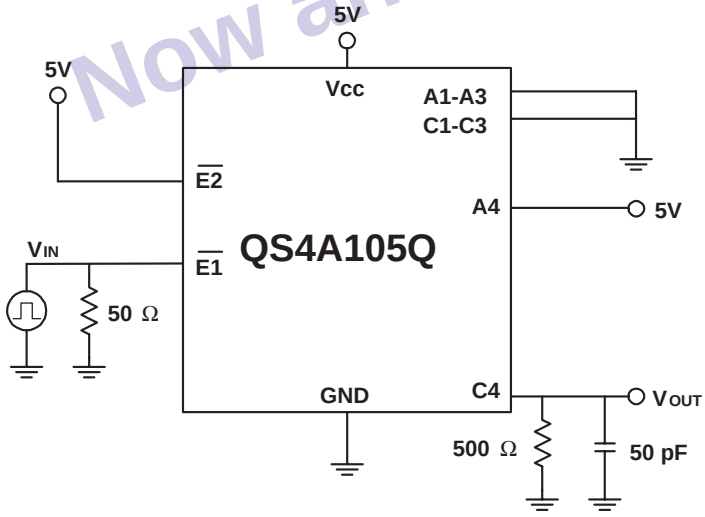
Note: 1. Insertion Loss = 20 log $|V_O/V_S|$

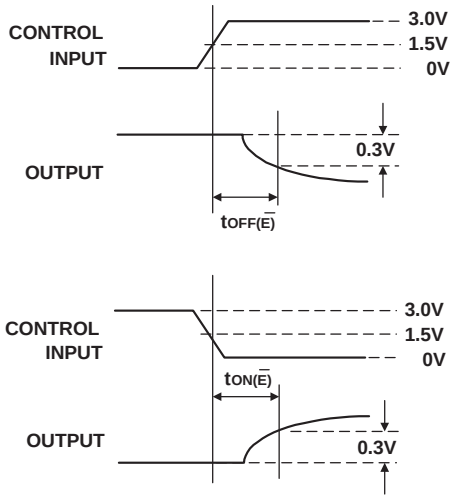
Figure 8. On-resistance vs. V_{IN}



TEST CIRCUITS

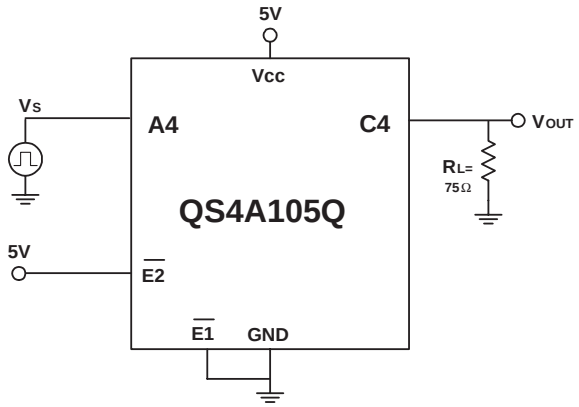
Figure 9. Switching Time





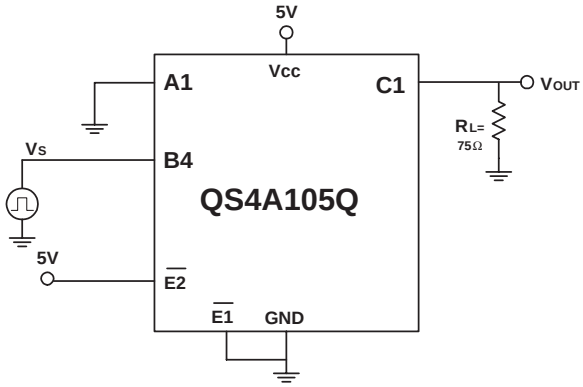
TEST CIRCUITS (continued)

Figure 10. Insertion Loss



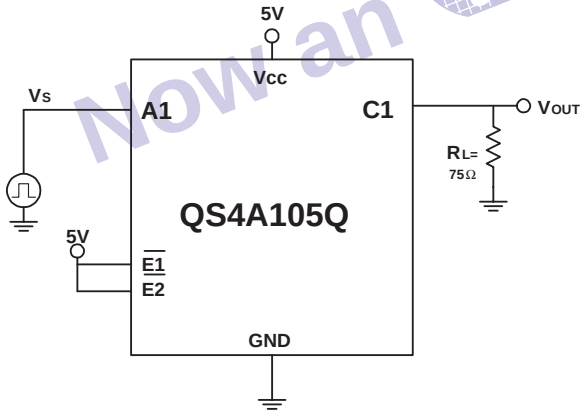
Note: 1. Insertion Loss = 20 log | V_O/V_S |
2. All unused pins are grounded.

Figure 11. Crosstalk



Note: 1. Crosstalk = 20 log | V_O/V_S |
2. All unused pins are grounded.

Figure 12. Off-isolation



Note: 1. Off-isolation = 20 log | V_O/V_S |
2. All unused pins are grounded.