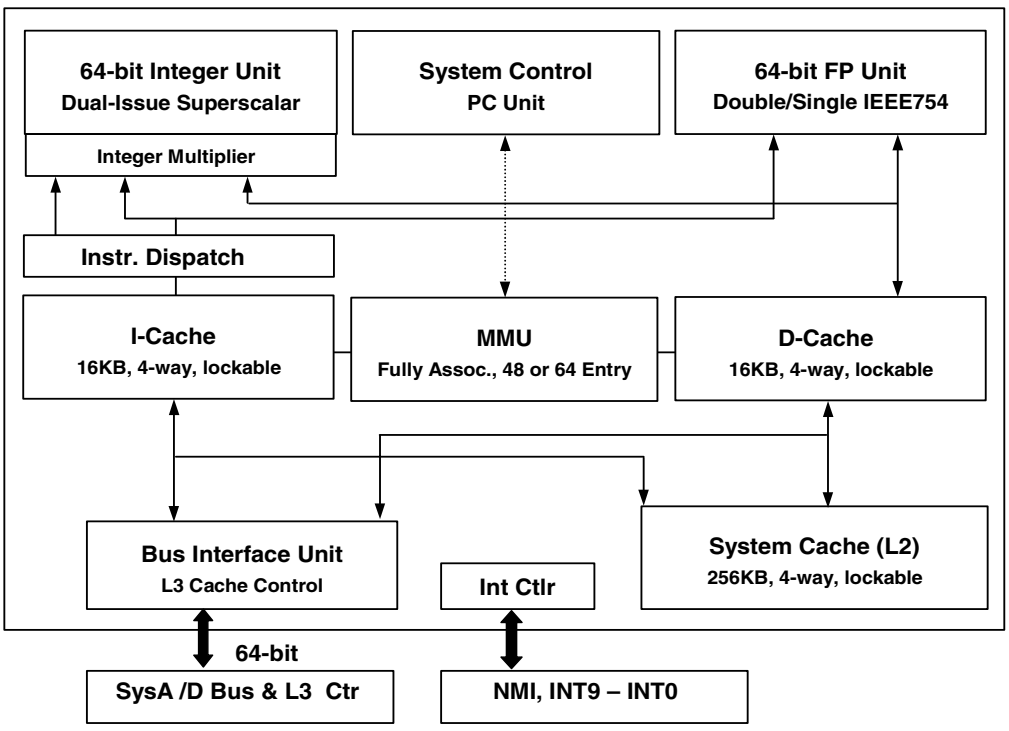
64-Bit MIPS RISC Microprocessor with Integrated L2 Cache

FEATURES

- Dual issue symmetric superscalar microprocessor with instruction prefetch optimized for system level price/performance
  - 533, 600 MHz operating frequency
  - >1080 Dhrystone 2.1 MIPS @ 600 MHz
- High-performance system interface
  - 1280 MB per second peak throughput
  - 200 MHz maximum frequency using HSTL signaling on the SysAD bus
  - Multiplexed address/data bus (SysAD) supports 1.5 V, 2.5 V, 3.3 V I/O logic
  - Processor clock multipliers 2, 2.5, 3, 3.5, 4, 4.5, 5, 6, 7, 8, 9
- Integrated primary and secondary caches
  - All are 4-way set associative with 32-byte line size
  - 16 KB instruction, 16 KB data, 256 KB on-chip secondary
  - Per line cache locking in primaries and secondary
  - Fast Packet Cache™ increases system efficiency in networking applications
- Integrated external cache controller (up to 64 MB)
  - User-selectable EZ Cache protocol eliminates the need for external tag RAMs.
- High-performance floating-point unit - 1600 MFLOPS maximum
  - Single cycle repeat rate for common single-precision operations and some double-precision operations
  - Single cycle repeat rate for single-precision combined multiply-add operations
  - Two cycle repeat rate for double-precision multiply and double-precision combined multiply-add operations
- MIPS IV superset instruction set architecture
  - Data PREFETCH instruction allows the processor to overlap cache miss latency and instruction execution
  - Single-cycle floating-point multiply-add
- Integrated memory management unit
  - Fully associative joint TLB (shared by I and D translations)
  - 64/48 dual entries map 128/96 pages
  - Variable page size
- Embedded application enhancements
  - Specialized DSP integer Multiply-Accumulate instructions, (MAD/MADU) and three-operand multiply instruction (MUL)
  - I&D Test/Break-point (Watch) registers for emulation & debug
  - Performance counter for system and software tuning & debug
  - Fourteen fully prioritized vectored interrupts - 10 external, 2 internal, 2 software
- Fully static CMOS design with dynamic power down logic
- Pin compatible with RM5271, RM7000, RM7000A and RM7000B in 304-pin TBGA package, 31x31 mm

BLOCK DIAGRAM



64-Bit MIPS RISC Microprocessor with Integrated L2 Cache

PACKAGING

- Fully Static 0.13µ CMOS design with dynamic power down logic
- 304 pin TBGA package, 31x31 mm

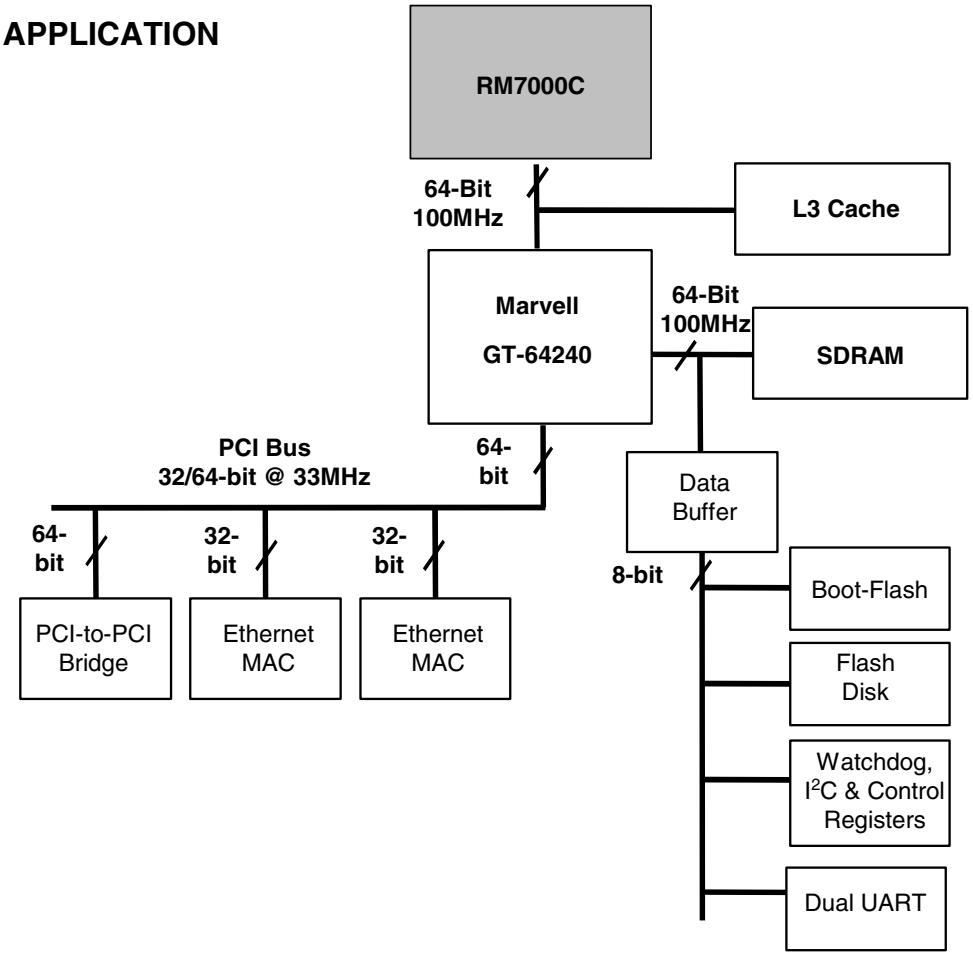
DEVELOPMENT TOOLS

- Operating Systems:
  - Linux by MontaVista and Red Hat
  - VxWorks by Wind River Systems
  - Nucleus by Accelerated Technology
  - Neutrino by QNX Software Systems
- Compiler Suites
  - Algorithmics
  - Green Hills Software
  - Red Hat
- Evaluation Boards and Companion Chips
  - Marvell Technology
    - EV-64120A-7000: 32/64-bit, 33/66MHz PCI
    - EV-64240-7000: 32/64-bit, 33/66MHz PCI
  - Momentum Computer
    - Ocelot-C Compact PCI Development Platform
  - Logic Analyzers and Emulation
    - HP
    - Tektronix
    - Corelis
    - Crescent Heart Software

APPLICATIONS

- Voice Gateways
- Multi-Service Access Platforms
- DSLAMs/Access Concentrators
- Remote Access Switches
- Web Switches
- Layer 3 Switches
- Backbone Switches/Routers
- RAIDs
- Set Top Boxes
- Networked Printers
- Cellular Base Stations

TYPICAL APPLICATION



Head Office:
PMC-Sierra, Inc.
8555 Baxter Place
Burnaby, B.C. V5A 4V7
Canada
Tel: 604.415.6000
Fax: 604.415.6200

To order documentation, send email to: document@pmc-sierra.com or contact the head office, Attn: Document Coordinator

All product documentation is available on our web site at: http://www.pmc-sierra.com For corporate information, send email to: info@pmc-sierra.com

PMC- 2011604 (R3)