PM8316

TEMUX 84

HIGH DENSITY T1/E1 FRAMER WITH INTEGRATED VT/TU MAPPER AND M13 MULTIPLEXER

REGISTER DESCRIPTIONS

Proprietary and Confidential

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Patents

The technology discussed is protected by one or more of the following Patents:

U.S. Patent No. 5,640,398, 6,584,521, 6,744,787, 6,774,693, 6,819,725

Canadian patent 2,161,921

Relevant patent applications and other patents may also exist.

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1 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the TEMUX 84. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[12]) is low.

Notes on Normal Mode Register Bits:

1) Writing values into unused register bits typically has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bit must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2) All configuration bits that can be written into can also be read back. This allows the processor controlling the TEMUX 84 to determine the programming state of the block.

3) Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4) Writing into read-only normal mode register bit locations does not affect TEMUX 84 operation unless otherwise noted.

5) The TEMUX 84 registers default to a DS3 M13 mux with T1 framers enabled. Default system side access is via the SBI bus without any tributaries enabled. The SONET/SDH blocks are by default in a reset state.

6) In the SONET/SDH register descriptions virtual tributaries, VT, and Tributary units, TU, are sometimes used interchangeably. Sometimes TU is only mentioned but the intention is that the register applies to both Tus and the equivalent VTs.

7) Some configurations of the device will hold certain sections of the TEMUX 84 in reset. The individual register descriptions indicate when certain registers are held in reset.

1.1 Tributary Indexing

The TEMUX 84 is capable of transporting 84 1.544 Mbit/s (T1) or 63 2.048 Mbit/s (E1) tributaries. This section explains the correspondence between the indexing

systems of the various mapping and multiplexing formats: SBI Bus, Telecom Bus, M13 and H-MVIP. The listed index systems are used throughout the document.

The SBI Bus tributary designation uses two integers: the first represents the byte interleaved SPE number (range 1 to 3) and the second is the link index within the SPE (range 1 to 28).

The Telecom Bus indexing follows the conventions of the ITU-T multiplexing structure. The bandwidth is divided into three TUG-3s numbered 1 through 3, each of which is composed of seven TUG-2s numbered 1 through 7, each of which is composed of either three TU-12s numbered 1 through 3 or four TU-11s numbered 1 through 4.

The three DS3s are divided into seven DS2s, each of which is composed of either four 1.544 Mbit/s or three 2.048 Mbit/s tributaries.

The payload capacity is divided into three equal portions. Each of the following lists represents one set of equivalent tributaries:

- SPE #1, TUG-3 #1, DS3 #1 and MVID/MVED[1:7]
- SPE #2, TUG-3 #2, DS3 #2 and MVID/MVED[8:14]
- SPE #3, TUG-3 #3, DS3 #3 and MVID/MVED[15:21]

Table 1 and Table 2 provide the equivalencies between the various multiplex and mapping formats. Alternately, the formats can be equated with the following formulae:

1.544Mbit/s SBI LINK # = 7*(TU11-1) + TUG2
= 4*(DS2-1)+DS1
= 4*(MVED index – 7*(SPE-1) – 1) + DS1

2.048Mbit/s SBI LINK # = 7*(TU12-1) + TUG2
= 3*(DS2-1)+E1
= 4*(MVED index – 7*(SPE-1) – 1) + E1

Table 1 Indexing for 1.544 Mbit/s Tributaries

SBI Bus SPE, LINK	Telecom Bus TUG-3, TUG-2, TU11	M13 DS3, DS2, DS1	H-MVIP port index, DS1
1,1	1,1,1	1,1,1	1,1
1,2	1,2,1	1,1,2	1,2
1,3	1,3,1	1,1,3	1,3
1,4	1,4,1	1,1,4	1,4
1,5	1,5,1	1,2,1	2,1
1,6	1,6,1	1,2,2	2,2
1,7	1,7,1	1,2,3	2,3
1,8	1,1,2	1,2,4	2,4
1,9	1,2,2	1,3,1	3,1
1,10	1,3,2	1,3,2	3,2
1,11	1,4,2	1,3,3	3,3
1,12	1,5,2	1,3,4	3,4
1,13	1,6,2	1,4,1	4,1
1,14	1,7,2	1,4,2	4,2
1,15	1,1,3	1,4,3	4,3
1,16	1,2,3	1,4,4	4,4
1,17	1,3,3	1,5,1	5,1
1,18	1,4,3	1,5,2	5,2
1,19	1,5,3	1,5,3	5,3
1,20	1,6,3	1,5,4	5,4
1,21	1,7,3	1,6,1	6,1
1,22	1,1,4	1,6,2	6,2
1,23	1,2,4	1,6,3	6,3
1,24	1,3,4	1,6,4	6,4
1,25	1,4,4	1,7,1	7,1
1,26	1,5,4	1,7,2	7,2
1,27	1,6,4	1,7,3	7,3
1,28	1,7,4	1,7,4	7,4
2,1	2,1,1	2,1,1	8,1
…	...	...	...

Table 2 Indexing for 2.048 Mbit/s Tributaries

SBI Bus SPE, LINK	Telecom Bus TUG-3, TUG-2, TU12	M13 DS3, DS2, E1	H-MVIP port index, E1
1,1	1,1,1	1,1,1	1,1
1,2	1,2,1	1,1,2	1,2
1,3	1,3,1	1,1,3	1,3
1,4	1,4,1	1,2,1	1,4
1,5	1,5,1	1,2,2	2,1
1,6	1,6,1	1,2,3	2,2
1,7	1,7,1	1,3,1	2,3
1,8	1,1,2	1,3,2	2,4
1,9	1,2,2	1,3,3	3,1
1,10	1,3,2	1,4,1	3,2
1,11	1,4,2	1,4,2	3,3
1,12	1,5,2	1,4,3	3,4
1,13	1,6,2	1,5,1	4,1
1,14	1,7,2	1,5,2	4,2
1,15	1,1,3	1,5,3	4,3
1,16	1,2,3	1,6,1	4,4
1,17	1,3,3	1,6,2	5,1
1,18	1,4,3	1,6,3	5,2
1,19	1,5,3	1,7,1	5,3
1,20	1,6,3	1,7,2	5,4
1,21	1,7,3	1,7,3	6,1
2,1	2,1,1	2,1,1	8,1
...	...	...	...

1.2 Top Level Master Registers

Register 0x0000: Revision

Bit	Type	Function	Default
Bit 7	R	TYPE3	0
Bit 6	R	TYPE2	0
Bit 5	R	TYPE1	1
Bit 4	R	TYPE0	0
Bit 3	R	ID3	0
Bit 2	R	ID2	0
Bit 1	R	ID1	1
Bit 0	R	ID0	0

ID[3:0]:

The version identification bits ID[3:0], are set to a fixed value representing the version number of the TEMUX 84. These bits can be read by software to determine the version number.

TYPE[3:0]:

The type identification bits TYPE[3:0], identify this device from other products in the same Asynchronous Multiplexer family of devices.

Register 0x0001: Global Reset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	RESET	0

RESET:

The RESET bit implements a software reset for the entire TEMUX 84. If the RESET bit is a logic 1, the entire TEMUX 84 is held in reset. This bit is not self-clearing; therefore, a logic 0 must be written to bring the TEMUX 84 out of reset. Holding the TEMUX 84 in a reset state effectively puts it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus deasserting the software reset.

Register 0x0002: Global Configuration

Bit	Type	Function	Default
Bit 7	R/W	MINTE	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	SYSOPT[1]	1
Bit 0	R/W	SYSOPT[0]	0

MINTE:

The Master Interrupt Enable allows internal interrupt statuses to be propagated to the interrupt output. If MINTE is logic 1, INTB will be asserted low upon the assertion of an interrupt status bit whose individual enable is set. If MINTE is logic 0, INTB is unconditionally high-impedance.

SYSOPT[1:0]:

The System Side Options bits, SYSOPT[1:0], configure the system side interface of the TEMUX 84. The possible system side interface selections are H-MVIP backplane interfaces, Scaleable Bandwidth Interconnect bus interface and a combination SBI bus with CAS or CCS H-MVIP interface. The following table shows the SYSOPT[1:0] values for each system side interface configuration:

SYSOPT[1:0]	System Interface Mode
00	Reserved
01	H-MVIP Interface Only valid for High Density Framer mode. If an SPE is not configured for High Density Framer mode, its associated H-MVIP outputs are arbitrary and its H-MVIP inputs are ignored.
10	SBI Interface. Valid for all modes including DS3/E3 Framer Only.

11	SBI Interface with CAS or CCS H-MVIP Interface (only valid for High Density Framer mode)

Register 0x0003: SPE #1 Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	E1T1B_SPE1	0
Bit 4	R/W	LINEOPT _SPE1[1]	0
Bit 3	R/W	LINEOPT _SPE1[0]	0
Bit 2	R/W	OPMODE _SPE1[2]	0
Bit 1	R/W	OPMODE _SPE1[1]	0
Bit 0	R/W	OPMODE _SPE1[0]	0

Register 0x0004: SPE #2 Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	E1T1B_SPE2	0
Bit 4	R/W	LINEOPT _SPE2[1]	0
Bit 3	R/W	LINEOPT _SPE2[0]	0
Bit 2	R/W	OPMODE _SPE2[2]	0
Bit 1	R/W	OPMODE _SPE2[1]	0
Bit 0	R/W	OPMODE _SPE2[0]	0

Register 0x0005: SPE #3 Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	E1T1B_SPE3	0
Bit 4	R/W	LINEOPT _SPE3[1]	0
Bit 3	R/W	LINEOPT _SPE3[0]	0
Bit 2	R/W	OPMODE _SPE3[2]	0
Bit 1	R/W	OPMODE _SPE3[1]	0
Bit 0	R/W	OPMODE _SPE3[0]	0

OPMODE_SPEx[2:0]:

Configures the operating mode for each of the SPEs/DS3s of the TEMUX 84 independent of the other two SPEs/DS3s.

OPMODE _SPEx[2:0]	Mode
000	High Density T1/E1 Framer mode. The T1/E1 framers are connected to the line via the DS3 multiplexer or SONET/SDH mapper.
001	Mapper/Multiplexer mode. The T1/E1 transmit framers are disabled, all the T1/E1 framers are configured to pass unframed data through to the system interface and the TEMUX 84 becomes a SONET/SDH mapper or DS3 multiplexer only. This mode cannot be used if byte synchronous mapping is in use.
010	Transmux mode. Unframed T1 or E1 streams are passed between the SONET/SDH bit asynchronous mapper and the DS3 multiplexer.

011	DS3/E3 Framer Only mode. The T1/E1 framers, the SONET/SDH T1/E1 mapper, the MX23, MX12 and DS2 blocks are disabled and the associated RDATOx, RFPOx/RMFPOx, RGAPCLKx/RSCLKx, ROVRHDx, TFPOx/TMFPOx outputs are enabled for serial clock and data mode. If the TXSBI bit of the DS3 and E3 Master Unchannelized Interface Options register is logic 1, the transmit data stream is derived from the SBI bus; otherwise, it is accepted from the TFPIx/TMFPIx, TGAPCLKx and TDATIx inputs.
100	Fractional DS3/E3 mode. The SBI bus is configured to transport an arbitrary bandwidth payload. The contents of the SBI bus are presented on the Flexible Bandwidth Port for the SPE. A typical application would be to use external logic to extract and insert the Flexible Bandwidth Port data from and into a DS3/E3 payload at the DS3 and E3 System Side Interface. This mode is only valid if the SYSOPT[1:0] bits are binary 10 or 11.
101	Reserved
110	Reserved
111	Reserved

LINEOPT_SPEx[1:0]:

The Line Side Options bits, LINEOPT_SPEx[1:0], select the line side multiplexing interface for each of the SPEs/DS3s of the TEMUX 84 independent of the other two SPEs/DS3s. When the TEMUX 84 is configured for high density T1/E1 framer mode, Mapper/Multiplexer mode or Fractional DS3/E3 mode, the LINEOPT_SPEx[1:0] bits select between a DS3 multiplexer, DS3 Mapper or T1/E1 mapper. When in DS3/E3 framer only mode, LINEOPT[1:0] selects the DS3 LIU interface or DS3 Mapper. These bits must be left selecting the LIU interface when in Transmux mode. The following table shows the LINEOPT[1:0] values for each line side interface configuration:

LINEOPT _SPEx[1:0]	Line Interface Mode
00	DS3 Mux with serial LIU interface
01	DS3 Mux with DS3 SONET/SDH Mapper

1X	T1/E1 Mapper

E1T1B_SPEx:

The E1T1B_SPEx bits configure the T1/E1 framers associated with an SPE to be configured as either 28 T1 framers or 21 E1 framers. When E1T1B_SPEx is a logic 0 the T1/E1 framers are configured as 28 T1 framers. When E1T1B_SPEx is a logic 1 the T1/E1 framers are configured as 21 E1 framers.

When switching an SPE between T1 and E1 modes via an E1T1B_SPEx bit, the T1/E1 register space of direct and indirect registers will retain their previously programmed values. If all three E1T1B_SPEx are changed simultaneously then the RESET bit of the T1/E1 Master Configuration register should be set then cleared to return the T1/E1 register to their default values. If only one or two of the E1T1B_SPEx bits are changed then all the corresponding T1/E1 register bits for those particular SPEs must be reprogrammed to their default values before the T1/E1 mode can be changed.

Register 0x0006: Bus Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	GSOE	0
Bit 5	R/W	SSTM[1]	1
Bit 4	R/W	SSTM[0]	0
Bit 3	R/W	LSTM1EN	0
Bit 2	R/W	LADDOE	0
Bit 1	R/W	LSTM[1]	0
Bit 0	R/W	LSTM[0]	0

LSTM[1:0]:

These bits are only relevant when the L77 input is high.

The Line STM-1 Select bits determine during which one of four byte interleaved STM-1s the TEMUX 84 drives LADATA[7:0] and expects data on LDDATA[7:0]:

LSTM[1:0]	Byte Alignment
00	Byte aligned to LAC1 and LDC1J1V1, and every fourth byte thereafter.
01	Byte after LAC1 and LDC1J1V1, and every fourth byte thereafter.
10	Two bytes after LAC1 and LDC1J1V1, and every fourth byte thereafter.
11	Three bytes after LAC1 and LDC1J1V1, and every fourth byte thereafter.

LADDOE:

The Line ADD Bus output enable bit, LADDOE, enables the Line ADD bus for use with an external multiplexer to merge the ADD busses from multiple TEMUX 84s. When LADDOE is a logic 1, the Line ADD Bus signals are

driven permanently and the LAOE signal is asserted high whenever the data on the line ADD bus is valid as specified by the per-tributary LAOE bit of the TTMP Tributary Control registers. When LADDOE is a logic 0, the Line ADD Bus signals are driven only during valid data and are otherwise tristated.

LADDOE only has effect for TU11/VT1.5 and TU12/VT2 tributaries. For TU-3 tributaries, the Line Add Bus signals are driven for all columns of the related SPE.

The Line ADD Bus defaults to high impedance upon reset.

LSTM1EN:

The Line ADD Bus STM-1 enable bit, LSTM1EN, enables the Line ADD bus to drive for all columns of the STM-1 chosen by the LSTM[1:0] bits. This allows the path overhead to be output, where it normally would be tristate.

LSTM1EN has no effect if LADDOE is logic 1. If LADDOE and LSTM1EN are both logic 0, the ADD bus is only driven during enabled tributaries.

SSTM[1:0]:

These bits are only relevant when the S77 input is high.

The Scalable Bus Interface STM-1 Select bits determine during which one of four byte interleaved STM-1s the TEMUX 84 drives SDDATA[7:0] and expects data on SADATA[7:0]:

SSTM[1:0]	Byte Alignment
00	Byte aligned to SAC1FP and SDC1FP, and every fourth byte thereafter.
01	Byte after SAC1FP and SDC1FP, and every fourth byte thereafter.
10	Two bytes after SAC1FP and SDC1FP, and every fourth byte thereafter.
11	Three bytes after SAC1FP and SDC1FP, and every fourth byte thereafter.

GSOE:

The Global SBI Output Enable (GSOE) determines whether the SBI Drop bus is driven. If GSOE is logic 0, the SDDATA[7:0], SDDP, SDPL, SDV5, SBIACT, and SAJUST_REQ outputs are unconditionally high impedance. If GSOE is logic 1, these outputs drive during the programmed tributaries.

The SBI Bus defaults to high impedance upon reset.

Register 0x0007: Global Performance Monitor Update

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	DS3_E3	0
Bit 1	R/W	E1T1_PRBS	0
Bit 0	R/W	E1T1_FRMR	0

Each write to this register triggers the selected performance monitors to be updated simultaneously and the associated internal counters to be reset to begin a new cycle of error accumulation. Be aware some performance counters maybe configured to be updated autonomously, so it may not be appropriate to update them via writing this register. Once transferred, the data in the microprocessor accessible registers remains valid until the next transfer.

Reserved:

A logic 0 should be written to this bit.

DS3_E3:

If a logic 1 is written to this bit, the performance monitor counts associated with the DS3 framers, E3 framers and DS2 framers are transferred to holding registers.

E1T1_PRBS:

If a logic 1 is written to this bit, the E1/T1 PRBS error counts for both the receive and transmit directions are transferred to holding registers. This includes the counts associated with the Full-Featured T1/E1 Pattern Detector.

E1T1_FRMR:

If a logic 1 is written to this bit, the performance monitor counts associated with the T1/E1 framers are transferred to holding registers.

Register 0x0008: Reference Clock Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	REFCLK[1]	0
Bit 0	R/W	REFCLK[0]	0

REFCLK[1:0]:

The Reference Clock select bits, REFCLK[1:0], select the source of the clock to be used as the common transmit T1/E1 clock. Regardless of the state of these bits, each tributary may also be loop timed or be slave to the system interface. The following table shows the REFCLK[1:0] selections:

REFCLK[1:0]	Clock
00	CTCLK pin
01	RECVCLK1 pin (generated internally)
10	RECVCLK2 pin (generated internally)
11	RECVCLK3 pin (generated internally)

Register 0x0009: Recovered Clock#1 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	RECV1SPE1	0
Bit 5	R/W	RECV1SPE0	0
Bit 4	R/W	RECV1LNK4	0
Bit 3	R/W	RECV1LNK3	0
Bit 2	R/W	RECV1LNK2	0
Bit 1	R/W	RECV1LNK1	0
Bit 0	R/W	RECV1LNK0	0

RECV1SPE[1:0], RECV1LNK[4:0]:

Select the source of the recovered clock that will be output on pin RECVCLK1. When this register is all zeros, no tributary is selected and the RECVCLK1 output frequency will be about 650ppm lower than nominal. RECV1SPE[1:0] values of 1 to 3 select the SPE or DS3 from which the clock is extracted. RECV1LNK[4:0] values from 1 to 28 select the recovered clock from one of the 28 T1/E1 framers per SPE/DS3. When in E1 mode, RECV1LNK[4:0] values from 22 through 28 will result in an invalid recovered clock.

Register 0x000A: Recovered Clock#2 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	RECV2SPE1	0
Bit 5	R/W	RECV2SPE0	0
Bit 4	R/W	RECV2LNK4	0
Bit 3	R/W	RECV2LNK3	0
Bit 2	R/W	RECV2LNK2	0
Bit 1	R/W	RECV2LNK1	0
Bit 0	R/W	RECV2LNK0	0

RECV2SPE[1:0], RECV2LNK[4:0]:

Select the source of the recovered clock that will be output on pin RECVCLK2. When this register is all zeros, no tributary is selected and the RECVCLK2 output frequency will be about 650ppm lower than nominal. RECV2SPE[1:0] values of 1 to 3 select the SPE or DS3 from which the clock is extracted. RECV2LNK[4:0] values from 1 to 28 select the recovered clock from one of the 28 T1/E1 framers per SPE/DS3. When in E1 mode, RECV2LNK[4:0] values from 22 through 28 will result in an invalid recovered clock.

Register 0x000B: Recovered Clock#3 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	RECV3SPE1	0
Bit 5	R/W	RECV3SPE0	0
Bit 4	R/W	RECV3LNK4	0
Bit 3	R/W	RECV3LNK3	0
Bit 2	R/W	RECV3LNK2	0
Bit 1	R/W	RECV3LNK1	0
Bit 0	R/W	RECV3LNK0	0

RECV3SPE[1:0], RECV3LNK[4:0]:

Select the source of the recovered clock that will be output on pin RECVCLK3. When this register is all zeros, no tributary is selected and the RECVCLK3 output frequency will be about 650ppm lower than nominal. RECV3SPE[1:0] values of 1 to 3 select the SPE or DS3 from which the clock is extracted. RECV3LNK[4:0] values from 1 to 28 select the recovered clock from one of the 28 T1/E1 framers per SPE/DS3. When in E1 mode, RECV3LNK[4:0] values from 22 through 28 will result in an invalid recovered clock.

Register 0x000C: Master H-MVIP Interface Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	CMVFPINV	1
Bit 3	R/W	CMVIFE	0
Bit 2	R/W	CMVIDE	0
Bit 1	R/W	CMMFP	0
Bit 0	R/W	CMVEDE	1

CMVEDE:

In H-MVIP mode when CMVEDE is set to logic 1, the egress H-MVIP signals (MVED[21:1], CASED[21:1], CCSED[3:1]) are sampled by the rising edge of CMV8MCLK. When CMVEDE is set to logic 0, the egress H-MVIP signals are sampled by the falling edge of CMV8MCLK.

CMMFP:

The CMMFP bit controls whether the common H-MVIP frame pulse, CMVFPB, indicates frame alignment or multiframe alignment. When CMMFP is a logic 1, the frame pulse, CMVFPB, indicates a multiframe boundary. To support any combination of SF, SLC-96, ESF and E1, the CMVFPB must pulse low (high if CMVFPINV is logic 0) at a multiple of 48 frames at the beginning of the frame. When CMMFP is a logic 0, CMVFPB indicates a frame boundary.

Indicating multiframe alignment assures the framing and signaling inserted by TEMUX 84 in the transmit direction aligns to the data being presented on the H-MVIP inputs. For example, the SLC-96 framing and data link may be presented on the MVED input while correctly aligned signaling is inserted into the robbed bit positions by the TEMUX 84.

CMMFP has no effect on the multiframe alignment of the ingress interface.

Note that frame slips must be avoided to achieve multiframe alignment. Therefore, the transmit clock must be referenced to CTCLK and CTCLK must

be frequency locked to CMVFPB when SYSOPT equals binary 01 (H-MVIP Interface). For the SBI interface with CAS or CCS H-MVIP interface, CTCLK need not be frequency locked to CMVFPB.

CMVIDE:

In H-MVIP mode when CMVIDE is set to logic 1, the ingress H-MVIP signals (MVID[21:1], CASID[21:1] and CCSID[3:1]) are updated on the rising edge of CMV8MCLK. When CMVIDE is set to logic 0, the ingress H-MVIP signals are updated on the falling edge of CMV8MCLK.

CMVIFE:

When using the H-MVIP interface, the CMVFPC clock rising edge is in the center of CMVFPB when CMVIFE is set to logic 1. When CMVIFE is set to logic 0, the CMVFPC clock falling edge is in the center of CMVFPB.

CMVFPINV:

When using using the H-MVIP interface and CMVFPINV is set to logic 1, the H-MVIP frame pulse, CMVFPB, is inverted. When inverted, CMVFPB is nominally high and pulses low to indicate a frame boundary. When CMVFPINV is a logic 0, CMVFPB is nominally low and pulses high to indicate a frame boundary.

Register 0x000D: Master Clock Monitor

Bit	Type	Function	Default
Bit 7	R	CMVFPA	X
Bit 6	R	CMV8MCLKA	X
Bit 5	R	CTCLKA	X
Bit 4	R	XCLK_E1A	X
Bit 3	R	XCLK_T1A	X
Bit 2	R	CLK52MA	X
Bit 1	R	LREFCLKA	X
Bit 0	R	SREFCLKA	X

When a monitored clock signal makes a low to high transition, the corresponding register bit is set to logic 1. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

SREFCLKA:

The SREFCLK active, SREFCLKA, bit detects low to high transitions on the SREFCLK input. SREFCLKA is set to logic 1 on a rising edge of SREFCLK, and is set to logic 0 when this register is read.

LREFCLKA:

The LREFCLK active, LREFCLKA, bit detects low to high transitions on the LREFCLK input. LREFCLKA is set to logic 1 on a rising edge of LREFCLK, and is set to logic 0 when this register is read.

CLK52MA:

The CLK52M active, CLK52MA, bit detects low to high transitions on the CLK52M input. CLK52MA is set to logic 1 on a rising edge of CLK52M, and is set to logic 0 when this register is read.

XCLK_T1A:

The XCLK_T1 active, XCLK_T1A, bit detects for low to high transitions on the XCLK_T1 input. XCLK_T1A is set to logic 1 on a rising edge of XCLK_T1, and is set to logic 0 when this register is read.

XCLK_E1A:

The XCLK_E1 active, XCLK_E1A, bit detects for low to high transitions on the XCLK_E1 input. XCLK_E1A is set to logic 1 on a rising edge of XCLK_E1, and is set to logic 0 when this register is read.

CTCLKA:

The CTCLK active, CTCLKA, bit detects for low to high transitions on the CTCLK input. CTCLKA is set to logic 1 on a rising edge of CTCLK, and is set to logic 0 when this register is read.

CMV8MCLKA:

The C8MVCLK active, C8MVCLKA, bit detects for low to high transitions on the C8MVCLK input. C8MVCLKA is set to logic 1 on a rising edge of C8MVCLK, and is set to logic 0 when this register is read.

CMVFPA:

The CMVFPB active, CMVFPA, bit detects for low to high transitions on the CMVFPB input. CMVFPA is set to logic 1 on a rising edge of CMVFPB, and is set to logic 0 when this register is read.

Register 0x0010: Master Interrupt Source

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	T1E1PRGD	X
Bit 5	R	T1E1INT	X
Bit 4	R	SBIINT	X
Bit 3	R	SDHINT	X
Bit 2	R	DS3E3INT	X
Bit 1	R	DS2INT	X
Bit 0	R	MX12INT	X

MX12INT:

If the MX12INT bit is a logic 1, at least one bit in the three Master Interrupt Source MX12 Registers is set.

DS2INT:

If the DS2INT bit is a logic 1, at least one bit in the three Master Interrupt Source DS2 Registers is set.

DS3E3INT:

If the DS3INT bit is a logic 1, at least one bit in the three Master Interrupt Source DS3/E3 Registers is set.

SDHINT:

If the SDHINT bit is a logic 1, at least one bit in the three Master Interrupt Source SDH Registers is set.

SBIINT:

If the SBIINT bit is a logic 1, at least one bit in the Master Interrupt Source SBI Register is set.

T1E1INT:

If the T1E1INT bit is a logic 1, at least one bit in the Master Interrupt Source T1E1 Register is set.

T1E1PRGD:

If T1E1PRGD is a logic 1, at least one of the six full featured T1/E1 pattern generators and detectors is generating an interrupt. To clear the interrupt signal, each T1/E1 Pattern Generator and Detector Interrupt Enable/Status register must be read.

Register 0x0011: Master Interrupt Source T1E1

Bit	Type	Function	Default
Bit 7	R	RHDL	X
Bit 6	R	THDL	X
Bit 5	R	RPRBS	X
Bit 4	R	TPRBS	X
Bit 3	R	RXELST	X
Bit 2	R	TXELST	X
Bit 1	R	SIGX	X
Bit 0	R	FRMR	X

FRMR:

If the FRMR bit is a logic 1, an interrupt has been generated by the T1/E1 framer. To clear the interrupt signal, clear all FRMRI[84:1] bits in the T1/E1 Framer Interrupt Status registers by writing logic 1 to them.

SIGX:

If the SIGX bit is a logic 1, an interrupt has been generated by the T1/E1 signaling extractor caused by a change in signaling state. To clear the interrupt signal, clear all COSSI[84:1] bits in the Change of Signaling Status registers by writing logic 1 to them.

TXELST:

If the TXELST bit is a logic 1, an interrupt has been generated by the transmit T1/E1 elastic store upon a controlled frame slip. To clear the interrupt signal, read the TX-ELST Slip Status registers.

RXELST:

If the RXELST bit is a logic 1, an interrupt has been generated by either the receive H-MVIP or receive SBI T1/E1 elastic store upon a controlled frame slip. To clear the interrupt signal, read the RX-SBI-ELST and/or the RX-MVIP-ELST Slip Status registers.

TPRBS:

If the TPRBS bit is a logic 1, an interrupt has been generated by an event related to monitoring a PRBS pattern in the transmit direction. To clear the interrupt signal, clear all TPCCI[84:1] bits in the T1/E1 Framer Interrupt Status registers by writing logic 1 to them.

RPRBS:

If the RPRBS bit is a logic 1, an interrupt has been generated by an event related to monitoring a PRBS pattern in the receive direction. To clear the interrupt signal, clear all RPCCI[84:1] bits in the RPCC-MVIP Interrupt Status registers and/or RPCC-SBI Interrupt Status registers by writing logic 1 to them.

THDL:

If the THDL bit is a logic 1, an interrupt has been generated by the T1/E1 transmit HDLC processor. To clear the interrupt signal, clear all THDLI[84:1] bits in the THDL Interrupt Status registers by writing logic 1 to them.

RHDL:

If the RHDL bit is a logic 1, an interrupt has been generated by the T1/E1 receive HDLC processor. To clear the interrupt signal, clear all RHDLI[84:1] bits in the RHDL Interrupt Status registers by writing logic 1 to them.

Register 0x0012: Master Interrupt Source SDH #1

Bit	Type	Function	Default
Bit 7	R	TBUSDLLINT	X
Bit 6	R	LDPINT	X
Bit 5	R	RTTBINT1	X
Bit 4	R	D3MAINT1	X
Bit 3	R	D3MDINT1	X
Bit 2	R	EVTPPINT1	X
Bit 1	R	IVTPPINT1	X
Bit 0	R	RTOPINT1	X

RTOPINT1:

If the RTOPINT1 bit is a logic 1, an interrupt has been generated by the RTOP block associated with SPE #1. The RTOP Interrupt register must be read to clear this interrupt.

IVTPPINT1:

If the IVTPPINT1 bit is a logic 1, an interrupt has been generated by the Ingress VTPP block associated with SPE #1. The Ingress VTPP Interrupt register must be read to clear this interrupt.

EVTPPINT1:

If the EVTPPINT1 bit is a logic 1, an interrupt has been generated by the egress VTPP block associated with SPE #1. The egress VTPP Interrupt register must be read to clear this interrupt.

D3MDINT1:

If the D3MDINT1 bit is a logic 1, the D3MD block associated with SPE #1 is generating an interrupt. The D3MD Interrupt register must be read to clear this interrupt.

D3MAINT1:

If the D3MAINT1 bit is a logic 1, the D3MA block associated with SPE #1 is generating an interrupt. The D3MA Interrupt register must be read to clear this interrupt.

RTTBINT1:

If the RTTBINT1 bit is a logic 1, the Receive Tributary Trace Buffer associated with SPE #1 is generating an interrupt. The RTTB Configuration and Status registers must be read to clear this interrupt.

LDPINT:

If the LDPINT bit is a logic 1, an interrupt has been generated from a parity error on the Line DROP bus. This is an indication that there may be multiple devices driving the Line DROP bus simultaneously. This interrupt is enabled with the LDPE bit in the SONET/SDH Master Ingress Configuration register. This Interrupt register will be cleared when read.

TBUSDLLINT:

This bit only has significance if the L77 input in pulled high. If the TBUSDLLINT bit is a logic 1, the TelecomBus DLL has generated an interrupt indicating it has errored. Register 0x073F DLL Control Status must be read to clear this interrupt.

Register 0x0013: Master Interrupt Source SDH #2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	RTTBINT2	X
Bit 4	R	D3MAINT2	X
Bit 3	R	D3MDINT2	X
Bit 2	R	EVTPPINT2	X
Bit 1	R	IVTPPINT2	X
Bit 0	R	RTOPINT2	X

RTOPINT2:

If the RTOPINT2 bit is a logic 1, an interrupt has been generated by the RTOP block associated with SPE #2. The RTOP Interrupt register must be read to clear this interrupt.

IVTPPINT2:

If the IVTPPINT2 bit is a logic 1, an interrupt has been generated by the Ingress VTPP block associated with SPE #2. The Ingress VTPP Interrupt register must be read to clear this interrupt.

EVTPPINT2:

If the EVTPPINT2 bit is a logic 1, an interrupt has been generated by the egress VTPP block associated with SPE #2. The Egress VTPP Interrupt register must be read to clear this interrupt.

D3MDINT2:

If the D3MDINT2 bit is a logic 1, the D3MD block associated with SPE #2 is generating an interrupt. The D3MD Interrupt register must be read to clear this interrupt.

D3MAINT2:

If the D3MAINT2 bit is a logic 1, the D3MA block associated with SPE #2 is generating an interrupt. The D3MA Interrupt register must be read to clear this interrupt.

RTTBINT2:

If the RTTBINT1 bit is a logic 2, the Receive Tributary Trace Buffer associated with SPE #2 is generating an interrupt. The RTTB Configuration and Status registers must be read to clear this interrupt.

Register 0x0014: Master Interrupt Source SDH #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	RTTBINT3	X
Bit 4	R	D3MAINT3	X
Bit 3	R	D3MDINT3	X
Bit 2	R	EVTPPINT3	X
Bit 1	R	IVTPPINT3	X
Bit 0	R	RTOPINT3	X

RTOPINT3:

If the RTOPINT3 bit is a logic 1, an interrupt has been generated by the RTOP block associated with SPE #3. The RTOP Interrupt register must be read to clear this interrupt.

IVTPPINT3:

If the IVTPPINT3 bit is a logic 1, an interrupt has been generated by the Ingress VTPP block associated with SPE #3. The Ingress VTPP Interrupt register must be read to clear this interrupt.

EVTPPINT3:

If the EVTPPINT3 bit is a logic 1, an interrupt has been generated by the egress VTPP block associated with SPE #3. The egress VTPP Interrupt register must be read to clear this interrupt.

D3MDINT3:

If the D3MDINT3 bit is a logic 1, the D3MD block associated with SPE #3 is generating an interrupt. The D3MD Interrupt register must be read to clear this interrupt.

D3MAINT3:

If the D3MAINT3 bit is a logic 1, the D3MA block associated with SPE #3 is generating an interrupt. The D3MA Interrupt register must be read to clear this interrupt.

RTTBINT3:

If the RTTBINT3 bit is a logic 1, the Receive Tributary Trace Buffer associated with SPE #3 is generating an interrupt. The RTTB Configuration and Status registers must be read to clear this interrupt.

Register 0x0015: Master Interrupt Source SBI

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	SBIDLLINT	X
Bit 5	R	EXSBIINT	X
Bit 4	R	INSBIINT	X
Bit 3	R/W	SDET1E	0
Bit 2	R/W	SDET0E	0
Bit 1	R	SDET1INT	X
Bit 0	R	SDET0INT	X

SDET0INT:

This bit only has significance if the S77 input is low.

If the SDET0INT bit is a logic 1, an interrupt has been generated by the SBIDET[0] signal high concurrently with this device driving the SBI DROP bus. This is an indication that there are multiple devices driving the SBI DROP bus simultaneously. The TEMUX 84 will not output data when SBIDET[0] is asserted. The SBIDET0 Collision Detect register should be read to determine which tributary was in conflict. This Interrupt register will be cleared when read.

SDET1INT:

This bit only has significance if the S77 input is low.

If the SDET1INT bit is a logic 1, an interrupt has been generated by the SBIDET[1] signal high concurrently with this device driving the SBI DROP bus. This is an indication that there are multiple devices driving the SBI DROP bus simultaneously. The TEMUX 84 will not output data when SBIDET[1] is asserted. The SBIDET1 Collision Detect register should be read to determine which tributary was in conflict. This Interrupt register will be cleared when read.

SDET0E:

This bit only has significance if the S77 input is low.

The SBI DROP activity detect interrupt enable bit, SDET0E, enables interrupts to be generated on INTB when the SBIDET[0] signal is asserted concurrently with this device driving the SBI DROP bus. When SDET0E is a logic 1, an interrupt will be generated when SBIDET[0] is active with this device driving the SBI DROP bus. When SBIDET[0] is a logic 0, errors are not generated due to SBIDET[0] concurrent with this device driving the SBI DROP bus.

SDET1E:

This bit only has significance if the S77 input is low.

The SBI DROP activity detect interrupt enable bit, SDET1E, enables interrupts to be generated on INTB when the SBIDET[1] signal is asserted concurrently with this device driving the SBI DROP bus. When SDET1E is a logic 1, an interrupt will be generated when SBIDET[1] is active with this device driving the SBI DROP bus. When SBIDET[1] is a logic 0, errors are not generated due to SBIDET[1] concurrent with this device driving the SBI DROP bus.

INSBIINT:

If the INSBIINT bit is a logic 1, the INSBI block is generating an interrupt due to a FIFO underrun or overrun. The INSBI Interrupt register must be read to clear this interrupt.

EXSBIINT:

If the EXSBIINT bit is a logic 1, the EXSBI block is generating an interrupt due to a FIFO underrun or overrun. The EXSBI Interrupt register must be read to clear this interrupt.

SBIDLLINT:

This bit only has significance if the S77 input in pulled high. If the SBIDLLINT bit is a logic 1, the SBI DLL has generated an interrupt indicating it has errored. Register 0x01C7 DLL Control Status must be read to clear this interrupt.

Register 0x0016: Master Interrupt Source DS3/E3 #1

Bit	Type	Function	Default
Bit 7	R	DS3E3PMON1	X
Bit 6	R	DS3E3RDLC1	X
Bit 5	R	DS3RBOC1	X
Bit 4	R	DS3E3FRMR1	X
Bit 3	R	DS3E3TDPR1	X
Bit 2	R	DS3XBOC1	X
Bit 1	R	MX231	X
Bit 0	R	DS3E3PRGD1	X

DS3E3PRGD1:

If the DS3E3PRGD1 bit is a logic 1, the PRGD (Pseudo Random Generator/Receiver) connected to the first DS3 or E3 framer is generating an interrupt. The PRGD #1 Interrupt Enable/Status register must be read to determine the source of the interrupt and to clear this interrupt signal.

MX231:

If the MX231 bit is a logic 1, the first MX23 block is generating an interrupt due to the detection of a DS2 loopback request. The MX23 #1 Loopback Request Interrupt register must be read to clear this interrupt.

DS3XBOC1:

If the DS3XBOC1 bit is a logic 1, the first DS3 XBOC block is generating an interrupt. The DS3 #1 FEAC XBOC Control register must be read to clear the interrupt.

DS3E3TDPR1:

If the DS3E3TDPR1 bit is a logic 1, the first DS3/E3 TDPR block is generating an interrupt. The DS3/E3 #1 TDPR Interrupt Status register must be read to determine which event in the DS3/E3 TDPR has caused the interrupt.

DS3E3FRMR1:

If the DS3FRMR1 bit is a logic 1, the first DS3 FRMR or E3 FRMR block is generating an interrupt. The DS3 #1 FRMR Interrupt status register or the E3

FRMR #1 Framing Interrupt Indication and Status register must be read to determine which event in the DS3 FRMR has caused the interrupt.

DS3RBOC1:

If the DS3RBOC1 bit is a logic 1, the first DS3 RBOC block is generating an interrupt. The DS3 #1 RBOC Interrupt Status register must be read to determine which event in the DS3 RBOC has caused the interrupt.

DS3E3RDLC1:

If the DS3E3RDLC1 bit is a logic 1, the first DS3/E3 RDLC block is generating an interrupt. The DS3/E3 #1 RDLC Status register must be read to determine which event in the DS3/E3 RDLC has caused the interrupt.

DS3E3PMON1:

If the DS3E3PMON1 bit is a logic 1, the first DS3/E3 PMON block is generating an interrupt. The DS3/E3 #1 PMON Interrupt Status register must be read to determine which event in the DS3/E3 PMON has caused the interrupt.

Register 0x0017: Master Interrupt Source DS2 #1

Bit	Type	Function	Default
Bit 7	R	TTB1	X
Bit 6	R	DS2 FRMR#7	X
Bit 5	R	DS2 FRMR#6	X
Bit 4	R	DS2 FRMR#5	X
Bit 3	R	DS2 FRMR#4	X
Bit 2	R	DS2 FRMR#3	X
Bit 1	R	DS2 FRMR#2	X
Bit 0	R	DS2 FRMR#1	X

TTB1:

If the TTB1 bit is a logic 1, the trail trace buffer associated with the first E3 FRMR is generating an interrupt. The TTB #1 Trail Trace Identifier Status register and the TTB #1 Payload Type Label Control/Status register must be read to determine which event has caused the interrupt.

DS2 FRMR#[7:1]:

Any DS2 FRMR#[7:1] bits which are a logic 1 indicate which of the seven DS2 Framers associated with DS3 #1 is generating an interrupt on the INTB output pin. The appropriate DS2 FRMR Interrupt Status register must be read to clear the interrupt.

Register 0x0018: Master Interrupt Source MX12 #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	MX12#7	X
Bit 5	R	MX12#6	X
Bit 4	R	MX12#5	X
Bit 3	R	MX12#4	X
Bit 2	R	MX12#3	X
Bit 1	R	MX12#2	X
Bit 0	R	MX12#1	X

MX12#[7:1]:

Any MX12#[7:1] bits which are a logic 1 indicate a MX12 block that is generating an interrupt on the INTB output pin due to the detection of a DS1 loopback request. The appropriate MX12 Loopback Interrupt register must be read to clear the interrupt.

Register 0x0019: Master Interrupt Source DS3/E3 #2

Bit	Type	Function	Default
Bit 7	R	DS3E3PMON2	X
Bit 6	R	DS3E3RDLC2	X
Bit 5	R	DS3RBOC2	X
Bit 4	R	DS3E3FRMR2	X
Bit 3	R	DS3E3TDPR2	X
Bit 2	R	DS3XBOC2	X
Bit 1	R	MX232	X
Bit 0	R	DS3E3PRGD2	X

DS3E3PRGD2:

If the DS3E3PRGD2 bit is a logic 1, the PRGD (Pseudo Random Generator/Receiver) connected to the second DS3 or E3 framer is generating an interrupt. PRGD #2 Interrupt Enable/Status register must be read to determine the source of the interrupt and to clear this interrupt signal.

MX232:

If the MX232 bit is a logic 1, the second MX23 block is generating an interrupt due to the detection of a DS2 loopback request. The MX23 Loopback Request Interrupt register must be read to clear this interrupt.

DS3XBOC2:

If the DS3XBOC2 bit is a logic 1, the second DS3 XBOC block is generating an interrupt. The DS3 #2 FEAC XBOC Control register must be read to clear the interrupt.

DS3E3TDPR2:

If the DS3E3TDPR2 bit is a logic 1, the second DS3/E3 TDPR block is generating an interrupt. The DS3/E3 #2 TDPR Interrupt Status register must be read to determine which event in the DS3/E3 TDPR has caused the interrupt.

DS3E3FRMR2:

If the DS3FRMR2 bit is a logic 1, the second DS3 FRMR or E3 FRMR block is generating an interrupt. The DS3 #2 FRMR Interrupt status register or the E3 FRMR #2 Framing Interrupt Indication and Status register must be read to determine which event in the DS3 FRMR has caused the interrupt.

DS3RBOC2:

If the DS3RBOC2 bit is a logic 1, the second DS3 RBOC block is generating an interrupt. The DS3 #2 RBOC Interrupt Status register must be read to determine which event in the DS3 RBOC has caused the interrupt.

DS3E3RDLC2:

If the DS3E3RDLC2 bit is a logic 1, the second DS3/E3 RDLC block is generating an interrupt. The DS3/E3 #2 RDLC Status register must be read to determine which event in the DS3/E3 RDLC has caused the interrupt.

DS3E3PMON2:

If the DS3E3PMON2 bit is a logic 1, the second DS3/E3 PMON block is generating an interrupt. The DS3/E3 #2 PMON Interrupt Status register must be read to determine which event in the DS3/E3 PMON has caused the interrupt.

Register 0x001A: Master Interrupt Source DS2 #2

Bit	Type	Function	Default
Bit 7	R	TTB2	X
Bit 6	R	DS2 FRMR#14	X
Bit 5	R	DS2 FRMR#13	X
Bit 4	R	DS2 FRMR#12	X
Bit 3	R	DS2 FRMR#11	X
Bit 2	R	DS2 FRMR#10	X
Bit 1	R	DS2 FRMR#9	X
Bit 0	R	DS2 FRMR#8	X

TTB2:

If the TTB2 bit is a logic 1, the trail trace buffer associated with the second E3 FRMR is generating an interrupt. The TTB #2 Trail Trace Identifier Status register and the TTB #2 Payload Type Label Control/Status register must be read to determine which event has caused the interrupt.

DS2 FRMR#[14:8]:

Any DS2 FRMR#[14:8] bits which are a logic 1 indicate which of the seven DS2 Framers associated with DS3 #2 is generating an interrupt on the INTB output pin. The appropriate DS2 FRMR Interrupt Status register must be read to clear the interrupt.

Register 0x001B: Master Interrupt Source MX12 #2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	MX12#14	X
Bit 5	R	MX12#13	X
Bit 4	R	MX12#12	X
Bit 3	R	MX12#11	X
Bit 2	R	MX12#10	X
Bit 1	R	MX12#9	X
Bit 0	R	MX12#8	X

MX12#[14:8]:

Any MX12#[14:8] bits which are a logic 1 indicate a MX12 block that is generating an interrupt on the INTB output pin due to the detection of a DS1 loopback request. The appropriate MX12 Loopback Interrupt register must be read to clear the interrupt.

Register 0x001C: Master Interrupt Source DS3/E3 #3

Bit	Type	Function	Default
Bit 7	R	DS3E3PMON3	X
Bit 6	R	DS3E3RDLC3	X
Bit 5	R	DS3RBOC3	X
Bit 4	R	DS3E3FRMR3	X
Bit 3	R	DS3E3TDPR3	X
Bit 2	R	DS3XBOC3	X
Bit 1	R	MX233	X
Bit 0	R	DS3E3PRGD3	X

DS3E3PRGD3:

If the DS3E3PRGD1 bit is a logic 1, the PRGD (Pseudo Random Generator/Receiver) connected to the third DS3 or E3 framer is generating an interrupt. PRGD #3 Interrupt Enable/Status register must be read to determine the source of the interrupt and to clear this interrupt signal.

MX233:

If the MX233 bit is a logic 1, the third MX23 block is generating an interrupt due to the detection of a DS2 loopback request. The MX23 #3 Loopback Request Interrupt register must be read to clear this interrupt.

DS3XBOC3:

If the DS3XBOC3 bit is a logic 1, the third DS3 XBOC block is generating an interrupt. The DS3 #3 FEAC XBOC Control register must be read to clear the interrupt.

DS3E3TDPR3:

If the DS3E3TDPR3 bit is a logic 1, the third DS3/E3 TDPR block is generating an interrupt. The DS3/E3 #3 TDPR Interrupt Status register must be read to determine which event in the DS3/E3 TDPR has caused the interrupt.

DS3E3FRMR3:

If the DS3FRMR3 bit is a logic 1, the third DS3 FRMR or E3 FRMR block is generating an interrupt. The DS3 #3 FRMR Interrupt status register or the E3 FRMR #3 Framing Interrupt Indication and Status register must be read to determine which event in the DS3 FRMR has caused the interrupt.

DS3RBOC3:

If the DS3RBOC3 bit is a logic 1, the third DS3 RBOC block is generating an interrupt. The DS3 #3 RBOC Interrupt Status register must be read to determine which event in the DS3 RBOC has caused the interrupt.

DS3E3RDLC3:

If the DS3E3RDLC3 bit is a logic 1, the third DS3/E3 RDLC block is generating an interrupt. The DS3/E3 #3 RDLC Status register must be read to determine which event in the DS3/E3 RDLC has caused the interrupt.

DS3E3PMON3:

If the DS3E3PMON3 bit is a logic 1, the third DS3/E3 PMON block is generating an interrupt. The DS3/E3 #3 PMON Interrupt Status register must be read to determine which event in the DS3/E3 PMON has caused the interrupt.

Register 0x001D: Master Interrupt Source DS2 #3

Bit	Type	Function	Default
Bit 7	R	TTB3	X
Bit 6	R	DS2 FRMR#21	X
Bit 5	R	DS2 FRMR#20	X
Bit 4	R	DS2 FRMR#19	X
Bit 3	R	DS2 FRMR#18	X
Bit 2	R	DS2 FRMR#17	X
Bit 1	R	DS2 FRMR#16	X
Bit 0	R	DS2 FRMR#15	X

TTB3:

If the TTB3 bit is a logic 1, the trail trace buffer associated with the third E3 FRMR is generating an interrupt. The TTB #3 Trail Trace Identifier Status register and the TTB #3 Payload Type Label Control/Status register must be read to determine which event has caused the interrupt.

DS2 FRMR#[21:15]:

Any DS2 FRMR#[21:15] bits which are a logic 1 indicate which of the seven DS2 Framers associated with DS3 #3 is generating an interrupt on the INTB output pin. The appropriate DS2 FRMR Interrupt Status register must be read to clear the interrupt.

Register 0x001E: Master Interrupt Source MX12 #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	MX12#21	X
Bit 5	R	MX12#20	X
Bit 4	R	MX12#19	X
Bit 3	R	MX12#18	X
Bit 2	R	MX12#17	X
Bit 1	R	MX12#16	X
Bit 0	R	MX12#15	X

MX12#[21:15]:

Any MX12#[21:15] bits which are a logic 1 indicate a MX12 block that is generating an interrupt on the INTB output pin due to the detection of a DS1 loopback request. The appropriate MX12 Loopback Interrupt register must be read to clear the interrupt.

Register 0x0020: Master SBIDET0 Collision Detect LSB

Bit	Type	Function	Default
Bit 7	R	COL7	X
Bit 6	R	COL6	X
Bit 5	R	COL5	X
Bit 4	R	COL4	X
Bit 3	R	COL3	X
Bit 2	R	COL2	X
Bit 1	R	COL1	X
Bit 0	R	COL0	X

Register 0x0021: Master SBIDET0 Collision Detect MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	COL8	X

COL[8:0]:

The SBIDET[0] Collision Detection identifier, COL[8:0], identifies the SBI column number of the last collision as indicated by the SDET0INT interrupt. The tributary experiencing contention is calculated from COL[8:0] as follows:
SPE# or DS3# = MOD(COL[8:0]-1,3)+1
T1# or TVT1.5# = SPE#, MOD(TRUNC((COL[8:0]-10)/3-1),28)+1
E1# or TVT2# = SPE#, MOD(TRUNC((COL[8:0]-10)/3-1),21)+1

Register 0x0022: Master SBIDET1 Collision Detect LSB

Bit	Type	Function	Default
Bit 7	R	COL7	X
Bit 6	R	COL6	X
Bit 5	R	COL5	X
Bit 4	R	COL4	X
Bit 3	R	COL3	X
Bit 2	R	COL2	X
Bit 1	R	COL1	X
Bit 0	R	COL0	X

Register 0x0023: Master SBIDET1 Collision Detect MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	COL8	X

COL[8:0]:

The SBIDET[1] Collision Detection identifier, COL[8:0], identifies the SBI column number of the last collision as indicated by the SDET1INT interrupt. The tributary experiencing contention is calculated from COL[8:0] as follows:
SPE# or DS3# = MOD(COL[8:0]-1,3)+1
T1# or TVT1.5# = SPE#, MOD(TRUNC((COL[8:0]-10)/3-1),28)+1
E1# or TVT2# = SPE#, MOD(TRUNC((COL[8:0]-10)/3-1),21)+1

1.3 T1/E1 Master Configuration Registers

Register 0x0040: T1/E1 Master Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	RX_SBI_SIGINS	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	EALMEN	0
Bit 0	R/W	RESET	0

RESET:

The RESET bit allows software to hold the T1/E1 framers in a reset condition. When RESET is a logic 1, the entire T1/E1 block will be held in a reset state which is also a low power state. This will force all registers to their default state. While in reset, the clocks can not be guaranteed accurate or existing. When RESET is a logic 0, the T1/E1 framers are in normal operating mode.

The T1/E1 framers cannot be held reset when running unchannelized DS3/E3 over SBI.

EALMEN:

The EALMEN bit enables an egress SBI alarm indication signal to force the transmit data stream into an all ones AIS. When EALMEN is a logic 1 and the SBI bus is selected, the ALM bit set to one in the SBI LinkRate Octet(V4) will force the transmit data to the VT/TU mapper and DS3 M13 multiplexer to all ones. When EALMEN is a logic 0, ALM bit will not affect the transmit data stream. A logic 1 in the TAISEN bit in the TJAT Indirect Channel Data register forces all ones in the tributary regardless of the state of EALMEN. This bit can be used with the EGRALMEN bit in the SONET/SDH Master Tributary Alarm AIS Control register. While TAISEN can only force all ones AIS into the data stream, EGRALMEN also enables the TTOP block to handle the state associated with going in and out of AIS and the New Data Flag in the V1 byte.

The diagnostic loopback point is upstream of this AIS insertion point.

Reserved:

These bits must be logic 0 for correct operation.

RX_SBI_SIGINS:

This bit enables the re-insertion of signaling into the T1 robbed-bit positions. By default, the signaling is extracted and presented in the S-bits. If RX_SBI_SIGINS is a logic 1 and the appropriate per-tributary configuration is done, the signaling is also inserted into the robbed bit positions as determined by the multiframe alignment being communicated across the SBI bus. These robbed bit positions may be different from the positions the signaling was received on. The inserted signaling is subjected to the same trunk conditioning, freezing and debouncing as the S-bits.

For the RX_SBI_SIGINS bit to have effect on a specific tributary, the following must be true: the global PCCE of the RPCC-SBI Configuration Bits register is logic 1, the per-tributary PCCE bit of the RPCC-SBI Indirect Channel Data Registers has been set to logic 1 and the SIGSRC[1:0] bits of the RPCC-SBI Indirect Channel Data Registers are 01 or 10.

Register 0x0042: T1/E1 PRGD #1 Tributary Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PRGD1SPE1	0
Bit 5	R/W	PRGD1SPE0	0
Bit 4	R/W	PRGD1LNK4	0
Bit 3	R/W	PRGD1LNK3	0
Bit 2	R/W	PRGD1LNK2	0
Bit 1	R/W	PRGD1LNK1	0
Bit 0	R/W	PRGD1LNK0	0

PRGD1SPE[1:0], PRGD1LNK[4:0]:

Selects the T1/E1 tributary associated with the first full featured pattern generator and receiver. When this register is all zeros, no tributary is selected and the generator/receiver pair is inactive. PRGD1SPE[1:0] values of 1 to 3 select the SPE or DS3 from which the tributary is extracted. PRGD1LNK[4:0] values from 1 to 28 select the tributary from one of the 28 T1/E1 tributaries per SPE/DS3. When in E1 mode, PRGD1LNK[4:0] values from 22 through 28 will disable the generator/receiver pair.

Register 0x0043: T1/E1 PRGD #2 Tributary Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PRGD2SPE1	0
Bit 5	R/W	PRGD2SPE0	0
Bit 4	R/W	PRGD2LNK4	0
Bit 3	R/W	PRGD2LNK3	0
Bit 2	R/W	PRGD2LNK2	0
Bit 1	R/W	PRGD2LNK1	0
Bit 0	R/W	PRGD2LNK0	0

PRGD2SPE[1:0], PRGD2LNK[4:0]:

Selects the T1/E1 tributary associated with the second full featured pattern generator and receiver. When this register is all zeros, no tributary is selected and the generator/receiver pair is inactive. PRGD2SPE[1:0] values of 1 to 3 select the SPE or DS3 from which the tributary is extracted. PRGD2LNK[4:0] values from 1 to 28 select the tributary from one of the 28 T1/E1 tributaries per SPE/DS3. When in E1 mode, PRGD2LNK[4:0] values from 22 through 28 will disable the generator/receiver pair.

Register 0x0044: T1/E1 PRGD #3 Tributary Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PRGD3SPE1	0
Bit 5	R/W	PRGD3SPE0	0
Bit 4	R/W	PRGD3LNK4	0
Bit 3	R/W	PRGD3LNK3	0
Bit 2	R/W	PRGD3LNK2	0
Bit 1	R/W	PRGD3LNK1	0
Bit 0	R/W	PRGD3LNK0	0

PRGD3SPE[1:0], PRGD3LNK[4:0]:

Selects the T1/E1 tributary associated with the third full featured pattern generator and receiver. When this register is all zeros, no tributary is selected and the generator/receiver pair is inactive. PRGD3SPE[1:0] values of 1 to 3 select the SPE or DS3 from which the tributary is extracted. PRGD3LNK[4:0] values from 1 to 28 select the tributary from one of the 28 T1/E1 tributaries per SPE/DS3. When in E1 mode, PRGD3LNK[4:0] values from 22 through 28 will disable the generator/receiver pair.

Register 0x0045: T1/E1 PRGD #4 Tributary Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PRGD4SPE1	0
Bit 5	R/W	PRGD4SPE0	0
Bit 4	R/W	PRGD4LNK4	0
Bit 3	R/W	PRGD4LNK3	0
Bit 2	R/W	PRGD4LNK2	0
Bit 1	R/W	PRGD4LNK1	0
Bit 0	R/W	PRGD4LNK0	0

PRGD4SPE[1:0], PRGD4LNK[4:0]:

Selects the T1/E1 tributary associated with the fourth full featured pattern generator and receiver. When this register is all zeros, no tributary is selected and the generator/receiver pair is inactive. PRGD4SPE[1:0] values of 1 to 3 select the SPE or DS3 from which the tributary is extracted. PRGD4LNK[4:0] values from 1 to 28 select the tributary from one of the 28 T1/E1 tributaries per SPE/DS3. When in E1 mode, PRGD4LNK[4:0] values from 22 through 28 will disable the generator/receiver pair.

Register 0x0046: T1/E1 PRGD #5 Tributary Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PRGD5SPE1	0
Bit 5	R/W	PRGD5SPE0	0
Bit 4	R/W	PRGD5LNK4	0
Bit 3	R/W	PRGD5LNK3	0
Bit 2	R/W	PRGD5LNK2	0
Bit 1	R/W	PRGD5LNK1	0
Bit 0	R/W	PRGD5LNK0	0

PRGD5SPE[1:0], PRGD5LNK[4:0]:

Selects the T1/E1 tributary associated with the fifth full featured pattern generator and receiver. When this register is all zeros, no tributary is selected and the generator/receiver pair is inactive. PRGD5SPE[1:0] values of 1 to 3 select the SPE or DS3 from which the tributary is extracted. PRGD5LNK[4:0] values from 1 to 28 select the tributary from one of the 28 T1/E1 tributaries per SPE/DS3. When in E1 mode, PRGD5LNK[4:0] values from 22 through 28 will disable the generator/receiver pair.

Register 0x0047: T1/E1 PRGD #6 Tributary Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PRGD6SPE1	0
Bit 5	R/W	PRGD6SPE0	0
Bit 4	R/W	PRGD6LNK4	0
Bit 3	R/W	PRGD6LNK3	0
Bit 2	R/W	PRGD6LNK2	0
Bit 1	R/W	PRGD6LNK1	0
Bit 0	R/W	PRGD6LNK0	0

PRGD6SPE[1:0], PRGD6LNK[4:0]:

Selects the T1/E1 tributary associated with the sixth full featured pattern generator and receiver. When this register is all zeros, no tributary is selected and the generator/receiver pair is inactive. PRGD6SPE[1:0] values of 1 to 3 select the SPE or DS3 from which the tributary is extracted. PRGD6LNK[4:0] values from 1 to 28 select the tributary from one of the 28 T1/E1 tributaries per SPE/DS3. When in E1 mode, PRGD6LNK[4:0] values from 22 through 28 will disable the generator/receiver pair.

1.4 T1/E1 Receive Jitter Attenuator (RJAT) Registers

Register 0x0048: RJAT Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0		Unused	

Writing to this register triggers an indirect channel register access.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the RJAT Indirect Channel Data register. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the RJAT Indirect Channel Data register.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the RJAT Indirect Channel Data register or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0049: RJAT Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the RJAT channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 3. CADDR[4:0] is the tributary index and ranges from 1 to 28.

Register 0x004A: RJAT Indirect Channel Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	DLOOP	0
Bit 2	R/W	Unused	0
Bit 1	R/W	TXPMON	0
Bit 0	R/W	RJATBYP	0

This register contains data read from the RJAT channel context RAM after an indirect read operation or data to be inserted into the RJAT channel context RAM in an indirect write operation.

The bits to be written to the RJAT channel context RAM, in an indirect channel write operation, must be set up in this register before triggering the write. Irregardless of writes to this register, reads will always return the data retrieved by the latest indirect read operation.

RJATBYP:

The RJATBYP bit disables jitter attenuation in the receive direction. When receive jitter attenuation is not being used, setting RJATBYP to logic 1 will reduce the latency through the receiver section by typically 40 bits. The receive jitter attenuator must not be bypassed when receiving T1 tributaries via the DS3 multiplexer.

RJATBYP must be logic 1 for tributaries that have been synchronously demapped.

TXPMON:

When in Mapper/Multiplexer mode (i.e. OPMODE_SPEx[1:0] is 01 binary) this bit selects performance monitoring for the transmit path. Performance monitoring includes maintenance of all T1/E1 framer counts and statuses plus HDLC termination. When TXPMON is logic 1, performance monitoring is performed on the egress tributary. When TXPMON is logic 0, performance

monitoring is performed on the ingress tributary. In Transmux mode (i.e. OPMODE_SPEx[1:0] is 10 binary), TXPMON set to 1 selects the mapper transmit stream for performance monitoring and TXPMON set to 0 selects the DS3 transmit stream for performance monitoring.

TXPMON can be used in High Density Framer mode for unchannelized tributaries or for byte synchronously mapped tributaries.

DLOOP:

The DLOOP bit selects the T1/E1 diagnostic loopback, where the tributary is configured to internally direct the output of the TJAT to the input of the RJAT. When DLOOP is set to logic 1, the diagnostic loopback mode is enabled. When DLOOP is set to logic 0, the diagnostic loopback mode is disabled. The TJATBYP context bit can be used to bypass the egress jitter attenuator FIFO to decrease latency.

In transmux mode, setting DLOOP to a logic 1 will enable a T1/E1 tributary loopback from the SONET/SDH demapper to the SONET/SDH mapper.

Reserved:

The Reserved bits must be logic 0 for correct operation.

Register 0x004B: RJAT Programmable Corner Frequency Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	M[2]	1
Bit 1	R/W	M[1]	0
Bit 0	R/W	M[0]	0

This register is used to program the corner frequency of the receive T1/E1 jitter attenuator. M[2:0] can be used to select one of eight possible corner frequencies as follows:

M[2:0]	T1	E1
000	18.0 Hz	25.0 Hz
001	9.0 Hz	12.0 Hz
010	6.0 Hz	8.0 Hz
011	4.4 Hz	6.0 Hz
100	3.4 Hz (default)	5.0 Hz (default)
101	3.0 Hz	4.0 Hz
110	2.5 Hz	3.3 Hz
111	2.1 Hz	3.0 Hz

1.5 T1/E1 Transmit Jitter Attenuator (TJAT) Registers

Register 0x004C: TJAT Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0		Unused	

Writing to this register triggers an indirect channel register access.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the TJAT Indirect Channel Data register. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the TJAT Indirect Channel Data register.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the TJAT Indirect Channel Data register or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x004D: TJAT Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the TJAT channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 3. CADDR[4:0] is the tributary index and ranges from 1 to 28.

Register 0x004E: TJAT Indirect Channel Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	REFSEL	0
Bit 5	R/W	LOOPT	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	LLOOP	0
Bit 2	R/W	Unused	0
Bit 1	R/W	TAISEN	0
Bit 0	R/W	TJATBYP	0

This register contains data read from the TJAT channel context RAM after an indirect read operation or data to be inserted into the TJAT channel context RAM in an indirect write operation.

The bits to be written to the TJAT channel context RAM, in an indirect channel write operation, must be set up in this register before triggering the write. Irregardless of writes to this register, reads will always return the data retrieved by the latest indirect read operation.

TJATBYP:

The TJATBYP bit bypasses the transmit jitter attention FIFO. Although setting TJATBYP has the effect of reducing latency, it also has the side effect of reducing jitter tolerance at the system interface. Jitter attenuation should be used when additional jitter attenuation is required on the external transmit reference clock or when in clock slave mode and the data needs jitter attenuation.

Note that the transmit jitter attenuator may be used to generate a transmit clock for clock master applications and when using the transmit elastic store even if TJATBYP is logic 1.

TJATBYP must be logic 1 for tributaries that are byte synchronously mapped.

TAISEN:

The TAISEN bit enables generation of an all ones AIS alarm in the egress tributary. When TAISEN is a logic 1 the egress data stream is forced to all ones. When TAISEN is a logic 0 the egress tributary operates normally. The diagnostic loopback point is upstream of this AIS insertion point.

LLOOP:

The LLOOP bit selects the line loopback mode, where the recovered data are internally directed to the inputs of egress mapper or multiplexer. When LLOOP is set to logic 1, the line loopback mode is enabled. When LLOOP is set to logic 0, the line loopback mode is disabled.

When LLOOP is logic 1, the RJATBYP bit for the tributary must be logic 0 unless the tributary is SONET/SDH byte synchronously mapped.

In transmux mode, setting LLOOP to a logic 1 will enable a T1/E1 tributary loopback from the M13 demultiplexer to the M13 multiplexer.

Reserved:

The reserved bit must be logic 0 for correct operation.

LOOPT, REFSEL:

The LOOPT context bit is used to enable loop-timing. The REFSEL input determines the reference for the egress data rate. If LLOOP is logic 1, the transmit data is automatically loop-timed.

LOOPT	REFSEL	Description
0	0	Transmit data locked to egress data rate at the SBI Add bus system interface. Legal only if transmit elastic store is bypassed. Cannot be used when SYSOPT[1:0] register bits are binary 01 or 11.
0	1	Transmit data locked to CTCLK or recovered clock selected by the REFCLK[1:0] bits of the

		Reference Clock Select register.
1	0	Transmit data locked to ingress recovered clock for the tributary.
1	1	Reserved.

Register 0x004F: TJAT Programmable Corner Frequency Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	M[2]	1
Bit 1	R/W	M[1]	0
Bit 0	R/W	M[0]	0

This register is used to program the corner frequency of the transmit T1/E1 jitter attenuator. M[2:0] can be used to select one of eight possible corner frequencies as follows:

M[2:0]	T1	E1
000	18.0 Hz	25.0 Hz
001	9.0 Hz	12.0 Hz
010	6.0 Hz	8.0 Hz
011	4.4 Hz	6.0 Hz
100	3.4 Hz (default)	5.0 Hz (default)
101	3.0 Hz	4.0 Hz
110	2.5 Hz	3.3 Hz
111	2.1 Hz	3.0 Hz

1.6 T1/E1 Receive H-MVIP Per-Channel Controller (RPCC) Registers

Register 0x0050: RPCC-MVIP Indirect Status/Time-slot Address

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5	R/W	TSACCESS	0
Bit 4	R/W	TSADDR[4]	0
Bit 3	R/W	TSADDR[3]	0
Bit 2	R/W	TSADDR[2]	0
Bit 1	R/W	TSADDR[1]	0
Bit 0	R/W	TSADDR[0]	0

Writing to this register triggers an indirect channel register access to the Receive Per-Channel Controller (RPCC-MVIP) context RAM.

TSADDR[4:0]:

The timeslot address determines the DS0 timeslot/channel accessed when an access is initiated with TSACCESS logic 1.

For T1 tributaries, the valid range is 1 to 24. For E1 tributaries, the valid range is 0 to 31.

TSACCESS:

The timeslot indirect access control bit determines whether the per-tributary or per-timeslot data is accessed. If TSACCESS is logic 0, the per-tributary data is accessed. If TSACCESS is logic 1, the per-timeslot data is accessed with the timeslot determined by the TSADDR[4:0] bits.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the RPCC-MVIP Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the RPCC-MVIP Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the RPCC-MVIP Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0051: RPCC-MVIP Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the RPCC-MVIP context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 3. CADDR[4:0] is the tributary index and ranges from 1 to 28.

Registers 0x0052-0x0056: RPCC-MVIP Indirect Channel Data Registers

These registers contain data read from the RPCC-MVIP channel context RAM after an indirect read operation or data to be inserted into the RPCC-MVIP channel context RAM in an indirect write operation.

The bits to be written to the RPCC-MVIP channel context RAM, in an indirect channel write operation, must be set up in these registers before triggering the write. All three registers from 0x0052 through 0x0054 inclusive must be written prior to each indirect write unless one desires the same configuration as the latest indirect write. The value returned by the latest indirect read has no bearing on indirect writes. Irregardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

The significance of the bits is dependent on the state of the TSACCESS bit of the RPCC-MVIP Indirect Status/Time-slot Address register. If TSACCESS is logic 1, context information for the timeslot/channel identified by TSADDR[4:0] is either written or read.

<u>TSACCESS=0:</u>

Address	**Offset**								
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default (‘b)**
0x0052	RPRBSLEN[2:0]			RPRBS UNF	MDTRK	MSTRK	PCCE	Unused	00000000
0x0053	T56K PRBS	TPRBS INV	TPRBSLEN[2:0]			TPRBS UNF	R56K PRBS	RPRBS INV	00000000
0x0054	PRBSERR[2:0]			PSYNCI	PSYNC	Reserved	PSYNCE	INV LAST	XXXXXX00
0x0055	PRBSERR[10:3]								XXXXXXXX
0x0056	Unused			PRBSERR[15:11]					XXXXXXXX

TSACCESS=1:

Address	Offset								
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default ('b)**
0x0052	SIGSRC	INV[1:0]		ALAW	DMW	IDLC	ZCS[1:0]		00000000
0x0053	IDLE[2:0]			A'	B'	C'	D'	Reserved	000000000
0x0054	Unused	TPRBS	RPRBS	IDLE[7:3]					XX000000
0x0055	Unused								XXXXXXXX
0x0056	Unused								XXXXXXXX

In the following bit descriptions, the system interface refers to the Ingress H-MVIP Interface. Be aware that the PRBS receiver documented is down stream of the frame slip buffer; therefore, controlled slips will corrupt the bit sequence and result in bit errors and momentary loss of synchronization.

PCCE:

The per-tributary configuration enable bit, PCCE, enables the configuration data to affect the signaling and PCM byte streams. If the PCCE is logic 1, it enables the both the TSACCESS=0 and TSACCESS=1 Configuration bits. The global PCCE bit of the RPCC-MVIP Configuration Bits register must also be logic 1 for this bit to have effect.

Upon setting this bit to logic 0, the PRBS shift registers and statuses are frozen.

MSTRK:

Master Signaling Trunk Conditioning. When this bit is logic 1, signaling substitution at the system interface (CASID output) is performed on all channels/time slots for a tributary. Setting MSTRK is equivalent to setting the SIGSRC bit to logic 1 for all channels/timeslots.

MDTRK:

Master Data Trunk Conditioning. When this bit is logic 1, idle code substitution at the system interface (MVID output) is performed on all channels/time slots for a tributary. For E1, this includes overwriting TS0 with its IDLE[7:0] bits. For T1, the F-bit is not altered. Setting MDTRK is equivalent to setting the IDLC Per-Channel context bit to logic 1 for all channels/timeslots.

RPRBSUNF:

If this bit is logic 1, the PRBS is expected to fill all bits in the tributary data stream received from the SONET/SDH mapper or DS3 multiplexer. This bit supercedes the Per-Channel RPRBS context bits and the R56KPRBS context bits. The T1 F-bit is excluded from the pattern, so setting RPRSBUNF is equivalent to setting all 24 RPRBS per-channel bits. For E1, the PRBS pattern fills all bit positions.

RPRBSLEN[2:0]:

The Receive PRBS Length field determines the sequence length of the expected bit pattern received from the SONET/SDH mapper or DS3 multiplexer:

RPRBSLEN	Sequence Length	Polynomial
000	$2^{11} - 1$	$x^{11} + x^9 + 1$
001	$2^{15} - 1$	$x^{15} + x^{14} + 1$
010	$2^{20} - 1$ (QRSS)	$x^{20} + x^{17} + 1$ with zero suppression
011	$2^{20} - 1$	$x^{20} + x^3 + 1$
100	$2^7 - 1$	$x^7 + x^3 + 1$ with XOR in the feedback path
101	$2^7 - 1$	$x^7 + x^3 + 1$ with XNOR in the feedback path

RPRBSINV:

If this bit is logic 1, the logical polarity of the received PRBS is inverted before comparison.

R56KPRBS:

If this bit is logic 1, the PRBS is expected to fill only the first seven bits of the selected channels/time slots. Otherwise, the PRBS is expected to occupy the entire selected channels/time slots. The T1 F-bit is excluded from the pattern, so setting RPRSBUNF is equivalent to setting all 24 RPRBS per-channel bits. For E1, the PRBS pattern fills all bit positions.

TPRBSUNF:

If this bit is logic 1, the PRBS fills all bits of the tributary at the system interface (H-MVIP MVID output). This bit supercedes the Per-Channel TPRBS context bits and the T56KPRBS context bits. The T1 F-bit is excluded

from the pattern, so setting TPRSBUNF is equivalent to setting all 24 TPRBS per-channel bits. For E1, the PRBS pattern fills all bit positions.

TPRBSLEN[2:0]:

The Transit PRBS Length field determines the sequence length of the generated bit pattern destined for the H-MVIP output:

TPRBSLEN	Sequence Length	Polynomial
000	$2^{11} - 1$	$x^{11} + x^9 + 1$
001	$2^{15} - 1$	$x^{15} + x^{14} + 1$
010	$2^{20} - 1$ (QRSS)	$x^{20} + x^{17} + 1$ with zero suppression
011	$2^{20} - 1$	$x^{20} + x^3 + 1$
100	$2^7 - 1$	$x^7 + x^3 + 1$ with XOR in the feedback path
101	$2^7 - 1$	$x^7 + x^3 + 1$ with XNOR in the feedback path

TPRBSINV:

If this bit is logic 1, the logical polarity of the generated PRBS is inverted before transmission.

T56KPRBS

If this bit is logic 1, the generated PRBS fills only the first seven bits of the selected channels/time slots. Otherwise, the PRBS occupies the entire selected channels/time slots.

INVLAST:

If this bit is logic 1, inversion (as controlled by the INV[1:0] Per-Channel context bits) is the last per-channel operation performed on the data. Otherwise, inversion is the first operation performed.

PSYNCE:

If this bit is a logic 1, the associated RPCCI[x] bit is set upon a change in the PSYNC context bit.

PSYNC:

PSYNC is the PRBS synchronization status. PSYNC becomes a logic 1 if the received data matched the expected sequence for the latest four bytes. PSYNC is set to logic 0 only if 3 consecutive bytes are in error.

PSYNCI:

PSYNCI becomes a logic 1 upon a change in the PSYNC context bit. It is cleared upon an indirect read access.

PRBSERR[15:0]:

The PRBS Error holding register contains a count of the discrepancies between the expected PRBS sequence and the receive data that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_PRBS bit to logic 1. The count saturates at all ones.

ZCS[1:0]:

These bits control the Zero Code Suppression on the MVID output as follows:

T1:

ZCS[1:0]	Description
00	No Zero Code Suppression
01	GTE Zero Code Suppression. The least significant bit (bit 8) of an all zeros channel is forced to a one, except for signaling frames where the second least significant bit is forced to a one.
10	DDS Zero Code Suppression. All zero channel data is replaced with the pattern "10011100"
11	Bell Zero Code Suppression. The second least significant bit (bit 7) of an all zeros channel is forced to a one.

E1:

ZCS[1:0]	Description
00	No Zero Code Suppression
01	Jammed bit-8. The least significant bit (bit 8) of an all zeros channel is forced to a one.
10	No Zero Code Suppression
11	Jammed bit-8.

Zero code suppression occurs after data inversion, idle code insertion, digital milliwatt insertion and signaling have occurred.

IDLC:

If this bit is logic 1, the channel/time slot data at the system interface (MVID output) is replaced by the value in the IDLE[7:0] field.

DMW:

If this bit is logic 1, the channel/time slot data at the system interface (MVID output) is replaced by the Digital Milliwatt signal. The encoding of the 1 kHz sine wave is determined by the ALAW context bit.

ALAW:

This bit determines the encoding of the Digital Milliwatt signal. If ALAW is logic 0, μ-law companding is respected. If ALAW is logic 1, A-law companding is respected.

INV[1:0]:

These bits invert the channel/time slot data on the MVID output:

INV[1:0]	T1 Description	E1 Description
00	No inversion (default)	No inversion (default)
01	Only the MSB of the received PCM channel data is inverted (Sign bit inversion)	Invert even bits
10	All bits EXCEPT the MSB of the received PCM channel data is inverted (Magnitude inversion)	Invert odd bits
11	Invert all bits	Invert all bits

SIGSRC:

This bit determines the source of signaling presented at the system interface (CASID output). If SIGSRC is logic 1, the signaling is taken from the A',B',C',D' bits. If SIGSRC is logic 0, received signaling is passed through to the system interface (subject to debouncing and bit fixing).

Reserved:

This bit must be logic 0 for correct operation.

A',B',C',D':

These signaling bits are inserted at the system interface (CASID output) when the MSTRK bit is logic 1 or if the SIGSRC bit is logic 1. For the T1 SF frame format, C' and D' must equal A' and B', respectively.

IDLE[7:0]:

This field contains the value inserted at the system interface (MVID output) if the MDTRK or IDLC bit is logic 1.

RPRBS:

If this bit is logic 1, a PRBS is expected in the channel/time slot received from the SONET/SDH mapper or DS3 multiplexer.

TPRBS:

If this bit is logic 1, a PRBS is generated in the channel/time slot destined for the H-MVIP output, MVID.

Register 0x0057: RPCC-MVIP Configuration Bits

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	INTE	0
Bit 3	R/W	Reserved	0
Bit 2	W12C	XFERI	X
Bit 1	R/W	XFERE	0
Bit 0	R/W	PCCE	0

INTE:

If this bit is a logic 1, the RPRBS bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the RPCCI[84:1] bits is a logic 1.

Reserved:

This bit must be logic 0 for correct operation.

XFERI:

The XFERI bit indicates that a transfer of accumulated PRBS error data has occurred. A logic 1 in this bit position indicates that the holding registers have been updated. This update is initiated by a write to the Global Performance Monitor Update register that sets the E1T1_PRBS bit to logic 1.

Logic 1 must be written to this bit to clear it to logic 0.

XFERE:

If this bit is a logic 1, the RPRBS bit of the Master Interrupt Source T1E1 register is logic 1 if the XFERI bit is a logic 1.

PCCE:

This global bit enables RPCC-MVIP per-channel/per-timeslot functions if logic 1. The per-tributary PCCE bits set through the RPCC-MVIP Indirect Channel Data Registers must also be set to enable individual tributaries.

Upon setting this bit to logic 0, the PRBS shift registers and statuses are frozen.

Register 0x0058: RPCC-MVIP Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R	REG11_12I	X
Bit 6	R	REGF_10I	X
Bit 5	R	REGC_D_EI	X
Bit 4	R	REG9_A_BI	X
Bit 3	W12C	RPCCI[4]	X
Bit 2	W12C	RPCCI[3]	X
Bit 1	W12C	RPCCI[2]	X
Bit 0	W12C	RPCCI[1]	X

RPCCI[84:1]:

A logic 1 in these bits indicate a change of PRBS synchronization state on the associated tributary since the bit was explicitly cleared. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG9_A_BI:

This bit is a logic 1 if at least one bit in Register 0x0059, 0x005A or 0x005B is logic 1.

REGC_D_EI:

This bit is a logic 1 if at least one bit in Register 0x005C, 0x005D or 0x005E is logic 1.

REGF_10I:

This bit is a logic 1 if at least one bit in Register 0x005F or 0x0060 is logic 1.

REG11_12I:

This bit is a logic 1 if at least one bit in Register 0x0061 or 0x0062 is logic 1.

Register 0x0059: RPCC-MVIP Interrupt Status #2

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[12]	X
Bit 6	W12C	RPCCI[11]	X
Bit 5	W12C	RPCCI[10]	X
Bit 4	W12C	RPCCI[9]	X
Bit 3	W12C	RPCCI[8]	X
Bit 2	W12C	RPCCI[7]	X
Bit 1	W12C	RPCCI[6]	X
Bit 0	W12C	RPCCI[5]	X

Register 0x005A: RPCC-MVIP Interrupt Status #3

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[20]	X
Bit 6	W12C	RPCCI[19]	X
Bit 5	W12C	RPCCI[18]	X
Bit 4	W12C	RPCCI[17]	X
Bit 3	W12C	RPCCI[16]	X
Bit 2	W12C	RPCCI[15]	X
Bit 1	W12C	RPCCI[14]	X
Bit 0	W12C	RPCCI[13]	X

Register 0x005B: RPCC-MVIP Interrupt Status #4

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[28]	X
Bit 6	W12C	RPCCI[27]	X
Bit 5	W12C	RPCCI[26]	X
Bit 4	W12C	RPCCI[25]	X
Bit 3	W12C	RPCCI[24]	X
Bit 2	W12C	RPCCI[23]	X
Bit 1	W12C	RPCCI[22]	X
Bit 0	W12C	RPCCI[21]	X

Register 0x005C: RPCC-MVIP Interrupt Status #5

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[36]	X
Bit 6	W12C	RPCCI[35]	X
Bit 5	W12C	RPCCI[34]	X
Bit 4	W12C	RPCCI[33]	X
Bit 3	W12C	RPCCI[32]	X
Bit 2	W12C	RPCCI[31]	X
Bit 1	W12C	RPCCI[30]	X
Bit 0	W12C	RPCCI[29]	X

Register 0x005D: RPCC-MVIP Interrupt Status #6

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[44]	X
Bit 6	W12C	RPCCI[43]	X
Bit 5	W12C	RPCCI[42]	X
Bit 4	W12C	RPCCI[41]	X
Bit 3	W12C	RPCCI[40]	X
Bit 2	W12C	RPCCI[39]	X
Bit 1	W12C	RPCCI[38]	X
Bit 0	W12C	RPCCI[37]	X

Register 0x005E: RPCC-MVIP Interrupt Status #7

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[52]	X
Bit 6	W12C	RPCCI[51]	X
Bit 5	W12C	RPCCI[50]	X
Bit 4	W12C	RPCCI[49]	X
Bit 3	W12C	RPCCI[48]	X
Bit 2	W12C	RPCCI[47]	X
Bit 1	W12C	RPCCI[46]	X
Bit 0	W12C	RPCCI[45]	X

Register 0x005F: RPCC-MVIP Interrupt Status #8

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[60]	X
Bit 6	W12C	RPCCI[59]	X
Bit 5	W12C	RPCCI[58]	X
Bit 4	W12C	RPCCI[57]	X
Bit 3	W12C	RPCCI[56]	X
Bit 2	W12C	RPCCI[55]	X
Bit 1	W12C	RPCCI[54]	X
Bit 0	W12C	RPCCI[53]	X

Register 0x0060: RPCC-MVIP Interrupt Status #9

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[68]	X
Bit 6	W12C	RPCCI[67]	X
Bit 5	W12C	RPCCI[66]	X
Bit 4	W12C	RPCCI[65]	X
Bit 3	W12C	RPCCI[64]	X
Bit 2	W12C	RPCCI[63]	X
Bit 1	W12C	RPCCI[62]	X
Bit 0	W12C	RPCCI[61]	X

Register 0x0061: RPCC-MVIP Interrupt Status #10

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[76]	X
Bit 6	W12C	RPCCI[75]	X
Bit 5	W12C	RPCCI[74]	X
Bit 4	W12C	RPCCI[73]	X
Bit 3	W12C	RPCCI[72]	X
Bit 2	W12C	RPCCI[71]	X
Bit 1	W12C	RPCCI[70]	X
Bit 0	W12C	RPCCI[69]	X

Register 0x0062: RPCC-MVIP Interrupt Status #11

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[84]	X
Bit 6	W12C	RPCCI[83]	X
Bit 5	W12C	RPCCI[82]	X
Bit 4	W12C	RPCCI[81]	X
Bit 3	W12C	RPCCI[80]	X
Bit 2	W12C	RPCCI[79]	X
Bit 1	W12C	RPCCI[78]	X
Bit 0	W12C	RPCCI[77]	X

Register 0x0063: RPCC-MVIP PRBS Error Insertion

Bit	Type	Function	Default
Bit 7	RW	TPRBS_ERR_INSERT	X
Bit 6	RW	TPRBS_ADDR[6]	X
Bit 5	RW	TPRBS_ADDR[5]	X
Bit 4	RW	TPRBS_ADDR[4]	X
Bit 3	RW	TPRBS_ADDR[3]	X
Bit 2	RW	TPRBS_ADDR[2]	X
Bit 1	RW	TPRBS_ADDR[1]	X
Bit 0	RW	TPRBS_ADDR[0]	X

TPRBS_ERR_INSERT:

The TPRBS Error insertion Enable bit causes a single bit error to be inserted in the PRBS pattern for the tributary addressed by TPRBS_ADDR[6:0]. A zero to one transition triggers the error insertion.

TPRBS_ADDR[6:0]:

Indicates the tributary into which a single bit error is to be inserted. TPRBS_ADDR[6:5] is the SPE index and ranges from 1 to 3. TPRBS_ADDR[4:0] is the tributary index and ranges from 1 to 28.

Register 0x0064: RPCC-MVIP PRBS Error Insert Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	W12C	TPRBS_ERR_INSERTED	X

TPRBS_ERR_INSERTED:

TPRBS_ERR_INSERTED indicates an error has been inserted. This bit is cleared to logic 0 upon writing a logic 1 to the bit position.

1.7 T1/E1 Receive SBI Per-Channel Controller (RPCC-SBI) Registers

Register 0x0068: RPCC-SBI Indirect Status/Time-slot Address

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5	R/W	TSACCESS	0
Bit 4	R/W	TSADDR[4]	0
Bit 3	R/W	TSADDR[3]	0
Bit 2	R/W	TSADDR[2]	0
Bit 1	R/W	TSADDR[1]	0
Bit 0	R/W	TSADDR[0]	0

Writing to this register triggers an indirect channel register access to the Receive Per-Channel Controller (RPCC-SBI) context RAM.

TSADDR:

The timeslot address determines the DS0 timeslot/channel accessed when an access is initiated with TSACCESS logic 1.

For T1 tributaries, the valid range is 1 to 24. For E1 tributaries, the valid range is 0 to 31.

TSACCESS:

The timeslot indirect access control bit determines whether the per-tributary or per-timeslot data is accessed. If TSACCESS is logic 0, the per-tributary data is accessed. If TSACCESS is logic 1, the per-timeslot data is accessed with the timeslot determined by the TSADDR[4:0] bits.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the RPCC-SBI Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the RPCC-SBI Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the RPCC-SBI Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0069: RPCC-SBI Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the RPCC-SBI context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 3. CADDR[4:0] is the tributary index and ranges from 1 to 28.

Registers 0x006A-0x006E: RPCC-SBI Indirect Channel Data Registers

These registers contain data read from the RPCC-SBI channel context RAM after an indirect read operation or data to be inserted into the RPCC-SBI channel context RAM in an indirect write operation.

The bits to be written to the RPCC-SBI channel context RAM, in an indirect channel write operation, must be set up in these registers before triggering the write. All three registers from 0x006A through 0x006C inclusive must be written prior to each indirect write unless one desires the same configuration as the latest indirect write. The value returned by the latest indirect read has no bearing on indirect writes. Irregardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

The significance of the bits is dependent on the state of the TSACCESS bit of the RPCC-SBI Indirect Status/Time-slot Address register. If TSACCESS is logic 1, context information for the timeslot/channel identified by TSADDR[4:0] is either written or read.

TSACCESS=0:

Address	Offset							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default (‘b)**
0x006A	RPRBSLEN[2:0]			RPRBS UNF	MDTRK	MSTRK	PCCE	Unused	00000000
0x006B	T56K PRBS	TPRBS INV	TPRBSLEN[2:0]			TPRBS UNF	R56K PRBS	RPRBS INV	00000000
0x006C	PRBSERR[2:0]			PSYNCI	PSYNC	Reserved	PSYNCE	INV LAST	XXXXXX00
0x006D	PRBSERR[10:3]								XXXXXXXX
0x006E	Unused			PRBSERR[15:11]					XXXXXXXX

TSACCESS=1:

Address	Offset								
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default ('b)**
0x006A	SIGSRC [0]	INV[1:0]		ALAW	DMW	IDLC	ZCS[1:0]		00000000
0x006B	IDLE[2:0]			A'	B'	C'	D'	SIGSRC [1]	000000000
0x006C	Unused	TPRBS	RPRBS	IDLE[7:3]					XX000000
0x006D	Unused								XXXXXXXX
0x006E	Unused								XXXXXXXX

In the following bit descriptions, the system interface refers to the SBI Drop bus. Be aware that the PRBS receiver documented is down stream of the frame slip buffer; therefore, controlled slips will corrupt the bit sequence and result in bit errors and momentary loss of synchronization.

PCCE:

The per-tributary configuration enable bit, PCCE, enables the configuration data to affect the signaling and PCM byte streams. If the PCCE is logic 1, it enables the both the TSACCESS=0 and TSACCESS=1 Configuration bits. The global PCCE bit of the RPCC-SBI Configuration Bits register must also be logic 1 for this bit to have effect.

Upon setting this bit to logic 0, the PRBS shift registers and statuses are frozen.

The PCCE context bit must be logic 0 if the tributary is not being used. This is the case when the SPE is configured for other than T1/E1 or both the PROV bit programmed through the RTDM Tributary Control register and the ENBL bit programmed through the Byte Synchronous Mapping Tributary Control Indirect Access Data register are logic 0 in SONET/SDH mapping applications. In the case where T1s are mapped into TU12s, the PCCE must be logic 0 for link indices 22 through 28.

MSTRK:

Master Signaling Trunk Conditioning. When this bit is logic 1, signaling substitution at the system interface is performed on all channels/time slots for

a tributary. Setting MSTRK is equivalent to setting the SIGSRC[1:0] bits to binary 01 for all channels/timeslots.

MDTRK:

Master Data Trunk Conditioning. When this bit is logic 1, idle code substitution at the system interface is performed on all channels/time slots for a tributary. For E1, this includes overwriting TS0 with its IDLE[7:0] bits. For T1, the F-bit is not altered. Setting MDTRK is equivalent to setting the IDLC Per-Channel context bit to logic 1 for all channels/timeslots.

RPRBSUNF:

If this bit is logic 1, the PRBS is expected to fill all bits in the tributary data stream received from the SONET/SDH mapper or DS3 multiplexer. This bit supercedes the Per-Channel RPRBS context bits and the R56KPRBS context bits.

RPRBSLEN[2:0]:

The Receive PRBS Length field determines the sequence length of the expected bit pattern received from the SONET/SDH mapper or DS3 multiplexer:

RPRBSLEN	Sequence Length	Polynomial
000	$2^{11} - 1$	$x^{11} + x^9 + 1$
001	$2^{15} - 1$	$x^{15} + x^{14} + 1$
010	$2^{20} - 1$ (QRSS)	$x^{20} + x^{17} + 1$ with zero suppression
011	$2^{20} - 1$	$x^{20} + x^3 + 1$
100	$2^7 - 1$	$x^7 + x^3 + 1$ with XOR in the feedback path
101	$2^7 - 1$	$x^7 + x^3 + 1$ with XNOR in the feedback path

RPRBSINV:

If this bit is logic 1, the logical polarity of the received PRBS is inverted before comparison.

R56KPRBS:

If this bit is logic 1, the PRBS is expected to fill only the first seven bits of the selected channels/time slots. Otherwise, the PRBS is expected to occupy the entire selected channels/time slots.

TPRBSUNF:

If this bit is logic 1, the PRBS fills all bits of the tributary at the system interface (SBI Drop bus). This bit supercedes the Per-Channel TPRBS context bits and the T56KPRBS context bits.

TPRBSLEN[2:0]:

The Transit PRBS Length field determines the sequence length of the generated bit pattern destined to the SBI Drop bus:

TPRBSLEN	Sequence Length	Polynomial
000	$2^{11} - 1$	$x^{11} + x^9 + 1$
001	$2^{15} - 1$	$x^{15} + x^{14} + 1$
010	$2^{20} - 1$ (QRSS)	$x^{20} + x^{17} + 1$ with zero suppression
011	$2^{20} - 1$	$x^{20} + x^3 + 1$
100	$2^7 - 1$	$x^7 + x^3 + 1$ with XOR in the feedback path
101	$2^7 - 1$	$x^7 + x^3 + 1$ with XNOR in the feedback path

TPRBSINV:

If this bit is logic 1, the logical polarity of the generated PRBS is inverted before transmission.

T56KPRBS

If this bit is logic 1, the generated PRBS fills only the first seven bits of the selected channels/time slots. Otherwise, the PRBS occupies the entire selected channels/time slots.

INVLAST:

If this bit is logic 1, inversion (as controlled by the INV[1:0] Per-Channel context bits) is the last per-channel operation performed on the data. Otherwise, inversion is the first operation performed.

PSYNCE:

If this bit is a logic 1, the associated RPCCI[x] bit is set upon a change in the PSYNC context bit.

PSYNC:

PSYNC is the PRBS synchronization status. PSYNC becomes a logic 1 if the received data matched the expected sequence for the latest four bytes. PSYNC is set to logic 0 only if 3 consecutive bytes are in error.

PSYNCI:

PSYNCI becomes a logic 1 upon a change in the PSYNC context bit. It is cleared upon an indirect read access.

PRBSERR[15:0]:

The PRBS Error holding register contains a count of the discrepancies between the expected PRBS sequence and the receive data that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_PRBS bit to logic 1. The count saturates at all ones.

ZCS[1:0]:

These bits control the Zero Code Suppression on the SBI Drop bus as follows:

T1:

ZCS[1:0]	Description
00	No Zero Code Suppression
01	GTE Zero Code Suppression. The least significant bit (bit 8) of an all zeros channel is forced to a one, except for signaling frames where the second least significant bit is forced to a one.
10	DDS Zero Code Suppression. All zero channel data is replaced with the patte“n "10011”00"
11	Bell Zero Code Suppression. The second least significant bit (bit 7) of an all zeros channel is forced to a one.

E1:

ZCS[1:0]	Description
00	No Zero Code Suppression
01	Jammed bit-8. The least significant bit (bit 8) of an all zeros channel is forced to a one.
10	No Zero Code Suppression
11	Jammed bit-8.

Zero code suppression occurs after data inversion, idle code insertion, digital milliwatt insertion and signaling have occurred.

IDLC:

If this bit is logic 1, the channel/time slot data at the system interface is replaced by the value in the IDLE[7:0] field.

DMW:

If this bit is logic 1, the channel/time slot data at the system interface is replaced by the Digital Milliwatt signal. The encoding of the 1 kHz sine wave is determined by the ALAW context bit.

ALAW:

This bit determines the encoding of the Digital Milliwatt signal. If ALAW is logic 0, μ-law companding is respected. If ALAW is logic 1, A-law companding is respected.

INV[1:0]:

These bits invert the channel/time slot data:

INV[1:0]	T1 Description	E1 Description
00	No inversion (default)	No inversion (default)
01	Only the MSB of the received PCM channel data is inverted (Sign bit inversion)	Invert even bits
10	All bits EXCEPT the MSB of the received PCM channel data is inverted (Magnitude inversion)	Invert odd bits
11	Invert all bits	Invert all bits

SIGSRC[1:0]:

These bits determine the source of signaling presented at the SBI Drop system interface.

SIGSRC[1:0]	Description
00	Extracted signaling is only presented in the “SSSS” bits of the SBI Drop bus.
01	Signaling taken from A' B' C' and D' context bits. May be presented in the robbed bits if the RX_SBI_SIGINS bit of the T1/E1 Master Configuration register is logic 1.
10	Extracted signaling presented in the “SSSS” bits of the SBI Drop bus plus the robbed bits if the RX_SBI_SIGINS bit of the T1/E1 Master Configuration register is logic 1.
11	Reserved.

Reserved:

This bit must be logic 0 for correct operation.

A’,B’,C’,D’:

These signaling bits are inserted at the system interface when the MSTRK bit is logic 1 or if the SIGSRC[1:0] bits are 01. For the T1 SF frame format, C’ and D’ must equal A’ and B’, respectively.

IDLE[7:0]:

This field contains the value inserted at the system inteface if the MDTRK or IDLC bit is logic 1.

RPRBS:

If this bit is logic 1, a PRBS is expected in the channel/time slot received from the SONET/SDH mapper or DS3 multiplexer.

TPRBS:

If this bit is logic 1, a PRBS is generated in the channel/time slot destined to the SBI Drop bus..

Register 0x006F: RPCC-SBI Configuration Bits

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	INTE	0
Bit 3	R/W	Reserved	0
Bit 2	W12C	XFERI	X
Bit 1	R/W	XFERE	0
Bit 0	R/W	PCCE	0

INTE:

If this bit is a logic 1, the RPRBS bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the RPCCI[84:1] bits is a logic 1.

Reserved:

This bit must be logic 0 for correct operation.

XFERI:

The XFERI bit indicates that a transfer of accumulated PRBS error data has occurred. A logic 1 in this bit position indicates that the holding registers have been updated. This update is initiated by a write to the Global Performance Monitor Update register that sets the E1T1_PRBS bit to logic 1.

Logic 1 must be written to this bit to clear it to logic 0.

XFERE:

If this bit is a logic 1, the RPRBS bit of the Master Interrupt Source T1E1 register is logic 1 if the XFERI bit is a logic 1.

PCCE:

This global bit enables RPCC-SBI per-channel/per-timeslot functions if logic 1. The per-tributary PCCE bits set through the RPCC-SBI Indirect Channel Data Registers must also be set to enable individual tributaries.

Upon setting this bit to logic 0, the PRBS shift registers and statuses are frozen.

Register 0x0070: RPCC-SBI Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R	REG9_AI	X
Bit 6	R	REG7_8I	X
Bit 5	R	REG4_5_6I	X
Bit 4	R	REG1_2_3I	X
Bit 3	W12C	RPCCI[4]	X
Bit 2	W12C	RPCCI[3]	X
Bit 1	W12C	RPCCI[2]	X
Bit 0	W12C	RPCCI[1]	X

RPCCI[84:1]:

A logic 1 in these bits indicate a change of PRBS synchronization state on the associated tributary since this register was last read. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG1_2_3I:

This bit is a logic 1 if at least one bit in Register 0x0071, 0x0072 or 0x0073 is logic 1.

REG4_5_6I:

This bit is a logic 1 if at least one bit in Register 0x0074, 0x0075 or 0x0076 is logic 1.

REG7_8I:

This bit is a logic 1 if at least one bit in Register 0x0077 or 0x0078 is logic 1.

REG9_AI:

This bit is a logic 1 if at least one bit in Register 0x0079 or 0x007A is logic 1.

Register 0x0071: RPCC-SBI Interrupt Status #2

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[12]	X
Bit 6	W12C	RPCCI[11]	X
Bit 5	W12C	RPCCI[10]	X
Bit 4	W12C	RPCCI[9]	X
Bit 3	W12C	RPCCI[8]	X
Bit 2	W12C	RPCCI[7]	X
Bit 1	W12C	RPCCI[6]	X
Bit 0	W12C	RPCCI[5]	X

Register 0x0072: RPCC-SBI Interrupt Status #3

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[20]	X
Bit 6	W12C	RPCCI[19]	X
Bit 5	W12C	RPCCI[18]	X
Bit 4	W12C	RPCCI[17]	X
Bit 3	W12C	RPCCI[16]	X
Bit 2	W12C	RPCCI[15]	X
Bit 1	W12C	RPCCI[14]	X
Bit 0	W12C	RPCCI[13]	X

Register 0x0073: RPCC-SBI Interrupt Status #4

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[28]	X
Bit 6	W12C	RPCCI[27]	X
Bit 5	W12C	RPCCI[26]	X
Bit 4	W12C	RPCCI[25]	X
Bit 3	W12C	RPCCI[24]	X
Bit 2	W12C	RPCCI[23]	X
Bit 1	W12C	RPCCI[22]	X
Bit 0	W12C	RPCCI[21]	X

Register 0x0074: RPCC-SBI Interrupt Status #5

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[36]	X
Bit 6	W12C	RPCCI[35]	X
Bit 5	W12C	RPCCI[34]	X
Bit 4	W12C	RPCCI[33]	X
Bit 3	W12C	RPCCI[32]	X
Bit 2	W12C	RPCCI[31]	X
Bit 1	W12C	RPCCI[30]	X
Bit 0	W12C	RPCCI[29]	X

Register 0x0075: RPCC-SBI Interrupt Status #6

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[44]	X
Bit 6	W12C	RPCCI[43]	X
Bit 5	W12C	RPCCI[42]	X
Bit 4	W12C	RPCCI[41]	X
Bit 3	W12C	RPCCI[40]	X
Bit 2	W12C	RPCCI[39]	X
Bit 1	W12C	RPCCI[38]	X
Bit 0	W12C	RPCCI[37]	X

Register 0x0076: RPCC-SBI Interrupt Status #7

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[52]	X
Bit 6	W12C	RPCCI[51]	X
Bit 5	W12C	RPCCI[50]	X
Bit 4	W12C	RPCCI[49]	X
Bit 3	W12C	RPCCI[48]	X
Bit 2	W12C	RPCCI[47]	X
Bit 1	W12C	RPCCI[46]	X
Bit 0	W12C	RPCCI[45]	X

Register 0x0077: RPCC-SBI Interrupt Status #8

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[60]	X
Bit 6	W12C	RPCCI[59]	X
Bit 5	W12C	RPCCI[58]	X
Bit 4	W12C	RPCCI[57]	X
Bit 3	W12C	RPCCI[56]	X
Bit 2	W12C	RPCCI[55]	X
Bit 1	W12C	RPCCI[54]	X
Bit 0	W12C	RPCCI[53]	X

Register 0x0078: RPCC-SBI Interrupt Status #9

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[68]	X
Bit 6	W12C	RPCCI[67]	X
Bit 5	W12C	RPCCI[66]	X
Bit 4	W12C	RPCCI[65]	X
Bit 3	W12C	RPCCI[64]	X
Bit 2	W12C	RPCCI[63]	X
Bit 1	W12C	RPCCI[62]	X
Bit 0	W12C	RPCCI[61]	X

Register 0x0079: RPCC-SBI Interrupt Status #10

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[76]	X
Bit 6	W12C	RPCCI[75]	X
Bit 5	W12C	RPCCI[74]	X
Bit 4	W12C	RPCCI[73]	X
Bit 3	W12C	RPCCI[72]	X
Bit 2	W12C	RPCCI[71]	X
Bit 1	W12C	RPCCI[70]	X
Bit 0	W12C	RPCCI[69]	X

Register 0x007A: RPCC-SBI Interrupt Status #11

Bit	Type	Function	Default
Bit 7	W12C	RPCCI[84]	X
Bit 6	W12C	RPCCI[83]	X
Bit 5	W12C	RPCCI[82]	X
Bit 4	W12C	RPCCI[81]	X
Bit 3	W12C	RPCCI[80]	X
Bit 2	W12C	RPCCI[79]	X
Bit 1	W12C	RPCCI[78]	X
Bit 0	W12C	RPCCI[77]	X

Register 0x007B: RPCC-SBI PRBS Error Insertion

Bit	Type	Function	Default
Bit 7	RW	TPRBS_ERR_INSERT	X
Bit 6	RW	TPRBS_ADDR[6]	X
Bit 5	RW	TPRBS_ADDR[5]	X
Bit 4	RW	TPRBS_ADDR[4]	X
Bit 3	RW	TPRBS_ADDR[3]	X
Bit 2	RW	TPRBS_ADDR[2]	X
Bit 1	RW	TPRBS_ADDR[1]	X
Bit 0	RW	TPRBS_ADDR[0]	X

TPRBS_ERR_INSERT:

The TPRBS Error insertion Enable bit causes a single bit error to be inserted in the PRBS pattern for the tributary addressed by TPRBS_ADDR[6:0]. A zero to one transition triggers the error insertion.

TPRBS_ADDR[6:0]:

Indicates the tributary into which a single bit error is to be inserted. TPRBS_ADDR[6:5] is the SPE index and ranges from 1 to 3. TPRBS_ADDR[4:0] is the tributary index and ranges from 1 to 28.

Register 0x007C: RPCC-SBI PRBS Error Insert Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	W12C	TPRBS_ERR_INSERTED	X

TPRBS_ERR_INSERTED:

TPRBS_ERR_INSERTED indicates an error has been inserted. This bit is cleared to logic 0 upon a writing a logic 1 to the bit position.

1.8 T1/E1 Receive H-MVIP Elastic Store (RX-MVIP-ELST) Registers

Register 0x0083: RX-MVIP-ELST Idle Code

Bit	Type	Function	Default
Bit 7	R/W	IDLECODE[7]	1
Bit 6	R/W	IDLECODE[6]	1
Bit 5	R/W	IDLECODE[5]	1
Bit 4	R/W	IDLECODE[4]	1
Bit 3	R/W	IDLECODE[3]	1
Bit 2	R/W	IDLECODE[2]	1
Bit 1	R/W	IDLECODE[1]	1
Bit 0	R/W	IDLECODE[0]	1

IDLECODE[7:0]:

The contents of this register are inserted into each DS0 of tributaries that are out of basic frame alignment (i.e. T1/E1 FRMR INF context bit is logic 0) and the TRKEN T1/E1 FRMR context bit is logic 1.

Register 0x0084: RX-MVIP-ELST Slip Status #1

Bit	Type	Function	Default
Bit 7	R	REGD_EI	X
Bit 6	R	REGB_CI	X
Bit 5	R	REG8_9_AI	X
Bit 4	R	REG5_6_7I	X
Bit 3	W12C	SLPI[4]	X
Bit 2	W12C	SLPI[3]	X
Bit 1	W12C	SLPI[2]	X
Bit 0	W12C	SLPI[1]	X

SLPI[84:1]:

A logic 1 in these bits indicate a slip has occurred on the associated tributary since the bit was explicitly cleared. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG5_6_7I:

This bit is a logic 1 if at least one bit in Register 0x00A5, 0x00A6 or 0x00A7 is logic 1.

REG8_9_AI:

This bit is a logic 1 if at least one bit in Register 0x00A8, 0x00A9 or 0x00AA is logic 1.

REGB_CI:

This bit is a logic 1 if at least one bit in Register 0x00AB or 0x00AC is logic 1.

REGD_EI:

This bit is a logic 1 if at least one bit in Register 0x00AD or 0x00AE is logic 1.

Register 0x0085: RX-MVIP-ELST Slip Status #2

Bit	Type	Function	Default
Bit 7	W12C	SLPI[12]	X
Bit 6	W12C	SLPI[11]	X
Bit 5	W12C	SLPI[10]	X
Bit 4	W12C	SLPI[9]	X
Bit 3	W12C	SLPI[8]	X
Bit 2	W12C	SLPI[7]	X
Bit 1	W12C	SLPI[6]	X
Bit 0	W12C	SLPI[5]	X

Register 0x0086: RX-MVIP-ELST Slip Status #3

Bit	Type	Function	Default
Bit 7	W12C	SLPI[20]	X
Bit 6	W12C	SLPI[19]	X
Bit 5	W12C	SLPI[18]	X
Bit 4	W12C	SLPI[17]	X
Bit 3	W12C	SLPI[16]	X
Bit 2	W12C	SLPI[15]	X
Bit 1	W12C	SLPI[14]	X
Bit 0	W12C	SLPI[13]	X

Register 0x0087: RX-MVIP-ELST Slip Status #4

Bit	Type	Function	Default
Bit 7	W12C	SLPI[28]	X
Bit 6	W12C	SLPI[27]	X
Bit 5	W12C	SLPI[26]	X
Bit 4	W12C	SLPI[25]	X
Bit 3	W12C	SLPI[24]	X
Bit 2	W12C	SLPI[23]	X
Bit 1	W12C	SLPI[22]	X
Bit 0	W12C	SLPI[21]	X

Register 0x0088: RX-MVIP-ELST Slip Status #5

Bit	Type	Function	Default
Bit 7	W12C	SLPI[36]	X
Bit 6	W12C	SLPI[35]	X
Bit 5	W12C	SLPI[34]	X
Bit 4	W12C	SLPI[33]	X
Bit 3	W12C	SLPI[32]	X
Bit 2	W12C	SLPI[31]	X
Bit 1	W12C	SLPI[30]	X
Bit 0	W12C	SLPI[29]	X

Register 0x0089: RX-MVIP-ELST Slip Status #6

Bit	Type	Function	Default
Bit 7	W12C	SLPI[44]	X
Bit 6	W12C	SLPI[43]	X
Bit 5	W12C	SLPI[42]	X
Bit 4	W12C	SLPI[41]	X
Bit 3	W12C	SLPI[40]	X
Bit 2	W12C	SLPI[39]	X
Bit 1	W12C	SLPI[38]	X
Bit 0	W12C	SLPI[37]	X

Register 0x008A: RX-MVIP-ELST Slip Status #7

Bit	Type	Function	Default
Bit 7	W12C	SLPI[52]	X
Bit 6	W12C	SLPI[51]	X
Bit 5	W12C	SLPI[50]	X
Bit 4	W12C	SLPI[49]	X
Bit 3	W12C	SLPI[48]	X
Bit 2	W12C	SLPI[47]	X
Bit 1	W12C	SLPI[46]	X
Bit 0	W12C	SLPI[45]	X

Register 0x008B: RX-MVIP-ELST Slip Status #8

Bit	Type	Function	Default
Bit 7	W12C	SLPI[60]	X
Bit 6	W12C	SLPI[59]	X
Bit 5	W12C	SLPI[58]	X
Bit 4	W12C	SLPI[57]	X
Bit 3	W12C	SLPI[56]	X
Bit 2	W12C	SLPI[55]	X
Bit 1	W12C	SLPI[54]	X
Bit 0	W12C	SLPI[53]	X

Register 0x008C: RX-MVIP-ELST Slip Status #9

Bit	Type	Function	Default
Bit 7	W12C	SLPI[68]	X
Bit 6	W12C	SLPI[67]	X
Bit 5	W12C	SLPI[66]	X
Bit 4	W12C	SLPI[65]	X
Bit 3	W12C	SLPI[64]	X
Bit 2	W12C	SLPI[63]	X
Bit 1	W12C	SLPI[62]	X
Bit 0	W12C	SLPI[61]	X

Register 0x008D: RX-MVIP-ELST Slip Status #10

Bit	Type	Function	Default
Bit 7	W12C	SLPI[76]	X
Bit 6	W12C	SLPI[75]	X
Bit 5	W12C	SLPI[74]	X
Bit 4	W12C	SLPI[73]	X
Bit 3	W12C	SLPI[72]	X
Bit 2	W12C	SLPI[71]	X
Bit 1	W12C	SLPI[70]	X
Bit 0	W12C	SLPI[69]	X

Register 0x008E: RX-MVIP-ELST Slip Status #11

Bit	Type	Function	Default
Bit 7	W12C	SLPI[84]	X
Bit 6	W12C	SLPI[83]	X
Bit 5	W12C	SLPI[82]	X
Bit 4	W12C	SLPI[81]	X
Bit 3	W12C	SLPI[80]	X
Bit 2	W12C	SLPI[79]	X
Bit 1	W12C	SLPI[78]	X
Bit 0	W12C	SLPI[77]	X

Register 0x008F: RX-MVIP-ELST Slip Direction #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	SLPD[4]	X
Bit 2	R	SLPD[3]	X
Bit 1	R	SLPD[2]	X
Bit 0	R	SLPD[1]	X

SLPD[84:1]:

A logic 1 in these bits indicate the direction of latest slip on the associated tributary. If SLPD[x] is a logic 0, the slip resulted in the repetition of a frame. If SLPD[x] is a logic 1, a frame was lost. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Register 0x0090: RX-MVIP-ELST Slip Direction #2

Bit	Type	Function	Default
Bit 7	R	SLPD[12]	X
Bit 6	R	SLPD[11]	X
Bit 5	R	SLPD[10]	X
Bit 4	R	SLPD[9]	X
Bit 3	R	SLPD[8]	X
Bit 2	R	SLPD[7]	X
Bit 1	R	SLPD[6]	X
Bit 0	R	SLPD[5]	X

Register 0x0091: RX-MVIP-ELST Slip Direction #3

Bit	Type	Function	Default
Bit 7	R	SLPD[20]	X
Bit 6	R	SLPD[19]	X
Bit 5	R	SLPD[18]	X
Bit 4	R	SLPD[17]	X
Bit 3	R	SLPD[16]	X
Bit 2	R	SLPD[15]	X
Bit 1	R	SLPD[14]	X
Bit 0	R	SLPD[13]	X

Register 0x0092: RX-MVIP-ELST Slip Direction #4

Bit	Type	Function	Default
Bit 7	R	SLPD[28]	X
Bit 6	R	SLPD[27]	X
Bit 5	R	SLPD[26]	X
Bit 4	R	SLPD[25]	X
Bit 3	R	SLPD[24]	X
Bit 2	R	SLPD[23]	X
Bit 1	R	SLPD[22]	X
Bit 0	R	SLPD[21]	X

Register 0x0093: RX-MVIP-ELST Slip Direction #5

Bit	Type	Function	Default
Bit 7	R	SLPD[36]	X
Bit 6	R	SLPD[35]	X
Bit 5	R	SLPD[34]	X
Bit 4	R	SLPD[33]	X
Bit 3	R	SLPD[32]	X
Bit 2	R	SLPD[31]	X
Bit 1	R	SLPD[30]	X
Bit 0	R	SLPD[29]	X

Register 0x0094: RX-MVIP-ELST Slip Direction #6

Bit	Type	Function	Default
Bit 7	R	SLPD[44]	X
Bit 6	R	SLPD[43]	X
Bit 5	R	SLPD[42]	X
Bit 4	R	SLPD[41]	X
Bit 3	R	SLPD[40]	X
Bit 2	R	SLPD[39]	X
Bit 1	R	SLPD[38]	X
Bit 0	R	SLPD[37]	X

Register 0x0095: RX-MVIP-ELST Slip Direction #7

Bit	Type	Function	Default
Bit 7	R	SLPD[52]	X
Bit 6	R	SLPD[51]	X
Bit 5	R	SLPD[50]	X
Bit 4	R	SLPD[49]	X
Bit 3	R	SLPD[48]	X
Bit 2	R	SLPD[47]	X
Bit 1	R	SLPD[46]	X
Bit 0	R	SLPD[45]	X

Register 0x0096: RX-MVIP-ELST Slip Direction #8

Bit	Type	Function	Default
Bit 7	R	SLPD[60]	X
Bit 6	R	SLPD[59]	X
Bit 5	R	SLPD[58]	X
Bit 4	R	SLPD[57]	X
Bit 3	R	SLPD[56]	X
Bit 2	R	SLPD[55]	X
Bit 1	R	SLPD[54]	X
Bit 0	R	SLPD[53]	X

Register 0x0097: RX-MVIP-ELST Slip Direction #9

Bit	Type	Function	Default
Bit 7	R	SLPD[68]	X
Bit 6	R	SLPD[67]	X
Bit 5	R	SLPD[66]	X
Bit 4	R	SLPD[65]	X
Bit 3	R	SLPD[64]	X
Bit 2	R	SLPD[63]	X
Bit 1	R	SLPD[62]	X
Bit 0	R	SLPD[61]	X

Register 0x0098: RX-MVIP-ELST Slip Direction #10

Bit	Type	Function	Default
Bit 7	R	SLPD[76]	X
Bit 6	R	SLPD[75]	X
Bit 5	R	SLPD[74]	X
Bit 4	R	SLPD[73]	X
Bit 3	R	SLPD[72]	X
Bit 2	R	SLPD[71]	X
Bit 1	R	SLPD[70]	X
Bit 0	R	SLPD[69]	X

Register 0x0099: RX-MVIP-ELST Slip Direction #11

Bit	Type	Function	Default
Bit 7	R	SLPD[84]	X
Bit 6	R	SLPD[83]	X
Bit 5	R	SLPD[82]	X
Bit 4	R	SLPD[81]	X
Bit 3	R	SLPD[80]	X
Bit 2	R	SLPD[79]	X
Bit 1	R	SLPD[78]	X
Bit 0	R	SLPD[77]	X

Register 0x009A: RX-MVIP-ELST Slip Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	SLPE	0

SLPE:

If this bit is a logic 1, the RXELST bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the SLPI[84:1] bits is a logic 1. This bit should be set to 0 if any link has its ELSTBYP bit set. When bypassed, the elastic store will constantly roll over and cause excessive interrupts

1.9 T1/E1 Receive SBI Elastic Store (RX-SBI-ELST) Registers

Register 0x00A0: RX-SBI-ELST Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Writing to this register triggers an indirect channel register access to the receive SBI elastic store (RX-SBI-ELST) context RAM.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the RX-SBI-ELST Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the RX-SBI-ELST Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the RX-SBI-ELST Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x00A1: RX-SBI-ELST Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the RX-SBI-ELST channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 3. CADDR[4:0] is the tributary index and ranges from 1 to 28.

Register 0x00A2: RX-SBI-ELST Indirect Channel Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	SYNCSBI	0
Bit 0	R/W	ELSTBYP	0

This register contains data read from the channel context RAM after an indirect read operation or data to be inserted into the channel context RAM in an indirect write operation.

The bits to be written to the channel context RAM, in an indirect channel write operation, must be set up in this register before triggering the write. Irregardless of writes to this register, reads will always return the data retrieved by the latest indirect read operation.

SYNCSBI:

The Synchronous SBI bit enables the T1/E1 framer to reference the output timing of its elastic store to the SBI bus clock, SREFCLK. When SYNCSBI is a logic 1 the framed T1 or E1 stream is synchronized to the SBI bus so that it can be inserted into the SBI bus with all DS0s or timeslots in fixed locations. The SYNCH_TRIB bit in the INSBI Tributary Control Indirect Access Data register must be set to logic 1 and the SBI bus must be selected in the SYSOPT[1:0] bits of the Global Configuration register for synchronous SBI operation. When SYNCSBI is a logic 0 then the timing of the elastic store is not referenced to the SBI bus. SYNCSBI should be set to a logic 0 for all modes of operation except for the Synchronous SBI operation as outlined above.

If SYNCSBI is logic 1, ELSTBYP must be logic 0.

ELSTBYP:

If the ELST Bypass bit is logic 1, the receive frame slip buffer is bypassed, thus eliminating a nominal one frame latency. The bypass may only be enabled when the SBI bus interface is enabled and the payload allowed to float, i.e. the SYSOPT[1:0] bits of the Global Configuration register are binary 10 and the per-tributary SYNCH_TRIB bit of the INSBI Tributary Control Indirect Access Data register is logic 0.

Register 0x00A3: RX-SBI-ELST Idle Code

Bit	Type	Function	Default
Bit 7	R/W	IDLECODE[7]	1
Bit 6	R/W	IDLECODE[6]	1
Bit 5	R/W	IDLECODE[5]	1
Bit 4	R/W	IDLECODE[4]	1
Bit 3	R/W	IDLECODE[3]	1
Bit 2	R/W	IDLECODE[2]	1
Bit 1	R/W	IDLECODE[1]	1
Bit 0	R/W	IDLECODE[0]	1

IDLECODE[7:0]:

The contents of this register are inserted into each DS0 of tributaries that are out of basic frame alignment (i.e. T1/E1 FRMR INF context bit is logic 0) and the TRKEN T1/E1 FRMR context bit is logic 1.

Register 0x00A4: RX-SBI-ELST Slip Status #1

Bit	Type	Function	Default
Bit 7	R	REGD_EI	X
Bit 6	R	REGB_CI	X
Bit 5	R	REG8_9_AI	X
Bit 4	R	REG5_6_7I	X
Bit 3	W12C	SLPI[4]	X
Bit 2	W12C	SLPI[3]	X
Bit 1	W12C	SLPI[2]	X
Bit 0	W12C	SLPI[1]	X

SLPI[84:1]:

A logic 1 in these bits indicate a slip has occurred on the associated tributary since the bit was explicitly cleared. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG5_6_7I:

This bit is a logic 1 if at least one bit in Register 0x00A5, 0x00A6 or 0x00A7 is logic 1.

REG8_9_AI:

This bit is a logic 1 if at least one bit in Register 0x00A8, 0x00A9 or 0x00AA is logic 1.

REGB_CI:

This bit is a logic 1 if at least one bit in Register 0x00AB or 0x00AC is logic 1.

REGD_EI:

This bit is a logic 1 if at least one bit in Register 0x00AD or 0x00AE is logic 1.

Register 0x00A5: RX-SBI-ELST Slip Status #2

Bit	Type	Function	Default
Bit 7	W12C	SLPI[12]	X
Bit 6	W12C	SLPI[11]	X
Bit 5	W12C	SLPI[10]	X
Bit 4	W12C	SLPI[9]	X
Bit 3	W12C	SLPI[8]	X
Bit 2	W12C	SLPI[7]	X
Bit 1	W12C	SLPI[6]	X
Bit 0	W12C	SLPI[5]	X

Register 0x00A6: RX-SBI-ELST Slip Status #3

Bit	Type	Function	Default
Bit 7	W12C	SLPI[20]	X
Bit 6	W12C	SLPI[19]	X
Bit 5	W12C	SLPI[18]	X
Bit 4	W12C	SLPI[17]	X
Bit 3	W12C	SLPI[16]	X
Bit 2	W12C	SLPI[15]	X
Bit 1	W12C	SLPI[14]	X
Bit 0	W12C	SLPI[13]	X

Register 0x00A7: RX-SBI-ELST Slip Status #4

Bit	Type	Function	Default
Bit 7	W12C	SLPI[28]	X
Bit 6	W12C	SLPI[27]	X
Bit 5	W12C	SLPI[26]	X
Bit 4	W12C	SLPI[25]	X
Bit 3	W12C	SLPI[24]	X
Bit 2	W12C	SLPI[23]	X
Bit 1	W12C	SLPI[22]	X
Bit 0	W12C	SLPI[21]	X

Register 0x00A8: RX-SBI-ELST Slip Status #5

Bit	Type	Function	Default
Bit 7	W12C	SLPI[36]	X
Bit 6	W12C	SLPI[35]	X
Bit 5	W12C	SLPI[34]	X
Bit 4	W12C	SLPI[33]	X
Bit 3	W12C	SLPI[32]	X
Bit 2	W12C	SLPI[31]	X
Bit 1	W12C	SLPI[30]	X
Bit 0	W12C	SLPI[29]	X

Register 0x00A9: RX-SBI-ELST Slip Status #6

Bit	Type	Function	Default
Bit 7	W12C	SLPI[44]	X
Bit 6	W12C	SLPI[43]	X
Bit 5	W12C	SLPI[42]	X
Bit 4	W12C	SLPI[41]	X
Bit 3	W12C	SLPI[40]	X
Bit 2	W12C	SLPI[39]	X
Bit 1	W12C	SLPI[38]	X
Bit 0	W12C	SLPI[37]	X

Register 0x00AA: RX-SBI-ELST Slip Status #7

Bit	Type	Function	Default
Bit 7	W12C	SLPI[52]	X
Bit 6	W12C	SLPI[51]	X
Bit 5	W12C	SLPI[50]	X
Bit 4	W12C	SLPI[49]	X
Bit 3	W12C	SLPI[48]	X
Bit 2	W12C	SLPI[47]	X
Bit 1	W12C	SLPI[46]	X
Bit 0	W12C	SLPI[45]	X

Register 0x00AB: RX-SBI-ELST Slip Status #8

Bit	Type	Function	Default
Bit 7	W12C	SLPI[60]	X
Bit 6	W12C	SLPI[59]	X
Bit 5	W12C	SLPI[58]	X
Bit 4	W12C	SLPI[57]	X
Bit 3	W12C	SLPI[56]	X
Bit 2	W12C	SLPI[55]	X
Bit 1	W12C	SLPI[54]	X
Bit 0	W12C	SLPI[53]	X

Register 0x00AC: RX-SBI-ELST Slip Status #9

Bit	Type	Function	Default
Bit 7	W12C	SLPI[68]	X
Bit 6	W12C	SLPI[67]	X
Bit 5	W12C	SLPI[66]	X
Bit 4	W12C	SLPI[65]	X
Bit 3	W12C	SLPI[64]	X
Bit 2	W12C	SLPI[63]	X
Bit 1	W12C	SLPI[62]	X
Bit 0	W12C	SLPI[61]	X

Register 0x00AD: RX-SBI-ELST Slip Status #10

Bit	Type	Function	Default
Bit 7	W12C	SLPI[76]	X
Bit 6	W12C	SLPI[75]	X
Bit 5	W12C	SLPI[74]	X
Bit 4	W12C	SLPI[73]	X
Bit 3	W12C	SLPI[72]	X
Bit 2	W12C	SLPI[71]	X
Bit 1	W12C	SLPI[70]	X
Bit 0	W12C	SLPI[69]	X

Register 0x00AE: RX-SBI-ELST Slip Status #11

Bit	Type	Function	Default
Bit 7	W12C	SLPI[84]	X
Bit 6	W12C	SLPI[83]	X
Bit 5	W12C	SLPI[82]	X
Bit 4	W12C	SLPI[81]	X
Bit 3	W12C	SLPI[80]	X
Bit 2	W12C	SLPI[79]	X
Bit 1	W12C	SLPI[78]	X
Bit 0	W12C	SLPI[77]	X

Register 0x00AF: RX-SBI-ELST Slip Direction #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	SLPD[4]	X
Bit 2	R	SLPD[3]	X
Bit 1	R	SLPD[2]	X
Bit 0	R	SLPD[1]	X

SLPD[84:1]:

A logic 1 in these bits indicate the direction of latest slip on the associated tributary. If SLPD[x] is a logic 0, the slip resulted in the repetition of a frame. If SLPD[x] is a logic 1, a frame was lost. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Register 0x00B0: RX-SBI-ELST Slip Direction #2

Bit	Type	Function	Default
Bit 7	R	SLPD[12]	X
Bit 6	R	SLPD[11]	X
Bit 5	R	SLPD[10]	X
Bit 4	R	SLPD[9]	X
Bit 3	R	SLPD[8]	X
Bit 2	R	SLPD[7]	X
Bit 1	R	SLPD[6]	X
Bit 0	R	SLPD[5]	X

Register 0x00B1: RX-SBI-ELST Slip Direction #3

Bit	Type	Function	Default
Bit 7	R	SLPD[20]	X
Bit 6	R	SLPD[19]	X
Bit 5	R	SLPD[18]	X
Bit 4	R	SLPD[17]	X
Bit 3	R	SLPD[16]	X
Bit 2	R	SLPD[15]	X
Bit 1	R	SLPD[14]	X
Bit 0	R	SLPD[13]	X

Register 0x00B2: RX-SBI-ELST Slip Direction #4

Bit	Type	Function	Default
Bit 7	R	SLPD[28]	X
Bit 6	R	SLPD[27]	X
Bit 5	R	SLPD[26]	X
Bit 4	R	SLPD[25]	X
Bit 3	R	SLPD[24]	X
Bit 2	R	SLPD[23]	X
Bit 1	R	SLPD[22]	X
Bit 0	R	SLPD[21]	X

Register 0x00B3: RX-SBI-ELST Slip Direction #5

Bit	Type	Function	Default
Bit 7	R	SLPD[36]	X
Bit 6	R	SLPD[35]	X
Bit 5	R	SLPD[34]	X
Bit 4	R	SLPD[33]	X
Bit 3	R	SLPD[32]	X
Bit 2	R	SLPD[31]	X
Bit 1	R	SLPD[30]	X
Bit 0	R	SLPD[29]	X

Register 0x00B4: RX-SBI-ELST Slip Direction #6

Bit	Type	Function	Default
Bit 7	R	SLPD[44]	X
Bit 6	R	SLPD[43]	X
Bit 5	R	SLPD[42]	X
Bit 4	R	SLPD[41]	X
Bit 3	R	SLPD[40]	X
Bit 2	R	SLPD[39]	X
Bit 1	R	SLPD[38]	X
Bit 0	R	SLPD[37]	X

Register 0x00B5: RX-SBI-ELST Slip Direction #7

Bit	Type	Function	Default
Bit 7	R	SLPD[52]	X
Bit 6	R	SLPD[51]	X
Bit 5	R	SLPD[50]	X
Bit 4	R	SLPD[49]	X
Bit 3	R	SLPD[48]	X
Bit 2	R	SLPD[47]	X
Bit 1	R	SLPD[46]	X
Bit 0	R	SLPD[45]	X

Register 0x00B6: RX-SBI-ELST Slip Direction #8

Bit	Type	Function	Default
Bit 7	R	SLPD[60]	X
Bit 6	R	SLPD[59]	X
Bit 5	R	SLPD[58]	X
Bit 4	R	SLPD[57]	X
Bit 3	R	SLPD[56]	X
Bit 2	R	SLPD[55]	X
Bit 1	R	SLPD[54]	X
Bit 0	R	SLPD[53]	X

Register 0x00B7: RX-SBI-ELST Slip Direction #9

Bit	Type	Function	Default
Bit 7	R	SLPD[68]	X
Bit 6	R	SLPD[67]	X
Bit 5	R	SLPD[66]	X
Bit 4	R	SLPD[65]	X
Bit 3	R	SLPD[64]	X
Bit 2	R	SLPD[63]	X
Bit 1	R	SLPD[62]	X
Bit 0	R	SLPD[61]	X

Register 0x00B8: RX-SBI-ELST Slip Direction #10

Bit	Type	Function	Default
Bit 7	R	SLPD[76]	X
Bit 6	R	SLPD[75]	X
Bit 5	R	SLPD[74]	X
Bit 4	R	SLPD[73]	X
Bit 3	R	SLPD[72]	X
Bit 2	R	SLPD[71]	X
Bit 1	R	SLPD[70]	X
Bit 0	R	SLPD[69]	X

Register 0x00B9: RX-SBI-ELST Slip Direction #11

Bit	Type	Function	Default
Bit 7	R	SLPD[84]	X
Bit 6	R	SLPD[83]	X
Bit 5	R	SLPD[82]	X
Bit 4	R	SLPD[81]	X
Bit 3	R	SLPD[80]	X
Bit 2	R	SLPD[79]	X
Bit 1	R	SLPD[78]	X
Bit 0	R	SLPD[77]	X

Register 0x00BA: RX-SBI-ELST Slip Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	SLPE	0

SLPE:

If this bit is a logic 1, the RXELST bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the SLPI[84:1] bits is a logic 1. This bit should be set to 0 if any link has its ELSTBYP bit set. When bypassed, the elastic store will constantly roll over and cause excessive interrupts

1.10 T1/E1 Transmit Elastic Store (TX-ELST) Registers

Register 0x00C0: TX-ELST Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Writing to this register triggers an indirect channel register access to the transmit elastic store (TX-ELST) context RAM.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the TX-ELST Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the TX-ELST Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the TX-ELST Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x00C1: TX-ELST Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the TX-ELST channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 3. CADDR[4:0] is the tributary index and ranges from 1 to 28.

Register 0x00C2: TX-ELST Indirect Channel Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	ELSTBYP	0

This register contains data read from the channel context RAM after an indirect read operation or data to be inserted into the channel context RAM in an indirect write operation.

The bits to be written to the channel context RAM, in an indirect channel write operation, must be set up in this register before triggering the write. Irregardless of writes to this register, reads will always return the data retrieved by the latest indirect read operation.

Reserved:

The reserved bit must be set to logic 0 for correct operation.

ELSTBYP:

If the ELST Bypass bit is logic 1, the transmit frame slip buffer is bypassed, thus eliminating a nominal one frame latency. The bypass may only be enabled when the SBI bus interface is enabled and the payload allowed to float, i.e. the SYSOPT[1:0] bits of the Global Configuration register are binary 10.

Register 0x00C4: TX-ELST Slip Status #1

Bit	Type	Function	Default
Bit 7	R	REGD_EI	X
Bit 6	R	REGB_CI	X
Bit 5	R	REG8_9_AI	X
Bit 4	R	REG5_6_7I	X
Bit 3	W12C	SLPI[4]	X
Bit 2	W12C	SLPI[3]	X
Bit 1	W12C	SLPI[2]	X
Bit 0	W12C	SLPI[1]	X

SLPI[84:1]:

A logic 1 in these bits indicate a slip has occurred on the associated tributary since the bit was explicitly cleared. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG5_6_7I:

This bit is a logic 1 if at least one bit in Register 0x00C5, 0x00C6 or 0x00C7 is logic 1.

REG8_9_AI:

This bit is a logic 1 if at least one bit in Register 0x00C8, 0x00C9 or 0x00CA is logic 1.

REGB_CI:

This bit is a logic 1 if at least one bit in Register 0x00CB or 0x00CC is logic 1.

REGD_EI:

This bit is a logic 1 if at least one bit in Register 0x00CD or 0x00CE is logic 1.

Register 0x00C5: TX-ELST Slip Status #2

Bit	Type	Function	Default
Bit 7	W12C	SLPI[12]	X
Bit 6	W12C	SLPI[11]	X
Bit 5	W12C	SLPI[10]	X
Bit 4	W12C	SLPI[9]	X
Bit 3	W12C	SLPI[8]	X
Bit 2	W12C	SLPI[7]	X
Bit 1	W12C	SLPI[6]	X
Bit 0	W12C	SLPI[5]	X

Register 0x00C6: TX-ELST Slip Status #3

Bit	Type	Function	Default
Bit 7	W12C	SLPI[20]	X
Bit 6	W12C	SLPI[19]	X
Bit 5	W12C	SLPI[18]	X
Bit 4	W12C	SLPI[17]	X
Bit 3	W12C	SLPI[16]	X
Bit 2	W12C	SLPI[15]	X
Bit 1	W12C	SLPI[14]	X
Bit 0	W12C	SLPI[13]	X

Register 0x00C7: TX-ELST Slip Status #4

Bit	Type	Function	Default
Bit 7	W12C	SLPI[28]	X
Bit 6	W12C	SLPI[27]	X
Bit 5	W12C	SLPI[26]	X
Bit 4	W12C	SLPI[25]	X
Bit 3	W12C	SLPI[24]	X
Bit 2	W12C	SLPI[23]	X
Bit 1	W12C	SLPI[22]	X
Bit 0	W12C	SLPI[21]	X

Register 0x00C8: TX-ELST Slip Status #5

Bit	Type	Function	Default
Bit 7	W12C	SLPI[36]	X
Bit 6	W12C	SLPI[35]	X
Bit 5	W12C	SLPI[34]	X
Bit 4	W12C	SLPI[33]	X
Bit 3	W12C	SLPI[32]	X
Bit 2	W12C	SLPI[31]	X
Bit 1	W12C	SLPI[30]	X
Bit 0	W12C	SLPI[29]	X

Register 0x00C9: TX-ELST Slip Status #6

Bit	Type	Function	Default
Bit 7	W12C	SLPI[44]	X
Bit 6	W12C	SLPI[43]	X
Bit 5	W12C	SLPI[42]	X
Bit 4	W12C	SLPI[41]	X
Bit 3	W12C	SLPI[40]	X
Bit 2	W12C	SLPI[39]	X
Bit 1	W12C	SLPI[38]	X
Bit 0	W12C	SLPI[37]	X

Register 0x00CA: TX-ELST Slip Status #7

Bit	Type	Function	Default
Bit 7	W12C	SLPI[52]	X
Bit 6	W12C	SLPI[51]	X
Bit 5	W12C	SLPI[50]	X
Bit 4	W12C	SLPI[49]	X
Bit 3	W12C	SLPI[48]	X
Bit 2	W12C	SLPI[47]	X
Bit 1	W12C	SLPI[46]	X
Bit 0	W12C	SLPI[45]	X

Register 0x00CB: TX-ELST Slip Status #8

Bit	Type	Function	Default
Bit 7	W12C	SLPI[60]	X
Bit 6	W12C	SLPI[59]	X
Bit 5	W12C	SLPI[58]	X
Bit 4	W12C	SLPI[57]	X
Bit 3	W12C	SLPI[56]	X
Bit 2	W12C	SLPI[55]	X
Bit 1	W12C	SLPI[54]	X
Bit 0	W12C	SLPI[53]	X

Register 0x00CC: TX-ELST Slip Status #9

Bit	Type	Function	Default
Bit 7	W12C	SLPI[68]	X
Bit 6	W12C	SLPI[67]	X
Bit 5	W12C	SLPI[66]	X
Bit 4	W12C	SLPI[65]	X
Bit 3	W12C	SLPI[64]	X
Bit 2	W12C	SLPI[63]	X
Bit 1	W12C	SLPI[62]	X
Bit 0	W12C	SLPI[61]	X

Register 0x00CD: TX-ELST Slip Status #10

Bit	Type	Function	Default
Bit 7	W12C	SLPI[76]	X
Bit 6	W12C	SLPI[75]	X
Bit 5	W12C	SLPI[74]	X
Bit 4	W12C	SLPI[73]	X
Bit 3	W12C	SLPI[72]	X
Bit 2	W12C	SLPI[71]	X
Bit 1	W12C	SLPI[70]	X
Bit 0	W12C	SLPI[69]	X

Register 0x00CE: TX-ELST Slip Status #11

Bit	Type	Function	Default
Bit 7	W12C	SLPI[84]	X
Bit 6	W12C	SLPI[83]	X
Bit 5	W12C	SLPI[82]	X
Bit 4	W12C	SLPI[81]	X
Bit 3	W12C	SLPI[80]	X
Bit 2	W12C	SLPI[79]	X
Bit 1	W12C	SLPI[78]	X
Bit 0	W12C	SLPI[77]	X

Register 0x00CF: TX-ELST Slip Direction #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	SLPD[4]	X
Bit 2	R	SLPD[3]	X
Bit 1	R	SLPD[2]	X
Bit 0	R	SLPD[1]	X

SLPD[84:1]:

A logic 1 in these bits indicate the direction of latest slip on the associated tributary. If SLPD[x] is a logic 0, the slip resulted in the repetition of a frame. If SLPD[x] is a logic 1, a frame was lost. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Register 0x00D0: TX-ELST Slip Direction #2

Bit	Type	Function	Default
Bit 7	R	SLPD[12]	X
Bit 6	R	SLPD[11]	X
Bit 5	R	SLPD[10]	X
Bit 4	R	SLPD[9]	X
Bit 3	R	SLPD[8]	X
Bit 2	R	SLPD[7]	X
Bit 1	R	SLPD[6]	X
Bit 0	R	SLPD[5]	X

Register 0x00D1: TX-ELST Slip Direction #3

Bit	Type	Function	Default
Bit 7	R	SLPD[20]	X
Bit 6	R	SLPD[19]	X
Bit 5	R	SLPD[18]	X
Bit 4	R	SLPD[17]	X
Bit 3	R	SLPD[16]	X
Bit 2	R	SLPD[15]	X
Bit 1	R	SLPD[14]	X
Bit 0	R	SLPD[13]	X

Register 0x00D2: TX-ELST Slip Direction #4

Bit	Type	Function	Default
Bit 7	R	SLPD[28]	X
Bit 6	R	SLPD[27]	X
Bit 5	R	SLPD[26]	X
Bit 4	R	SLPD[25]	X
Bit 3	R	SLPD[24]	X
Bit 2	R	SLPD[23]	X
Bit 1	R	SLPD[22]	X
Bit 0	R	SLPD[21]	X

Register 0x00D3: TX-ELST Slip Direction #5

Bit	Type	Function	Default
Bit 7	R	SLPD[36]	X
Bit 6	R	SLPD[35]	X
Bit 5	R	SLPD[34]	X
Bit 4	R	SLPD[33]	X
Bit 3	R	SLPD[32]	X
Bit 2	R	SLPD[31]	X
Bit 1	R	SLPD[30]	X
Bit 0	R	SLPD[29]	X

Register 0x00D4: TX-ELST Slip Direction #6

Bit	Type	Function	Default
Bit 7	R	SLPD[44]	X
Bit 6	R	SLPD[43]	X
Bit 5	R	SLPD[42]	X
Bit 4	R	SLPD[41]	X
Bit 3	R	SLPD[40]	X
Bit 2	R	SLPD[39]	X
Bit 1	R	SLPD[38]	X
Bit 0	R	SLPD[37]	X

Register 0x00D5: TX-ELST Slip Direction #7

Bit	Type	Function	Default
Bit 7	R	SLPD[52]	X
Bit 6	R	SLPD[51]	X
Bit 5	R	SLPD[50]	X
Bit 4	R	SLPD[49]	X
Bit 3	R	SLPD[48]	X
Bit 2	R	SLPD[47]	X
Bit 1	R	SLPD[46]	X
Bit 0	R	SLPD[45]	X

Register 0x00D6: TX-ELST Slip Direction #8

Bit	Type	Function	Default
Bit 7	R	SLPD[60]	X
Bit 6	R	SLPD[59]	X
Bit 5	R	SLPD[58]	X
Bit 4	R	SLPD[57]	X
Bit 3	R	SLPD[56]	X
Bit 2	R	SLPD[55]	X
Bit 1	R	SLPD[54]	X
Bit 0	R	SLPD[53]	X

Register 0x00D7: TX-ELST Slip Direction #9

Bit	Type	Function	Default
Bit 7	R	SLPD[68]	X
Bit 6	R	SLPD[67]	X
Bit 5	R	SLPD[66]	X
Bit 4	R	SLPD[65]	X
Bit 3	R	SLPD[64]	X
Bit 2	R	SLPD[63]	X
Bit 1	R	SLPD[62]	X
Bit 0	R	SLPD[61]	X

Register 0x00D8: TX-ELST Slip Direction #10

Bit	Type	Function	Default
Bit 7	R	SLPD[76]	X
Bit 6	R	SLPD[75]	X
Bit 5	R	SLPD[74]	X
Bit 4	R	SLPD[73]	X
Bit 3	R	SLPD[72]	X
Bit 2	R	SLPD[71]	X
Bit 1	R	SLPD[70]	X
Bit 0	R	SLPD[69]	X

Register 0x00D9: TX-ELST Slip Direction #11

Bit	Type	Function	Default
Bit 7	R	SLPD[84]	X
Bit 6	R	SLPD[83]	X
Bit 5	R	SLPD[82]	X
Bit 4	R	SLPD[81]	X
Bit 3	R	SLPD[80]	X
Bit 2	R	SLPD[79]	X
Bit 1	R	SLPD[78]	X
Bit 0	R	SLPD[77]	X

Register 0x00DA: TX-ELST Slip Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	SLPE	0

SLPE:

If this bit is a logic 1, the TXELST bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the SLPI[84:1] bits is a logic 1. This bit should be set to 0 if any link has its ELSTBYP bit set. When bypassed, the elastic store will constantly roll over and cause excessive interrupts

1.11 T1/E1 Transmit Per-Channel Controller (TPCC) Registers

Register 0x0100: TPCC Indirect Status/Time-slot Address

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5	R/W	TSACCESS	0
Bit 4	R/W	TSADDR[4]	0
Bit 3	R/W	TSADDR[3]	0
Bit 2	R/W	TSADDR[2]	0
Bit 1	R/W	TSADDR[1]	0
Bit 0	R/W	TSADDR[0]	0

Writing to this register triggers an indirect channel register access to the Transmit Per-Channel Controller (TPCC) context RAM.

TSADDR:

The timeslot address determines the DS0 timeslot/channel accessed when an access is initiated with TSACCESS logic 1.

For T1 tributaries, the valid range is 1 to 24. For E1 tributaries, the valid range is 0 to 31.

TSACCESS:

The timeslot indirect access control bit determines whether the per-tributary or per-timeslot data is accessed. If TSACCESS is logic 0, the per-tributary data is accessed. If TSACCESS is logic 1, the per-timeslot data is accessed with the timeslot determined by the TSADDR[4:0] bits.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the TPCC Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the TPCC Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the TPCC Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0101: TPCC Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the TPCC context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 3. CADDR[4:0] is the tributary index and ranges from 1 to 28.

Registers 0x0102-0x0106: TPCC Indirect Channel Data Registers

These registers contain data read from the TPCC channel context RAM after an indirect read operation or data to be inserted into the TPCC channel context RAM in an indirect write operation.

The bits to be written to the TPCC channel context RAM, in an indirect channel write operation, must be set up in these registers before triggering the write. All three registers from 0x0102 through 0x0104 inclusive must be written prior to each indirect write unless one desires the same configuration as the latest indirect write. The value returned by the latest indirect read has no bearing on indirect writes. Irregardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

The significance of the bits is dependent on the state of the TSACCESS bit of the TPCC Indirect Status/Time-slot Address register. If TSACCESS is logic 1, context information for the timeslot/channel identified by TSADDR[4:0] is either written or read.

TSACCESS=0:

Address	Offset								
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default (‘b)**
0x0102	RPRBSLEN[2:0]			RPRBS UNF	MDTRK	MSTRK	PCCE	Unused	00000000
0x0103	T56K PRBS	TPRBS INV	TPRBSLEN[2:0]			TPRBS UNF	R56K PRBS	RPRBS INV	00000000
0x0104	PRBSERR[2:0]			PSYNCI	PSYNC	Reserved	PSYNCE	INV LAST	XXXXXX00
0x0105	PRBSERR[10:3]								XXXXXXXX
0x0106	Unused			PRBSERR[15:11]					XXXXXXXX

TSACCESS=1:

Address	Offset								
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default ('b)**
0x0102	SIGC[0]	INV[1:0]		ALAW	DMW	IDLC	ZCS[1:0]		00000000
0x0103	IDLE[2:0]			A'	B'	C'	D'	SIGC[1]	000000000
0x0104	Unused	TPRBS	RPRBS	IDLE[7:3]					X0000000
0x0105	Unused								XXXXXXXX
0x0106	Unused								XXXXXXXX

In the following bit descriptions, the system interface refers to either the SBI Add bus or the Egress H-MVIP Interface. Be aware that the PRBS receiver documented is down stream of the frame slip buffer; therefore, controlled slips will corrupt the bit sequence and result in bit errors and momentary loss of synchronization.

PCCE:

The per-tributary configuration enable bit, PCCE, enables the per-timeslot configuration data to affect the signaling and PCM byte streams. If the PCCE is logic 1, it enables the both the TSACCESS=0 and TSACCESS=1 Configuration bits. The global PCCE bit of the TPCC Configuration Bits register must also be logic 1 for this bit to have effect.

Upon setting this bit to logic 0, the PRBS shift registers and statuses are frozen.

The PCCE context bit must be logic 0 if the tributary is not being used. This is the case when the SPE is configured for other than T1/E1 or the ENBL bit programmed through the EXSBI Tributary Control Indirect Access Data register is logic 0 in SBI applications.

MSTRK:

Master Signaling Trunk Conditioning. When this bit is logic 1, signaling substitution is performed on all channels/time slots for a tributary. Setting MSTRK is equivalent to setting the SIGC[1:0] bits to binary 01 for all channels/timeslots.

MDTRK:

Master Data Trunk Conditioning. When this bit is logic 1, idle code substitution is performed on all channels/time slots for a tributary. Setting MDTRK is equivalent to setting the IDLC Per-Channel context bit to logic 1 for all channels/timeslots.

RPRBSUNF:

If this bit is logic 1, the PRBS is expected to fill all bits in the tributary data stream received from the system interface (SBI Add bus or H-MVIP). This bit supercedes the Per-Channel RPRBS context bits and the R56KPRBS context bits.

RPRBSLEN[2:0]:

The Receive PRBS Length field determines the sequence length of the expected bit pattern received from the system interface (SBI Add bus or H-MVIP):

RPRBSLEN	Sequence Length	Polynomial
000	$2^{11} - 1$	$x^{11} + x^9 + 1$
001	$2^{15} - 1$	$x^{15} + x^{14} + 1$
010	$2^{20} - 1$ (QRSS)	$x^{20} + x^{17} + 1$ with zero suppression
011	$2^{20} - 1$	$x^{20} + x^3 + 1$
100	$2^7 - 1$	$x^7 + x^3 + 1$ with XOR in the feedback path
101	$2^7 - 1$	$x^7 + x^3 + 1$ with XNOR in the feedback path

RPRBSINV:

If this bit is logic 1, the logical polarity of the received PRBS is inverted before comparison.

R56KPRBS:

If this bit is logic 1, the PRBS is expected to fill only the first seven bits of the selected channels/time slots. Otherwise, the PRBS is expected to occupy the entire selected channels/time slots.

TPRBSUNF:

If this bit is logic 1, the PRBS fills all bits of the of the mapped or multiplexed tributary. This bit supercedes the Per-Channel TPRBS context bits and the

T56KPRBS context bits. If TPRBSUNF is logic 1, the FDIS and CASDIS bits must be set to logic 1 through the T1/E1 Transmitter Indirect Channel Data registers. Common channel signaling must also be disabled.

TPRBSLEN[2:0]:

The Transit PRBS Length field determines the sequence length of the generated bit pattern destined for the SONET/SDH mapper or DS3 multiplexer:

TPRBSLEN	Sequence Length	Polynomial
000	$2^{11} – 1$	$x^{11} + x^9 + 1$
001	$2^{15} – 1$	$x^{15} + x^{14} + 1$
010	$2^{20} – 1$ (QRSS)	$x^{20} + x^{17} + 1$ with zero suppression
011	$2^{20} – 1$	$x^{20} + x^3 + 1$
100	$2^7 – 1$	$x^7 + x^3 + 1$ with XOR in the feedback path
101	$2^7 – 1$	$x^7 + x^3 + 1$ with XNOR in the feedback path

TPRBSINV:

If this bit is logic 1, the logical polarity of the generated PRBS is inverted before transmission.

T56KPRBS

If this bit is logic 1, the generated PRBS fills only the first seven bits of the selected channels/time slots. Otherwise, the PRBS occupies the entire selected channels/time slots.

INVLAST:

If this bit is logic 1, inversion (as controlled by the INV[1:0] Per-Channel context bits) is the last per-channel operation performed on the data. Otherwise, inversion is the first operation performed.

PSYNCE:

If this bit is a logic 1, the associated TPCCI[x] bit is set upon a change in the PSYNC context bit.

PSYNC:

PSYNC is the PRBS synchronization status. PSYNC becomes a logic 1 if the received data matched the expected sequence for the latest four bytes. PSYNC is set to logic 0 only if 3 consecutive bytes are in error.

PSYNCI:

PSYNCI becomes a logic 1 upon a change in the PSYNC context bit. It is cleared upon an indirect read access.

PRBSERR[15:0]:

The PRBS Error holding register contains a count of the discrepancies between the expected PRBS sequence and the receive data that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_PRBS bit to logic 1. The count saturates at all ones.

ZCS[1:0]:

These bits control the Zero Code Suppression in the transmitted tributary as follows:

T1:

ZCS[1:0]	Description
00	No Zero Code Suppression
01	GTE Zero Code Suppression. The least significant bit (bit 8) of an all zeros channel is forced to a one, except for signaling frames where the second least significant bit is forced to a one.
10	DDS Zero Code Suppression. All zero channel data is replaced with the patte“n "10011”00"
11	Bell Zero Code Suppression. The second least significant bit (bit 7) of an all zeros channel is forced to a one.

E1:

ZCS[1:0]	Description
00	No Zero Code Suppression
01	Jammed bit-8. The least significant bit (bit 8) of an all zeros channel is forced to a one.
10	No Zero Code Suppression
11	Jammed bit-8.

Zero code suppression occurs after data inversion, idle code insertion, digital milliwatt insertion and signaling have occurred.

IDLC:

If this bit is logic 1, the channel/time slot data is replaced by the value in the IDLE[7:0] field.

DMW:

If this bit is logic 1, the channel/time slot data is replaced by the Digital Milliwatt signal. The encoding of the 1 kHz sine wave is determined by the ALAW context bit.

ALAW:

This bit determines the encoding of the Digital Milliwatt signal. If ALAW is logic 0, μ-law companding is respected. If ALAW is logic 1, A-law companding is respected.

INV[1:0]:

These bits invert the channel/time slot data:

INV[1:0]	T1 Description	E1 Description
00	No inversion (default)	No inversion (default)
01	Only the MSB of the received PCM channel data is inverted (Sign bit inversion)	Invert even bits
10	All bits EXCEPT the MSB of the received PCM channel data is inverted (Magnitude inversion)	Invert odd bits
11	Invert all bits	Invert all bits

Signaling is not subjected to inversion.

SIGC[1:0]:

These bits determine the source of inserted signaling:

SIGC[1:0]	Description

00	No signaling insertion.
01	Signaling taken from A' B' C' and D' context bits.
10	Signaling taken from system interface.
11	Reserved.

The SIGC bits should be “00” if the INBANDCTL bit of the TPCC Configuration register is logic 1.

A’,B’,C’,D’:

These signaling bits are inserted at the system interface when the MSTRK bit is logic 1 or if the SIGC[1:0] bits are binary 01. For the T1 SF frame format, C’ and D’ must equal A’ and B’, respectively.

IDLE[7:0]:

This field contains the value inserted if the MDTRK or IDLC bit is logic 1.

RPRBS:

If this bit is logic 1, a PRBS is expected in the channel/time slot received from the system interface (SBI Add bus or H-MVIP).

TPRBS:

If this bit is logic 1, a PRBS is generated in the channel/time slot destined for the SONET/SDH mapper or DS3 mulitplexer.

Register 0x0107: TPCC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	INTE	0
Bit 3	R/W	INBANDCTL	0
Bit 2	W12C	XFERI	X
Bit 1	R/W	XFERE	0
Bit 0	R/W	PCCE	0

INTE:

If this bit is a logic 1, the TPRBS bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the TPCCI[84:1] bits is a logic 1.

INBANDCTL:

This bit enables the control of the signaling insertion via an inband mechanism. If INBANDCTL is logic 1, the robbed bit signaling insertion is controlled by the third and fourth bits in each octet received on CASED[1:21]. If INBANDCTL is logic 0, robbed bit signaling is strictly controlled by the TPCC SIGC[1:0] context bits.

INBANDCTL only has effect for T1 tributaries and only if the CAS source is H-MVIP (i.e. SYSOPT[1:0] register bits are 01 or 11).

XFERI:

The XFERI bit indicates that a transfer of accumulated PRBS error data has occurred. A logic 1 in this bit position indicates that the holding registers have been updated. This update is initiated by a write to the Global Performance Monitor Update register that sets the E1T1_PRBS bit to logic 1.

Logic 1 must be written to this bit to clear it to logic 0.

XFERE:

If this bit is a logic 1, the TPRBS bit of the Master Interrupt Source T1E1 register is logic 1 if the XFERI bit is a logic 1.

PCCE:

This global bit enables per-channel/per-timeslot functions in the transmit direction if logic 1. The per-tributary PCCE bits set through the TPCC Indirect Channel Data Registers must also be set to enable individual tributaries.

Upon setting this bit to logic 0, the PRBS shift registers and statuses are frozen.

Register 0x0108: TPCC Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R	REG11_12I	X
Bit 6	R	REGF_10I	X
Bit 5	R	REGC_D_EI	X
Bit 4	R	REG9_A_BI	X
Bit 3	R	TPCCI[4]	X
Bit 2	R	TPCCI[3]	X
Bit 1	R	TPCCI[2]	X
Bit 0	R	TPCCI[1]	X

TPCCI[84:1]:

A logic 1 in these bits indicate indicate a change of PRBS synchronization state on the associated tributary since this register was last read. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG9_A_BI:

This bit is a logic 1 if at least one bit in Register 0x0109, 0x010A or 0x010B is logic 1.

REGC_D_EI:

This bit is a logic 1 if at least one bit in Register 0x010C, 0x010D or 0x010E is logic 1.

REGF_10I:

This bit is a logic 1 if at least one bit in Register 0x010F or 0x0100 is logic 1.

REG11_12I:

This bit is a logic 1 if at least one bit in Register 0x0101 or 0x0102 is logic 1.

Register 0x0109: TPCC Interrupt Status #2

Bit	Type	Function	Default
Bit 7	R	TPCCI[12]	X
Bit 6	R	TPCCI[11]	X
Bit 5	R	TPCCI[10]	X
Bit 4	R	TPCCI[9]	X
Bit 3	R	TPCCI[8]	X
Bit 2	R	TPCCI[7]	X
Bit 1	R	TPCCI[6]	X
Bit 0	R	TPCCI[5]	X

Register 0x010A: TPCC Interrupt Status #3

Bit	Type	Function	Default
Bit 7	R	TPCCI[20]	X
Bit 6	R	TPCCI[19]	X
Bit 5	R	TPCCI[18]	X
Bit 4	R	TPCCI[17]	X
Bit 3	R	TPCCI[16]	X
Bit 2	R	TPCCI[15]	X
Bit 1	R	TPCCI[14]	X
Bit 0	R	TPCCI[13]	X

Register 0x010B: TPCC Interrupt Status #4

Bit	Type	Function	Default
Bit 7	R	TPCCI[28]	X
Bit 6	R	TPCCI[27]	X
Bit 5	R	TPCCI[26]	X
Bit 4	R	TPCCI[25]	X
Bit 3	R	TPCCI[24]	X
Bit 2	R	TPCCI[23]	X
Bit 1	R	TPCCI[22]	X
Bit 0	R	TPCCI[21]	X

Register 0x010C: TPCC Interrupt Status #5

Bit	Type	Function	Default
Bit 7	R	TPCCI[36]	X
Bit 6	R	TPCCI[35]	X
Bit 5	R	TPCCI[34]	X
Bit 4	R	TPCCI[33]	X
Bit 3	R	TPCCI[32]	X
Bit 2	R	TPCCI[31]	X
Bit 1	R	TPCCI[30]	X
Bit 0	R	TPCCI[29]	X

Register 0x010D: TPCC Interrupt Status #6

Bit	Type	Function	Default
Bit 7	R	TPCCI[44]	X
Bit 6	R	TPCCI[43]	X
Bit 5	R	TPCCI[42]	X
Bit 4	R	TPCCI[41]	X
Bit 3	R	TPCCI[40]	X
Bit 2	R	TPCCI[39]	X
Bit 1	R	TPCCI[38]	X
Bit 0	R	TPCCI[37]	X

Register 0x010E: TPCC Interrupt Status #7

Bit	Type	Function	Default
Bit 7	R	TPCCI[52]	X
Bit 6	R	TPCCI[51]	X
Bit 5	R	TPCCI[50]	X
Bit 4	R	TPCCI[49]	X
Bit 3	R	TPCCI[48]	X
Bit 2	R	TPCCI[47]	X
Bit 1	R	TPCCI[46]	X
Bit 0	R	TPCCI[45]	X

Register 0x010F: TPCC Interrupt Status #8

Bit	Type	Function	Default
Bit 7	R	TPCCI[60]	X
Bit 6	R	TPCCI[59]	X
Bit 5	R	TPCCI[58]	X
Bit 4	R	TPCCI[57]	X
Bit 3	R	TPCCI[56]	X
Bit 2	R	TPCCI[55]	X
Bit 1	R	TPCCI[54]	X
Bit 0	R	TPCCI[53]	X

Register 0x0110: TPCC Interrupt Status #9

Bit	Type	Function	Default
Bit 7	R	TPCCI[68]	X
Bit 6	R	TPCCI[67]	X
Bit 5	R	TPCCI[66]	X
Bit 4	R	TPCCI[65]	X
Bit 3	R	TPCCI[64]	X
Bit 2	R	TPCCI[63]	X
Bit 1	R	TPCCI[62]	X
Bit 0	R	TPCCI[61]	X

Register 0x0111: TPCC Interrupt Status #10

Bit	Type	Function	Default
Bit 7	R	TPCCI[76]	X
Bit 6	R	TPCCI[75]	X
Bit 5	R	TPCCI[74]	X
Bit 4	R	TPCCI[73]	X
Bit 3	R	TPCCI[72]	X
Bit 2	R	TPCCI[71]	X
Bit 1	R	TPCCI[70]	X
Bit 0	R	TPCCI[69]	X

Register 0x0112: TPCC Interrupt Status #11

Bit	Type	Function	Default
Bit 7	R	TPCCI[84]	X
Bit 6	R	TPCCI[83]	X
Bit 5	R	TPCCI[82]	X
Bit 4	R	TPCCI[81]	X
Bit 3	R	TPCCI[80]	X
Bit 2	R	TPCCI[79]	X
Bit 1	R	TPCCI[78]	X
Bit 0	R	TPCCI[77]	X

Register 0x0113: TPCC PRBS Error Insertion

Bit	Type	Function	Default
Bit 7	RW	TPRBS_ERR_INSERT	X
Bit 6	RW	TPRBS_ADDR[6]	X
Bit 5	RW	TPRBS_ADDR[5]	X
Bit 4	RW	TPRBS_ADDR[4]	X
Bit 3	RW	TPRBS_ADDR[3]	X
Bit 2	RW	TPRBS_ADDR[2]	X
Bit 1	RW	TPRBS_ADDR[1]	X
Bit 0	RW	TPRBS_ADDR[0]	X

TPRBS_ERR_INSERT:

The TPRBS Error insertion Enable bit causes a single bit error to be inserted in the PRBS pattern for the tributary addressed by TPRBS_ADDR[6:0]. A zero to one transition triggers the error insertion.

TPRBS_ADDR[6:0]:

Indicates the tributary into which a single bit error is to be inserted. TPRBS_ADDR[6:5] is the SPE index and ranges from 1 to 3. TPRBS_ADDR[4:0] is the tributary index and ranges from 1 to 28.

Register 0x0114: TPCC PRBS Error Insert Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	W12C	TPRBS_ERR_INSERTED	X

TPRBS_ERR_INSERTED:

TPRBS_ERR_INSERTED indicates an error has been inserted. This bit is cleared to logic 0 upon a writing a logic 1 to the bit position.

1.12 T1/E1 Receive HDLC Controller (RHDL) Registers

Register 0x0118: RHDL Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0		Unused	

Writing to this register triggers an indirect channel register access.

An indirect write access is illegal when the FACCESS bit of the RHDL Indirect Channel Address Register is logic 1. The result would be that CBUSY would remain logic 1 until this register is written again.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. The data to be written must be set up in the RHDL Indirect Channel Data registers (0x011A - 0x011D) before setting CRWB=0. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not

expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0119: RHDL Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7	R/W	FACCESS	0
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 3. CADDR[4:0] is the tributary index and ranges from 1 to 28.

FACCESS:

If FACCESS is logic 1, the indirect access will be to the packet FIFO. If FACCESS is logic 0, the indirect access will be to the configuration data.

Registers 0x011A – 0x011D: RHDL Indirect Channel Data Registers

This registers contain data read from the channel context RAM after an indirect read operation or data to be inserted into the channel context RAM in an indirect write operation.

The bits to be written to the channel context RAM, in an indirect channel write operation, must be set up in this register before triggering the write. All four registers from 0x011A through 0x011D inclusive must be written prior to each indirect write unless one desires the same configuration as the latest indirect write (One need not write 0x011B through 0x011D if MEN is logic 0). The value returned by the latest indirect read has no bearing on indirect writes. Irregardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

FACCESS = 0:

Bit Range	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x011A	Unused	MEN	MM	INVERT	CRC[1:0]		DELIN	EN	X0000000
0x011B	PA[7:0]								00000000
0x011C	SA[7:0]								00000000
0x011D	TA[7:0]								00000000

FACCESS = 1:

Bit Range	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x011A	HDLCDATA[7:0]								XXXXXXXX
0x011B	CBUSY	Unused	FE	OVR	PKIN	PBS[2:0]			XXXXXXXX
0x011C	Unused								XXXXXXXX
0x011D	Unused								XXXXXXXX

EN:

The enable (EN) bit controls the overall operation of the receive HDLC processor. When EN is logic 1, receive HDLC processor is enabled to identify and buffer packets. When EN is logic 0, the FIFO buffer and interrupts are all cleared.

DELIN:

The indirect delineate enable bit (DELIN) configures the receive HDLC processor to perform flag sequence delineation and bit de-stuffing on the incoming data stream. The delineate enable bit to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When DELIN is set to logic 1, flag sequence delineation and bit de-stuffing is performed on the incoming data stream. When DELIN is set to logic 0, the HDLC does not perform any processing (flag sequence delineation, bit de-stuffing nor CRC verification) on the incoming stream. DELIN reflects the value written until the completion of a subsequent indirect channel read operation.

CRC[1:0]:

The CRC algorithm (CRC[1:0]) configures the HDLC processor to perform CRC verification on the incoming data stream. The value of CRC[1:0] to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. The value of CRC[1:0] is ignored when DELIN is low. CRC[1:0] reflects the value written until the completion of a subsequent indirect channel read operation.

CRC[1]	CRC[0]	Operation
0	0	No Verification
0	1	CRC-CCITT
1	0	CRC-32
1	1	Illegal

INVERT:

The HDLC data inversion bit (INVERT) configures the HDLC processor to logically invert the incoming HDLC stream before processing it. When INVERT is set to logic 1, the HDLC stream is logically inverted before processing. When INVERT is set to logic 0, the HDLC stream is not inverted before processing. INVERT reflects the value written until the completion of a subsequent indirect channel read operation.

HDLCDATA[7:0]:

This is the data link byte that has been read from the 127 byte FIFO by the indirect read. It's significance is indicated PBS[2:0] bits. The entire packet including the frame check sequence, but excluding delimiting flags is available to be read from the FIFO except when the DELIN bit is logic 0, in which case the entire data stream is available to be read.

When the REVERSE bit of the RHDL Interrupt Control register is set to logic 0, the least significant bit of each byte of the data bus (HDLCDATA[0]) is the first HDLC bit received (datacom standard). When REVERSE is set to logic 1, HDLCDATA[7] is the first HDLC bit received (telecom standard).

MM:

Setting the Match Mask (MM) bit to logic 1 ignores the PA[1:0] bits of the Primary Address Match field, the SA[1:0] bits of the Secondary Address Match field, the TA[1:0] bits of the Tertiary Address Match field and the two least significant bits of the universal all ones address when performing the address comparison.

MEN:

Setting the Match Enable (MEN) bit to logic 1 enables the detection and storage in the FIFO of only those packets whose first data byte matches either of the bytes written to the Primary, Secondary or Tertiary Match Address Registers, or the universal all ones address. When the MEN bit is logic 0, all packets received are written into the FIFO.

PA[7:0]:

If MEN is logic 1, the first byte received after a flag character is compared against the Primary Address, PA[7:0]. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[7] corresponds to the first bit of the packet. The MM bit in the Configuration Register is used mask off PA[1:0] during the address comparison.

SA[7:0]:

If MEN is logic 1, the first byte received after a flag character is compared against the Secondary Address, SA[7:0]. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[7] corresponds to the first bit of the packet. The MM bit in the Configuration Register is used mask off SA[1:0] during the address comparison.

TA[7:0]:

If MEN is logic 1, the first byte received after a flag character is compared against the Tertiary Address, TA[7:0]. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. TA[7] corresponds to the first bit of the packet. The MM bit in the Configuration Register is used mask off TA[1:0] during the address comparison.

PBS[2:0]:

The packet byte status (PBS[2:0]) bits indicate the status of the data read concurrently from the FIFO.

PBS[2:0]	Description
000	The data byte read from the FIFO is not special. This code is used for every byte when the DELIN bit is logic 0.
001	Unused
010	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive. An abort may occur on the initiation of a bit oriented code.
011	Unused
100	The previous data byte read from the FIFO was the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes. The current HDLCDATA[7:0] value contains no valid data.
101	The previous data byte read from the FIFO must be discarded because there was a non-integer number of bytes in the packet. The current HDLCDATA[7:0] value contains no valid data.
110	The previous data byte read from the FIFO was the last byte of a normally terminated packet with a CRC error. The packet was received in error. The current HDLCDATA[7:0] value contains no valid data.
111	Unused

PKIN:

The Packet In (PKIN) bit is logic 1 when the last byte of a packet has been written into the FIFO or an abort has occurred. The appropriate RHDLI[84:1] bit will be set coincidentally. The PKIN bit is cleared to logic 0 after an indirect read.

OVR:

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the FIFO buffer. The appropriate RHDLI[84:1] bit will be set coincidentally. This bit is not reset to logic 0 until an indirect read. Upon an overflow the contents of the FIFO are emptied.

Because the integrity of the HDLC data is suspect upon a FIFO overflow, it is recommended the FIFO be flushed through indirect reads until an end-of-packet indication is read.

FE:

The FIFO buffer empty (FE) bit is set to logic 1 when the last FIFO buffer entry is read. The FE bit goes to logic 0 when the FIFO is loaded with new data.

CBUSY:

This bit is identical to the CBUSY bit of the RHDL Indirect Status register.

Register 0x011E: RHDL Interrupt Control

Bit	Type	Function	Default
Bit 7	R/W	INTE	0
Bit 6	R/W	REVERSE	0
Bit 5	R/W	INTC[5]	0
Bit 4	R/W	INTC[4]	0
Bit 3	R/W	INTC[3]	0
Bit 2	R/W	INTC[2]	0
Bit 1	R/W	INTC[1]	0
Bit 0	R/W	INTC[0]	0

INTC[5:0]:

The FIFO Interrupt Controls determine the FIFO threshold at which an interrupt event is generated. When the number of bytes in the FIFO increases above the binary value of INTC[5:0], the appropriate RHDLI[84:1] bit is set. Only the crossing of the threshold causes the event. The RHDLI[84:1] bits will also be set upon a complete packet.

REVERSE:

The REVERSE bit controls the bit ordering of the HDLC data transferred to the microprocessor port. When REVERSE is set to logic 0, the least significant bit of each byte of the data bus (HDLCDATA[0]) is the first HDLC bit received and the most significant bit of each byte (HDLCDATA[7]) is the last HDLC bit received (datacom standard). When REVERSE is set to logic 1, HDLCDATA[0] is the last HDLC bit received while HDLCDATA[7] is the first HDLC bit received (telecom standard).

INTE:

If this bit is logic 1, the INTB output becomes asserted low if any of the RHDLI[84:1] bits are logic 1.

Register 0x011F: RHDL Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R	REG8_9I	X
Bit 6	R	REG6_7I	X
Bit 5	R	REG3_4_5I	X
Bit 4	R	REG0_1_2I	X
Bit 3	W12C	RHDLI[4]	X
Bit 2	W12C	RHDLI[3]	X
Bit 1	W12C	RHDLI[2]	X
Bit 0	W12C	RHDLI[1]	X

RHDLI[84:1]:

A logic 1 in these bits indicate a change in link status, reception of a complete packet, a FIFO overflow or the crossing if the programmed FIFO fill level on the associated tributary since this register was last read. The associated SPE index is equal to the trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position. The associated RHDLI bit is also cleared to logic 0 upon an indirect read that returns the FE (FIFO empty) bit as a logic 1.

REG0_1_2I:

This bit is a logic 1 if at least one bit in Register 0x0120, 0x0121 or 0x0122 is logic 1.

REG3_4_5I:

This bit is a logic 1 if at least one bit in Register 0x0123, 0x0124 or 0x0125 is logic 1.

REG6_7I:

This bit is a logic 1 if at least one bit in Register 0x0126 or 0x0127 is logic 1.

REG8_9I:

This bit is a logic 1 if at least one bit in Register 0x0128 or 0x0129 is logic 1.

Register 0x0120: RHDL Interrupt Status #2

Bit	Type	Function	Default
Bit 7	W12C	RHDLI[12]	X
Bit 6	W12C	RHDLI[11]	X
Bit 5	W12C	RHDLI[10]	X
Bit 4	W12C	RHDLI[9]	X
Bit 3	W12C	RHDLI[8]	X
Bit 2	W12C	RHDLI[7]	X
Bit 1	W12C	RHDLI[6]	X
Bit 0	W12C	RHDLI[5]	X

Register 0x0121: RHDL Interrupt Status #3

Bit	Type	Function	Default
Bit 7	W12C	RHDLI[20]	X
Bit 6	W12C	RHDLI[19]	X
Bit 5	W12C	RHDLI[18]	X
Bit 4	W12C	RHDLI[17]	X
Bit 3	W12C	RHDLI[16]	X
Bit 2	W12C	RHDLI[15]	X
Bit 1	W12C	RHDLI[14]	X
Bit 0	W12C	RHDLI[13]	X

Register 0x0122: RHDL Interrupt Status #4

Bit	Type	Function	Default
Bit 7	W12C	RHDLI[28]	X
Bit 6	W12C	RHDLI[27]	X
Bit 5	W12C	RHDLI[26]	X
Bit 4	W12C	RHDLI[25]	X
Bit 3	W12C	RHDLI[24]	X
Bit 2	W12C	RHDLI[23]	X
Bit 1	W12C	RHDLI[22]	X
Bit 0	W12C	RHDLI[21]	X

Register 0x0123: RHDL Interrupt Status #5

Bit	Type	Function	Default
Bit 7	W12C	RHDLI[36]	X
Bit 6	W12C	RHDLI[35]	X
Bit 5	W12C	RHDLI[34]	X
Bit 4	W12C	RHDLI[33]	X
Bit 3	W12C	RHDLI[32]	X
Bit 2	W12C	RHDLI[31]	X
Bit 1	W12C	RHDLI[30]	X
Bit 0	W12C	RHDLI[29]	X

Register 0x0124: RHDL Interrupt Status #6

Bit	Type	Function	Default
Bit 7	W12C	RHDLI[44]	X
Bit 6	W12C	RHDLI[43]	X
Bit 5	W12C	RHDLI[42]	X
Bit 4	W12C	RHDLI[41]	X
Bit 3	W12C	RHDLI[40]	X
Bit 2	W12C	RHDLI[39]	X
Bit 1	W12C	RHDLI[38]	X
Bit 0	W12C	RHDLI[37]	X

Register 0x0125: RHDL Interrupt Status #7

Bit	Type	Function	Default
Bit 7	W12C	RHDLI[52]	X
Bit 6	W12C	RHDLI[51]	X
Bit 5	W12C	RHDLI[50]	X
Bit 4	W12C	RHDLI[49]	X
Bit 3	W12C	RHDLI[48]	X
Bit 2	W12C	RHDLI[47]	X
Bit 1	W12C	RHDLI[46]	X
Bit 0	W12C	RHDLI[45]	X

Register 0x0126: RHDL Interrupt Status #8

Bit	Type	Function	Default
Bit 7	W12C	RHDLI[60]	X
Bit 6	W12C	RHDLI[59]	X
Bit 5	W12C	RHDLI[58]	X
Bit 4	W12C	RHDLI[57]	X
Bit 3	W12C	RHDLI[56]	X
Bit 2	W12C	RHDLI[55]	X
Bit 1	W12C	RHDLI[54]	X
Bit 0	W12C	RHDLI[53]	X

Register 0x0127: RHDL Interrupt Status #9

Bit	Type	Function	Default
Bit 7	W12C	RHDLI[68]	X
Bit 6	W12C	RHDLI[67]	X
Bit 5	W12C	RHDLI[66]	X
Bit 4	W12C	RHDLI[65]	X
Bit 3	W12C	RHDLI[64]	X
Bit 2	W12C	RHDLI[63]	X
Bit 1	W12C	RHDLI[62]	X
Bit 0	W12C	RHDLI[61]	X

Register 0x0128 RHDL Interrupt Status #10

Bit	Type	Function	Default
Bit 7	W12C	RHDLI[76]	X
Bit 6	W12C	RHDLI[75]	X
Bit 5	W12C	RHDLI[74]	X
Bit 4	W12C	RHDLI[73]	X
Bit 3	W12C	RHDLI[72]	X
Bit 2	W12C	RHDLI[71]	X
Bit 1	W12C	RHDLI[70]	X
Bit 0	W12C	RHDLI[69]	X

Register 0x0129: RHDL Interrupt Status #11

Bit	Type	Function	Default
Bit 7	W12C	RHDLI[84]	X
Bit 6	W12C	RHDLI[83]	X
Bit 5	W12C	RHDLI[82]	X
Bit 4	W12C	RHDLI[81]	X
Bit 3	W12C	RHDLI[80]	X
Bit 2	W12C	RHDLI[79]	X
Bit 1	W12C	RHDLI[78]	X
Bit 0	W12C	RHDLI[77]	X

1.13 T1/E1 Transmit HDLC Controller (THDL) Registers

Register 0x0130: THDL Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5	R/W	HDLC_PROV_DIS	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

HDLC_PROV_DIS:

The channel indirect access control bit (HDLC_PRV_DIS) disbles a configure (write) or interrogate (read) access to the HDLC context bits (as opposed to the FIFO configuration). Writing a logic 1 to HDLC_PRV_DIS, indicates that only the LFILLE, UDRE, OVRE, FULLE, FIFOCLR, LINT, UTHR, SW_ABT and REVERSE bits are updated by a configuration (faccess = 0) indirect write operation. Writing a logic 0 to HDLC_PRV_DIS enables configuration writes to the HDLC processor context bits (DELIN, IDLE, CRC[1:0], DCRC and INVERT) as well as the FIFO configuration during an indirect write operation. When an indirect write is performed when HDLC_PROV_DIS is logic 0, the HDLC processor is reset and an abort is always issued.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB configures an indirect write operation. A write to the first Indirect Channel Data register triggers the actual write access. Data to be written is taken from the Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register or the first THDL Indirect Channel Data register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the THDL Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0131: THDL Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7	R/W	FACCESS	0
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 3. CADDR[4:0] is the tributary index and ranges from 1 to 28.

FACCESS:

If FACCESS is logic 1, the indirect access will be to the packet FIFO. If FACCESS is logic 0, the indirect access will be to the configuration data.

Register 0x0132 – 0x0136: THDL Indirect Channel Data Registers

This registers contain data read from the THDL channel context or FIFO RAM after an indirect read operation or data to be inserted into the THDL channel context RAM in an indirect write operation.

The bits to be written to the channel context RAM, in an indirect channel write operation, must be set up in these registers before triggering the write. All five registers from 0x0132 through 0x0136 inclusive must be written prior to each indirect write with FACCESS=0 unless one desires the same configuration as the latest indirect write. Only 0x0132 and 0x0133 need to be written if FACCESS=1. The value returned by the latest indirect read has no bearing on indirect writes. Irregardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

An indirect write can be initiated by the act of writing to 0x0132. The CRWB must be logic 0 for the indirect write to occur. If one is streaming in a packet, one need only set up the channel address (CADDR[6:0]) at the beginning and perform consecutive writes to 0x0132.

FACCESS=0:

Bit Index	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x0132	INVERT	DCRC	CRC[1:0]		IDLE	DELIN	Unused	Unused	000000XX
0x0133	Unused	Unused	ABT	FIFOCLR	FULLE	OVRE	UDRE	LFILLE	XX000000
0x0134	Unused	Unused	Unused	Unused	Unused	INTE*	FLG SHAREB*	REV ERSE	XXXXX000
0x0135	Unused	UTHR[6:0]							X0000000
0x0136	Unused	LINT[6:0]							X0000000

* These are global bits that affect all tributaries immediately upon a write. An indirect write operation is not required.

FACCESS=1:

	Offset								
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default ('b)**
0x0132	HDLCDATA[7:0]								XXXXXXXX
0x0133	EMPTY	FULL	BLFILL	FULLI	OVRI	UDRI	LFILLI	EOM	XXXXXXX0
0x0134	Unused								XXXXXXXX
0x0135	Unused								XXXXXXXX
0x0136	Unused								XXXXXXXX

FIFOCLR:

The FIFOCLR bit resets the FIFO. When set to logic 1, FIFOCLR will cause the FIFO to be cleared.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 01111111 code (the 0 is transmitted first) to be transmitted after the current byte from the FIFO is transmitted. The FIFO is then reset. All data in the FIFO will be lost. Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic 0. At least one Abort sequence will be sent when the ABT bit transitions from logic 0 to logic 1. Note that PRM insertion takes precedence over the ABT register bit. When a PRM frame is available, the 2 flag sequences before will be transmitted before and 1 or 2 flag sequences (depending on the FLGSHAREB bit setting) after the PRI frame. If the ABT bit is still set, the transmit the Abort sequence will be transmitted again.

DELIN:

The indirect delineate enable bit (DELIN) configures the HDLC processor to perform flag sequence insertion and bit stuffing on the outgoing data stream. The delineate enable bit to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When DELIN is set high, flag sequence insertion, bit stuffing and, optionally, CRC generation is performed on the outgoing HDLC data stream. When DELIN is set low, the HDLC does not perform any processing (bit stuffing nor CRC generation) on the outgoing stream. DELIN reflects the value written until the completion of a subsequent indirect channel read operation.

The option to set DELIN to logic 0 is provided to support clear channel

applications on the data link. When DELIN is logic 0, it is assumed the process writing to the FIFO will prevent it from becoming empty. Failure to do so will result in a bit sequence that resembles an HDLC abort followed by HDLC flags.

IDLE:

The interframe time fill bit (IDLE) configures the HDLC processor to use flag bytes or HDLC idle as the interframe time fill between HDLC packets. The value of IDLE to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When IDLE is set low, the HDLC processor uses flag bytes as the interframe time fill. When IDLE is set high, the HDLC processor uses HDLC idle (all one's bit with no bit-stuffing pattern is transmitted) as the interframe time file. IDLE reflects the value written until the completion of a subsequent indirect channel read operation.

CRC[1:0]:

The CRC algorithm (CRC[1:0]) configures the HDLC processor to perform CRC generation on the outgoing HDLC data stream. The value of CRC[1:0] to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. The value of CRC[1:0] is ignored when DELIN is low. CRC[1:0] reflects the value written until the completion of a subsequent indirect channel read operation.

CRC[1]	CRC[0]	Operation
0	0	No Generation
0	1	CRC-CCITT Generated
1	0	CRC-32 Generated
1	1	Reserved

DCRC:

The HDLC diagnostic CRC bit (DCRC) configures the HDLC processor to logically invert the inserted FCS on the outgoing HDLC stream for diagnostic purposes. The value of DCRC to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When DCRC is set high, the FCS value inserted by the HDLC processor is logically inverted. The inserted FCS is not inverted when DCRC are set low. DCRC is ignored when DELIN is set low or CRC[1:0] is equal to ”00". DCRC reflects the value written until the completion of a subsequent indirect channel read operation.

INVERT:

The HDLC data inversion bit (INVERT) configures the HDLC processor to logically invert the outgoing HDLC stream on TXDAT[7:0]. The value of INVERT to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When INVERT is set to one, the outgoing HDLC stream is logically inverted. The outgoing HDLC stream is not inverted when INVERT is set to zero. INVERT reflects the value written until the completion of a subsequent indirect channel read operation.

LFILLE:

A logic 1 in this position enables the associated THDLI[x] bit to be set upon the LFILLI bit transitioning to logic 1.

UDRE:

A logic 1 in this position enables the associated THDLI[x] bit to be set upon the UDRI bit transitioning to logic 1.

OVRE:

A logic 1 in this position enables the associated THDLI[x] bit to be set upon the OVRI bit transitioning to logic 1.

FULLE:

A logic 1 in this position enables the associated THDLI[x] bit to be set upon the FULLI bit transitioning to logic 1.

HDLCDATA[7:0]:

Data to be transmitted on the channel.

When the REVERSE bit is logic 0, the least significant bit (HDLCDATA[0]) is the first HDLC bit transmitted. When REVERSE is logic 1, HDLCDATA[0] is the last HDLC bit transmitted.

HDLCDATA[7:0] is write-only. Arbitrary data is returned upon an indirect read.

EOM:

The EOM bit indicates that the current byte of data is the end of the present data packet. Minimum packet size for THDL is 2 bytes. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated.

EOM is write-only. An arbitrary value is returned upon an indirect read.

LFILLI:

The LFILLI bit will transition to logic 1 when the THDL FIFO level transitions to empty or falls below the programmed LINT[6:0] value. This flag is also asserted after an overflow condition has occurred. LFILLI is cleared upon an indirect read access.

UDRI:

The UDRI bit will transition to 1 when the THDL FIFO underruns. That is, the THDL was in the process of transmitting a packet when it ran out of data to transmit. UDRI is cleared upon an indirect read access.

OVRI:

The OVRI bit will transition to 1 when the THDL FIFO overruns. That is, the THDL FIFO was already full when another data byte was written via an indirect write. OVRI is cleared upon an indirect read access.

FULLI:

The FULLI bit will transition to logic 1 when the THDL FIFO is full. FULLI is cleared upon an indirect read access.

BLFILL:

The BLFILL bit is set to logic 1 if the current FIFO fill level is below the LINT[7:0] level or is empty. This flag is also asserted after an overflow condition has occurred.

FULL:

The FULL bit reflects the current condition of the FIFO. If FULL is a logic 1, the THDL FIFO already contains 128-bytes of data and can accept no more.

EMPTY:

The status of the addressed channel's FIFO empty flag. When logic 1, the FIFO is empty. This flag is also asserted after an overflow condition has occurred. When logic 0, the FIFO contains data.

INTE:

If this bit is logic 1, the INTB output becomes asserted low if any of the THDLI[84:1] bits are logic 1.

FLGSHAREB:

The FLGSHAREB bit configures the HDLC transmittter to share the opening and closing flags between successive frames. If FLGSHAREB is logic 0, then the opening and closing flags between successive frames are shared. If FLGSHAREB is logic 1, then separate closing and opening flags are inserted between successive frames.

REVERSE:

The REVERSE bit controls the bit ordering of the HDLC data transferred from the microprocessor port. When REVERSE is logic 0, the least significant bit of the data bus (HDLCDATA[0]) is the first HDLC bit transmitted and the most significant bit (HDLCDATA[7]) is the last HDLC bit transmitted (datacom standard). When REVERSE is logic 1, HDLCDATA[0] is the last HDLC bit transmitted and HDLCDATA[7] is the first HDLC bits transmitted (telecom standard).

UTHR[6:0]:

The UTHR[6:0] bits define the FIFO fill level which will automatically cause the bytes stored in the FIFO to be transmitted. Once the fill level exceeds the UTHR[6:0] value, transmission will begin. Transmission will not stop until the last complete packet is transmitted and the FIFO fill level is below UTHR[6:0] + 1.

The value of UTHR[6:0] must always be greater than the value of LINT[6:0] unless both values are equal to 0x7F. If UTHR is 0x7F, transmission of packets only occurs upon writing an end-of-message byte to the FIFO.

LINT[6:0]:

The LINT[6:0] bits define the FIFO fill level which causes an internal interrupt (LFILLI) to be generated. Once the FIFO level decrements to empty or to a value less than LINT[6:0], the LFILLI context bit will be set to logic 1. LFILLI will cause an interrupt on INT if LFILLE is set to logic 1.

The value of LINT[6:0] must always be less than the value of UTHR[6:0] unless both values are equal to 0x00.

Register 0x0137: THDL Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R	REG10_11I	X
Bit 6	R	REGE_FI	X
Bit 5	R	REGB_C_DI	X
Bit 4	R	REG8_9_AI	X
Bit 3	W12C	THDLI[4]	X
Bit 2	W12C	THDLI[3]	X
Bit 1	W12C	THDLI[2]	X
Bit 0	W12C	THDLI[1]	X

THDLI[84:1]:

A logic 1 in these bits indicate a change of FIFO state (eg. threshold crossing, full, underflow) on the associated tributary since this register was last read. The associated SPE index is equal to the trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG8_9_AI:

This bit is a logic 1 if at least one bit in Register 0x0138, 0x0139 or 0x013A is logic 1.

REGB_C_DI:

This bit is a logic 1 if at least one bit in Register 0x013B, 0x013C or 0x013D is logic 1.

REGE_FI:

This bit is a logic 1 if at least one bit in Register 0x013E or 0x013F is logic 1.

REG10_11I:

This bit is a logic 1 if at least one bit in Register 0x0140 or 0x0141 is logic 1.

Register 0x0138: THDL Interrupt Status #2

Bit	Type	Function	Default
Bit 7	W12C	THDLI[12]	X
Bit 6	W12C	THDLI[11]	X
Bit 5	W12C	THDLI[10]	X
Bit 4	W12C	THDLI[9]	X
Bit 3	W12C	THDLI[8]	X
Bit 2	W12C	THDLI[7]	X
Bit 1	W12C	THDLI[6]	X
Bit 0	W12C	THDLI[5]	X

Register 0x0139: THDL Interrupt Status #3

Bit	Type	Function	Default
Bit 7	W12C	THDLI[20]	X
Bit 6	W12C	THDLI[19]	X
Bit 5	W12C	THDLI[18]	X
Bit 4	W12C	THDLI[17]	X
Bit 3	W12C	THDLI[16]	X
Bit 2	W12C	THDLI[15]	X
Bit 1	W12C	THDLI[14]	X
Bit 0	W12C	THDLI[13]	X

Register 0x013A: THDL Interrupt Status #4

Bit	Type	Function	Default
Bit 7	W12C	THDLI[28]	X
Bit 6	W12C	THDLI[27]	X
Bit 5	W12C	THDLI[26]	X
Bit 4	W12C	THDLI[25]	X
Bit 3	W12C	THDLI[24]	X
Bit 2	W12C	THDLI[23]	X
Bit 1	W12C	THDLI[22]	X
Bit 0	W12C	THDLI[21]	X

Register 0x013B: THDL Interrupt Status #5

Bit	Type	Function	Default
Bit 7	W12C	THDLI[36]	X
Bit 6	W12C	THDLI[35]	X
Bit 5	W12C	THDLI[34]	X
Bit 4	W12C	THDLI[33]	X
Bit 3	W12C	THDLI[32]	X
Bit 2	W12C	THDLI[31]	X
Bit 1	W12C	THDLI[30]	X
Bit 0	W12C	THDLI[29]	X

Register 0x013C: THDL Interrupt Status #6

Bit	Type	Function	Default
Bit 7	W12C	THDLI[44]	X
Bit 6	W12C	THDLI[43]	X
Bit 5	W12C	THDLI[42]	X
Bit 4	W12C	THDLI[41]	X
Bit 3	W12C	THDLI[40]	X
Bit 2	W12C	THDLI[39]	X
Bit 1	W12C	THDLI[38]	X
Bit 0	W12C	THDLI[37]	X

Register 0x013D: THDL Interrupt Status #7

Bit	Type	Function	Default
Bit 7	W12C	THDLI[52]	X
Bit 6	W12C	THDLI[51]	X
Bit 5	W12C	THDLI[50]	X
Bit 4	W12C	THDLI[49]	X
Bit 3	W12C	THDLI[48]	X
Bit 2	W12C	THDLI[47]	X
Bit 1	W12C	THDLI[46]	X
Bit 0	W12C	THDLI[45]	X

Register 0x013E: THDL Interrupt Status #8

Bit	Type	Function	Default
Bit 7	W12C	THDLI[60]	X
Bit 6	W12C	THDLI[59]	X
Bit 5	W12C	THDLI[58]	X
Bit 4	W12C	THDLI[57]	X
Bit 3	W12C	THDLI[56]	X
Bit 2	W12C	THDLI[55]	X
Bit 1	W12C	THDLI[54]	X
Bit 0	W12C	THDLI[53]	X

Register 0x013F: THDL Interrupt Status #9

Bit	Type	Function	Default
Bit 7	W12C	THDLI[68]	X
Bit 6	W12C	THDLI[67]	X
Bit 5	W12C	THDLI[66]	X
Bit 4	W12C	THDLI[65]	X
Bit 3	W12C	THDLI[64]	X
Bit 2	W12C	THDLI[63]	X
Bit 1	W12C	THDLI[62]	X
Bit 0	W12C	THDLI[61]	X

Register 0x0140: THDL Interrupt Status #10

Bit	Type	Function	Default
Bit 7	W12C	THDLI[76]	X
Bit 6	W12C	THDLI[75]	X
Bit 5	W12C	THDLI[74]	X
Bit 4	W12C	THDLI[73]	X
Bit 3	W12C	THDLI[72]	X
Bit 2	W12C	THDLI[71]	X
Bit 1	W12C	THDLI[70]	X
Bit 0	W12C	THDLI[69]	X

Register 0x0141: THDL Interrupt Status #11

Bit	Type	Function	Default
Bit 7	W12C	THDLI[84]	X
Bit 6	W12C	THDLI[83]	X
Bit 5	W12C	THDLI[82]	X
Bit 4	W12C	THDLI[81]	X
Bit 3	W12C	THDLI[80]	X
Bit 2	W12C	THDLI[79]	X
Bit 1	W12C	THDLI[78]	X
Bit 0	W12C	THDLI[77]	X

1.14 T1/E1 Signaling Extractor Registers

Register 0x0150: SIGX Indirect Status/Time-slot Address

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5	R/W	TSACCESS	0
Bit 4	R/W	TSADDR[4]	0
Bit 3	R/W	TSADDR[3]	0
Bit 2	R/W	TSADDR[2]	0
Bit 1	R/W	TSADDR[1]	0
Bit 0	R/W	TSADDR[0]	0

Writing to this register triggers a SIGX indirect channel register access.

TSADDR:

The timeslot address determines the DS0 timeslot/channel accessed when an access is initiated with TSACCESS logic 1.

For T1 tributaries, the valid range is 1 to 24. For E1 tributaries, the valid range is 0 to 31.

TSACCESS:

The timeslot indirect access control bit determines whether the per-tributary or per-timeslot data is accessed. If TSACCESS is logic 0, the per-tributary data is accessed. If TSACCESS is logic 1, the per-timeslot data is accessed with the timeslot determined by the TSADDR[4:0] bits.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the SIGX Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the SIGX Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the SIGX Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

Register 0x0151: SIGX Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 3. CADDR[4:0] is the tributary index and ranges from 1 to 28.

Registers 0x0152-0x0156: SIGX Indirect Channel Data Registers

These registers contain data read from the SIGX channel context RAM after an indirect read operation or data to be inserted into the SIGX channel context RAM in an indirect write operation.

The bits to be written to the SIGX channel context RAM, in an indirect channel write operation, must be set up in these registers before triggering the write. All five registers from 0x0152 through 0x0156 inclusive must be written prior to each indirect write with TSACCESS=0 unless one desires the same configuration as the latest indirect write. Only 0x0152 needs to be written if TSACCESS=1. The value returned by the latest indirect read has no bearing on indirect writes. Irregardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

The significance of the bits is dependent on the state of the TSACCESS bit of the SIGX Indirect Status/Time-slot Address register. If TSACCESS is logic 1, context information for the timeslot/channel identified by TSADDR[4:0] is either written or read.

TSACCESS=0:

Address	Offset							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x0152	COSS[5:1]					RAWSIG	SIGE	PCCE	XXXXX000
0x0153	COSS[13:6]								XXXXXXXX
0x0154	COSS[21:14]								XXXXXXXX
0x0155	COSS[29:22]								XXXXXXXX
0x0156	Unused						COSS[31:30]		XXXXXXXX

TSACCESS=1:

Address	Offset								
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default ('b)**
0x0152	A	B	C	D	Unused	FIX	POL	DEBE	XXXXXXXX
0x0153	Unused								XXXXXXXX
0x0154	Unused								XXXXXXXX
0x0155	Unused								XXXXXXXX
0x0156	Unused								XXXXXXXX

RAWSIG:

This bit only has effect for tributaries that have been byte synchronously mapped and shall only be set for T1 tributaries.

When RAWSIG is a logic 1, the signaling presented on the SBI DROP bus or the H-MVIP CAS bus is retrieved directly from the S-bit positions of the byte synchronous mapping format without subjecting it to debouncing or freezing. When RAWSIG is logic 0, the signaling is extracted from the demapped T1 stream.

If RAWSIG is a logic 1, the RJATBYP bit for the tributary must also be set.

The RAWSIG bit has no effect when the SYSOPT[1:0] bits are 11 (i.e. SBI with H-MVIP CAS). With this system interface configuration, only robbed bit signaling is available.

When RAWSIG is set to 1, the CAS multiframe alignment bits of the SBI structure, PP bits, will not necessarily be aligned to the multiframe pulse alignment of the SDC1FP pulse. Make sure the device connected to the TEMUX 84 can tolerate the PP bits not being aligned to the SDC1FP pulse if RAWSIG = 1 is to be used.

PCCE:

The per-timeslot configuration enable bit, PCCE, enables the configuration data to affect the signaling and PCM byte streams. If the PCCE is logic 1, the Per-Timeslot Configuration bits are enabled. Refer to the Per-timeslot Configuration descriptions for configuration bit details.

SIGE:

When logic 1, the SIGE bit enables a change of signaling state in any one of the 24 timeslots (T1 mode) or 30 timeslots for (E1 mode) to set the associated COSSI[x] bit in the Change of Signaling Status registers.

COSS[31:1]

The change of signaling state (COSS) bits will be set to logic 1 if a change of signaling state occurs on the corresponding E1 or T1 timeslot. The COSS bits are cleared upon an indirect read access. Although there are only 30 signalling timeslots for E1, the maintenance information from timeslot 16 is extracted by SIGX. Hence there are 31 COSS bits.

DEBE:

The DEBE bit enables debouncing of timeslot/channel signaling bits. A logic 1 in this bit position enables signaling debouncing while a logic 0 disables it. When debouncing is selected, per-timeslot/per-channel signaling transitions are ignored until two consecutive, equal values are sampled. Debouncing is performed on the entire signaling state.

FIX, POL:

In T1 mode, if the FIX bit is a logic 1, the signaling bit position in the PCM data stream is forced to the value of the POL bit. The substitution occurs during signaling frames only.

A,B,C,D:

This is the extracted, optionally debounced, signaling state. For the T1 SF framing format, the A and B bits are the signaling bits for every even superframe, and the C and D bits are the signaling bits every odd superframe. This presentation allows the representation of the SLC-96 nine-state signaling. The associated COSS[x] bit is set of logic 1 whenever the state of these bits changes.

Register 0x0157: SIGX Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	GPCCE	0

GPCCE:

This bit globally enables per-channel/per-timeslot functions. This global enable and the per-channel PCCE bit must be both to set to logic 1 for the POL and FIX per-timeslot bits to have any effect.

Register 0x0158: Change of Signaling Status #1

Bit	Type	Function	Default
Bit 7	R	REG11_12I	X
Bit 6	R	REGF_10I	X
Bit 5	R	REGC_D_EI	X
Bit 4	R	REG9_A_BI	X
Bit 3	R	COSSI[4]	X
Bit 2	R	COSSI[3]	X
Bit 1	R	COSSI[2]	X
Bit 0	R	COSSI[1]	X

COSSI[84:1]:

A logic 1 in these bits indicate a change of signaling state on the associated tributary since the bit was explicitly cleared. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon an indirect read of the associated SIGX Indirect Channel Data Registers.

REG9_A_BI:

This bit is a logic 1 if at least one bit in Register 0x0159, 0x015A or 0x015B is logic 1.

REGC_D_EI:

This bit is a logic 1 if at least one bit in Register 0x015C, 0x015D or 0x015E is logic 1.

REGF_10I:

This bit is a logic 1 if at least one bit in Register 0x015F or 0x0160 is logic 1.

REG11_12I:

This bit is a logic 1 if at least one bit in Register 0x0161 or 0x0162 is logic 1.

Register 0x0159: Change of Signaling Status #2

Bit	Type	Function	Default
Bit 7	R	COSSI[12]	X
Bit 6	R	COSSI[11]	X
Bit 5	R	COSSI[10]	X
Bit 4	R	COSSI[9]	X
Bit 3	R	COSSI[8]	X
Bit 2	R	COSSI[7]	X
Bit 1	R	COSSI[6]	X
Bit 0	R	COSSI[5]	X

Register 0x015A: Change of Signaling Status #3

Bit	Type	Function	Default
Bit 7	R	COSSI[20]	X
Bit 6	R	COSSI[19]	X
Bit 5	R	COSSI[18]	X
Bit 4	R	COSSI[17]	X
Bit 3	R	COSSI[16]	X
Bit 2	R	COSSI[15]	X
Bit 1	R	COSSI[14]	X
Bit 0	R	COSSI[13]	X

Register 0x015B: Change of Signaling Status #4

Bit	Type	Function	Default
Bit 7	R	COSSI[28]	X
Bit 6	R	COSSI[27]	X
Bit 5	R	COSSI[26]	X
Bit 4	R	COSSI[25]	X
Bit 3	R	COSSI[24]	X
Bit 2	R	COSSI[23]	X
Bit 1	R	COSSI[22]	X
Bit 0	R	COSSI[21]	X

Register 0x015C: Change of Signaling Status #5

Bit	Type	Function	Default
Bit 7	R	COSSI[36]	X
Bit 6	R	COSSI[35]	X
Bit 5	R	COSSI[34]	X
Bit 4	R	COSSI[33]	X
Bit 3	R	COSSI[32]	X
Bit 2	R	COSSI[31]	X
Bit 1	R	COSSI[30]	X
Bit 0	R	COSSI[29]	X

Register 0x015D: Change of Signaling Status #6

Bit	Type	Function	Default
Bit 7	R	COSSI[44]	X
Bit 6	R	COSSI[43]	X
Bit 5	R	COSSI[42]	X
Bit 4	R	COSSI[41]	X
Bit 3	R	COSSI[40]	X
Bit 2	R	COSSI[39]	X
Bit 1	R	COSSI[38]	X
Bit 0	R	COSSI[37]	X

Register 0x015E: Change of Signaling Status #7

Bit	Type	Function	Default
Bit 7	R	COSSI[52]	X
Bit 6	R	COSSI[51]	X
Bit 5	R	COSSI[50]	X
Bit 4	R	COSSI[49]	X
Bit 3	R	COSSI[48]	X
Bit 2	R	COSSI[47]	X
Bit 1	R	COSSI[46]	X
Bit 0	R	COSSI[45]	X

Register 0x015F: Change of Signaling Status #8

Bit	Type	Function	Default
Bit 7	R	COSSI[60]	X
Bit 6	R	COSSI[59]	X
Bit 5	R	COSSI[58]	X
Bit 4	R	COSSI[57]	X
Bit 3	R	COSSI[56]	X
Bit 2	R	COSSI[55]	X
Bit 1	R	COSSI[54]	X
Bit 0	R	COSSI[53]	X

Register 0x0160: Change of Signaling Status #9

Bit	Type	Function	Default
Bit 7	R	COSSI[68]	X
Bit 6	R	COSSI[67]	X
Bit 5	R	COSSI[66]	X
Bit 4	R	COSSI[65]	X
Bit 3	R	COSSI[64]	X
Bit 2	R	COSSI[63]	X
Bit 1	R	COSSI[62]	X
Bit 0	R	COSSI[61]	X

Register 0x0161: Change of Signaling Status #10

Bit	Type	Function	Default
Bit 7	R	COSSI[76]	X
Bit 6	R	COSSI[75]	X
Bit 5	R	COSSI[74]	X
Bit 4	R	COSSI[73]	X
Bit 3	R	COSSI[72]	X
Bit 2	R	COSSI[71]	X
Bit 1	R	COSSI[70]	X
Bit 0	R	COSSI[69]	X

Register 0x0162: Change of Signaling Status #11

Bit	Type	Function	Default
Bit 7	R	COSSI[84]	X
Bit 6	R	COSSI[83]	X
Bit 5	R	COSSI[82]	X
Bit 4	R	COSSI[81]	X
Bit 3	R	COSSI[80]	X
Bit 2	R	COSSI[79]	X
Bit 1	R	COSSI[78]	X
Bit 0	R	COSSI[77]	X

Register 0x0163: Change of Signaling Status Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	COSSE	0

COSSE:

If this bit is a logic 1, the SIGX bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the COSSI[84:1] bits is a logic 1.

1.15 T1/E1 Transmitter Registers

Register 0x0168: T1/E1 Transmitter Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Writing to this register triggers an indirect channel register access.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the T1/E1 Transmitter channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the T1/E1 Transmitter Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the T1/E1 Transmitter Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the T1/E1 Transmitter Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

When the T1/E1 Transmitter (TRAN) blocks come out of reset, time is needed for its RAM to get fully initialized. After a reset of the TEMUX 84, each block of indirect RAM will initialize.

During the RAM initialization of the T1/E1 TRAN indirect RAM, the CBUSY bit of Register 0x0168 will NOT be logic '1'. Indirect accesses initiated by writing the T1/E1 Transmitter Indirect Status Register (0x0168) will appear to be permitted but any indirect access to the TRAN indirect RAM during the RAM initialization will not be successful.

The time required for the TRAN RAM initialization to complete is 26.39us (513 19.44MHz SREFCLK cycles or 2052 77.76MHz SREFCLK cycles) after the device comes out of reset. Indirect accesses to the TRAN RAM during this time should not be attempted, as they will not be successful.

Register 0x0169: T1/E1 Transmitter Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the T1/E1 Transmitter channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 3. CADDR[4:0] is the tributary index and ranges from 1 to 28.

Registers 0x016A-0x016F: T1/E1 Transmitter Indirect Channel Data Registers

These registers contain data read from the channel context RAM after an indirect read operation or data to be inserted into the channel context RAM in an indirect write operation.

The bits to be written to the channel context RAM, in an indirect channel write operation, must be set up in these registers before triggering the write. All six registers from 0x016A through 0x016F inclusive must be written prior to each indirect write unless one desires the same configuration as the latest indirect write. The value returned by the latest indirect read has no bearing on indirect writes. Irregardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

The significance of the bits is dependent on the state of the associated E1/T1B bits in the SPE Configuration registers. If The E1/T1B bit associated with a tributary is logic 1, the E1 bit descriptions hold; otherwise, the T1 bit descriptions are valid.

T1 Bit Map:

Address	Offset								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (‘b)
0x016A	FDIS	XAIS	XYEL	CCSEN	JPN	FMS[1:0]		ESF	00000000
0x016B	IBC[4:0]					IBCL[1:0]		XIBC	00000000
0x016C	BC[3:0]				XBOC	IBC[7:5]			00000000
0x016D	Unused			AISCI	RAICI	T1_FDL_DIS	BC[5:4]		XXXXX000
0x016E	Unused	DL_TS[4:0]					DL_ODD	DL_EVEN	00000000
0x016F	DL_EN[7:0]								00000000

E1 Bit Map:

Address	Offset								
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default ('b)**
0x016A	XDIS	CASDIS	TS16AIS	FEBEDIS	GENCRC	INDIS	FDIS	AIS	00000000
0x016B	SPATINV	SPLRINV	FPATINV	RMA	RAI	CCS31EN	CCS15EN	CCS16EN	00000000
0x016C	SaX[4]	SaX_EN[1:4]				SaSEL[2:0]			00000000
0x016D	X[4]	X[3]	X[1]	Si[1:0]		SaX[1:3]			00000000
0x016E	DL_EN [0]	DL_TS[4:0]					DL_ODD	DL_ EVEN	00000000
0x016F	Unusd	DL_EN[7:1]							00000000

T1 Bit Descriptions:

ESF:

A logic 0 selects the SF frame format. A logic 1 selects the ESF frame format.

FMS[1:0]:

These bits determine the format of the facility datalink:

ESF	FMS[1:0]	Facility Datalink
0	00	No datalink; standard SF
0	01	Reserved
0	10	Reserved
0	10	Reserved
1	00	4 kbit/s data link
1	01	2 kbit/s data link (frames 3, 7, 11, 15, 19, 23)
1	10	2 kbit/s data link (frames 1, 5, 9, 13, 17, 21)
1	11	4 kbit/s data link

JPN:

The JPN bit enables Japanese variations of the standard framing formats. If the JPN bit is a logic 1 and the ESF format is selected (ESF bit is logic 1), the F-bits are included in the CRC-6 calculation, instead of replacing them with ones. If the JPN bit is a logic 1 and the SF format is selected, the framing bit of frame 12 is forced to logic 1 when a Yellow alarm is declared. Otherwise, bit 2 in all of the channels is forced to logic 0 to indicate Yellow alarm.

Framing insertion must be enabled (the FDIS bit must be logic 0) in order to transmit the alternate SF Yellow alarm.

CCSEN:

If this bit is logic 1, Channel 24 data is taken from the CCSED[1] input; otherwise, it is derived from the PCM data stream.

This bit must be set to a 0 when using the unframed tributary type with the SBI bus.

XYEL:

The XYEL bit controls the transmission of the Yellow Alarm signal (a.k.a. RAI). In SF mode, a logic 1 in the XYEL bit causes bit 2 of all channels to be forced to logic 0. If forcing bit 2 would otherwise result in all zeros in a channel, bit 7 is forced to logic 1. In Japanese SF mode, a logic 1 in the XYEL bit causes the F-bit of the twelth frame of the superframe to be forced to logic 1. In ESF mode, a logic 1 in the XYEL bit causes the pattern “0000000011111111” to be repeated in the facility datalink.

If the AUTOYELLOW T1/E1 Framer context bit is a logic 1, a Yellow Alarm is also inserted if the T1/E1 Framer is out-of-frame.

XAIS:

The active high transmit alarm indication (XAIS) signal is used to initiate transmission of an alarm indication signal (all ones).

XAIS supercedes all other configuration bits.

FDIS:

The framing disable (FDIS) bit is used to disable framing of the PCM data stream. When FDIS is logic 0, PCM data is framed; when FDIS is logic 1, insertion of framing into the F-bit position is disabled. Setting this bit allows transmission of unframed Inband Loopback Codes.

This bit must be set to a 1 when using the unframed tributary type with the SBI bus.

XIBC:

The transmit inband code (XIBC) bit is used to enable the transmission of inband codes. When XIBC is logic 1, the repetitive code defined by the IBC[7:0] bits occupies the entire data stream except the F-bit position if FDIS

is logic 0. If FDIS is logic 0, the framing bits simply supercede the inband code bits.

IBCL[1:0]:

The inband code length indicates the length of the inband loopback code sequence, as follows:

IBCL[1:0]	Code Length
00	5
01	6
10	7
11	8

Codes of three or four bits in length may be accommodated by treating them as half of a double-sized code.

IBC[7:0]:

Bits IBC[7:0] contain the inband loopback code pattern to be transmitted. Since IBC[7] is the first bit transmitted, followed by IBC[6], the code should always be aligned with the MSB in the Bit 7 position (for example, a 5-bit code would occupy positions Bit 7 through Bit 2). Note that 3 or 4-bit patterns must be paired to form a double-sized code (for example, the 3-bit code ‘011' would be entered as the 6-bit code '011011').

XBOC:

The XBOC bit enables the transmission of bit oriented codes (BOCs) in the facility datalink. If XBOC is logic 1, the sixteen bit sequence of 8 ones, 1 zero, BC[0] to BC[5], and 1 trailing zero is repeated in the facility datalink if the ESF bit is logic 1. XBOC has no effect if ESF is logic 0 or FDIS is logic 1. The XYEL bit takes precedence in that it forces transmission of a “1111111100000000” BOC.

BC[5:0]:

These bits select the 6-bit BOC to be transmitted. To enable these bits to be transmitted as a BOC, the XBOC bit must be logic 1. BC[0] is the first bit transmitted.

The latest code is transmitted at least 10 times. If a second code is written before ten repetitions of the first have been transmitted, the second code will be transmitted immediately after the tenth transmission of the first code. If a third consecutive code is desired, its write must be delayed until the

transmission of the second code has started, lest the third code over write the second.

RAICI:

When this bit is logic 1 and the selected frame format is ESF, the RAI-CI alarm is transmitted in the facility data link. RAI-CI is a repetitive pattern within the ESF data link with a period of 1.08 seconds. It consists of sequentially interleaving 0.99 seconds of 00000000 11111111 (right-to-left) with 90 ms of 00111110 11111111.

AISCI:

When this bit is a logic 1, AIS-CI is transmitted. AIS-CI is a repetitive pattern of 1.26 seconds. It consists of 1.11 seconds of an unframed all ones pattern and 0.15 seconds of all ones modified by the AIS-CI signature. The AIS-CI signature is a repetitive pattern 6176 bits in length in which, if the first bit is numbered bit 0, bits 3088, 3474 and 5790 are logical zeros and all other bits in the pattern are logical ones.

T1_FDL_DIS:

The T1 data link disable bit allows the generation of the ESF data links when in T1 mode. If T1_FDL_DIS is a logic 0, the ESF and FMS[1:0] context bits determine the bit locations into which the data link is inserted. When the T1_FDL_DIS bit is a logic 0, the values of the DL_CH[4:0], DL_EVEN and DL_ODD bits are irrelevant. When T1_FDL_DIS is logic 1, the value transmitted in the Facility Data Link bit positions is that received from the system interface.

DL_EVEN:

DL_EVEN controls whether or not the data link is inserted into even numbered frames. If DL_EVEN is a logic 1, then the data link is inserted into even numbered frames. If DL_EVEN is a logic 0, then the data link is not inserted into even numbered frames. For T1 tributaries, the frames in a superframe are considered to be numbered from 1 to 12 or 24.

DL_ODD:

DL_ODD controls whether or not the data link is inserted into odd numbered frames. If DL_ODD is a logic 1, then the data link is inserted into odd numbered frames. If DL_ODD is a logic 0, then the data link is not inserted into odd numbered frames. For T1 tributaries, the frames in a superframe are considered to be numbered from 1 to 12 or 24.

DL_TS[4:0]:

DL_TS gives a binary representation of the time slot into which the data link is to be inserted. Note that T1 channels 1 to 24 are mapped to values 0 to 23. The DL_TS[4:0] bits have no effect when DL_EVEN and DL_ODD are both a logic 0.

DL_EN[7:0]:

DL_EN controls which bits of the time slot indicated by DL_TS are to be written with the data link. If DL_EN[X] is a logic 1, then the data link will be inserted into bit X, with bit 7 being the first transmitted.. To insert the data link into the entire time slot, all eight DL_EN bits must be a logic 1.

E1 Bit Descriptions:

AIS:

AIS controls the transmission of the alarm indication signal (unframed all-ones). When AIS is a logic 1 the transmit data is forced to all ones. The AIS will be looped back if a diagnostic loopback is enabled.

FDIS:

FDIS controls the generation of the framing alignment signal. When FDIS is a logic 1, generation of the framing pattern in TS0 is disabled. When FDIS is a logic 0, generation of the framing pattern in TS0 is enabled; the contents of TS0 is determined by the INDIS, GENCRC, FEBEDIS, SaSEL[1:4], SaEN[1:4], SaX[1:4], and Si[1:0] bits.

This bit must be set to a 1 when using the unframed tributary type with the SBI bus.

INDIS:

INDIS controls the insertion of the international and national bits into TS0. When INDIS is set to logic 0, the international and national bits are inserted. The bit values used for the international bits are dependent upon the GENCRC, FEBEDIS, and Si[1:0] context bits. The bit values used for the national bits are dependent upon SaSEL[2:0], Sax_EN[1:4], and SaX[1:4]. When INDIS is a logic 1, the international and national bits are taken directly from the system interface.

GENCRC:

GENCRC controls the generation of the CRC multiframe bits. When GENCRC is a logic 1, the CRC multiframe alignment signal is generated. The

CRC bits are calculated and inserted, and the E bits are inserted according to FEBEDIS. The CRC bits transmitted during the first sub-multiframe (SMF) are indeterminate and should be ignored. The CRC bits calculated during the transmission of the nth SMF (SMF n) are transmitted in the following SMF (SMF n+1). When GENCRC is a logic 0, CRC insertion is disabled. The international bitsof FAS frames are set to Si[1] and the international bit of NFAS frames are set to Si[0].

FEBEDIS:

FEBEDIS controls the ‘E’ bits of a multiframe. If FEBEDIS is logic 1, the ‘E’ bits are encoded with the contents of the Si[1:0] context bits. If FEBEDIS is logic 0, each ‘E’ bit is encoded with a 0 when a FEBE is to be transmitted and a 1 when a FEBE is not to be transmitted.

TS16AIS:

TS16AIS controls the transmission of the TS16 alarm indication signal. When TS16AIS is a logic 1, TS16 of all frames is forced to all-ones.

CASDIS:

CASDIS controls the generation of the channel associated signaling multiframe formatting. When CASDIS is a logic 0, the CAS framing overhead is inserted into TS16 of frame 0. When CASDIS is a logic 1, the CAS framing overhead is not inserted.

This bit must be set to a 1 for unframed data.

XDIS:

XDIS controls the insertion of the extra bits in TS16 of frame 0 of the signaling multiframe as follows. When XDIS is set to a logic 0, the contents of the X[1], X[3] and X[4] context bits are inserted into TS16, frame 0. When XDIS is a logic 1, the values for those bits positions are taken from the system interface.

CCS16EN:

CCS16EN controls the insertion of Common Channel Signaling (CCS) into TS16. When CCS16EN is a logic 1, TS16 CCS is enabled. TS16 data is taken directly from the CCSED[1] input. When CCS16EN is a logic 0, TS16 CCS is disabled.

CCS15EN:

CCS15EN controls the insertion of CCS into TS15. When CCS15EN is a logic 1, TS15 CCS is enabled. TS15 data is taken directly from the CCSED[2] input. When CCS15EN is a logic 0, TS15 CCS is disabled.

CCS31EN:

CCS31EN controls the insertion of CCS into TS31. When CCS31EN is a logic 1, TS31 CCS is enabled. TS31 data is taken directly from the CCSED[3] input. When CCS31EN is a logic 0, TS31 CCS is disabled.

RAI:

RAI controls the transmission of the remote alarm indication. A logic 1 in the RAI bit position causes bit 3 of NFAS frames to be forced to logic 1. Logic 0 in the RAI bit position causes the transmission of the RAI to be controlled exclusively by the AUTOYELLOW T1/E1 Framer context bit and the alarm state of the framer.

If the AUTOYELLOW T1/E1 Framer context bit is a logic 1, RAI is also inserted if the T1/E1 Framer is out-of-frame or AIS has been declared.

RMA:

RMA controls the transmission of the signaling multiframe remote alarm indication. A logic 1 in the RMA bit position causes the y-bit (bit 6) of TS16 of frame 0 of the signaling multiframe to be forced to logic 1. Logic 0 in the RMA bit position causes the transmission of the signaling multiframe remote alarm to be controlled exclusively by the AUTOYELLOW T1/E1 Framer context bit and the alarm state of the framer..

If the AUTOYELLOW T1/E1 Framer context bit is a logic 1, multiframe remote alarm is also inserted if the T1/E1 Framer is out-of-frame.

FPATINV:

FPATINV is a diagnostic control bit. When set to logic 1, FPATINV forces the frame alignment signal (FAS) written into TS0 to be inverted (i.e., the correct FAS, 0011011, is substituted with 1100100); when set to logic 0, the FAS is unchanged.

SPLRINV:

SPLRINV is a diagnostic control bit. When set to logic 1, SPLRINV forces the "spoiler bit" written into bit 2 of TS0 of NFAS frames to be inverted (i.e., the spoiler bit is forced to 0); when set to logic 0, the spoiler bit is unchanged.

SPATINV:

SPATINV is a diagnostic control bit. When set to logic 1, SPATINV forces the signaling multiframe alignment signal written into bits 1-4 of TS16 of frame 0 of the signaling multiframe to be inverted (i.e., the correct signaling multiframe alignment signal 0000 is substituted with 1111); when set to logic 0, the signaling multiframe alignment signal is unchanged.

The SPATINV still has effect if the CASDIS bit is logic 1. In this case, four TS16 bits are inverted every 16 frames.

SaSEL[2:0]:

SaSEL[2:0] selects which national bit codeword is present in the SaX[1:4] bits. These bits map to the codeword selection as follows:

SaSEL[2:0]	National Bit Codeword
000	Undefined
001	Undefined
010	Undefined
011	Sa4
100	Sa5
101	Sa6
110	Sa7
111	Sa8

SaX_EN[1:4]:

SaX_EN[1:4] enables the bits SaX[1:4] (where X = 4, 5, 6, 7 or 8) respectively. If bits SaX_EN[1: 4] are set to logic 1, then the contents of bits SaX[1:4] are substituted into bit X of TS0 of NFAS frames 1, 3, 5, and 7 of SMF I, or into NFAS frames 9, 11, 13, and 15 of SMF II. If any one or more of the SaX_EN[1:4] bits are set to logic 0, the respective SaX[1:4] register bit is disabled and will not be written into the G.704 CRC multiframe (i.e. the SaX bit that has been disabled will pass through transparently).

SaX[1:4]:

The code word SaX[1:4], (where X = 4, 5, 6, 7, or 8) appears in bit X of TS0 in frames 1, 3, 5 and 7 respectively (SMF I) and in frames 9, 11, 13 and 15 respectively (SMF II) of a G.704 CRC-4 multiframe. If X = 4, the Sa4[1:4] bits appear in bit 4 of frames 1, 3, 5, and 7 respectively (SMF I) and in bit 4 of frames 9, 11, 13, and 15 respectively (SMF II) of a G.704 CRC-4 multiframe. If X = 8, the codeword is inserted into bit 8 of TS 0 in frames 1, 3, 5 and 7 respectively (SMF I), and in frames 9, 11, 13 and 15 respectively (SMF II) of a

G.704 CRC-4 multiframe.

The code word written in bits SaX[1:4] is latched internally and is updated every sub-multiframe. Therefore, if the code word is written during SMF I of a G.704 CRC-4 multiframe, it will appear in the SaX[1:4] bits of SMF II of the same multiframe. If the code word is written during SMF II of a multiframe, its contents will be latched internally and will appear in SMF I of the next multiframe.

Si[1:0]:

Si[1] and Si[0] correspond to the international bits and can be programmed to any value. When GENCRC = 0, Si[1] is inserted into bit 1 of TS0 of FAS frames and Si[0] is inserted into bit 1 of TS0 of NFAS frames. When GENCRC is logic 1 and FEBEDIS of logic 1, Si[1] will be inserted into the E bit position of frame 13 and Si[0] will be inserted into the E bit position of frame 15.

The Si[1] and Si[0], bits should be programmed to a logic 1 when not being used to carry information.

X[1], X[3], X[4]:

X[1], X[3], and X[4] control the value programmed in the X[1], X[3], and X[4] bit locations (bits 5, 7, and 8) in TS16 of frame 0 of the signaling multiframe. X[1], X[3], and X[4] should be programmed to a logic 1 when not being used to carry information.

DL_EVEN:

DL_EVEN controls whether or not the data link is inserted into even numbered frames. If DL_EVEN is a logic 1, then the data link is inserted into even numbered frames. If DL_EVEN is a logic 0, then the data link is not inserted into even numbered frames. For E1 tributaries, the frames in an E1 CRC-4 multiframe are considered to be numbered from 0 to 15.

DL_ODD:

DL_ODD controls whether or not the data link is inserted into odd numbered frames. If DL_ODD is a logic 1, then the data link is inserted into odd numbered frames. If DL_ODD is a logic 0, then the data link is not inserted into odd numbered frames. For E1 tributaries, the frames in an E1 CRC-4 multiframe are considered to be numbered from 0 to 15.

DL_TS[4:0]:

DL_TS gives a binary representation of the time slot into which the data link is to be inserted. The DL_TS[4:0] bits have no effect when DL_EVEN and DL_ODD are both a logic 0.

DL_EN[7:0]:

DL_EN controls which bits of the time slot indicated by DL_TS are to be written with the data link. If DL_EN[X] is a logic 1, then the data link will be inserted into bit X, with bit 7 being the first transmitted. To insert the data link into the entire time slot, all eight DL_EN bits must be a logic 1.

1.16 T1/E1 Framer Registers

Register 0x0170: T1/E1 Framer Indirect Status

Bit	Type	Function	Default
Bit 7	R	CBUSY	X
Bit 6	R/W	CRWB	0
Bit 5	R/W	DIS_R2C	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Writing to this register triggers an indirect T1/E1 Framer channel register access.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the T1/E1 Framer channel context RAM. Writing a logic 0 to CRWB triggers an indirect write operation. Data to be written is taken from the T1/E1 Framer Indirect Channel Data registers. Writing a logic 1 to CRWB triggers an indirect read operation. The read data can be found in the T1/E1 Framer Indirect Channel Data registers.

CBUSY:

The indirect channel access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set to logic 1 when a write to this register triggers an indirect access and will remain logic 1 until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the T1/E1 Framer Indirect Channel Data registers or to determine when a new indirect write operation may commence. The CBUSY is not expected to remain at logic 1 for more than 86 SREFCLK cycles. The mean duration for CBUSY asserted shall be less than 9 SREFCLK cycles.

DIS_R2C:

The disable read-to-clear bit (DIS_R2C) allows the clearing of interrupt status bits to be suppressed upon an indirect read access. Writing a logic 0 to DIS_R2C indicates that the indirect read access will cause a clear of the channel interrupt status bits. Writing a logic 1 indicates that as a result of the indirect read access the interrupts will not be cleared. The DIS_R2C has no effect on an indirect write access.

Register 0x0171: T1/E1 Framer Indirect Channel Address Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CADDR[6]	0
Bit 5	R/W	CADDR[5]	0
Bit 4	R/W	CADDR[4]	0
Bit 3	R/W	CADDR[3]	0
Bit 2	R/W	CADDR[2]	0
Bit 1	R/W	CADDR[1]	0
Bit 0	R/W	CADDR[0]	0

This register provides the channel address number used to access the T1/E1 Framer channel context RAM.

CADDR[6:0]:

The indirect channel address number (CADDR [6:0]) indicates the channel to be configured or interrogated in the indirect channel access.

CADDR[6:5] is the SPE index and ranges from 1 to 3. CADDR[4:0] is the tributary index and ranges from 1 to 28.

Register 0x0172 – 0x0186: T1/E1 Framer Indirect Channel Data Registers

These registers contain data read from the channel context RAM after an indirect read operation or data to be inserted into the channel context RAM in an indirect write operation.

The bits to be written to the T1/E1 Framer channel context RAM in an indirect channel write operation must be set up in these registers before triggering the write. All twelve registers from 0x0172 through 0x017B inclusive must be written prior to each indirect write unless one desires the same configuration as the latest indirect write. The value returned by the latest indirect read has no bearing on indirect writes. Irregardless of writes to these registers, reads will always return the data retrieved by the latest indirect read operation. Although the indirect reads and writes share the same register space, they are independent of each other.

T1 Bit Map:

Address	Offset								
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default ('b)**
0x0172	DL_ODD	DL_EVEN	T1_FDL _DIS	DL_CH[4:0]					00000000
0x0173	DL_BIT[7:0]								00000000
0x0174	FASTD	M2O[1:0]		ESFFA	ESF	FMS[1:0]		JPN	00000000
0x0175	LBACT[5:0]						LBASEL[1:0]		00000000
0x0176	LBDACT[3:0]				LBDSEL[1:0]		LBACT[7:6]		00000000
0x0177	BOCE	CR	PRMEN	CCOFA	LBDACT[7:4]				00000000
0x0178	REDE	YELE	COFAE	FERE	BEEE	SEFE	INFE	IDLE	00000000
0x0179	TRKEN	RAIS	OFFLINE	LBDE	LBAE	AISCIE	RAICIE	AISE	00000000
0x017A	DISFREZ	Unused	Unused	IOOFEN	IREDEN	AUTO OOF	AUTORED	AUTO YELLOW	00000000
0x017B	ALMDE	CONNOUT[6:0]							00000000
0x017C	LBA	AISCI	RAICI	AIS	RED	YEL	INF	OVR	00000000
0x017D	REDI	YELI	COFAI	FERI	BEEI	SEFI	INFI	LBD	00000000

0x017E	BOC[0]	LBDI	LBAI	BOCI	IDLEI	AISCII	RAICII	AISI	00000000
0x017F	BEE[2:0]			BOC[5:1]					00000000
0x0180	FER[1:0]		BEE[8:3]						00000000
0x0181	AISD	Unused	OOF[2:0]			FER[4:2]			00000000
0x0182	Unused								00000000
0x0183	Unused								00000000
0x0184	Unused								00000000
0x0185	AISDI	YELD	LBDD	LBAD	Unused				00000000
0x0186	Unused					YELDI	LBDDI	LBADI	00000000

E1 Bit Map:

Address	Offset								
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default ('b)**
0x0172	DL_BIT [0]	DL_ODD	DL_ EVEN	DL_TS[4:0]					00000000
0x0173	UN FRAMED	DL_BIT[7:1]							00000000
0x0174	SMFASC	BIT2C	REFRDIS	REF CRCEN	REFR	C2NC IWCK	CASDIS	CRCEN	00000000
0x0175	CNT NFAS	OOSMF AIS	SaSEL[2:0]			AISC	RAIC	TS16C	00000000
0x0176	SMFERE	FERE	COFAE	INCMFE	INSMFE	INFE	C2NC IWE	WORD ERR	00000000
0x0177	FEBEE	TS16 AISDE	AISE	REDE	AISDE	RMAIE	RAIE	CMFERE	00000000
0x0178	ICMFPE	ICSMFPE	IFPE	V52 LINKE	CFEBEE	RAIC CRCE	OOOFE	CRCEE	00000000
0x0179	RAIS	OFFLINE	Sa8E	Sa7E	Sa6E	Sa5E	Sa4E	ISMFPE	00000000
0x017A	G706AN NBRAI	OOCMF E0	IOOFEN	IREDEN	AUTO OOF	AUTO RED	AUTO YELLOW	TRKEN	00000000
0x017B	CONNOUT[6:0]							DISFREZ	00000000
0x017C	CMFERI	SMFERI	FERI	COFAI	INCMFI	INSMFI	INFI	C2NCIWI	00000000

0x017D	CRCEI	FEBEI	TS16 AISDI	AISI	REDI	AISDI	RMAII	RAII	00000000
0x017E	ISMFPI	ICMFPI	ICSMFPI	IFPI	V52 LINKI	CFEBEI	RAIC CRCI	OOOFI	00000000
0x017F	INSMF	INF	C2NCIW	Sa8I	Sa7I	Sa6I	Sa5I	Sa4I	00000000
0x0180	AISD	RMAI	RAI	V52LINK	CFEBE	RAIC CRC	OOOF	INCMF	00000000
0x0181	Sa[5:4]		A	Si[2:1]		TS16 AISD	AIS	RED	00000000
0x0182	EXCRC ERR	X[3]	Y	X[1]	X[0]	Sa[8:6]			00000000
0x0183	CRCERR[2:0]			OVR	SaX[4:1]				00000000
0x0184	FER[0]	CRCERR[9:3]							00000000
0x0185	FEBE[1:0]		FER[6:1]						00000000
0x0186	FEBE[9:2]								00000000

OFFLINE:

When a logic 1, the OFFLINE bit suppresses frame realignments at the system interface such that the data is carried clear channel. The frame still attempts to find frame, extract a HDLC datalink, accumulate performance data and to maintain alarm status. This is in contrast with the unframed modes where all maintenance activity is suppressed.

Note that this bit has no effect for Mapper/Multiplexer mode (i.e. OPMODE_SPEx = 001) because the framer is unconditionally already off line.

For byte synchronously mapped T1 tributaries, setting OFFLINE to logic 1 is usually optimal. For byte synchronously mapped E1 tributaries, OFFLINE must be set to logic 0 if channel associated signaling is being transported. The E1 byte synchronous mapping does not preserve multiframe alignment, so signaling multiframe alignment must be re-established before signaling may be extracted correctly.

RAIS:

When a logic 1, the RAIS bit forces all ones into the ingress data stream. The current signaling will be frozen if DISFREZ is logic 0.

TRKEN:

The TRKEN bit enables receive trunk conditioning upon an out-of-frame condition. If TRKEN is logic 1, the contents of the RX-ELST Idle Code register are inserted into all time slots (including TS0 and TS16) of the ingress data when the framer is out-of-basic frame (i.e. the INF context bit is logic 0). The TRKEN bit has no effect in SBI async mode since the receive elastic store is bypassed in this mode. If TRKEN is a logic 0, receive trunk conditioning can still be performed on a per-timeslot basis via the RPCC MSTRK and MDTRK context bits.

AUTOYELLOW:

In T1 mode, when the AUTOYELLOW bit is set to logic 1, whenever the alarm integrator declares a Red alarm in the receive direction, Yellow alarm will be transmitted to the far end. When AUTOYELLOW is set to logic 0, Yellow alarm will only be transmitted when the XYEL bit of T1/E1 Transmitter bit is set. Note that the Red alarm is not deasserted on detection of AIS.

In E1 mode, when the AUTOYELLOW bit is set to logic 1, the RAI bit in the transmit stream is set to a logic 1 for the duration of a loss of frame alignment or AIS, and the Remote Multiframe Alarm bit (a.ka. 'Y' bit) in the transmit stream is set to a logic 1 for the duration of a loss of signaling multiframe alignment. The G706ANNBRAI bit optionally also allows for the transmission of RAI when CRC-to-non-CRC interworking has been established. When AUTOYELLOW is set to logic 0, RAI will only be transmitted when the RAI bit of T1/E1 Transmitter bit is set and RMA will only be transmitted when the RMA bit of T1/E1 Transmitter bit is set.

AUTORED:

The AUTORED bit allows global trunk conditioning to be applied to the ingress data and signaling streams immediately upon declaration of Red carrier failure alarm. When AUTORED is set to logic 1, the ingress data and signaling for each channel is replaced with the data programmed into the IDLE[7:0] and A'B'C'D' fields of the Receive Per-Channel Controller (RPCC) while Red CFA is declared. When AUTORED is set to logic 0, the ingress data is not automatically conditioned when Red CFA is declared.

AUTOOOF:

The AUTOOOF bit allows global trunk conditioning to be applied to the ingress data stream immediately upon declaration of out of frame (OOF). When AUTOOOF is set to logic 1, while OOF is declared, the ingress data on each channel is replaced with the data programmed into the IDLE[7:0] and

A'B'C'D' fields of the Receive Per-Channel Controllers (RPCC-SBI and RPCC-MVIP). When AUTOOOF is set to logic 0, the ingress data is not automatically conditioned by RPCC when OOF is declared. However, if the RX-ELST is not bypassed, the RX-ELST trouble code will still be inserted in channel data while OOF is declared if the TRKEN register bit is logic 1. Note that RPCC data and signaling trunk conditioning overwrites the RX-ELST trouble code.

IREDEN:

The IREDEN bit enables a received RED alarm to generate an ingress alarm indication onto the SBI bus. When IREDEN is a logic 1, a received RED alarm will force an alarm indication onto the SBI bus. When IREDEN is a logic 0, a received RED alarm will not force an alarm indication onto the SBI bus.

IOOFEN:

The IOOFEN bit enables a received Out Of Frame condition to generate an ingress alarm indication onto the SBI bus. When IOOFEN is a logic 1, an out of frame condition will force an alarm indication onto the SBI bus. When IOOFEN is a logic 0, a received out of frame will not force an alarm indication onto the SBI bus.

OOCMFE0:

When in E1 mode, the OOCMFE0 bit selects between two modes of operation concerning the transmission of E-bits when the E1 framer is out of CRC-4 multiframe. When OOCMFE0 is logic 0, the E1 framer transmits ones for the E-bits while out of CRC-4 multiframe. When OOCMFE0 is logic 1, the E1 framer transmits zeroes for the E-bits while out of CRC-4 multiframe. The option to transmit zeroes as E-bits while out of CRC-4 multiframe is provided to allow compliance with the CRC-4 to non-CRC-4 interworking procedure in Annex B of G.706.

This bit only has effect in E1 mode.

G706ANNBRAI:

When in E1 mode, the G.706 Annex B RAI bit, G706ANNBRAI, selects between two modes of operation concerning the transmission of RAI when the E1 framer is out of CRC-4 multiframe. When G706ANNBRAI is logic 1, the behavior of RAI follows Annex B of G.706, i.e., RAI is transmitted only when out of basic frame, not when CRC-4-to-non-CRC-4 interworking is declared, nor when the offline framer is out of frame. When G706ANNBRAI is logic 0, the behavior of RAI follows ETSI standards, i.e., RAI is transmitted

when out of basic frame, when CRC-4-to-non-CRC-4 interworking is declared, and when the offline framer is out of frame.

This bit only has effect in E1 mode.

DISFREZ

A logic 1 in this bit location will disables signal freezing that normally occurs upon an out-of-frame condition.

CONNOUT[6:0]

If the XCONNEN bit of the T1/E1 Framer Configuration and Status register is logic 1, the CONNOUT[6:0] indicates the SBI SPE/tributary or H-MVIP line/timeslot to which the ingress T1/E1 stream will be connected.. If XCONNEN is logic 0, these bits are ignored and tributaries remain indexed as they were demultiplexed or demapped.

CONNOUT[6:0] stipulates the SPE and tributary within the SPE. The binary value of CONNOUT[6:5] gives the SPE number and has a valid range of 1 to 3. The binary value of CONNOUT[4:0] gives the tributary index and ranges from 1 to 28 for T1 and 1 to 21 to E1. The programming of these bits is subject to two constraints:

1. All tributaries within an SPE must remain of the same type (i.e. E1 or T1).
2. Each CONNOUT[6:0] value must be unique relative to all other tributaries.

Failure to respect these constraints will result in the loss of data.

DL_CH[4:0]/DL_TS[4:0]:

The data link time slot (DL_CH[4:0]) bits gives a binary representation of the channel from which the data link is to be extracted. Note that T1 channels 1 to 24 are mapped to values 0 to 23. The DL_CH[4:0] bits have no effect when DL_EVEN and DL_ODD are both a logic 0.

T1_FDL_DIS:

The T1 data link disable bit allows the termination of the ESF data links when in T1 mode. If T1_FDL_DIS is a logic 0, the ESF and FMS[1:0] context bits determine the bit locations from which the data link is extracted. When the T1_FDL_DIS bit is a logic 0, the value of the DL_CH[4:0], DL_EVEN and DL_ODD bits is irrelevant. When T1_FDL_DIS is logic 1, a data link may be extracted from any one of the 24 DS0s as determined by the DL_CH[4:0], DL_EVEN and DL_ODD bits.

DL_EVEN:

The data link even select (DL_EVEN) bit controls whether or not the data link is extracted from the even frames of the receive data stream. If DL_EVEN is a logic 0, the data link is not extracted from the even frames. If DL_EVEN is a logic 1, the data link is extracted from the even frames. For T1, the frames in a superframe are numbered from 1 to 12 (or 1 to 24 in an extended superframe). For E1, the frames within a CRC multiframe are numbered from 0 to 15. If both DL_EVEN and DL_ODD are logic 1, then the datalink is extracted from all frames. If both DL_EVEN and DL_ODD are logic 0 (and T1_FDL_DIS is logic 1 for T1s), no data link is extracted.

DL_ODD:

The data link odd select (DL_ODD) bit controls whether or not the data link is extracted from the odd frames of the receive data stream. If DL_ODD is a logic 0, the data link is not extracted from the odd frames. If DL_ODD is a logic 1, the data link is extracted from the odd frames. If both DL_EVEN and DL_ODD are logic 1, then the datalink is extracted from all frames. If both DL_EVEN and DL_ODD are logic 0 (and T1_FDL_DIS is logic 1 for T1s), no data link is extracted.

DL_BIT[7:0]:

The data link bit select (DL_BIT[7:0]) bits controls which bits of the time slot/channel are to be extracted and passed to the HDLC controller. If DL_BIT[x] is a logic 1, that bit is extracted as part of the data link. To extract the data link from the entire time slot, all eight DL_BIT[x] bits must be set to a logic 1. DL_BIT[7] corresponds to the most significant bit (bit 1, the first bit received) of the time slot and DL_BIT[0] corresponds to the least significant bit (bit 8, the last bit received) of the time slot. The DL_BIT[7:0] bits have no effect when the DL_EVEN and DL_ODD bits are both logic 0.

JPN:

The JPN bit enables Japanese variations of the standard framing formats. If the JPN bit is a logic 1 and the ESF format is selected (ESF bit is logic 1), the CRC-6 is calculated using the F-bits as received, instead of replacing them with ones (as would be the case for ESF = logic 1 and JPN = logic 0). If the JPN bit is a logic 1 and a non-ESF format is selected (ESF bit is logic 0), it is assumed that the 12^{th} F-bit of the superframe carries a far end receive failure alarm. The alarm is extracted and the framing is modified to be robust (12^{th} F-bit is X in framing sequence) when the alarm is active.

ESF, FMS[1:0]:

The ESF bit selects ESF framing format, and determines the function of the frame mode select (FMS[1:0]) bits. When the ESF bit set to logic 1, the FMS[1:0] bits select the data rate and the source channel for the facility data link (FDL) data. The FRMR-84 may receive FDL data at the full 4 kHz rate from every odd frame, at a 2 kHz rate from frames 3, 7, 11, 15, 19, and 23, or at a 2 kHz rate from frames 1, 5, 9, 13, 17, and 21. When the ESF bit is set to logic 0, the FMS[1:0] bits select either SF or transparent framing modes. The valid combinations of the ESF, and FMS[1:0] bits are summarized in the table below:

ESF	FMS[1]	FMS[0]	Mode
0	0	0	Select SF framing format
0	0	1	Transparent – no attempt is made to frame
0	1	0	SLC-96
0	1	X	Reserved
1	0	0	Select ESF framing format and 4 kHz FDL data rate
1	0	1	Select ESF framing format and 2 kHz FDL data rate using frames 3, 7, 11,15,19, 23
1	1	0	Select ESF framing format and 2 kHz FDL data rate using frames 1, 5, 9, 13, 17, 21
1	1	1	Select ESF framing format and default to 4 kHz FDL data rate

ESFFA:

The ESFFA bit selects one of two framing algorithms for ESF frame search in the presence of mimic framing patterns. A logic 0 selects an ESF algorithm where the FRMR-84 does not set INF high while more than one framing bit candidate is following the framing pattern in the PCM stream. A logic 1 selects an ESF algorithm where a CRC-6 calculation is performed on each framing bit candidate, and is compared to the CRC bits associated with the framing bit candidate to determine the most likely framing bit position.

Under most situations, it is recommended that ESFFA be set to logic 1. Setting ESFFA to logic 1 reduces the probability f framing to a mimic framng pattern at the expense of a slightly longer average time to frame. ESFFA

logic 1 is more robust at dealing the special situation where a repetitive payload pattern results in a persistent mimic.

M2O[1:0]:

The M2O[1:0] bits are used to set the error threshold for declaring out-of-frame (OOF). For SF and ESF framing formats:

M2O[1]	M2O[0]	OOF Threshold
0	0	2-of-4 framing bits in error
0	1	2-of-5 framing bits in error
1	0	2-of-6 framing bits in error
1	1	Locked in-frame

While locked in-frame criteria is selected, OOF is never declared, regardless of the number of framing bit errors.

FASTD:

Enables the fast deassertion of the Red alarm within 120 ms, the AIS alarm within 180 ms and the AIS-CI alarm within two seconds. A logic 1 in the FASTD bit position enables the fast deassertion mode; a logic 0 disables the fast deassertion mode.

LBASEL[1:0]:

The Loopback Activate Select bits allow for the selection of a loopback code length from three bits to eight bits long as follows:

LBASEL[1]	LBASEL[0]	Code Length
0	0	5 bits
0	1	6 (or 3*) bits
1	0	7 bits
1	1	8 (or 4*) bits

LBACT[7:0]:

This 8-bit field allows the selection of the activate code sequence that is to be detected. If the code is less than 8 bits long, the first 8 bits of the repeated sequence must be used to fill the field. For example, if the code sequence is '00101', the first 8 bits of '0000100001'… are '00001000'). Note that bit 7 is the first code bit received.

LBDSEL[1:0]:

The Loopback Deactivate Select bits allow for the selection of a loopback code length from three bits to eight bits long as follows:

LBDSEL[1]	LBDSEL[0]	Code Length
0	0	5 bits
0	1	6 (or 3*) bits
1	0	7 bits
1	1	8 (or 4*) bits

LBDACT[7:0]:

This 8-bit field allows the selection of the deactivate code sequence that is to be detected. If the code is less than 8 bits long, the first 8 bits of the repeated sequence must be used to fill the field. For example, if the code sequence is '10011', the first 8 bits of '1001110011'… are '10011100'). Note that bit 7 is the first code bit received.

CCOFA:

The CCOFA bit determines whether Change-of-Frame Alignment (COFA) events or out-of-frame (OOF) events are counted and stored in the OOF[2:0] context bits. If CCOFA is a logic 1, COFA events are counted.

PRMEN:

When logic 1, the Performance Report Message Enable (PRMEN) bit enables the generation of PRMs upon counter transfers. This bit only has effect in ESF mode.

CR:

The value of this bit is copied into the C/R bit position of each performance reporting message transferred.

BOCE:

The BOCE bit position enables or disables the generation of an interrupt when a valid BOC is detected or removed. A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the BOCI context bit.

IDLE:

The IDLE bit position enables or disables the generation of an interrupt when there is a transition from a validated BOC to idle code (defined as the bit

sequence 1111111101111110). A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the IDLEI context bit.

INFE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the INF context bit.

SEFE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the SEFI bit becoming logic 1.

BEEE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the BEEI bit becoming logic 1.

FERE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the FERI bit becoming logic 1.

COFAE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the COFAI bit becoming logic 1.

YELE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the YEL context bit.

REDE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the RED context bit.

AISE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the AIS context bit.

RAICIE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the RAICI context bit.

AISCIE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the AISCI context bit.

LBAE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the LBA context bit.

LBDE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the LBD context bit.

ALMDI:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in any one of the AISD, LBAD, LBDD or YELD context bits.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred, and that the contents of the holding registers have been overwritten. OVR is set to logic 0 when this bit is accessed by an indirect read.

If the DIS_R2C bit is a logic 1 when an indirect read occurs, OVR will not accurately reflect that the holding registers have been read.

INF:

INF is the inframe status. In E1 mode, INF indicates basic alignment, as opposed to CRC-4 or signaling multiframe alignment.

YEL:

YEL is the integrated T1 Yellow Alarm status. YEL becomes logic 1 when a Yellow alarm has persisted for 400 ms (±50 ms). YEL becomes logic 0 when the alarm has been absent for 400 ms (±50 ms).

RED:

RED is the integrated RED Alarm status.

T1: The RED bit is a logic 1 if an out of frame condition has persisted for

2.55 s (±40 ms). The RED bit returns to a logic 0 when an out of frame condition has been absent for 16.6 s (±500 ms).

E1: The RED bit is a logic 1 if an out of frame condition has persisted for 100 ms. The RED bit returns to a logic 0 when an out of frame condition has been absent for 100 ms.

AIS:

AIS is the integrated AIS Alarm status.

T1: The AIS bit is a logic 1 when an out of frame all-ones condition has persisted for 2.55 s (±100 ms). The AIS bit returns to a logic 0 when the AIS condition has been absent for 16.6 s (±500 ms).

E1: The AIS bit is a logic 1 when an out of frame all-ones condition has persisted for 100 ms. The AIS bit returns to a logic 0 when the AIS condition has been absent for 100 ms.

RAICI:

RAICI is the integrated RAICI Alarm status.

AISCI:

AISCI is the integrated AIS-CI Alarm status.

LBA:

This bit is set if the inband code programmed by the LBASEL[1:0] and LBACT[7:0] fields have persisted for a minimum of 5.08 seconds (± 40 ms).

The bit is cleared if the code has been absent for 5.08 seconds (± 40 ms).

LBD:

This bit is set if the inband code programmed by the LBDSEL[1:0] and LBDACT[7:0] fields have persisted for a minimum of 5.08 seconds (± 40 ms).

The bit is cleared if the code has been absent for 5.08 seconds (± 40 ms).

INFI:

INFI becomes a logic 1 upon a change in the INF context bit. It is cleared upon an indirect read access.

SEFI:

SEFI becomes a logic 1 upon a severely errored frame event. It is cleared upon an indirect read access.

A Severely Errored Frame (SEF) event is defined as follows:

- SF - 2 or more F_t or F_s bits are in error during a 1.5 ms interval, as delimited by the 12 frame superframe boundary
- SLC96 - 2 or more F_t or F_s bits are in error during a 1.5 ms interval, as delimited by the 12 frame superframe boundary
- ESF - 2 or more F_e bits are in error during a 3 ms interval, as delimited by the 24 frame superframe boundary.

BEEI:

BEEI becomes a logic 1 upon a bit error event. It is cleared upon an indirect read access. A bit error event (BEE) is defined as an F-bit error for SF and SLC®96 framing format or a CRC-6 error for ESF framing format.

FERI:

T1: FERI becomes a logic 1 upon a framing error event. It is cleared upon an indirect read access. A framing bit error (FER) is defined as an F_s or F_t error for SF and SLC®96 and an F_e error for ESF framing format.

E1: FERI becomes a logic 1 upon an error in the FAS or NFAS bit positions. It is cleared upon an indirect read access.

COFAI:

COFAI becomes a logic 1 upon a change of frame alignment. It is cleared upon an indirect read access. A change of frame alignment is declared upon frame acquisition (i.e. upon INF becoming logic 1) if the new F-bit's location is different from the previously established frame alignment. The position within the superframe/multiframe is relevant as well as the location within the 193 bit T1 of 256 bit E1 frame.

YELI:

YELI becomes a logic 1 upon a change in the YEL context bit. It is cleared upon an indirect read access.

REDI:

REDI becomes a logic 1 upon a change in the RED context bit. It is cleared upon an indirect read access.

AISI:

AISI becomes a logic 1 upon a change in the AIS context bit. It is cleared upon an indirect read access.

RAICII:

RAICII becomes a logic 1 upon a change in the RAICI context bit. It is cleared upon an indirect read access.

AISCII:

AISCII becomes a logic 1 upon a change in the AISCI context bit. It is cleared upon an indirect read access.

IDLEI:

IDLEI becomes a logic 1 upon validation of an idle bit oriented code (defined as the bit sequence 1111111101111110). It is cleared upon an indirect read access.

BOCI:

BOCI becomes a logic 1 upon validation or removal of a bit oriented code. It is cleared upon an indirect read access.

Note that the transition from one validated code to another will produce two indications. The first will be upon recognizing the first code has been removed (BOC bits will be “111111”) and the second will be after the third repetition of the new code. With a 4kHz datalink, these two interrupts will be 8ms apart.

LBAI:

LBAI becomes a logic 1 upon a change in the LBA context bit. It is cleared upon an indirect read access.

LBDI:

LBDI becomes a logic 1 upon a change in the LBD context bit. It is cleared upon an indirect read access.

BOC[5:0]:

These six bits contain the latest validated bit oriented code. BOC[0] is the first bit received. An update of these bits is accompanied by an assertion of the BOCI bit. If no code has been validated or an idle code (defined as the bit sequence 1111111101111110) is being received, these bits are all ones.

BEE[8:0]:

The Bit Error Event holding register contains the count of bit error events that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomously once per second if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1. The count saturates at all ones.

A bit error event (BEE) is defined as an F-bit error for SF and SLC®96 framing format or a CRC-6 error for ESF framing format.

FER[4:0]:

The Framing Error Event holding register contains the count of framing bit error events that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomously once per second if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1. The count saturates at all ones.

A framing bit error (FER) is defined as an F_S or F_t error for SF and SLC®96 and an F_e error for ESF framing format.

OOF[2:0]:

The Out of Frame Event holding register contains the count of logic 1 to logic 0 transitions on the INF bit that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomously once per second if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1. The count saturates at all ones.

AISD:

This bit is set if AIS condition has been detected over a 40ms period. The bit is cleared if the tributary becomes in frame or has sufficient number of zeros within a 40ms period for AIS.

LBAD:

This bit is set if the inband code programmed by the LBASEL[1:0] and LBACT[7:0] fields have been detected over a 40 ms period. The bit is cleared if the code has been absent over a 40 ms period.

LBDD:

This bit is set if the inband code programmed by the LBDSEL[1:0] and LBDACT[7:0] fields have been detected over a 40 ms period. The bit is cleared if the code has been absent over a 40 ms period.

YELD:

This bit is set if Yellow alarm has been detected over a 40ms period. The bit is cleared upon the failure to detect the yellow alarm over a 40ms period or the framer drops out of frame.

AISDI:

AISDI becomes a logic 1 upon a change in the AISD context bit. It is cleared upon an indirect read access.

LBADI:

LBADI becomes a logic 1 upon a change in the LBAD context bit. It is cleared upon an indirect read access.

LBDDI:

LBDDI becomes a logic 1 upon a change in the LBDD context bit. It is cleared upon an indirect read access.

YELDI:

YELDI becomes a logic 1 upon a change in the YELD context bit. It is cleared upon an indirect read access.

UNFRAMED:

If this bit is a logic 1, the framer will not attempt to find frame. The data is passed through transparently with no channel alignment.

CRCEN:

The CRCEN bit enables framing to the CRC multiframe. When the CRCEN bit is logic 1, the framer searches for CRC multiframe alignment and monitors for errors in the alignment. A logic 0 in the CRCEN bit position disables

searching for multiframe and suppresses the INCMF, CRCEI, CMFERI, FEBE, CFEBE, RAICCRC and C2NCIW statuses, forcing them to logic 0.

CASDIS:

The CASDIS bit enables framing to the Channel Associated Signaling multiframe when set to a logic 0. When CAS is enabled, the framer searches for signaling multiframe alignment and monitors for errors in the alignment. A logic 1 in the CASDIS bit position disables searching for multiframe and suppresses the INSMF and the SMFER bits, forcing them to logic 0.

C2NCIWCK:

The C2NCIWCK bit enables the continuous checking for CRC multiframe while in the CRC to non-CRC interworking mode. If this bit is a logic 0, the framer will cease searching for CRC multiframe alignment once in CRC to non-CRC interworking mode. If this bit is a logic 1, the framer will continue searching for CRC multiframe alignment, even if CRC to non-CRC interworking has been declared.

REFR:

A transition from logic 0 to logic 1 in the REFR bit position forces the re-synchronization to a new frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to generate subsequent re-synchronizations.

REFCRCEN:

The REFCRCEN bit enables excessive CRC errors (≥ 915 errors in one second) to force a re-synchronization to a new frame alignment. Setting the REFCRCEN bit position to logic 1 enables reframe due to excessive CRC errors; setting the REFCRCEN bit to logic 0 disables CRC errors from causing a reframe.

REFRDIS:

The REFRDIS bit disables reframing under any error condition once frame alignment has been found; reframing can be initiated by software via the REFR bit. A logic 1 in the REFRDIS bit position causes the framer to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur based on the various error criteria (FER, excessive CRC errors, etc.). Note that while the framer remains locked in frame due to REFRDIS=1, a received AIS will not be detected since the framer must be out-of-frame to detect AIS.

BIT2C:

The BIT2C bit enables the additional criterion that loss of frame is declared when bit 2 in time slot 0 of NFAS frames has been received in error on 3 consecutive occasions. A logic 1 in the BIT2C position enables declaration of loss of frame alignment when bit 2 is received in error; a logic 0 in BIT2C enables declaration of loss of frame alignment based on the absence of FAS frames only.

SMFASC:

The SMFASC bit selects the criterion used to declare loss of signaling multiframe alignment. A logic 0 in the SMFASC bit position enables declaration of loss of signaling multiframe alignment when 2 consecutive multiframe alignment patterns have been received in error. A logic 1 in the SMFASC bit position enables declaration of loss of signaling multiframe when 2 consecutive multiframe alignment patterns have been received in error or when time slot 16 contains logic 0 in all bit positions for 1 or 2 multiframes based on the criterion selected by TS16C.

TS16C:

The TS16C bit selects the criterion used to declare loss of signaling multiframe alignment signal when enabled by the SMFASC. A logic 0 in the TS16C bit position enables declaration of loss of signaling multiframe alignment when time slot 16 contains logic 0 in all bit positions for 1 multiframe. A logic 1 in the TS16C bit position enables declaration of loss of signaling multiframe when time slot 16 contains logic 0 in all bit positions for 2 consecutive signaling multiframes.

RAIC:

The RAIC bit selects criterion used to declare a Remote Alarm Indication (RAI). If RAIC is logic 0, the RAI indication is asserted upon reception of any A=1 (A is bit 3 of NFAS frames) and is deasserted upon reception of any A=0. If RAIC is logic 1, the RAI indication is asserted if A=1 is received on 4 or more consecutive occasions, and is cleared upon reception of any A=0.

AISC:

The AISC bit selects the criterion used for determining AIS alarm indication. If AISC is logic 0, AIS is declared if there is a loss of frame (LOF) indication and a 512 bit period is received with less than 3 zeros. If AISC is a logic 1, AIS is declared if less than 3 zeros are detected in each of 2 consecutive 512 bit periods and is cleared when 3 or more zeros are detected in each of 2 consecutive 512 bit intervals.

EXCRCERR:

The EXCRCERR bit is an active high status bit indicating that excessive CRC evaluation errors (i.e. ≥ 915 error in one second) have occurred, thereby initiating a reframe if enabled by the REFCRCEN bit of the Frame Alignment Options register. The EXCRCERR bit is reset to logic 0 after an indirect read access.

SaSEL[2:0]:

The SaSEL[2:0] bits select which National Bit Codeword appears in the SaX[1:4] bits of the National Bit Codeword register. These bits map to the codeword selection as follows:

SaSEL[2:0]	National Bit Codeword
001	Undefined
010	Undefined
011	Undefined
100	Sa4
101	Sa5
110	Sa6
111	Sa7
000	Sa8

OOSMFAIS:

This bit controls the signaling trunk conditioning in an out of signaling multiframe (OOSMF) condition. If OOSMFAIS is logic 1, an OOSMF indication will cause the CASID[x] or the SBI CAS fields to be set to all 1's.

CNTNFAS:

When CNTNFAS is logic 1, a zero in bit 2 of time slot 0 of non-frame alignment signal (NFAS) frames results in an increment of the framing error count. If WORDERR is also a logic 1, the word is defined as the eight bits consisting of the seven bit FAS pattern and bit 2 of time slot 0 of the next NFAS frame. When CNTNFAS is logic 0, only errors in the FAS affect the framing error count.

WORDERR:

The WORDERR bit determines how frame alignment signal (FAS) errors are reported. When WORDERR is logic 1, one or more errors in the seven bit FAS word results in a single framing error count. When WORDERR is logic 0, each error in a FAS word results in a single framing error count.

C2NCIWE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the C2NCIW context bit.

INFE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the INF context bit.

INSMFE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the INSMF context bit.

INCMFE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the INCMF context bit.

COFAE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in basic frame alignment.

FERE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon an error in the FAS or NFAS bit positions.

SMFERE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon an error in the signaling multiframe alignment pattern.

CMFERE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon an error in the CRC multiframe alignment pattern.

RAIE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the RAI context bit.

RMAIE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the RMAI context bit.

AISDE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the AISD context bit.

TS16AISDE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the TS16AISD context bit.

FEBEE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set when a logic zero is received in the Si bits (bit 1; E bits) of frames 13 or 15.

CRCEE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set when the calculated CRC differs from the received CRC remainder.

OOOFE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the OOOF context bit.

RAICRCE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the RAICCRC context bit.

CFEBEE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the CFEBE context bit.

V52LINKE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon a change in the V52LINK context bit.

IFPE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the first bit of each frame.

ICSMFPE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the first bit of each CRC sub-multiframe.

ICMFPE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the first bit of each CRC multiframe.

ISMFPE:

A logic 1 in this bit position enables the associated FRMRI[x] bit to be set upon the first bit of each signaling multiframe.

Sa4E, Sa5E, Sa6E, Sa7E, Sa8E:

The National Use interrupt enables allow changes in Sa code word values to generate an interrupt. If SaNE is a logic 1, a logic 1 in the SaNI bit of the International Bits/National Interrupt Status register will result in the assertion the associated FRMRI[x] bit.

C2NCIWI:

C2NCIWI becomes a logic 1 upon a change in the C2NCIW context bit. It is cleared upon an indirect read access.

INFI:

INFI becomes a logic 1 upon a change in the INF context bit. It is cleared upon an indirect read access.

INSMFI:

INSMFI becomes a logic 1 upon a change in the INSMF context bit. It is cleared upon an indirect read access.

INCMFI:

INCMFI becomes a logic 1 upon a change in the INCMF context bit. It is cleared upon an indirect read access.

SMFERI:

SMFERI becomes a logic 1 upon an error in the signaling multiframe alignment pattern. It is cleared upon an indirect read access.

CMFERI:

CMFERI becomes a logic 1 upon an error in the CRC multiframe alignment pattern. It is cleared upon an indirect read access.

RAII:

RAII becomes a logic 1 upon a change in the RAI context bit. It is cleared upon an indirect read access.

RMAII:

RMAII becomes a logic 1 upon a change in the RMAI context bit. It is cleared upon an indirect read access.

AISDI:

AISDI becomes a logic 1 upon a change in the AISD context bit. It is cleared upon an indirect read access.

REDI:

REDI becomes a logic 1 upon a change in the RED context bit. It is cleared upon an indirect read access.

AISI:

AISI becomes a logic 1 upon a change in the AIS context bit. It is cleared upon an indirect read access.

TS16AISDI:

TS16AISDI becomes a logic 1 upon a change in the TS16AISD context bit. It is cleared upon an indirect read access.

FEBEI:

FEBEI becomes a logic 1 when a logic zero is received in the Si bits of frames 13 or 15. It is cleared upon an indirect read access.

CRCEI:

CRCEI becomes a logic 1 when the calculated CRC differs from the received CRC remainder. It is cleared upon an indirect read access.

OOOFI:

OOOFI becomes a logic 1 upon a change in the OOOF context bit. It is cleared upon an indirect read access.

RAICRCI:

RAICCRCI becomes a logic 1 upon a change in the RAICCRC context bit. It is cleared upon an indirect read access.

CFEBEI:

CFEBEI becomes a logic 1 upon a change in the CFEBE context bit. It is cleared upon an indirect read access.

V52LINKI:

V52LINKI becomes a logic 1 upon a change in the V52LINK context bit. It is cleared upon an indirect read access.

IFPI:

IFPI becomes a logic 1 upon the first bit of each frame. It is cleared upon an indirect read access. This bit is primarily for diagnostic purposes.

ICSMFPI:

ICSMFPI becomes a logic 1 upon the first bit of each CRC sub-multiframe. It is cleared upon an indirect read access. This bit is primarily for diagnostic purposes.

ICMFPI:

ICMFPI becomes a logic 1 upon the first bit of each CRC multiframe. It is cleared upon an indirect read access. This bit is primarily for diagnostic purposes.

ISMFPI:

ISMFPI becomes a logic 1 upon the first bit of each signaling multiframe. It is cleared upon an indirect read access. This bit is primarily for diagnostic purposes.

Sa4I, Sa5I, Sa6I, Sa7I, Sa8I

The National Use interrupt status bits indicate if the debounced version of the individual bits has changed since the last indirect read access. A logic 1 in one of the bit positions indicates a new nibble codeword is available in the associated SaN[1:4] bits, where N is 4 through 8.

C2NCIW:

The C2NCIW bit is set to logic 1 while the framer is operating in CRC to non-CRC interworking mode. The C2NCIW bit is set to a logic zero while the framer is not operating in CRC to non-CRC interworking mode. The C2NCIWCK bit may remain at a logic 1 if the CRCEN bit of register 0x0174 is cleared while the E1 framer is 'inframe'. The C2NCIWCK bit status will not

correctly update until an E1 reframe occurs which can be force via the REFR bit of register 0x0174.

INF:

The INF bit is a logic 0 when basic frame alignment has been lost. The INF bit goes to a logic 1 once frame alignment has been regained.

INSMF:

The INSMF bit is a logic 0 when signaling multiframe alignment has been lost. The INSMF bit goes to a logic 1 once signaling multiframe alignment has been regained.

INCMF:

The INCMF bit is a logic 0 when CRC multiframe alignment has been lost. The INCMF bit goes to a logic 1 once CRC multiframe alignment has been regained.

OOOF:

This bit indicates the current state of the out of offline frame (OOOF) indicator. OOOF is asserted when the offline framer in the CRC multiframe find procedure is searching for frame alignment.

RAICCRC:

This bit indicates the current state of the RAI and continuous CRC indicator. RAICCRC is asserted when the remote alarm (A bit) is set to logic 1 and the CRC error (E bit) is set to logic 0 for a period of 10 ms.

CFEBE:

This bit indicates the current state of the continuous FEBE indicator. CFEBE is asserted when the CRC error (E bit) is set to logic 1 on more than 990 occasions in each second (out of 1000 possible occasions) for the last 5 consecutive seconds.

V52LINK:

This bit indicates the current state of the V5.2 link identification signal indicator. V52LINK will be asserted if 2 out of last 3 Sa7 bits are received as a logic 0.

RAI:

The RAI bit indicates the remote alarm indication (RAI) value. The RAI bit is set to logic one when the 'A' bit (bit 3 in time slot 0 of the non-frame alignment signal frame) has been logic one for an interval specified by the RAIC bit. When the RAIC bit is a logic 1, RAI is set when A=1 for 4 or more consecutive intervals, and is cleared upon reception of any A=0. When the RAIC bit is a logic 0, RAI is set upon reception of any A=1, and is cleared upon reception of any A=0. The RAI output is updated every two frames.

RMAI:

The RMAI bit indicates the remote multiframe alarm indication (RMAI) value. The RMAI bit is set to logic one when the 'Y' bit (bit 6 in time slot 16 in frame 0 of the signaling multiframes) has been a logic one for 3 consecutive signaling multiframes, and is cleared upon reception of any Y=0. The RMAI bit is updated every 16 frames.

AISD:

The AISD bit indicates the alarm indication signal (AIS) defect value. The AISD bit is set to logic one when the incoming data stream has a low zero-bit density for an interval specified by the AISC bit. When the AISC bit is a logic 0, AISD is asserted when 512 bit periods have been received with 2 or fewer zeros. The indication is cleared when a 512 bit period is received with 3 or more zeros. When the AISC bit is a logic 1, AISD is asserted when two consecutive 512 bit periods have been received with 2 or fewer zeros. The indication is cleared when 2 consecutive 512 bit periods are received, with each period containing 3 or more zeros. The AISD bit is updated once every 512-bit period.

TS16AISD:

The time slot 16 Alarm Indication Signal detect (TS16AISD) signal goes high to indicate that the incoming TS 16 data stream has a low zero-bit density. TS16AISD is detected when the incoming TS16 signal has 3 or less zeroes in each of 2 consecutive multi-frames. The indication is cleared when 4 or more zeros are detected in each of two consecutive multi-frame periods, or when the signaling multi-frame signal has been found, or when basic frame alignment is lost.

Si[2:1]:

The Si[1] bit contains the International bit in the last received FAS frame. The Si[2] bit contains the International bit in the last received NFAS frame (note that this does not necessarily refer to a CRC bit).

A:

The A bit position contains the Remote Alarm Indication (RAI) bit in the last received NFAS frame.

Sa[4:8]:

These bits contain the National bit values in the last received NFAS frame. Note that the contents of this field are not updated while out of CRC multiframe.

X[3], Y, X[1], X[0]:

These bits contain the value of the Extra bits (X[3], X[1] and X[0]) and the Remote Signaling Multiframe Alarm bit (Y) in frame 0, timeslot 16 of the last received signaling multiframe. Note that the contents of this field are not updated while out of signaling multiframe.

SaX[4:1]:

These bits contain the SaX nibble code word extracted from the sub-multiframe., where 'X' corresponds to the National bit selected by the SaSEL[2:0] bits. SaX[1] is from the first SaX bit of the sub-multiframe; SaX[4] is from the last. A change in these bit values sets the SaI[X] bit.

CRCERR[9:0]

The CRC Error holding register contains the count of CRC-4 errors that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomously once per second if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1. The count saturates at all ones.

FER[6:0]:

The Framing Error holding register contains the count of framing bit errors that occurred during the latest accumulation interval. The value is updated by a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomously once per second if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1. The count saturates at all ones.

FEBE[9:0]:

The Far End Block Error holding register contains the count of number of zero E-bits during the latest accumulation interval. The value is updated by a write

to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomously once per second if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1. The count saturates at all ones.

Register 0x0187: T1/E1 Framer Configuration and Status

Bit	Type	Function	Default
Bit 7	W12C	XFERI	X
Bit 6	R/W	XFERE	0
Bit 5	R/W	INTE	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	XCONNEN	0
Bit 0	R/W	AUTOUPDATE	0

AUTOUPDATE:

If this bit is logic 1, the transfer of performance counts to holding registers is initiated every 19440000 SREFCLK cycles if S77 is low or 77760000 SREFCLK cycles if S77 is high, which is nominally one second. Upon a transfer, the associated internal counters are reset to begin a new cycle of error accumulation. The T1 transmitter also sends an ANSI T1.403-formatted performance report message (PRM) on the T1 facility data link. The XFERI status bit is set to logic 1 upon completion of the transfer.

Regardless of the state of AUTOUPDATE, transfers and PRMs may be initiated by a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1.

XCONNEN:

The Cross-Connect Enable (XCONNEN) bit enables the grooming of T1/E1 tributaries. If XCONNEN is logic 1, the tributaries are presented in the timeslots specified by the CONNOUT[6:0] field in the context RAM. If XCONNEN is logic 0, tributaries remain indexed as they were demultiplexed or demapped.

If XCONNEN is logic 1 for a tributary, the ELSTBYP bit of the RX-SBI-ELST Indirect Channel Data Register for the tributary must be logic 0.

Note that the bit asynchronous and byte synchronous demappers contain their own time switches, which may be used with fewer restrictions.

Therefore, it is recommended XCONNEN be set only when performing DS3 demultiplexing.

INTE:

If this bit is a logic 1, the FRMR bit of the Master Interrupt Source T1E1 register is logic 1 if at least one of the FRMRI[84:1] bits is a logic 1.

XFERE:

If this bit is a logic 1, the FRMR bit of the Master Interrupt Source T1E1 register is logic 1 if the XFERI bit is a logic 1.

XFERI:

Subsequent to a write to the Global Performance Monitor Update register that sets the E1T1_FRMR bit to logic 1 or autonomous update, the XFERI status bit is set to logic 1 when the counter transfers have been completed for all 84 links. This bit is cleared upon writing a logic 1 to the bit position.

Register 0x0188: T1/E1 Framer Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R	REG1_2I	X
Bit 6	R	REGF_0I	X
Bit 5	R	REGC_D_EI	X
Bit 4	R	REG9_A_BI	X
Bit 3	W12C	FRMRI[4]	X
Bit 2	W12C	FRMRI[3]	X
Bit 1	W12C	FRMRI[2]	X
Bit 0	W12C	FRMRI[1]	X

FRMRI[84:1]:

A logic 1 in these bits indicate framing events on the associated tributary since the bit was explicitly cleared. The associated SPE index is equal to trunc((bit index –1)/28) + 1. The associated LINK index is equal to (bit index-1 mod 28) + 1.

Each bit is cleared to logic 0 upon writing a logic 1 to the bit position.

REG9_A_BI:

This bit is a logic 1 if at least one bit in Register 0x0189, 0x018A or 0x018B is logic 1.

REGC_D_EI:

This bit is a logic 1 if at least one bit in Register 0x018C, 0x018D or 0x018E is logic 1.

REGF_0I:

This bit is a logic 1 if at least one bit in Register 0x018F or 0x0190 is logic 1.

REG1_2I:

This bit is a logic 1 if at least one bit in Register 0x0191 or 0x0192 is logic 1.

Register 0x0189: T1/E1 Framer Interrupt Status #2

Bit	Type	Function	Default
Bit 7	W12C	FRMRI[12]	X
Bit 6	W12C	FRMRI[11]	X
Bit 5	W12C	FRMRI[10]	X
Bit 4	W12C	FRMRI[9]	X
Bit 3	W12C	FRMRI[8]	X
Bit 2	W12C	FRMRI[7]	X
Bit 1	W12C	FRMRI[6]	X
Bit 0	W12C	FRMRI[5]	X

Register 0x018A: T1/E1 Framer Interrupt Status #3

Bit	Type	Function	Default
Bit 7	W12C	FRMRI[20]	X
Bit 6	W12C	FRMRI[19]	X
Bit 5	W12C	FRMRI[18]	X
Bit 4	W12C	FRMRI[17]	X
Bit 3	W12C	FRMRI[16]	X
Bit 2	W12C	FRMRI[15]	X
Bit 1	W12C	FRMRI[14]	X
Bit 0	W12C	FRMRI[13]	X

Register 0x018B: T1/E1 Framer Interrupt Status #4

Bit	Type	Function	Default
Bit 7	W12C	FRMRI[28]	X
Bit 6	W12C	FRMRI[27]	X
Bit 5	W12C	FRMRI[26]	X
Bit 4	W12C	FRMRI[25]	X
Bit 3	W12C	FRMRI[24]	X
Bit 2	W12C	FRMRI[23]	X
Bit 1	W12C	FRMRI[22]	X
Bit 0	W12C	FRMRI[21]	X

Register 0x018C: T1/E1 Framer Interrupt Status #5

Bit	Type	Function	Default
Bit 7	W12C	FRMRI[36]	X
Bit 6	W12C	FRMRI[35]	X
Bit 5	W12C	FRMRI[34]	X
Bit 4	W12C	FRMRI[33]	X
Bit 3	W12C	FRMRI[32]	X
Bit 2	W12C	FRMRI[31]	X
Bit 1	W12C	FRMRI[30]	X
Bit 0	W12C	FRMRI[29]	X

Register 0x018D: T1/E1 Framer Interrupt Status #6

Bit	Type	Function	Default
Bit 7	W12C	FRMRI[44]	X
Bit 6	W12C	FRMRI[43]	X
Bit 5	W12C	FRMRI[42]	X
Bit 4	W12C	FRMRI[41]	X
Bit 3	W12C	FRMRI[40]	X
Bit 2	W12C	FRMRI[39]	X
Bit 1	W12C	FRMRI[38]	X
Bit 0	W12C	FRMRI[37]	X

Register 0x018E: T1/E1 Framer Interrupt Status #7

Bit	Type	Function	Default
Bit 7	W12C	FRMRI[52]	X
Bit 6	W12C	FRMRI[51]	X
Bit 5	W12C	FRMRI[50]	X
Bit 4	W12C	FRMRI[49]	X
Bit 3	W12C	FRMRI[48]	X
Bit 2	W12C	FRMRI[47]	X
Bit 1	W12C	FRMRI[46]	X
Bit 0	W12C	FRMRI[45]	X

Register 0x018F: T1/E1 Framer Interrupt Status #8

Bit	Type	Function	Default
Bit 7	W12C	FRMRI[60]	X
Bit 6	W12C	FRMRI[59]	X
Bit 5	W12C	FRMRI[58]	X
Bit 4	W12C	FRMRI[57]	X
Bit 3	W12C	FRMRI[56]	X
Bit 2	W12C	FRMRI[55]	X
Bit 1	W12C	FRMRI[54]	X
Bit 0	W12C	FRMRI[53]	X

Register 0x0190: Framer Interrupt Status #9

Bit	Type	Function	Default
Bit 7	W12C	FRMRI[68]	X
Bit 6	W12C	FRMRI[67]	X
Bit 5	W12C	FRMRI[66]	X
Bit 4	W12C	FRMRI[65]	X
Bit 3	W12C	FRMRI[64]	X
Bit 2	W12C	FRMRI[63]	X
Bit 1	W12C	FRMRI[62]	X
Bit 0	W12C	FRMRI[61]	X

Register 0x0191: T1/E1 Framer Interrupt Status #10

Bit	Type	Function	Default
Bit 7	W12C	FRMRI[76]	X
Bit 6	W12C	FRMRI[75]	X
Bit 5	W12C	FRMRI[74]	X
Bit 4	W12C	FRMRI[73]	X
Bit 3	W12C	FRMRI[72]	X
Bit 2	W12C	FRMRI[71]	X
Bit 1	W12C	FRMRI[70]	X
Bit 0	W12C	FRMRI[69]	X

Register 0x0192: T1/E1 Framer Interrupt Status #11

Bit	Type	Function	Default
Bit 7	W12C	FRMRI[84]	X
Bit 6	W12C	FRMRI[83]	X
Bit 5	W12C	FRMRI[82]	X
Bit 4	W12C	FRMRI[81]	X
Bit 3	W12C	FRMRI[80]	X
Bit 2	W12C	FRMRI[79]	X
Bit 1	W12C	FRMRI[78]	X
Bit 0	W12C	FRMRI[77]	X

1.17 Scaleable Bandwidth Interconnect Master Configuration Register

Register 0x01C0 SBI Master Reset / Bus Signal Monitor

Bit	Type	Function	Default
Bit 7	R	SDC1FPA	X
Bit 6	R	SAC1FPA	X
Bit 5	R	SADA	X
Bit 4	R	SAV5A	X
Bit 3	R	SAPLA	X
Bit 2	R	SBIDET1A	X
Bit 1	R	SBIDET0A	X
Bit 0	R/W	RESET	0

When a monitored SBI Bus signal makes a low to high transition, the corresponding register bit is set to logic 1. The bit will remain high until this register is read, at which point all the bits in this register (except RESET) are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

RESET:

The RESET bit forces a software reset of all the SBI blocks. This will force all direct and indirect registers to their default values. When the RESET bit is set to a logic 1 the SBI blocks are held reset which is also the low power state. When RESET is set to logic 0 the SBI is operational. The SBI blocks are operational by default.

SBIDET0A:

The SBIDET0 active, SBIDET0A, bit monitors for low to high transitions on the SBIDET0 input. SBIDET0A is set to logic 1 on a rising edge of SBIDET0, and is set to logic 0 when this register is read.

SBIDET1A:

The SBIDET1 active, SBIDET1A, bit monitors for low to high transitions on the SBIDET1 input. SBIDET1A is set to logic 1 on a rising edge of SBIDET1, and is set to logic 0 when this register is read.

SAPLA:

The SAPL active, SAPLA, bit monitors for low to high transitions on the SAPL input. SAPLA is set to logic 1 on a rising edge of SAPL, and is set to logic 0 when this register is read.

SAV5A:

The SAV5 active, SAV5A, bit monitors for low to high transitions on the SAV5 input. SAV5A is set to logic 1 on a rising edge of SAV5, and is set to logic 0 when this register is read.

SADA:

The SADATA bus active, SADA, bit monitors for low to high transitions on the least significant data bit of the SBI Add bus, SADATA[0], as an indication of bus activity on the SBI Add bus data and parity signals. SADA is set to logic 1 when a rising edge has been observed on SADATA[0], and is set to logic 0 when this register is read.

SAC1FPA:

The SAC1FP active, SAC1FPA, bit monitors for low to high transitions on the SAC1FP input. SAC1FPA is set to logic 1 on a rising edge of SAC1FP, and is set to logic 0 when this register is read.

SDC1FPA:

The SDC1FP active, SDC1FPA, bit monitors for low to high transitions on the SDC1FP input. SDC1FPA is set to logic 1 on a rising edge of SDC1FP, and is set to logic 0 when this register is read.

Register 0x01C1 SBI Master Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SDC1FPMSTR	0
Bit 5	R/W	MFSDC1FP	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

MFSDC1FP:

The multiframe SDC1FP alignment bit, MFSDC1FP, enables the TEMUX 84 for signaling multiframe alignment on the SBI Drop bus. When the TEMUX 84 is enabled to generate the SDC1FP signal via setting SC1FPMSTR to logic 1, it will generate SDC1FP either every 4 if MFSDC1FP is logic 0 or every 48 SBI frames if MFSDC1FP is logic 1. MFSDc1FPmust be set to logic 1 if SC1FPMSTR is logic 0, the bus is configured for 77.76MHz operation (i.e. S77 input is high) and at least one T1/E1 tributary is configured in synchronous mode (i.e INSBI SYNCH_TRIB register bit is logic 1).

SDC1FPMSTR:

The SDC1FP master mode bit, SDC1FPMSTR, enables the TEMUX 84 to be the SDC1FP master in an SBI system. Only one device per SBI bus can be SDC1FP master. When SDC1FPMSTR is high the TEMUX 84 will generate the SDC1FP pulse at a period set by the MFSDC1FP register bit. When SDC1FPMSTR is low the TEMUX 84 will listen to the SDC1FP pulse which is generated elsewhere.

Register 0x01C2 SBI Bus Master Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	BUSMASTER	0

BUSMASTER:

This SBI Bus Master bit, BUSMASTER, enables the TEMUX 84 to drive the SBI Drop bus whenever no other SBI device is driving the bus. When BUSMASTER is set to 0, the TEMUX 84 drives the SBI Drop bus only during links that are enabled for this device . During all other links or SBI overhead bytes, the TEMUX 84 will tri-state the SBI Drop bus signals. When BUSMASTER is logic 1 and s77 is low, the TEMUX 84 will drive the SBI Drop bus during all links and SBI overhead bytes except when it detects other SBI devices are driving the bus when the SBIDET[1:0] signals are high. When BUSMASTER is logic 1 and s77 is high, the TEMUX 84 will drive the SBI Drop bus during all SBI overhead bytes for the configured STS-3 (via the SSTM(1:0) configuration bits in the Bus Configuration register 0x0006); individual links will be driven only when enabled.

Register 0x01C4: DLL Configuration (SBI Bus)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The DLL Configuration Register controls the basic operation of the DLL.

ERRORE:

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, the INTB output is asserted low upon assertion of the ERROR bit of the DLL Control Status register. When ERRORE is set low, changes in the ERROR bit does not generate an interrupt.

Reserved:

The reserved bits must be set low for correct operation.

Register 0x01C6: DLL Delay Tap Status (SBI Bus)

Bit	Type	Function	Default
Bit 7	R	TAP[7]	X
Bit 6	R	TAP[6]	X
Bit 5	R	TAP[5]	X
Bit 4	R	TAP[4]	X
Bit 3	R	TAP[3]	X
Bit 2	R	TAP[2]	X
Bit 1	R	TAP[1]	X
Bit 0	R	TAP[0]	X

The DLL Delay Tap Status Register indicates the delay tap used by the DLL to generate the outgoing clock.

Writing to this register performs a software reset of the DLL. A software reset requires a maximum of 24*256 SREFCLK cycles for the DLL to regain lock. During this time the SBI output propagation delays may vary.

TAP[7:0]:

The tap status register bits (TAP[7:0]) specifies the delay line tap the DLL is using to generate its outgoing clock.
When TAP[7:0] is logic zero, the DLL is using the delay line tap with minimum phase delay. When TAP[7:0] is equal to 255, the DLL is using the delay line tap with maximum phase delay.

Register 0x01C7: DLL Control Status (SBI Bus)

Bit	Type	Function	Default
Bit 7	R	SREFCLKI	X
Bit 6	R	DLLCLKI	X
Bit 5	R	ERRORI	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1		Unused	X
Bit 0	R	RUN	X

The DLL Control Status Register provides information of the DLL operation.

RUN:

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the variable delay clock and the rising edge of SREFCLK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.
The RUN register bit is cleared only by a hardware or a software reset.

ERROR:

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. ERROR is set low when the DLL captures lock again.
When this bit is a logic 1, it is recommended the DLL be re-initialized by writing any value to the DLL Delay Tap Status register.

ERRORI:

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one and is cleared upon read.

DLLCLKI:

The reference clock event register bit DLLCLKI provides a method to monitor activity on the variable delay clock. When the internal DLLCLK changes from a logic zero to a logic one, the DLLCLKI register bit is set to logic one and cleared upon read.

In the unlikely event this bit is logic 0, the DLL should be re-initiated by writing any value to the DLL Delay Tap Status register.

SREFCLKI:

The system clock event register bit SREFCLKI provides a method to monitor activity on the SREFCLK input clock. When the SREFCLK primary input changes from a logic zero to a logic one, the SREFCLKI register bit is set to logic one. The SREFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

1.18 EXSBI Extract Scaleable Bandwidth Interconnect Registers

Register 0x01D0: EXSBI Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	DC_RSTEN	1
Bit 5	R/W	DC_RESYNCE	0
Bit 4	R/W	FIFO_OVRE	0
Bit 3	R/W	FIFO_UDRE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	SBI_PERR_EN	0
Bit 0	R/W	SBI_PAR_CTL	1

SBI_PAR_CTL:

The SBI_PAR_CTL bit is used to configure the Parity mode for checking of the SBI parity signal, SADP. When SBI_PAR_CTL is a logic 0 parity will be even. When SBI_PAR_CTL is logic 1 parity will be odd

SBI_PERR_EN:

The SBI_PERR_EN bit is used to enable the SBI Parity Error interrupt generation. When SBI_PERR_EN is a logic 1 SBI parity errors will result in the assertion low of the INTB output.

FIFO_UDRE:

This bit is set to enable the assertion low of the INTB output when a FIFO under-run is detected.

FIFO_OVRE:

This bit is set to enable the assertion low of the INTB output when a FIFO over-run is detected.

DC_RESYNCE:

This depth check and bus resynchronization interrupt enable bit, DC_RESYNCE, enables the generation of an interrupt when either a Depth Check error or an external resynchronization event occurs on either the

SAC1FP or internal synchronization signals. When DC_RESYNCE is logic 1 the INTB output is asserted low when one of the depth check or resynchronization errors occur. When DC_RESYNCE is a logic 0 INTB will not be asserted due to these events.

Depth check events should only happen when the SBI bus is misconfigured and will reset the link. SAC1FP resynchronization events will reset the entire SBI bus interface and are reported by the SAC1FP_SYNCI. Internal synchronization errors should only occur during configuration and are reported by the SBIIP_SYNCI.

DC_RSTEN:

The Depth check automatic reset enable bit, DC_RSTEN, allows the EXSBI to automatically reset a link if it underruns or overruns. When DC_RSTEN is a 1 the link will automatically reset when a depth check error is detected. When DC_RSTEN is a 0 the link must be reset manually when a depth check error is detected and reported via the depth check error interrupt, DC_ERRI bit in the EXSBI Depth Check Interrupt Status register.

When DC_RSTEN is a logic 0, interrupts must be enabled via the DC_RESYNCE interrupt enable bit. When DC_RSTEN is a 1 and depth check interrupts are enabled via DC_RESYNCE, multiple interrupts can be expected until the link FIFO is at the correct operating level.

Reserved:

These bits must be left as a logic 0 for proper operation.

Register 0x01D1: EXSBI FIFO Underrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_UDRI	X

This register is cleared when read.

Back to back reads of this register must be at least 250 ns apart.

This Underrun interrupt register is the output of a priority encoder of the underrun history of all links. The most significant links have the highest priority and will be reported first if underruns simultaneously occur on multiple links.

If bit 0 is zero, no links have entered underrun since the last read, and all pending underrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is one, the register contents are valid, and indicate a link has entered underrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note that if a tributary is misbehaving so that it frequently enters underrun, the reporting of the multiple underruns can prevent the reporting of underrun on lower priority links. Such misbehaving links should be disabled (ENBL=0) to obtain the complete underrun history.

FIFO_UDRI:

This bit is set when a FIFO under-run is detected.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the over-run was detected.
Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.

Register 0x01D2: EXSBI FIFO Overrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE1	X
Bit 6	R	SPE0	X
Bit 5	R	LINK4	X
Bit 4	R	LINK3	X
Bit 3	R	LINK2	X
Bit 2	R	LINK1	X
Bit 1	R	LINK0	X
Bit 0	R	FIFO_OVRI	X

This register is cleared when read.

Back to back reads of this register must be at least 250 ns apart.

This Overrun interrupt register is the output of a priority encoder of the overrun history of all links. The most significant links have the highest priority and will be reported first if overruns simultaneously occur on multiple links.

If bit 0 is zero, no links have overrun since the last read, and all pending overrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is one, the register contents are valid, and indicate a link has overrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note that if a tributary is misbehaving so that it frequently overruns, the reporting of the multiple overruns can prevent the reporting of overruns on lower priority links. Such misbehaving links should be disabled (ENBL=0) to obtain the complete overrun history.

FIFO_OVRI:

This bit is set when a FIFO over-run is detected.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the over-run was detected.
Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.

Register 0x01D3: EXSBI Tributary RAM Indirect Access Address

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] fields are used to fully specify which SBI tributary the Control register write or read operation will apply.
TRIB[4:0] specifies the SBI tributary number within the SBI SPE as specified by the SPE[1:0] field. Legal values for TRIB[4:0] are b’00001’ through b‘11100’ in T1 mode, b’00001’ through b‘10101 in E1 mode and b’00001 in DS3 mode. Legal values for SPE[1:0] are b’01’ through b‘11’.

When an SPE is configured for E1, indirect accesses are not permitted to TRIB indexes b’10110 through b’11100. When an SPE is configured for DS3 or E3, indirect accesses are not permitted to TRIB indexes b’00010 through b’11100.

Reserved:

This bit must always be written as a logic 0 for correct operation.

Register 0x01D4: EXSBI Tributary RAM Indirect Access Control

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RWB	0
Bit 0	R/W	Reserved	0

Reserved:

A logic 0 must be written to this bit for proper operation.

RWB:

The indirect access control bit, RWB selects between a configure (write) or interrogate (read) access to the tributary control configuration RAM. Writing a logic 0 to RWB triggers an indirect write operation. Data to be written is taken from the Extract Tributary Control Indirect Access Data Register. Writing a logic 1 to RWB triggers an indirect read operation. The data read can be found in the Extract Tributary Control Indirect Access Data Register.

BUSY:

The indirect access status bit, BUSY reports the progress of an indirect access. BUSY is set to logic 1 when a write to this register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Data register or to determine when a new indirect write operation may commence. If SREFCLK disappears during an access, the BUSY bit can stay high.

Register 0x01D6: EXSBI Tributary Control Indirect Access Data

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CLK_MODE[1]	0
Bit 5	R/W	CLK_MODE[0]	0
Bit 4	R/W	CLK_MSTR	0
Bit 3	R/W	TRIB_TYP[1]	0
Bit 2	R/W	TRIB_TYP[0]	0
Bit 1		Unused	X
Bit 0	R/W	ENBL	0

ENBL:

The ENBL bit is used to enable the Tributary. Writing to the EXSBI Tributary RAM Indirect Access Control Register with the ENBL bit set enables the EXSBI to transmit tributary data from an SBI tributary.

If ENBL is logic 0, it is recommended the egress tributary rate be locked to CTCLK and that AIS or trunk conditioning be inserted into the data stream.

TRIB_TYP[1:0]

The TRIB_TYP[1:0] field is used to specify the characteristics of the SBI tributary as shown in Table 3.

Table 3 EXSBI TRIB_TYP Encoding

TRIB_TYP	Description	CAS Enabled	Framed
00	Framed with CAS	True	True
01	Framed without CAS	False	True
10	Unframed	False	False
11	Reserved	X	X

The Reserved value for TRIB_TYP must not be used for proper operation of the TEMUX 84.

CLK_MSTR:

The CLK_MSTR bit is used to specify whether the Extract block tributary functions as a clock master or a clock slave. When this bit is a logic 1, the TEMUX 84 is the clock master for the selected tributary and will use the SAJUST_REQ SBI signal to speed-up or slow-down SBI slaves connected to that tributary. When this bit is a logic 0, the TEMUX 84 is a clock slave for the selected tributary and will adapt to the incoming tributary rate.

CLK_MODE[1:0]:

The CLK_MODE[1:0] field controls how the Extracted Link Rate octet is used. In applications where the Link Rate octet is not used, CLK_MODE[1:0] must be 00. When Link Rate is available CLK_MODE[1:0] can be configured to use the Link Rate information to produce a smoother egress DS3/E3 clock.

The CLK_MODE bits have no effect for T1/E1 tributaries; the Link Rate octet is always ignored.

CLK_MODE[1:0]	Description
00	Link Rate octet not used
01	Use only ClkRate field of Link Rate octet
10	Reserved – must not be used for normal operation
11	Reserved – must not be used for normal operation

Register 0x01D7: SBI Parity Error Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	TRIB[4]	X
Bit 4	R	TRIB[3]	X
Bit 3	R	TRIB[2]	X
Bit 2	R	TRIB[1]	X
Bit 1	R	TRIB[0]	X
Bit 0	R	PERRI	X

PERRI:

When set PERRI indicates that an SBI parity error has been detected. This bit is cleared when read.

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] field are used to specify the SBI tributary for which a parity error was detected. These fields are only valid only when PERRI is set.

Register 0x01D8: EXSBI MIN_DEPTH for T1 and E1 Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_DEP_E1[3]	0
Bit 6	R/W	MIN_DEP_E1[2]	1
Bit 5	R/W	MIN_DEP_E1[1]	1
Bit 4	R/W	MIN_DEP_E1[0]	1
Bit 3	R/W	MIN_DEP_T1[3]	0
Bit 2	R/W	MIN_DEP_T1[2]	1
Bit 1	R/W	MIN_DEP_T1[1]	1
Bit 0	R/W	MIN_DEP_T1[0]	1

MIN_DEP_E1[3:0]:

Used to modify the MIN_DEPTH for E1 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO

MIN_DEP_T1[3:0]:

Used to modify the MIN_DEPTH for T1 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO

Register 0x01D9: EXSBI MIN_DEPTH for DS3 and E3 Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_DEP_E3[3]	1
Bit 6	R/W	MIN_DEP_E3[2]	1
Bit 5	R/W	MIN_DEP_E3[1]	1
Bit 4	R/W	MIN_DEP_E3[0]	1
Bit 3	R/W	MIN_DEP_DS3[3]	1
Bit 2	R/W	MIN_DEP_DS3[2]	1
Bit 1	R/W	MIN_DEP_DS3[1]	1
Bit 0	R/W	MIN_DEP_DS3[0]	0

MIN_DEP_DS3[3:0]:

Used to modify the MIN_DEPTH for DS3 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO

MIN_DEP_E3[7:0]:

Used to modify the MIN_DEPTH for E3 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO

Register 0x01DA: EXSBI T1 Threshold Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_T1[3]	0
Bit 6	R/W	MIN_THR_T1[2]	0
Bit 5	R/W	MIN_THR_T1[1]	1
Bit 4	R/W	MIN_THR_T1[0]	0
Bit 3	R/W	MAX_THR_T1[3]	1
Bit 2	R/W	MAX_THR_T1[2]	1
Bit 1	R/W	MAX_THR_T1[1]	0
Bit 0	R/W	MAX_THR_T1[0]	1

MAX_THR_T1[3:0]:

Used to modify the Maximum Threshold for T1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a positive justification request in clock master mode.

MIN_TRH_T1[3:0]:

Used to modify the Minimum Threshold for T1 tributaries. The Minimum threshold is the FIFO depth below which a negative justification request is generated in clock master mode.

Register 0x01DB: EXSBI E1 Threshold Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_E1[3]	0
Bit 6	R/W	MIN_THR_E1[2]	0
Bit 5	R/W	MIN_THR_E1[1]	1
Bit 4	R/W	MIN_THR_E1[0]	0
Bit 3	R/W	MAX_THR_E1[3]	1
Bit 2	R/W	MAX_THR_E1[2]	1
Bit 1	R/W	MAX_THR_E1[1]	0
Bit 0	R/W	MAX_THR_E1[0]	1

MAX_THR_E1[3:0]:

Used to modify the Maximum Threshold for E1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a positive justification request in clock master mode.

MIN_TRH_E1[3:0]:

Used to modify the Minimum Threshold for E1 tributaries. The Minimum threshold is the FIFO depth below which a negative justification request is generated in clock master mode.

Register 0x01DC: EXSBI DS3 Threshold Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_DS3[3]	0
Bit 6	R/W	MIN_THR_DS3[2]	0
Bit 5	R/W	MIN_THR_DS3[1]	1
Bit 4	R/W	MIN_THR_DS3[0]	0
Bit 3	R/W	MAX_THR_DS3[3]	1
Bit 2	R/W	MAX_THR_DS3[2]	1
Bit 1	R/W	MAX_THR_DS3[1]	0
Bit 0	R/W	MAX_THR_DS3[0]	1

MAX_THR_DS3[3:0]:

Used to modify the Maximum Threshold for DS3 tributaries. The actual Maximum threshold used is the programmed value plus sixteen. The Maximum threshold is the FIFO depth which when exceeded will cause a positive justification request in clock master mode.

MIN_TRH_DS3[3:0]:

Used to modify the Minimum Threshold for DS3 tributaries. The Minimum threshold is the FIFO depth below which a negative justification request is generated in clock master mode.

Register 0x01DD: EXSBI E3 Threshold Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_E3[3]	0
Bit 6	R/W	MIN_THR_E3[2]	0
Bit 5	R/W	MIN_THR_E3[1]	1
Bit 4	R/W	MIN_THR_E3[0]	0
Bit 3	R/W	MAX_THR_E3[3]	1
Bit 2	R/W	MAX_THR_E3[2]	1
Bit 1	R/W	MAX_THR_E3[1]	0
Bit 0	R/W	MAX_THR_E3[0]	1

MAX_THR_E3[3:0]:

Used to modify the Maximum Threshold for E3 tributaries. The actual Maximum threshold used is the programmed value plus sixteen. The Maximum threshold is the FIFO depth which when exceeded will cause a positive justification request in clock master mode.

MIN_TRH_E3[3:0]:

Used to modify the Minimum Threshold for E3 tributaries. The Minimum threshold is the FIFO depth below which a negative justification request is generated in clock master mode.

Register 0x01DE EXSBI Depth Check Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	DC_ERRI	X

DC_ERRI:

This bit is set when a Depth Check error is detected. Reading this register clears this bit unless another Depth Check Interrupt is pending. Pending interrupts can occur when many links are reset simultaneously due to a reconfiguration or SBI bus resynchronization. Multiple pending interrupts can also occur on a single link when the DC_RSTEN bit is set, persisting until the link FIFO is stable.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI tributary associated with the FIFO buffer in which the depth check error was detected. Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. When an over run has not been detected the LINK field may contain an out of range link value. Values in these fields are only valid when DC_ERRI is a '1'.

Register 0x01DF Extract External ReSynch Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	FI_EMPTY_ENBL	0
Bit 6	R/W	FRACT_THR_HIGH	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	SBIIP_SYNCI	X
Bit 0	R	SAC1FP_SYNCI	X

SAC1FP_SYNCI:

This bit is set when a SAC1FP realignment has been detected. Reading this register clears this interrupt source.

SBIIP_SYNCI:

This bit is set when an internal SBI bus realignment has been detected. Reading this register clears this interrupt source.

FRACT_THR_HIGH:

This bit selects the FIFO threshold used for flow control of fractional rate links. When this bit is a logic 0 the fractional rate threshold is set to be 32. When this bit is logic 1 the fractional rate threshold is set to be 256. The fractional rate threshold determines the FIFO depth that must be exceeded before the SAJUST_REQ output is deasserted to request the fractional rate SBI transmitter cease transmission until SAJUST_REQ is asserted again. When the FIFO threshold exceeds the fractional rate threshold for a fractional rate link, SAJUST_REQ is de-asserted and when the FIFO threshold is lower than the fractional rate threshold for a fractional rate link SAJUST_REQ is asserted.

Setting FRACT_THR_HIGH to logic 1 is only required when there is a large time delay between the assertion of SAJUST_REQ and the assertion of SAPL in response. One should set FRACT_THR_HIGH to logic 0 if the application allows it to minimize the latency of the datapath.

FI_EMPTY_ENBL:

This bit should be set to logic 1 for correct operation.

If FI_EMPTY_ENBL is logic 1, no data bytes are emitted when a link FIFO empties. If FI_EMPTY_ENBL is logic 0, stuff bytes are generated when a FIFO is empty, thus causing slips. This bit is used globally to control behavior for all SPE_TYPEs.

1.19 INSBI Insert Scaleable Bandwidth Interconnect Registers

Register 0x01E0: INSBI Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	DC_RSTEN	1
Bit 5	R/W	DC_RESYNCE	0
Bit 4	R/W	FIFO_OVRE	0
Bit 3	R/W	FIFO_UDRE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	SBI_PAR_CTL	1

SBI_PAR_CTL:

The SBI_PAR_CTL bit is used to configure the Parity mode for generation of the SBI data parity signal, SDDP. When SBI_PAR_CTL is a logic 0 parity will be even. When SBI_PAR_CTL is a logic 1 parity will be odd.

FIFO_UDRE:

The FIFO_UDRE bit is used to enable/disable the generation of an interrupt when a FIFO underrun is detected. When FIFO_UDRE is a logic 1, the INTB output is asserted low when the SBI Add bus FIFO underruns.

FIFO_OVRE:

The FIFO_OVRE bit is used to enable/disable the generation of an interrupt when a FIFO overrun is detected. When FIFO_OVRE is a logic 1, the INTB output is asserted low when the SBI Add bus FIFO overruns.

DC_RESYNCE:

This DC_RESYNCE bit enables the generation of an interrupt when either a Depth Check error or an external resynchronization event occurs on either the SDC1FP or internal synchronization signals. When DC_RESYNCE is a 1 interrupts will be generated when one of the depth check or resynchronization errors occur. When DC_RESYNCE is a logic 0, the INTB output will not be asserted due to these events.

Depth check events should only happen when the SBI bus is misconfigured and will reset the link. SDC1FP resynchroniztion events will reset the entire SBI bus interface and are reported by the SDC1FP_SYNCI bit. Internal synchronization errors should only occur during configuration and are reported by the SBIIP_SYNCI.

DC_RSTEN:

The Depth check automatic reset enable bit, DC_RSTEN, allows the INSBI to automatically reset a link if it underruns or overruns. When DC_RSTEN is a 1 the link will automatically reset when a depth check error is detected. When DC_RSTEN is a 0 the link must be reset manually when a depth check error is detected and reported via the depth check error interrupt, DC_ERRI bit in the INSBI Depth Check Interrupt Status register.

When DC_RSTEN is a logic 0 interrupts must be enabled via the DC_RESYNCE interrupt enable bit. When DC_RSTEN is a 1 and depth check interrupts are enabled via DC_RESYNCE, multiple interrupts can be expected until the link FIFO is at the correct operating level.

Reserved:

These bits must be left as a logic 0 for proper operation.

Register 0x01E1: INSBI FIFO Underrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_UDRI	X

This interrupt status register is cleared when read.

If an underrun condition is reported for a link, the link should be reset by writing to the tributary control RAM location for the tributary corresponding to that link.

If an underrun condition is reported for a link, the link should be reset by writing to the tributary control RAM location for the tributary corresponding to that link.

Back to back reads of this register must be at least 250 ns apart.

This underrun interrupt register is the output of a priority encoder of the underrun history of all links. The most significant links have the highest priority and will be reported first if underruns occur simultaneously on multiple links.

If bit 0 is logic zero, no links have underrun since the last read, and all pending underrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is logic one, the register contents are valid, and indicate a link has underrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note that if a tributary is misbehaving so that it frequently underruns, the reporting of the multiple underruns can prevent the reporting of underruns on lower priority links. Such misbehaving links should be disabled (ENBL=0) to obtain the complete underrun history.

FIFO_UDRI:

This bit is set when a FIFO underrun is detected.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the underrun was detected.
Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.
LINK[4:0] and SPE[1:0] are invalid unless FIFO_UDRI is set.

Register 0x01E2: INSBI FIFO Overrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_OVRI	X

This interrupt status register is cleared when read.

If an overflow condition is reported for a link, the link should be reset by writing to the tributary control RAM location for the tributary corresponding to that link.

Back to back reads of this register must be at least 250 ns apart.

This Overrun interrupt register is the output of a priority encoder of the overrun history of all links. The most significant links have the highest priority and will be reported first if overruns simultaneously occur on multiple links.

If bit 0 is zero, no links have overrun since the last read, and all pending overrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is one, the register contents are valid, and indicate a link has overrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note that if a tributary is misbehaving so that it frequently overruns, the reporting of the multiple overruns can prevent the reporting of overruns on lower priority links. Such misbehaving links should be disabled (ENBL=0) to obtain the complete overrun history.

FIFO_OVRI:

This bit is set when a FIFO overrun is detected.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the overrun was detected.
Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.
LINK[4:0] and SPE[1:0] are invalid unless FIFO_OVRI is set.

Register 0x01E3: INSBI Tributary Register Indirect Access Address

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] fields are used to fully specify for which SBI tributary the Control register write or read operation will apply.
TRIB[4:0] specifies the SBI tributary number within the SBI SPE as specified by the SPE[1:0] field. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.

When an SPE is configured for E1, indirect accesses are not permitted to TRIB indexes b'10110 through b'11100. When an SPE is configured for DS3 or E3, indirect accesses are not permitted to TRIB indexes b'00010 through b'11100.

Reserved:

A logic 0 must be written to this bit for proper operation.

Register 0x01E4: INSBI Tributary Register Indirect Access Control

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RWB	0
Bit 0	R/W	Reserved	0

Reserved:

A logic 0 must be written to this bit for proper operation.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary control configuration RAM. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the Insert Tributary Control Indirect Access Data Register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the Insert Tributary Control Indirect Access Data Register.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when a write to this register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Data register or to determine when a new indirect write operation may commence. The BUSY bit is asserted for up to 4.32us after a page switch. If SREFCLK disappears during an access, the BUSY bit can stay high.

Register 0x01E6: INSBI Tributary Control Indirect Access Data

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	SYNCH_TRIB	0
Bit 4		Unused	X
Bit 3	R/W	TRIB_TYP[1]	0
Bit 2	R/W	TRIB_TYP[0]	0
Bit 1	R/W	ITVT	0
Bit 0	R/W	ENBL	0

ENBL:

The ENBL bit is used to enable the Tributary. Writing to the INSBI Tributary Register Indirect Access Control Register with the ENBL bit set to a logic 1 enables the INSBI to take tributary data from an internal link and transmit that data to the SBI tributary mapped to that link. This bit must also be set to a logic 1 when ingress Transparent VTs are enabled via the ITVT bit in this register.

If ENBL is logic 0, the SBI DROP bus is high impedance.

ITVT:

The Ingress Transparent Virtual Tributary bit, ITVT, selects a Transparent VT in place of the tributary specified by SPE[1:0] and TRIB[4:0] in the INSBI Insert Tributary Mapping Indirect Access Data Register. This capability is only applicable for VTs coming from the SONET/SDH mapper and will result in incorrect data for the selected tributary when used with the DS3 multiplexer. The ENBL bit in this register must also be set to logic 1 when ITVT is set to logic 1.

The Ingress VTPPs must not be bypassed when TVTs exist; the IVTPPBYP bit of the SONET/SDH Master Ingress VTPP Configuration register must be logic 0.

TRIB_TYP[1:0]

The TRIB_TYP[1:0] field is used to specify the characteristics of the SBI tributary as shown in the table Table 4.

Table 4 INSBI TRIB_TYP Encoding

TRIB_TYP	Description	CAS Enabled	Framed
00	Framed with CAS	True	True
01	Framed without CAS	False	True
10	Unframed	False	False
11	Reserved	X	X

The Reserved value for TRIB_TYP must not be used for proper operation of the TEMUX 84.

SYNCH_TRIB:

The Synchronous Tributary mode select bit, SYNCH_TRIB, sets the tributary to operate in synchronous mode on the SBI DROP bus. When SYNCH_TRIB is logic 1, the selected framed tributary DS0s or timeslots are locked in a fixed location within the SBI structure. In this mode the, corresponding T1/E1 framer must be operating synchronously to the SBI bus; therefore, the tributary must pass through the elastic store with its output timed to the SBI bus clock, SREFCLK. When SYNCH_TRIB is set to logic 1, the RX-SBI-ELST SYNCSBI bit for the tributary must also be set to logic 1 to ensure the elastic store is timed from the SBI bus clock. When SYNCH_TRIB is logic 0, the tributary is allowed to float within the SBI structure and there is no need for the elastic store.

Note that this bit must be set before the tributary is enabled and should only be changed when the tributary is disabled.

Register 0x01E7: INSBI MIN_DEPTH for T1 and E1 Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_DEP_E1[3]	0
Bit 6	R/W	MIN_DEP_E1[2]	1
Bit 5	R/W	MIN_DEP_E1[1]	1
Bit 4	R/W	MIN_DEP_E1[0]	1
Bit 3	R/W	MIN_DEP_T1[3]	0
Bit 2	R/W	MIN_DEP_T1[2]	1
Bit 1	R/W	MIN_DEP_T1[1]	1
Bit 0	R/W	MIN_DEP_T1[0]	1

MIN_DEP_E1[3:0]:

Used to modify the MIN_DEPTH for E1 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO.

MIN_DEP_T1[3:0]:

Used to modify the MIN_DEPTH for T1 tributaries. The Minimum Depth is the depth that must be reached before the FIFO reader starts to take data from the FIFO.

Register 0x01E9: INSBI T1 Thresholds Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_T1[3]	0
Bit 6	R/W	MIN_THR_T1[2]	1
Bit 5	R/W	MIN_THR_T1[1]	1
Bit 4	R/W	MIN_THR_T1[0]	0
Bit 3	R/W	MAX_THR_T1[3]	1
Bit 2	R/W	MAX_THR_T1[2]	1
Bit 1	R/W	MAX_THR_T1[1]	1
Bit 0	R/W	MAX_THR_T1[0]	0

MIN_THR_T1[3:0]:

Used to modify the Minimum Threshold for T1 tributaries. The Minimum threshold is the FIFO depth below which a positive justification is performed in clock master mode.

MAX_THR_T1[3:0]:

Used to modify the Maximum Threshold for T1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a negative justification in clock master mode.

MAX_THR_T1 should be set to 1100 to guarantee correct operation.

Register 0x01EA: INSBI E1 Thresholds Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_E1[3]	0
Bit 6	R/W	MIN_THR_E1[2]	0
Bit 5	R/W	MIN_THR_E1[1]	1
Bit 4	R/W	MIN_THR_E1[0]	0
Bit 3	R/W	MAX_THR_E1[3]	1
Bit 2	R/W	MAX_THR_E1[2]	1
Bit 1	R/W	MAX_THR_E1[1]	1
Bit 0	R/W	MAX_THR_E1[0]	0

MIN_THR_E1[3:0]:

Used to modify the Minimum Threshold for E1 tributaries. The Minimum threshold is the FIFO depth below which a positive justification is performed in clock master mode.

MAX_THR_E1[3:0]:

Used to modify the Maximum Threshold for E1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a negative justification in clock master mode.

MAX_THR_E1 should be set to 1010 to guarantee correct operation.

Register 0x01F1: INSBI Depth Check Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	DC_ERRI	X

DC_ERRI:

This bit is set when a Depth Check error is detected. Reading this register clears this bit unless another Depth Check Interrupt is pending. Pending interrupts can occur when many links are reset simultaneously due to a reconfiguration or SBI bus resynchronization. Multiple pending interrupts can also occur on a single link when the DC_RSTEN bit is set, persisting until the link FIFO is stable.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI tributary associated with the FIFO buffer in which the depth check error was detected. Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. When an over run has not been detected the LINK field may contain an out of range link value. Values in these fields are only valid when DCR_INTI is a '1'.

Register 0x01F2: Insert External ReSynch Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	SBIIP_SYNCI	X
Bit 0	R	SDC1FP_SYNCI	X

SDC1FP_SYNCI:

This bit is set when a SDC1FP realignment has been detected. Reading this register clears this interrupt source.

When operating with a 77.76MHz bus (i.e. the S77 input is high), this SDC1FP_SYNCI may not be asserted if the new alignment is within four SREFCLK cycles of the old alignment.

SBIIP_SYNCI:

This bit is set when an internal SBI bus realignment has been detected. Reading this register clears this interrupt source.

1.20 DS3/M13 Master Registers (N=0 to 2)

A set of registers is associated with each DS3 or E3. The inputs and outputs are referenced without their index.

Registers in the range 0x0200 to 0x02D5 correspond to DS3/E3 #1.

Registers in the range 0x0300 to 0x03D5 correspond to DS3/E3 #2.

Registers in the range 0x0400 to 0x04D5 correspond to DS3/E3 #3.

Register 0x0200 + 0x100*N: DS3 and E3 Master Reset

Bit	Type	Function	Default
Bit 7	R	RCLKA	X
Bit 6	R	TICLKA	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	PMONRST	0
Bit 0	R/W	RESET	0

RESET:

The RESET bit allows software to hold the DS3 M13 Mux in a reset condition. When RESET is a logic 1, the DS3 M13 multiplexer block and DS3/E3 framers and transmitters will be held in a reset state which is also a low power state. This will force all related registers to their default state. While in reset the clocks can not be guaranteed accurate or existing. When RESET is a logic 0, the DS3 M13 multiplexer block and DS3/E3 framers and transmitters are in normal operating mode.

PMONRST:

The performance monitor reset bit, PMONRST, forces the DS3/E3 PMON block into reset. When PMONRST is a logic 1 the DS3/E3 PMON block will be held in a reset state. When PMONRST is a logic 0 the DS3/E3 PMON block is in normal operating mode.

TICLKA:

The TICLK active, TICLKA, bit detects low to high transitions on the associated TICLK input. TICLKA is set to logic 1 on a rising edge of the associated TICLK, and is set to logic 0 when this register is read.

RCLKA:

The RCLK active, RCLKA, bit detects low to high transitions on the associated RCLK input. RCLKA is set to logic 1 on a rising edge of the associated RCLK, and is set to logic 0 when this register is read.

Register 0x0201 + 0x100*N: DS3 and E3 Master Data Source

Bit	Type	Function	Default
Bit 7	R/W	PLOOP	0
Bit 6	R/W	DLOOP	0
Bit 5	R/W	LLOOP	0
Bit 4	R/W	LOOPT	0
Bit 3	R/W	DLINV	0
Bit 2	R/W	SBICLKMODE	0
Bit 1	R/W	RCVCLR	0
Bit 0	R/W	E3DS3B	0

E3DS3B:

This bit determines the data rate and framing format for the combined DS3 and E3 interface. If E3DS3B is logic 1, the RCLK and TICLK inputs are expected to be 34.368MHz and the DS3 and E3 Line Side Interface data is expected to be in one of the two supported E3 formats. If E3DS3B is logic 0, the RCLK and TICLK inputs are expected to be 44.736MHz and the DS3 and E3 Line Side Interface data is expected to be DS3 frame formatted.

RCVCLR:

The DS3 and E3 clear channel bit, RCVCLR, bypasses the DS3 and E3 TRAN, which selects clear channel DS3 or E3 data to be accessed over the SBI bus or the DS3 or E3 system interface when the TEMUX 84 is configured for DS3/E3 framer only mode (i.e. OPMODE_SPEx[2:0] = 011). When RCVCLR is a logic 1 a clear channel DS3 or E3 is transmitted from the SBI bus or DS3/E3 system interface. When RCVCLR is a logic 0, the DS3 or E3 payload is accessed from the SBI bus or DS3/E3 system interface and DS3 framing is inserted by the TEMUX 84. This should only be set when the TEMUX 84 is configured for DS3/E3 framer only mode via the associated SPE Configuration register.

SBICLKMODE:

The SBI clock mode bit, SBICLKMODE, selects the egress clocking mode used over the SBI bus. When SBICLKMODE is a logic 1 and the TEMUX 84 is configured for DS3/E3 framer only mode over the SBI system interface via the associated SPE Configuration register, the TEMUX 84 is the egress clock

master and the egress clock will be TICLK or RCLK (if LOOPT is logic 1). When SBICLKMODE is a logic 0 and the TEMUX 84 is configured for DS3/E3 framer only mode over the SBI system interface, the TEMUX 84 is slave to the DS3/E3 clock from the SBI bus. The CLK_MSTR bit for TRIB_TYP[1] in the EXSBI Tributary Control Indirect Access Data must be set to match the setting of SBICLKMODE.

When SBICLKMODE is logic 0, the TCLK output clock will be highly jittered. The transmit clock and data must be jitter attenuated before being presented to a Line Interface Unit (LIU).

The SBICLKMODE bit must be set before the tributaries within the SBI are enabled.

DLINV:

The DLINV bit provides polarity control for the DS3 C-bit Parity path maintenance data link which is located in the 3 C-bits of M-subframe 5 or E3 G.832 datalink. When a logic 1 is written to DLINV, the received path maintenance data link is inverted before being processed and the transmitted path maintenance data link is inverted before insertion into the overhead. The rationale behind this bit is as follows: currently ANSI standard T1.107 specifies that the C-bits (which carry the path maintenance data link) be set to all zeros while the AIS maintenance signal is transmitted. The data link is obviously inactive during AIS transmission, and ideally the HDLC idle sequence (all ones) should be transmitted. By inverting the data link, the all zeros C-bit pattern becomes an idle sequence and the data link is terminated gracefully. Although this inversion is currently not specified in ANSI T1.107a, this bit is provided to safe-guard the TEMUX 84 in case the inversion is required in the future.

LOOPT:

The Transmit Timing Source Select bit selects the transmit timing source. When a logic 1 is written to LOOPT, the transmitter is loop-timed to the receiver. When loop timing is enabled, the receive clock RCLK is used as the transmit timing source. When a logic 0 is written to LOOPT, the transmit clock TICLK is used as the transmit timing source. Setting the LOOPT bit disables the effect of the TICLK bit. The transition from internal to looptiming is not hitless. This will not cause any long-term problems.

If the SBI bus is being used, the SBICLKMODE bit must be logic 1 if LOOPT is logic 1.

LLOOP:

The LLOOP bit controls the line loopback. When a logic 0 is written to LLOOP, line loopback is disabled. When a logic 1 is written to LLOOP, the stream received on RPOS/RDAT and RNEG/RLCV is looped to the TPOS/TDAT and TNEG/TMFP outputs. Note that the TPOS, TNEG, and TCLK outputs are referenced to RCLK when LLOOP is logic 1.

A DS3 demapped from the Telecom Drop Bus may also be looped back to the Add Bus.

DLOOP:

The DLOOP bit controls the diagnostic loopback. When a logic 0 is written to DLOOP, diagnostic loopback is disabled. When a logic 1 is written to DLOOP, the transmit data stream is looped in the receive direction. The DLOOP should not be set to a logic 1 when either the PLOOP, LLOOP, or LOOPT bit is a logic 1. The TUNI register bit in the DS3/E3 Transmit Line Options register should be set to the same value as the UNI bit in the DS3 FRMR Configuration or E3 FRMR Framing Options register.

PLOOP:

The PLOOP bit controls the E3 and DS3 payload loopback. When a logic 0 is written to PLOOP, DS3 or E3 payload loopback is disabled. When a logic 1 is written to PLOOP, the DS3 or E3 overhead bits are regenerated and inserted into the received DS3 or E3 stream and the resulting stream is transmitted. Setting the PLOOP bit disables the effect of the TICLK bit in the TEMUX 84 Transmit Line Options register, thereby forcing flow-through timing. TXGAPEN in the DS3 and E3 Master Unchannelized Interface Options register must be set to logic 0 when payload loopback is enabled.

Register 0x0202 + 0x100*N: DS3 and E3 Master Unchannelized Interface Options

Bit	Type	Function	Default
Bit 7	R/W	TDATIFALL	0
Bit 6	R/W	TXGAPEN	0
Bit 5	R/W	TXMFPO	0
Bit 4	R/W	TXMFPI	0
Bit 3	R/W	TXSBI	0
Bit 2	R/W	RXMFPO	0
Bit 1	R/W	RXGAPEN	0
Bit 0	R/W	RSCLKR	0

This register controls the framer only system side interface for unchannelized DS3 and E3 operation.

RSCLKR:

The RSCLKR bit has effect only when DS3/E3 framer only mode is selected in the associated SPE Configuration register. When RSCLKR is a logic 1, the RDATO, RMFPO, and ROVRHD outputs are updated on the rising edge of RSCLK. When RSCLKR is a logic 0, the RDATO, RMFPO, and ROVRHD outputs are updated on the falling edge of RSCLK. If the RXGAPEN bit is a logic 1, then RSCLKR affects RGAPCLK in the same manner as it affects RSCLK.

RXGAPEN:

The RXGAPEN bit configures the TEMUX 84 to enable the RGAPCLK outputs. When RXGAPEN is a logic 1, then the RGAPCLK output is enabled. When RXGAPEN is a logic 0, then the RSCLK output is enabled. DS3/E3 framer only mode must be selected in the associated SPE Configuration register for RXGAPEN to have affect.

RXMFPO:

The RXMFPO bit controls which of the outputs RMFPO or RFPO is valid. If RXMFPO is a logic 1, then RMFPO will be available. If RXMFPO is a logic 0,

then RFPO will be available. This bit has effect only if DS3/E3 framer only mode is selected in the associated SPE Configuration register.

TXSBI:

The TXSBI bit controls the source of the unchannelized DS3/E3. If TXSBI is logic 1, the transmit DS3/E3 is sourced from the SBI interface. If TXSBI is logic 0, the, the transmit DS3/E3 is sourced from the DS3/E3 System Interface (i.e. TDATI[x]).

This bit has no effect on the receive direction. The unchannelized DS3/E3 is always presented on both the receive DS3/E3 System Interface (i.e. RDATO[x]) and the SBI interface if enabled to carry DS3.

If TXSBI is logic 1, the TXGAPEN bit must be logic 0.

TXMFPI:

The TXMFPI bit controls which of the inputs TMFPI or TFPI is valid. If TXMFPI is a logic 1, then TMFPI will be expected. If TXMFPI is a logic 0, then TFPI will be expected. This bit has effect only if DS3/E3 framer only mode is selected in the associated SPE Configuration register.

If the DS3/E3 data is being sourced from the SBI bus (i.e. TXSBI = 1), TXMFPI must be a logic 1. Also, this bit should be set to logic 1 for unchannelized M23 applications (i.e. CBIT bit of the DS3 TRAN Configuration register is logic 0) to ensure the C-bits that are not overwritten align to the correct M-subframe.

TXMFPO:

The TXMFPO bit controls which of the outputs TMFPO or TFPO is valid. If TXMFPO is a logic 1, then TMFPO will be available. If TXMFPO is a logic 0, then TFPO will be available. This bit has effect only if DS3/E3 framer only mode is selected in the associated SPE Configuration register and the TXGAPEN bit is a logic 0.

TXGAPEN:

The TXGAPEN bit configures the TEMUX 84 to enable the TGAPCLK output. When TXGAPEN is a logic 1, then the TGAPCLK output is enabled. When TXGAPEN is a logic 0, then either the TFPO or TMFPO output is enabled, depending on the setting of the TXMFPO register bit. DS3/E3 framer only mode must be selected in the associated SPE Configuration register for TXGAPEN to have affect.

TDATIFALL:

The TDATIFALL bit configures the sampling edge of the DS3 or E3 framer transmit data signal, TDATI, the sampling edge of the framer transmit framing pulse input signal TFPI/TMFPI and the updating edge of the framer transmit framing pulse output signal TFPO/TMFPO. When TDATIFALL is a logic 1, TDATI and TFPI/TMFPI will be sampled on the falling edge of TICLK when TXGAPEN is a logic zero, and will be sampled on the falling edge of TGAPCLK when TXGAPEN is a logic 1. When TDATIFALL is a logic 0, TDATI and TFPI/TMFPI will be sampled on the rising edge of either TICLK or TGAPCLK. TFPO/TMFPO will be updated on the falling edge of TICLK when TDATIFALL is a logic 0 and on the rising edge when TDATIFALL is a logic 1.

Register 0x0203 + 0x100*N: DS3/E3 Master Transmit Line Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	PRGD_EN	0
Bit 4	R/W	TICLK	0
Bit 3	R/W	TNEGINV	0
Bit 2	R/W	TPOSINV	0
Bit 1	R/W	TRISE	0
Bit 0	R/W	TUNI	0

Reserved:

The reserved bit must be logic 0 for correct operation.

TICLK:

The Transmit Clocking Select bit selects the transmit clock used to update the TPOS/TDAT and TNEG/TMFP outputs. When a logic 0 is written to TICLK, the buffered version of the input transmit clock, TCLK, is used to update TPOS/TDAT and TNEG/TMFP on the edge selected by the TRISE bit. When a logic 1 is written to TICLK, TPOS/TDAT and TNEG/TMFP are updated by TICLK on the edge selected by the TRISE bit, eliminating the flow-through TCLK signal. The TICLK bit has no effect if the LOOPT bit or the PLOOP bit in the DS3/E3 Master Data Source register is a logic 1.

For channelized DS3 applications using the DS3 LIU interface, setting the TICLK bit to logic 1 requires the TXSBI bit of Register 0x202+ 0x100*N: DS3 and E3 Master Unchannelized Interface Options be set to logic 1 or the SBICLKMODE bit of Register 0x0201 + 0x100*N: DS3 and E3 Master Data Source be set to logic 1.

TNEGINV:

The TNEGINV bit provides polarity control for outputs TNEG/TMFP. When a logic 0 is written to TNEGINV, the TNEG/ TMFP output is not inverted. When a logic 1 is written to TNEGINV, the TNEG/ TMFP output is inverted. The TNEGINV bit setting does not affect the loopback data in diagnostic loopback.

TNEGINV must be a logic 0 when mapping the DS3 signal into the SONET/SDH line interface through the D3MA block.

TPOSINV:

The TPOSINV bit provides polarity control for outputs TPOS/TDAT. When a logic 0 is written to TPOSINV , the TPOS/TDAT output is not inverted. When a logic 1 is written to TPOSINV , the TPOS/TDAT output is inverted. The TPOSINV bit setting does not affect the loopback data in diagnostic loopback.

TPOSINV must be a logic 0 when mapping the DS3 signal into the SONET/SDH line interface through the D3MA block.

TRISE:

The TRISE bit provides clock edge control for the outputs TPOS/TDAT and TNEG/TMFP. When a logic 0 is written to TRISE, TPOS/TDAT and TNEG/TMFP are updated on the falling edge of TCLK or TICLK as selected by the TICLK bit. When a logic 1 is written to TRISE, TPOS/TDAT and TNEG/TMFP are updated on the rising edge of TCLK or TICLK.
TRISE must be a logic 0 when mapping the DS3 signal into the SONET/SDH line interface through the D3MA block.

TUNI:

The transmit unipolar bit configures the DS3/E3 transmit interface for unipolar or dual rail operation. When TUNI is a logic 1, the transmit interface is configured as TDAT and TMFP. When TUNI is a logic 0, the transmit interface is configured as TPOS and TNEG.

TUNI must be a logic 1 when mapping the DS3 signal into the SONET/SDH line interface through the D3MA block.

PRGD_EN:

The PRGD enable bit, PRGD_EN, controls the insertion of the PRGD pattern generator in the transmit DS3 and E3 path. When PRGD_EN is a logic 1 the PRGD pattern is inserted in the transmit DS3 payload and will overwrite everything except the DS3 or E3 framing bits. When PRGD_EN is a logic 0 the PRGD pattern generator is removed from the transmit path.

Register 0x0204 + 0x100*N: DS3/E3 Master Receive Line Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	RNEGINV	0
Bit 1	R/W	RPOSINV	0
Bit 0	R/W	RFALL	0

RNEGINV:

The RNEGINV bit provides polarity control for input RNEG/RLCV. When a logic 0 is written to RNEGINV, the input RNEG/RLCV is not inverted. When a logic 1 is written to RNEGINV, the input RNEG/RLCV is inverted. The RNEGINV bit setting does not affect the loopback data in diagnostic loopback.

RNEGINV must be a logic 0 when demapping the DS3 signal from the SONET/SDH line interface through the D3MD block.

RPOSINV:

The RPOSINV bit provides polarity control for input RPOS/RDAT. When a logic 0 is written to RPOSINV , the input RPOS/RDAT is not inverted. When a logic 1 is written to RPOSINV , the input RPOS/RDAT is inverted. The RPOSINV bit setting does not affect the loopback data in diagnostic loopback.

RPOSINV must be a logic 0 when demapping the DS3 signal from the SONET/SDH line interface through the D3MD block.

RFALL:

The RFALL bit provides polarity control for input RCLK. When a logic 0 is written to RFALL, RPOS/RDAT and RNEG/RLCV are sampled on the rising edge of RCLK. When a logic 1 is written to RFALL, RPOS/RDAT and RNEG/RLCV are sampled on the falling edge of RCLK.

RFALL must be a logic 0 when demapping the DS3 signal from the SONET/SDH line interface through the D3MD block.

Register 0x0205 + 0x100*N: DS3/E3 Master Alarm Enable

Bit	Type	Function	Default
Bit 7	R/W	FEBEEN	0
Bit 6	R/W	ALTFEBE	0
Bit 5	R/W	REDEN	0
Bit 4	R/W	AISEN	0
Bit 3	R/W	OOFEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	RED3ALME	0
Bit 0	R/W	DS3ALME	0

FEBEEN:

The Far End Block Error Enable bit enables the automatic generation of the transmit DS3 or E3 FEBE during all receive frame conditions. When FEBEEN is a logic 1, a FEBE will be generated in the C-bit Parity DS3 or E3 G.832 transmit stream during a receive OOF condition. When FEBEEN is a logic 0, transmit FEBE indications will not be generated during receive OOF.

ALTFEBE:

The Alternate Far End Block Error bit selects the error conditions detected to define a FEBE indication. If ALTFEBE is a logic 1, a FEBE indication is generated if either one or more framing bit errors or a C-bit parity error has occurred in the last received M-frame. If no framing bit errors nor C-bit parity errors have occurred, then no FEBE is generated. If ALTFEBE is a logic 0, a FEBE indication is generated in the outgoing C-bit Parity DS3 transmit stream if a C-bit parity error occurred in the last received M-frame. If no C-bit parity error occurred, no FEBE is generated.

This bit only has effect for DS3, not E3.

REDEN:

The REDEN bit enables the receive RED alarm (persistent out of frame) indication to automatically generate a FERF (aka RAI) indication in the DS3 transmit stream. When REDEN is logic 1, assertion of the RED indication by the DS3 framer causes a FERF to be transmitted by the DS3 transmitter for the duration of the RED assertion. Also the OOFEN bit is internally forced to

logic 0 when REDEN is logic 1. When REDEN is logic 0, assertion of the RED indication does not cause transmission of a FERF.

REDEN has no effect on E3 operation.

AISEN:

The AISEN bit enables the receive alarm indication signal to automatically generate a FERF indication in the DS3/E3 transmit stream. When AISEN is logic 1, assertion of the AIS indication by the DS3 or E3 framer causes a FERF to be transmitted by the DS3 or E3 TRAN for the duration of the AIS assertion. When AISEN is logic 0, assertion of the AIS indication does not cause transmission of a FERF.

OOFEN:

The OOFEN bit enables the receive out of frame indication to automatically generate a FERF indication in the DS3 or E3 transmit stream. This bit only operates when the REDEN bit is logic 0. When OOFEN is logic 1, assertion of the OOF indication by the framer causes a FERF to be transmitted by TRAN for the duration of the OOF assertion. When OOFEN is logic 0, assertion of the OOF indication does not cause transmission of a FERF.

LOSEN:

The LOSEN bit enables the receive loss of signal indication to automatically generate a FERF in the DS3 transmit stream. When LOSEN is logic 1, assertion of the LOS indication by the DS3 framer causes a FERF to be transmitted by TRAN for the duration of the LOS assertion. When LOSEN is logic 0, assertion of the LOS indication does not cause transmission of a FERF.

RED3ALME:

The RED DS3 Alarm Enable bit works in conjunction with the DS3ALME bit and enables detection of DS3 RED condition to be used in place of DS3 loss of signal and DS3 out-of-frame in the above criteria for demultiplexed AIS generation. When DS3ALME is set to logic 1 and REDALME is set to logic 1, the occurrence of LOS or OOF for 127 consecutive M-frames (or 21 consecutive M-frames, if FDET is set to logic 1 in the DS3 FRMR configuration register) causes a DS3 RED alarm condition and generates the DS2 AIS. When DS3ALME is set to logic 1 and REDALME is set to logic 0, any occurrence of LOS or OOF generates the DS2 AIS. If DS3ALME is a logic 0, the REDALME bit is ignored.

DS3ALME:

The DS3 Alarm Enable bit allows the automatic generation of AIS in all of the demultiplexed DS2s upon a DS3 alarm condition. If DS3ALME is a logic 1, a DS3 loss of signal (>175 zeros), a DS3 out-of-frame (OOF) condition (i.e. immediately after 3-of-n F-bit errors where n is 8 or 16, or 3-of-4 M-frames containing M-bit errors), DS3 idle code detection or DS3 AIS detection causes all of the DS2s to be replaced by an unframed all ones pattern immediately. Generation of AIS continues while the detected alarm condition persists. If DS3ALME is a logic 0, AIS can still be generated in the demultiplexed DS2s under software control by setting the bits in the MX23 Demux AIS Insert Register.

In unchannelized DS3 or E3 applications, the stated criteria causes all ones to be presented on RDATO[N+1] and/or inserted into the SBI DS3/E3 payload. The ALM bit on the SBI Drop bus is also set to logic 1 for the duration of the alarm.

Register 0x0206 + 0x100*N: DS2 Master Alarm Enable / DS3 Network Requirement Bit

Bit	Type	Function	Default
Bit 7	R/W	TNR	1
Bit 6	R	RNR	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RED2ALME	0
Bit 0	R/W	DS2ALME	0

TNR:

The Transmit Network Requirement (TNR) bit determines the value inserted into the Network Requirement (N_r) bit transmitted in the second C-bit in M-subframe 1 when in DS3 C-bit parity mode. A logic 1 in the TNR bit causes a one to be transmitted in the N_r overhead bit timeslot. The TNR bit is set to a logic 1 upon either a hardware or software reset. If C-bit parity is not selected, the TNR bit has no effect.

When the TEMUX 84 is set for transmission of DS3 AIS via the DS3 TRAN Configuration register Bit 6 in C-bit parity mode, all C-bits are forced to 0 except for the network requirement bit which is forced to the TNR register bit value. The TNR bit must be cleared when TRAN is enabled to generate AIS in C-bit parity mode.

RNR:

The Receive Network Requirement bit reflects the real time value of the Network Requirement (N_r) bit presented in the second C-bit in M-subframe 1 when in DS3 C-bit parity mode. The RNR bit is a logic 1 if a logic one occurs in the N_r overhead bit timeslot. If C-bit parity is not selected, the value of RNR is meaningless and random.

RED2ALME:

The RED DS2 Alarm Enable (RED2ALME) bit works in conjunction with the DS2ALME and enables detection of DS2 RED condition to be used in place of DS2/G.747 out-of-frame in the above criteria for demultiplexed AIS generation. When DS2ALME is set to logic 1 and RED2ALME is set to logic 1, the occurrence of OOF for 53 consecutive DS2/G.747 "M-frames" causes a DS2 RED alarm condition and generates the DS1 AIS. When DS2ALME is set to logic 1 and RED2ALME is set to logic 0, any occurrence of OOF generates the DS1 AIS. If DS2ALME is a logic 0, the RED2ALME bit is ignored.

DS2ALME:

The DS2 Alarm Enable (DS2ALME) bit allows the automatic generation of AIS in the DS1s demultiplexed from a DS2 or G.747 stream which is in an alarm condition. If DS2ALME is a logic 1,a DS2 or G.747 out-of-frame (OOF) condition (i.e. immediately after 2-of-n F-bit errors where n is 4 or 5, or 3-of-4 M-frames containing M-bit errors for DS2, or immediately after 4 consecutive framing word errors for G.747) or detection of DS2 or G.747 AIS causes each of the associated DS1s to be replaced by an unframed all ones pattern immediately. If DS2ALME is a logic 0, AIS can still be generated in the demultiplexed DS1s under software control by setting the bits in the appropriate MX12 AIS Insert Register. Note that the removal of the auto all-ones insertion is performed upon the first DS2 M-frame or G.747 frame pulse after the DS2 FRMR has found frame alignment.

Register 0x0207 + 0x100*N: E3 Data Link Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	PYLD&JUST	0
Bit 1	R/W	TNETOP	0
Bit 0	R/W	RNETOP	0

RNETOP:

The RNETOP bit enables the Network Operator Byte (NR) extracted from the G.832 E3 stream to be terminated by the internal HDLC receiver, RDLC. When RNETOP is logic 1, the NR byte is extracted from the G.832 stream and terminated by RDLC. When RNETOP is logic 0, the GC byte is extracted from the G.832 stream and terminated by RDLC. Both the NR byte and the GC byte are extracted and output on the ROH pin for external processing.

RNETOP only has effect in E3 mode.

TNETOP:

The TNETOP bit enables the Network Operator Byte (NR) inserted in the G.832 E3 stream to be sourced by the internal HDLC transmitter, TDPR. When TNETOP is logic 1, the NR byte is inserted into the G.832 stream through the TDPR block. When TNETOP is logic 0, the GC byte is inserted into the G.832 stream through the TDPR block. All ones signal will be inserted into the NR byte.

For G.751 E3 streams, the National Use bit is sourced by the TDPR block if TNETOP and the NATUSE bit (from the E3 TRAN Configuration Register) are both logic 0. If either TNETOP or NATUSE is logic 1, the National Use bit will be logic 0.

TNETOP only has effect in E3 mode.

PYLD&JUST:

The PYLD&JUST bit selects whether the bits available for justification (i.e. bits 5 through 8 of Set IV) in framing mode G.751 are indicated as overhead or payload for the purposes of generating the TGAPCLK output and for PRBS insertion. When PYLD&JUST is logic 1, TGAPCLK output will not be gapped during the bits available for justification and PRBS may be inserted into the same bits. When PYLD&JUST is logic 0, TGAPCLK output will be gapped during the bits available for justification and PRBS will not be inserted into the same bits.

Note that the justification service bits (i.e. bits 1 through 4 for Sets II, III and IV) are always treated as overhead. This is different than the treatment by the E3 framer as determined by the PYLD&JUST bit of the E3 FRMR Maintenance Options register.

1.21 DS3 TRAN Transmitter Registers

Register 0x0208 + 0x100*N: DS3 TRAN Configuration

Bit	Type	Function	Default
Bit 7	R/W	CBTRAN	0
Bit 6	R/W	AIS	0
Bit 5	R/W	IDL	0
Bit 4	R/W	FERF	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1	R/W	TSIG	0
Bit 0	R/W	CBIT	0

CBIT:

The CBIT bit enables the DS3 C-bit parity application. When CBIT is written with a logic 1, C-bit parity is enabled, and the TEMUX 84 modifies the C-bits as required to include the path maintenance data link, the FEAC channel, the far end block error indication, and the path parity. When CBIT is written with a logic 0, the M23 application is selected, and the C-bits are passed transparently through the DS3 TRAN.

TSIG:

The TSIG bit forces a 100… pattern on TDAT, or the corresponding encoded 100… signal on the B3ZS outputs, TPOS and TNEG. The test signal is inserted when TSIG is logic 1, and disabled when TSIG is logic 0. The signal insertion is provided for test purposes, and will overwrite any input data stream. The signal provides a minimum number of transitions on the encoded B3ZS output signal to allow pulse mask testing.

FERF:

The FERF bit enables insertion of the far end receive failure maintenance signal in the DS3 stream. When FERF is written with a logic 1, the X1 and X2 overhead bit positions are set to logic 0. When FERF is written with a logic 0, the X1 and X2 overhead bit positions in the DS3 stream are set to logic 1.

IDL:

The IDL bit enables the transmission of the DS3 Idle signal. When IDL is logic 1, the incoming DS3 data stream is overwritten with the pattern 1100… When CBTRAN is logic 0 and IDL is logic 1, the C-bits in the third M-subframe are set to 0. When CBTRAN is logic 1, all C-bits are passed transparently.

AIS:

The AIS bit enables the transmission of the DS3 alarm indication signal. When AIS is logic 1, the incoming DS3 data stream is overwritten with the pattern 1010... When CBTRAN is logic 0 and AIS is logic 1, the C-bits are all set to 0 with the exception of the network requirement bit which is forced to the TNR register bit value. When CBTRAN is logic 1, all C-bits are passed transparently. When this bit is set to logic 1, the CBIT bit in this register must also be set to logic 1.

CBTRAN:

The CBTRAN bit controls the C-bits during AIS and IDLE transmission. When CBTRAN is a logic 0, the C-bits are overwritten with zeros during AIS transmission (as is currently specified in ANSI T1.107a Section 8.1.3.1). The only exception is the network requirement bit in C-bit parity mode, which is forced to the TNR register bit value as specified in the DS3 Network Requirement Bit register. During IDLE transmission and CBTRAN is a logic 0 the C-bits in the third M-subframe are overwritten with zeros. When CBTRAN is a logic 1 and the M23 application is enabled, the C-bits pass through transparently during AIS and IDLE transmission. When CBTRAN is a logic 1, and the C-bit parity application is enabled, the C-bits are overwritten with the appropriate C-bit parity functions during AIS and IDLE transmission.

Reserved:

The reserved bit must be programmed to logic 0 for proper operation.

Register 0x0209 + 0x100*N: DS3 TRAN Diagnostic

Bit	Type	Function	Default
Bit 7	R/W	DLOS	0
Bit 6	R/W	DLCV	0
Bit 5		Unused	X
Bit 4	R/W	DFERR	0
Bit 3	R/W	DMERR	0
Bit 2	R/W	DCPERR	0
Bit 1	R/W	DPERR	0
Bit 0	R/W	DFEBE	0

DFEBE:

The DFEBE bit controls the insertion of far end block errors in the DS3 stream. When DFEBE is written with a logic 1, and the C-bit parity application is enabled, the three C-bits in M-subframe 4 are set to a logic 0. When DFEBE is written with a logic 0, FEBEs are indicated based on receive framing bit errors and path parity errors.

DPERR:

The DPERR bit controls the insertion of parity errors (P-bit errors) in the DS3 stream. When DPERR is written with a logic 1, the P-bits are inverted before insertion. When DPERR is written with a logic 0, the parity is calculated and inserted normally.

DCPERR:

The DCPERR bit controls the insertion of path parity errors in the DS3 stream. When DCPERR is written with a logic 1 and the C-bit parity application is enabled, the three C-bits in M-subframe 3 are inverted before insertion. When DCPERR is written with a logic 0, the path parity is calculated and inserted normally.

DMERR:

The DMERR bit controls the insertion of M-bit framing errors in the DS3 stream. When DMERR is written with a logic 1, the M-bits are inverted before

insertion. When DMERR is written with a logic 0, the M-bits are inserted normally.

DFERR:

The DFERR bit controls the insertion of F-bit framing errors in the DS3 stream. When DFERR is written with a logic 1, the F-bits are inverted before insertion. When DFERR is written with a logic 0, the F-bits are inserted normally.

DLCV:

The DLCV bit controls the insertion of a single line code violation in the DS3 stream. When DLCV is written with a logic 1, a line code violation is inserted by generating an incorrect polarity of violation in the next B3ZS signature. The data being transmitted must therefore contain periods of three consecutive zeros in order for the line code violation to be inserted. For example, line code violations may not be inserted when transmitting AIS, but may be inserted when transmitting the idle signal. DLCV is automatically cleared upon insertion of the line code violation.

DLOS:

The DLOS bit controls the insertion of loss of signal in the DS3 stream. When DLOS is written with a logic 1, the data on outputs TPOS/TDAT and TNEG/TMFP is forced to continuous zeros.

1.22 DS3 FRMR Receive Framer Registers

Register 0x020C + 0x100*N: DS3 FRMR Configuration

Bit	Type	Function	Default
Bit 7	R/W	AISPAT	1
Bit 6	R/W	FDET	0
Bit 5	R/W	MBDIS	0
Bit 4	R/W	M3O8	0
Bit 3	R/W	UNI	0
Bit 2	R/W	REFR	0
Bit 1	R/W	AISC	0
Bit 0	R/W	CBE	0

CBE:

The CBE bit enables the DS3 C-bit parity application. When a logic 1 is written to CBE, C-bit parity mode is enabled. When a logic 0 is written to CBE, the DS3 M23 format is selected. While the C-bit parity application is enabled, C-bit parity error events, far end block errors are accumulated.

AISC:

The AISC bit controls the algorithm used to detect the alarm indication signal (AIS). When a logic 1 is written to AISC, the algorithm checks that a framed DS3 signal with all C-bits set to logic 0 is observed for a period of time before declaring AIS. The payload contents are checked to the pattern selected by the AISPAT bit. When a logic 0 is written to AISC, the AIS detection algorithm is determined solely by the settings of AISPAT and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

REFR:

The REFR bit initiates a DS3 reframe. When a logic 1 is written to REFR, the TEMUX 84 is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a low to high transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transition.

UNI:

The UNI bit configures the TEMUX 84 to accept either dual-rail or single-rail receive DS3 streams. When a logic 1 is written to UNI, the TEMUX 84 accepts a single-rail DS3 stream on RDAT. The TEMUX 84 accumulates line code violations on the RLCV input. When a logic 0 is written to UNI, the TEMUX 84 accepts B3ZS-encoded dual-rail data on RPOS and RNEG. UNI must be set to a logic 1 when demapping the DS3 signal from the SONET/SDH interface through the D3MD block.

M3O8:

The M3O8 bit controls the DS3 out of frame decision criteria. When a logic 1 is written to M3O8, DS3 out of frame is declared when 3 of 8 framing bits (F-bits) are in error. When a logic 0 is written to M3O8, the 3 of 16 framing bits in error criteria is used, as recommended in ANSI T1.107

MBDIS:

The MBDIS bit disables the use of M-bit errors as a criteria for losing frame alignment. When MBDIS is set to logic 1, M-bit errors are disabled from causing an OOF; the loss of frame criteria is based solely on the number of F-bit errors selected by the M3O8 bit. When MBDIS is set to logic 0, errors in either M-bits or F-bits are enabled to cause an OOF. When MBDIS is logic 0, an OOF can occur when one or more M-bit errors occur in 3 out of 4 consecutive M-frames, or when the F-bit error ratio selected by the M3O8 bit is exceeded.

FDET:

The FDET bit selects the fast detection timing for AIS, IDLE and RED. When FDET is set to logic 1, the AIS, IDLE, and RED detection time is 2.23 ms; when FDET is set to logic 0, the detection time is 13.5 ms.

AISPAT:

The AISPAT bit controls the pattern used to detect the alarm indication signal (AIS). When a logic 1 is written to AISPAT, the AIS detection algorithm checks that a framed DS3 signal containing the repeating pattern 1010... is present. The C-bits are checked for the value specified by the AISC bit setting. When a logic 0 is written to AISPAT, the AIS detection algorithm is determined solely by the settings of AISC and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

Register 0x020D + 0x100*N: DS3 FRMR Interrupt Enable (ACE=0)

Bit	Type	Function	Default
Bit 7	R/W	COFAE	0
Bit 6	R/W	REDE	0
Bit 5	R/W	CBITE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	IDLE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	OOFE	0
Bit 0	R/W	LOSE	0

LOSE:

The LOSE bit enables interrupt generation when a DS3 loss of signal defect is declared or removed. The interrupt is enabled when a logic 1 is written.

OOFE:

The OOFE bit enables interrupt generation when a DS3 out of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

AISE:

The AISE bit enables interrupt generation when the DS3 AIS maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

IDLE:

The IDLE bit enables interrupt generation when the DS3 IDLE maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

FERFE:

The FERFE bit enables interrupt generation when a DS3 far end receive failure defect is declared or removed. The interrupt is enabled when a logic 1 is written.

CBITE:

The CBITE bit enables interrupt generation when the TEMUX 84 detects a change of state in the DS3 application identification channel. The interrupt is enabled when a logic 1 is written.

REDE:

The REDE bit enables an interrupt to be generated when a change of state of the DS3 RED indication occurs. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register. When REDE is set to logic 1, the interrupt output, INTB, is set to logic 0 when the state of the RED indication changes.

COFAE:

The COFAE bit enables interrupt generation when the TEMUX 84 detects a DS3 change of frame alignment. The interrupt is enabled when a logic 1 is written.

Register 0x020D + 0x100*N: DS3 FRMR Additional Configuration (ACE=1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	AISONES	0
Bit 4	R/W	BPVO	0
Bit 3	R/W	EXZSO	0
Bit 2	R/W	EXZDET	0
Bit 1	R/W	SALGO	0
Bit 0	R/W	DALGO	0

<u>DALGO:</u>

The DALGO bit determines the criteria used to decode a valid B3ZS signature. When DALGO is set to logic 1, a valid B3ZS signature is declared and 3 zeros substituted whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen. When the DALGO bit is set to logic 0, a valid B3ZS signature is declared and the 3 zeros are substituted whenever a zero followed by a bipolar violation is observed.

<u>SALGO:</u>

The SALGO bit determines the criteria used to establish a valid B3ZS signature used to map BPVs to line code violation indications. Any BPV that is not part of a valid B3ZS signature is indicated as an LCV. When the SALGO bit is set to logic 1, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation is observed. When SALGO is set to logic 0, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen.

<u>EXZDET:</u>

The EXZDET bit determines the type of zero occurrences to be included in the LCV indication. When EXZDET is set to logic 1, the occurrence of an excessive zero generates a single pulse indication that is used to indicate an LCV. When EXZDET is set to logic 0, every occurrence of 3 consecutive zeros generates a pulse indication that is used to indicate an LCV. For example, if a sequence of 15 consecutive zeros were received, with EXZDET=1 only a single LCV would be indicated for this string of excessive

zeros; with EXZDET=0, five LCVs would be indicated for this string (i.e. one LCV for every 3 consecutive zeros).

EXZSO:

The EXZSO bit enables only summed zero occurrences to be accumulated in the PMON EXZS Count Registers. When EXZSO is set to logic 1, any excessive zeros occurrences over an 85 bit period increments the PMON EXZS counter by one. When EXZSO is set to logic 0, summed LCVs are accumulated in the PMON EXZS Count Registers. A summed LCV is defined as the occurrence of either BPVs not part of a valid B3ZS signature or 3 consecutive zeros (or excessive zeros if EXZDET=1) occurring over an 85 bit period; each summed LCV occurrence increment the PMON EXZS counter by one.

BPVO:

The BPVO bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. When BPVO is set to logic 1, only BPVs not part of a valid B3ZS signature generate an LCV indication and increment the PMON LCV counter. When BPVO is set to logic 0, both BPVs not part of a valid B3ZS signature, and either 3 consecutive zeros or excessive zeros generate an LCV indication and increment the PMON LCV counter.

Table 5 DS3 FRMR EXZS/LCV Count Configurations

Register Bit			Counter Function	
EXZSO	**BPVO**	**EXZDET**	**PMON EXZ Count**	**PMON LCV Count**
0	0	0	Summed LCVs	BPVs & every 3 consecutive zeros
0	0	1	Summed LCVs	BPVs & every string of 3+ consecutive zeros
0	1	0	Reserved	Reserved
0	1	1	Reserved	Reserved
1	0	0	Summed excessive zeros	BPVs & every 3 consecutive zeros
1	0	1	Summed excessive zeros	BPVs & every string of 3+ consecutive zeros
1	1	0	Summed excessive zeros	Only BPVs
1	1	1	Summed excessive zeros	Only BPVs

AISONES:

The AISONES bit controls the pattern used to detect the alarm indication signal (AIS) when both AISPAT and AISC bits in DS3 FRMR Configuration register are logic 0; if either AISPAT or AISC are logic 1, the AISONES bit is ignored. When a logic 0 is written to AISONES, the algorithm checks that a framed all-ones payload pattern (1111...) signal is observed for a period of time before declaring AIS. Only the payload bits are observed to follow an all-ones pattern, the overhead bits (X, P, M, F, C) are ignored. When a logic 1 is written to AISONES, the algorithm checks that an unframed all-ones pattern (1111...) signal is observed for a period of time before declaring AIS. In this case all the bits, including the overhead, are observed to follow an all-ones pattern. The valid combinations of AISPAT, AISC, and AISONES bits are summarized below:

AISPAT	AISC	AISONES	AIS Detected
1	0	X	Framed DS3 stream containing repeating 1010… pattern; overhead bits ignored.
0	1	X	Framed DS3 stream containing C-bits all logic 0; payload bits ignored.
1	1	X	Framed DS3 stream containing repeating 1010… pattern and C-bits all logic 0.
0	0	0	Framed DS3 stream containing all-ones payload pattern; overhead bits ignored.
0	0	1	Unframed all-ones DS3 stream.

Register 0x020E + 0x100*N: DS3 FRMR Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	X
Bit 6	R	REDI	X
Bit 5	R	CBITI	X
Bit 4	R	FERFI	X
Bit 3	R	IDLI	X
Bit 2	R	AISI	X
Bit 1	R	OOFI	X
Bit 0	R	LOSI	X

LOSI:

The LOSI bit is set to logic 1 when a loss of signal defect is detected or removed. The LOSI bit position is set to logic 0 when this register is read.

OOFI:

The OOFI bit is set to logic 1 when an out of frame defect is detected or removed. The OOFI bit position is set to logic 0 when this register is read.

AISI:

The AISI bit is set to logic 1 when the DS3 AIS maintenance signal is detected or removed. The AISI bit position is set to logic 0 when this register is read.

IDLI:

The IDLI bit is set to logic 1 when the DS3 IDLE maintenance signal is detected or removed. The IDLI bit position is set to logic 0 when this register is read.

FERFI:

The FERFI bit is set to logic 1 when a FERF defect is detected or removed. The FERFI bit position is set to logic 0 when this register is read.

CBITI:

The CBITI bit is set to logic 1 when a change of state is detected in the DS3 application identification channel. The CBITI bit position is set to logic 0 when this register is read.

REDI:

The REDI bit indicates that a change of state of the DS3 RED indication has occurred. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register. When the REDI bit is a logic 1, a change in the RED state has occurred. When the REDI bit is logic 0, no change in the RED state has occurred.

COFAI:

The COFAI bit is set to logic 1 when a change of frame alignment is detected. A COFA is generated when a new DS3 frame alignment is determined that differs from the last known frame alignment. The COFAI bit position is set to logic 0 when this register is read.

Register 0x020F + 0x100*N: DS3 FRMR Status

Bit	Type	Function	Default
Bit 7	R/W	ACE	0
Bit 6	R	REDV	X
Bit 5	R	CBITV	X
Bit 4	R	FERFV	X
Bit 3	R	IDLV	X
Bit 2	R	AISV	X
Bit 1	R	OOFV	X
Bit 0	R	LOSV	X

LOSV:

The LOSV bit indicates the current loss of signal defect state. LOSV is a logic 1 when a sequence of 175 zeros is detected on the B3ZS encoded DS3 receive stream. LOSV is a logic 0 when a signal with a ones density greater than 33% for 175 ± 1 bit periods is detected.

OOFV:

The OOFV bit indicates the current DS3 out of frame defect state. When the TEMUX 84 has lost frame alignment and is searching for the new alignment, OOFV is set to logic 1. When the TEMUX 84 has found frame alignment, the OOFV bit is set to logic 0.

AISV:

The AISV bit indicates the alarm indication signal state. When the TEMUX 84 detects the AIS maintenance signal, AISV is set to logic 1.

IDLV:

The IDLV bit indicates the IDLE signal state. When the TEMUX 84 detects the IDLE maintenance signal, IDLV is set to logic 1.

FERFV:

The FERFV bit indicates the current far end receive failure defect state. When the TEMUX 84 detects an M-frame with the X1 and X2 bits both set to

zero, FERFV is set to logic 1. When the TEMUX 84 detects an M-frame with the X1 and X2 bits both set to one, FERFV is set to logic 0.

CBITV:

The CBITV bit indicates the application identification channel (AIC) state. CBITV is set to logic 1 (indicating the presence of the C-bit parity application) when the AIC bit is set to logic 1 for 63 consecutive M-frames. CBITV is set to logic 0 (indicating the presence of the M23 or SYNTRAN applications) when AIC is set to logic 0 for 2 or more M-frames in the last 15.

REDV:

The REDV bit indicates the current state of the DS3 RED indication. When the REDV bit is a logic 1, the DS3 FRMR frame alignment acquisition circuitry has been out of frame for 2.23ms (or for 13.5ms when FDET is logic 0). When the REDV bit is logic 0, the frame alignment circuitry has found frame (i.e. OOFV=0) for 2.23ms (or 13.5ms if FDET=0).

ACE:

The ACE bit selects the Additional Configuration Register. This register is located at address 0x020D, and is only accessible when the ACE bit is set to logic 1. When ACE is set to logic 0, the Interrupt Enable register is accessible at address 0x020D.

1.23 DS3 and E3 Performance Monitoring Registers

Register 0x0210 + 0x100*N: DS3/E3 PMON Performance Meters

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	LCVCH	X
Bit 4	R	FERRCH	X
Bit 3	R	EXZSCH	X
Bit 2	R	PERRCH	X
Bit 1	R	CPERRCH	X
Bit 0	R	FEBECH	X

FEBECH:

The FEBECH bit is set to logic 1 if one or more FEBE events have occurred during the latest PMON accumulation interval.

CPERRCH:

The CPERRCH bit is set to logic 1 if one or more path parity error events have occurred during the latest PMON accumulation interval.

PERRCH:

The PERRCH bit is set to logic 1 if one or more parity error events have occurred during the latest PMON accumulation interval.

EXZSCH:

The EXZSCH bit is set to logic 1 if one or more summed line code violation events in DS3 mode have occurred during the latest PMON accumulation interval.

FERRCH:

The FERRCH bit is set to logic 1 if one or more F-bit or M-bit error events have occurred during the latest PMON accumulation interval.

LCVCH:

The LCVCH bit is set to logic 1 if one or more line code violation events have occurred during the latest PMON accumulation interval.

Register 0x0211 + 0x100*N: DS3/E3 PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	X
Bit 0	R	OVR	X

OVR:

The OVR bit indicates the overrun status of the PMON holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

INTR:

The INTR bit indicates the current status of the interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the holding registers has occurred; a logic 0 indicates that no transfer has occurred. The INTR bit is set to logic 0 when this register is read.

INTE:

The INTE bit enables the generation of an interrupt when the PMON counter values are transferred to the holding registers. When a logic 1 is written to INTE, the interrupt generation is enabled.

Register 0x0214 + 0x100*N: DS3/E3 PMON Line Code Violation Event Count LSB

Bit	Type	Function	Default
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Register 0x0215 + 0x100*N: DS3/E3 PMON Line Code Violation Event Count MSB

Bit	Type	Function	Default
Bit 7	R	LCV[15]	X
Bit 6	R	LCV[14]	X
Bit 5	R	LCV[13]	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

LCV[15:0]:

LCV[15:0] represents the number of DS3 or E3 line code violation errors that have been detected since the last time the LCV counter was polled. This counter (and all other counters in the PMON) is polled by writing to any of the DS3/E3 PMON register addresses or to the Global PMON update register. Such a write transfers the internally accumulated count to the LCV Error Count Registers and simultaneously resets the internal counter to begin

a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 3 RCLK cycles to complete.

Register 0x0216 + 0x100*N: DS3/E3 PMON Framing Bit Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FERR[7]	X
Bit 6	R	FERR[6]	X
Bit 5	R	FERR[5]	X
Bit 4	R	FERR[4]	X
Bit 3	R	FERR[3]	X
Bit 2	R	FERR[2]	X
Bit 1	R	FERR[1]	X
Bit 0	R	FERR[0]	X

Register 0x0217 + 0x100*N: DS3/E3 PMON Framing Bit Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	FERR[9]	X
Bit 0	R	FERR[8]	X

FERR[9:0]:

FERR[9:0] represents the number of DS3 F-bit and M-bit errors, or E3 framing pattern errors, that have been detected since the last time the framing error counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the DS3/E3 PMON register addresses or to the Global PMON update register.

Such a write transfers the internally accumulated count to the FERR Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 3 RCLK cycles to complete.

Register 0x0218 + 0x100*N: DS3 PMON Excessive Zeros LSB

Bit	Type	Function	Default
Bit 7	R	EXZS[7]	X
Bit 6	R	EXZS[6]	X
Bit 5	R	EXZS[5]	X
Bit 4	R	EXZS[4]	X
Bit 3	R	EXZS[3]	X
Bit 2	R	EXZS[2]	X
Bit 1	R	EXZS[1]	X
Bit 0	R	EXZS[0]	X

Register 0x0219 + 0x100*N: DS3 PMON Excessive Zeros MSB

Bit	Type	Function	Default
Bit 7	R	EXZS[15]	X
Bit 6	R	EXZS[14]	X
Bit 5	R	EXZS[13]	X
Bit 4	R	EXZS[12]	X
Bit 3	R	EXZS[11]	X
Bit 2	R	EXZS[10]	X
Bit 1	R	EXZS[9]	X
Bit 0	R	EXZS[8]	X

EXZS[15:0]:

In DS3 mode, EXZS[15:0] represents the number of summed Excessive Zeros (EXZS) that occurred during the previous accumulation interval. One or more excessive zeros occurrences within an 85 bit DS3 information block is counted as one summed excessive zero. Excessive zeros are accumulated by this register only when the EXZSO and EXZDET are logic 1 in the DS3 FRMR Additional Configuration Register. This register accumulates summed line code violations when the EXZSO is logic 0. The count of summed line code violations is defined as the number of DS3

information blocks (85 bits) that contain one or more line code violations since the last time the summed LCV counter was polled.
This counter is forced to zero when the TEMUX 84 is configured for E3 mode.

The counter (and all other counters in the PMON) is polled by writing to any of the DS3/E3 PMON register addresses or to the Global PMON update register. Such a write transfers the internally accumulated count to the EXZS Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 3 RCLK cycles to complete.

Register 0x021A + 0x100*N: DS3/E3 PMON Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	PERR[7]	X
Bit 6	R	PERR[6]	X
Bit 5	R	PERR[5]	X
Bit 4	R	PERR[4]	X
Bit 3	R	PERR[3]	X
Bit 2	R	PERR[2]	X
Bit 1	R	PERR[1]	X
Bit 0	R	PERR[0]	X

Register 0x021B + 0x100*N: DS3/E3 PMON Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 7	R	PERR[15]	X
Bit 6	R	PERR[14]	X
Bit 5	R	PERR[13]	X
Bit 4	R	PERR[12]	X
Bit 3	R	PERR[11]	X
Bit 2	R	PERR[10]	X
Bit 1	R	PERR[9]	X
Bit 0	R	PERR[8]	X

PERR[15:0]:

PERR[15:0] represents the number of DS3 P-bit errors or the number of E3 G.832 BIP-8 errors. This counter is not used when configured for E3 G.751 applications and is forced to zero.

The counter (and all other counters in the PMON) is polled by writing to any of the DS3/E3 PMON register addresses or to the Global PMON update register. Such a write transfers the internally accumulated count to the PERR Error Count Registers and simultaneously resets the internal counter to begin a

new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 3 RCLK cycles to complete.

Register 0x021C + 0x100*N: DS3 PMON Path Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	CPERR[7]	X
Bit 6	R	CPERR[6]	X
Bit 5	R	CPERR[5]	X
Bit 4	R	CPERR[4]	X
Bit 3	R	CPERR[3]	X
Bit 2	R	CPERR[2]	X
Bit 1	R	CPERR[1]	X
Bit 0	R	CPERR[0]	X

Register 0x021D + 0x100*N: DS3 PMON Path Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	CPERR[13]	X
Bit 4	R	CPERR[12]	X
Bit 3	R	CPERR[11]	X
Bit 2	R	CPERR[10]	X
Bit 1	R	CPERR[9]	X
Bit 0	R	CPERR[8]	X

CPERR[13:0]:

Valid only for DS3.

When configured for DS3 applications, CPERR[13:0] represents the number of DS3 path parity errors that have been detected since the last time the DS3 path parity error counter was polled. This counter is forced to zero when the TEMUX 84 is configured for E3 applications.

The counter (and all other counters in the PMON) is polled by writing to any of the DS3/E3 PMON register addresses or to the Global PMON update register. Such a write transfers the internally accumulated count to the CPERR Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 3 RCLK cycles to complete.

Register 0x021E + 0x100*N: DS3/E3 PMON FEBE Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 0x021F + 0x100*N: DS3/E3 PMON FEBE Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	FEBE[13]	X
Bit 4	R	FEBE[12]	X
Bit 3	R	FEBE[11]	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

FEBE[13:0]:

FEBE[13:0] represents the number of DS3 or E3 G.832 far end block errors that have been detected since the last time the FEBE error counter was polled. This counter is set to 0 for E3 G.751 applications.

The counter (and all other counters in the PMON) is polled by writing to any of the DS3/E3 PMON register addresses or to the Global PMON update register. Such a write transfers the internally accumulated count to the FEBE Event Count Registers and simultaneously resets the internal counter to begin a

new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 3 RCLK cycles to complete.

1.24 DS3/E3 Transmit HDLC Controller Registers

Register 0x0220 + 0x100*N: DS3/E3 TDPR Configuration

Bit	Type	Function	Default
Bit 7	R/W	FLGSHAREB	1
Bit 6	R/W	FIFOCLR	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	R/W	EOM	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	1
Bit 0	R/W	EN	0

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the line rate clock, thus consecutive reads and writes should not occur at greater than 5.5 MHz in DS3 mode or 4.2 MHz in E3 mode.

EN:

The EN bit enables the TDPR functions. When EN is set to logic 1, the TDPR is enabled and flag sequences are sent until data is written into the TDPR Transmit Data register. When the EN bit is set to logic 0, the TDPR is disabled and an all 1's Idle sequence is transmitted on the datalink.

CRC:

The CRC enable bit controls the generation of the CCITT_CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the CCITT-CRC generator and appends the 16-bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 01111111 code (the 0 is transmitted first) to be transmitted after the current byte from the TDPR FIFO is transmitted. The TDPR FIFO is then reset. All data in the TDPR FIFO will be lost. Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic 0. At least one Abort sequence will be sent when the ABT bit transitions from logic 0 to logic 1.

EOM:

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared upon a write to the TDPR Transmit Data register.

Reserved:

This bit should be set to logic 0 for proper operation.

FIFOCLR:

The FIFOCLR bit resets the TDPR FIFO. When set to logic 1, FIFOCLR will cause the TDPR FIFO to be cleared.

FLGSHAREB:

The FLGSHAREB bit configures the TDPR to share the opening and closing flags between successive frames. If FLGSHAREB is logic 0, then the opening and closing flags between successive frames are shared. If FLGSHAREB is logic 1, then separate closing and opening flags are inserted between successive frames.

Register 0x0221 + 0x100*N: DS3/E3 TDPR Upper Transmit Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	UTHR[6]	1
Bit 5	R/W	UTHR[5]	0
Bit 4	R/W	UTHR[4]	0
Bit 3	R/W	UTHR[3]	0
Bit 2	R/W	UTHR[2]	0
Bit 1	R/W	UTHR[1]	0
Bit 0	R/W	UTHR[0]	0

UTHR[6:0]:

The UTHR[6:0] bits define the TDPR FIFO fill level which will automatically cause the bytes stored in the TDPR FIFO to be transmitted. Once the fill level exceeds the UTHR[6:0] value, transmission will begin. Transmission will not stop until the last complete packet is transmitted and the TDPR FIFO fill level is below UTHR[6:0] + 1.

The value of UTHR[6:0] must always be greater than the value of LINT[6:0] unless both values are equal to 00H.

Register 0x0222 + 0x100*N: DS3/E3 TDPR Lower Interrupt Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	LINT[6]	0
Bit 5	R/W	LINT[5]	0
Bit 4	R/W	LINT[4]	0
Bit 3	R/W	LINT[3]	0
Bit 2	R/W	LINT[2]	1
Bit 1	R/W	LINT[1]	1
Bit 0	R/W	LINT[0]	1

LINT[6:0]:

The LINT[6:0] bits define the TDPR FIFO fill level which causes an internal interrupt (LFILLI) to be generated. Once the TDPR FIFO level decrements to empty or to a value less than LINT[6:0], LFILLI and BLFILL register bits will be set to logic 1. LFILLI will cause an interrupt on INTB if LFILLE is set to logic 1.

The value of LINT[6:0] must always be less than the value of UTHR[6:0] unless both values are equal to 00H.

Register 0x0223 + 0x100*N: DS3/E3 TDPR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	FULLE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	UDRE	0
Bit 0	R/W	LFILLE	0

LFILLE:

The LFILLE enables a transition to logic 1 on LFILLI to generate an interrupt on INTB. If LFILLE is a logic 1, a transition to logic 1 on LFILLI will generate an interrupt on INTB. If LFILLE is a logic 0, a transition to logic 1 on LFILLI will not generate an interrupt on INTB.

UDRE:

The UDRE enables a transition to logic 1 on UDRI to generate an interrupt on INTB. If UDRE is a logic 1, a transition to logic 1 on UDRI will generate an interrupt on INTB. If UDRE is a logic 0, a transition to logic 1 on UDRI will not generate an interrupt on INTB.

OVRE:

The OVRE enables a transition to logic 1 on OVRI to generate an interrupt on INTB. If OVRE is a logic 1, a transition to logic 1 on OVRI will generate an interrupt on INTB. If OVRE is a logic 0, a transition to logic 1 on OVRI will not generate an interrupt on INTB.

FULLE:

The FULLE enables a transition to logic 1 on FULLI to generate an interrupt on INTB. If FULLE is a logic 1, a transition to logic 1 on FULLI will generate an interrupt on INTB. If FULLE is a logic 0, a transition to logic 1 on FULLI will not generate an interrupt on INTB.

Reserved:

This bit should be set to logic 0 for proper operation.

Register 0x0224 + 0x100*N: DS3/E3 TDPR Interrupt Status/UDR Clear

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FULL	X
Bit 5	R	BLFILL	X
Bit 4	R	Reserved	X
Bit 3	R	FULLI	X
Bit 2	R	OVRI	X
Bit 1	R	UDRI	X
Bit 0	R	LFILLI	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the line rate clock, thus consecutive reads and writes should not occur at greater than 5.5 MHz in DS3 mode or 4.2 MHz in E3 mode.

LFILLI:

The LFILLI bit will transition to logic 1 when the TDPR FIFO level transitions to empty or falls below the value of LINT[6:0] programmed in the TDPR Lower Interrupt Threshold register. LFILLI will assert INTB if it is a logic 1 and LFILLE is programmed to logic 1. LFILLI is cleared when this register is read.

UDRI:

The UDRI bit will transition to 1 when the TDPR FIFO underruns. That is, the TDPR was in the process of transmitting a packet when it ran out of data to transmit. UDRI will assert INTB if it is a logic 1 and UDRE is programmed to logic 1. UDRI is cleared when this register is read.

OVRI:

The OVRI bit will transition to 1 when the TDPR FIFO overruns. That is, the TDPR FIFO was already full when another data byte was written to the TDPR Transmit Data register. OVRI will assert INTB if it is a logic 1 and OVRE is programmed to logic 1. OVRI is cleared when this register is read.

FULLI:

The FULLI bit will transition to logic 1 when the TDPR FIFO is full. FULLI will assert INTB if it is a logic 1 and FULLE is programmed to logic 1. FULLI is cleared when this register is read.

Reserved:

This bit is not used in TEMUX 84 applications.

BLFILL:

The BLFILL bit is set to logic 1 if the current FIFO fill level is below the LINT[7:0] level or is empty.

FULL:

The FULL bit reflects the current condition of the TDPR FIFO. If FULL is a logic 1, the TDPR FIFO already contains 128-bytes of data and can accept no more.

Register 0x0225 + 0x100*N: DS3/E3 TDPR Transmit Data

Bit	Type	Function	Default
Bit 7	R/W	TD[7]	X
Bit 6	R/W	TD[6]	X
Bit 5	R/W	TD[5]	X
Bit 4	R/W	TD[4]	X
Bit 3	R/W	TD[3]	X
Bit 2	R/W	TD[2]	X
Bit 1	R/W	TD[1]	X
Bit 0	R/W	TD[0]	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the line rate clock, thus consecutive reads and writes should not occur at greater than 5.5 MHz in DS3 mode or 4.2 MHz in E3 mode.

TD[7:0]:

The TD[7:0] bits contain the data to be transmitted on the data link. Data written to this register is serialized and transmitted (TD[0] is transmitted first).

1.25 DS3/E3 Receive HDLC Controller Registers

Register 0x0228 + 0x100*N: DS3/E3 RDLC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	MEN	0
Bit 2	R/W	MM	0
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

EN:

The EN bit controls the overall operation of the RDLC. When EN is set to logic 1, RDLC is enabled; when set to logic 0, RDLC is disabled. When RDLC is disabled, the RDLC FIFO buffer and interrupts are all cleared. When RDLC is enabled, it will immediately begin looking for flags.

TR:

Setting the terminate reception (TR) bit to logic 1 forces the RDLC to immediately terminate the reception of the current data frame, empty the RDLC FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RDLC handles a terminate reception event in the same manner as it would the toggling of the EN bit from logic 1 to logic 0 and back to logic 1. Thus, the RDLC state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit will reset itself to logic 0 after the register write operation is completed and a rising and falling edge occurs on the internal datalink clock input. If the RDLC Configuration Register is read after this time, the TR bit value returned will be logic 0.

MEN:

Setting the Match Enable (MEN) bit to logic 1 enables the detection and storage in the RDLC FIFO of only those packets whose first data byte

matches either of the bytes written to the Primary or Secondary Match Address Registers, or the universal all ones address. When the MEN bit is logic 0, all packets received are written into the RDLC FIFO.

MM:

Setting the Match Mask (MM) bit to logic 1 ignores the PA[1:0] bits of the Primary Address Match Register, the SA[1:0] bits of the Secondary Address Match Register, and the two least significant bits of the universal all ones address when performing the address comparison.

Reserved:

This register bit should be set to logic 0 for proper operation.

Register 0x0229 + 0x100*N: DS3/E3 RDLC Interrupt Control

Bit	Type	Function	Default
Bit 7	R/W	INTE	0
Bit 6	R/W	INTC[6]	0
Bit 5	R/W	INTC[5]	0
Bit 4	R/W	INTC[4]	0
Bit 3	R/W	INTC[3]	0
Bit 2	R/W	INTC[2]	0
Bit 1	R/W	INTC[1]	0
Bit 0	R/W	INTC[0]	0

INTC[6:0]:

The INTC[6:0] bits control the assertion of FIFO fill level set point interrupts.

INTE:

The Interrupt Enable bit (INTE) must set to logic 1 to allow the internal interrupt status to be propagated to the INTB output. When the INTE bit is logic 0 the RDLC will not assert INTB.

The contents of the Interrupt Control Register should only be changed when the EN bit in the RDLC Configuration Register is logic 0. This prevents any erroneous interrupt generation.

Register 0x022A + 0x100*N: DS3/E3 RDLC Status

Bit	Type	Function	Default
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	COLS	X
Bit 4	R	PKIN	X
Bit 3	R	PBS[2]	X
Bit 2	R	PBS[1]	X
Bit 1	R	PBS[0]	X
Bit 0	R	INTR	X

Consecutive reads of the RDLC Status and Data registers should not occur at rates greater than 1/10 that of the line rate clock, thus consecutive reads should not occur at greater than 4.4 MHz in DS3 mode or 3.4 MHz in E3 mode.

INTR:

The interrupt (INTR) bit reflects the status of the internal RDLC interrupt. If the INTE bit in the RDLC Interrupt Control Register is set to logic 1, a RDLC interrupt (INTR is a logic 1) will cause INTB to be asserted low. The INTR register bit will be set to logic 1 when one of the following conditions occurs:

1. the number of bytes specified in the RDLC Interrupt Control register have been received on the data link and written into the FIFO
2. RDLC FIFO buffer overrun has been detected
3. the last byte of a packet has been written into the RDLC FIFO
4. the last byte of an aborted packet has been written into the RDLC FIFO
5. transition of receiving all ones to receiving flags has been detected.

PBS[2:0]:

The packet byte status (PBS[2:0]) bits indicate the status of the data last read from the FIFO as indicated in the following table:

PBS[2:0]	Data Status
000	The data byte read from the FIFO is not special.
001	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the first HDLC flag sequence (01111110) was detected. This indicates that the data link became active.
010	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive.
011	Unused.
100	The data byte read from the FIFO is the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes.
101	The data byte read from the FIFO must be discarded because there was a non-integer number of bytes in the packet.
110	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error. The packet was received in error.
111	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error and a non-integer number of bytes. The packet was received in error.

PKIN:

The Packet In (PKIN) bit is logic 1 when the last byte of a non-aborted packet is written into the FIFO. The PKIN bit is cleared to logic 0 after the RDLC Status Register is read.

COLS:

The Change of Link Status (COLS) bit is set to logic 1 if the RDLC has detected the HDLC flag sequence (01111110) or HDLC abort sequence (01111111) in the data. This indicates that there has been a change in the data link status. The COLS bit is cleared to logic 0 by reading this register or by clearing the EN bit in the RDLC Configuration Register. For each change in link status, a byte is written into the FIFO. If the COLS bit is found to be logic 1 then the RDLC FIFO must be read until empty. The status of the data link is determined by the PBS[2:0] bits associated with the data read from the RDLC FIFO.

OVR:

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the RDLC FIFO buffer. This bit is not reset to logic 0 until after the Status Register is read. While the OVR bit is logic 1, the RDLC and RDLC FIFO buffer are held in the reset state, causing the COLS and PKIN bits to be reset to logic 0.

FE:

The FIFO buffer empty (FE) bit is set to logic 1 when the last RDLC FIFO buffer entry is read. The FE bit goes to logic 0 when the FIFO is loaded with new data.

Register 0x022B + 0x100*N: DS3/E3 RDLC Data

Bit	Type	Function	Default
Bit 7	R	RD[7]	X
Bit 6	R	RD[6]	X
Bit 5	R	RD[5]	X
Bit 4	R	RD[4]	X
Bit 3	R	RD[3]	X
Bit 2	R	RD[2]	X
Bit 1	R	RD[1]	X
Bit 0	R	RD[0]	X

Consecutive reads of the RDLC Status and Data registers should not occur at rates greater than 1/10 that of the line rate clock, thus consecutive reads should not occur at greater than 4.4 MHz in DS3 mode or 3.4 MHz in E3 mode.

RD[7:0]:

RD[7:0] contains the received data link information. RD[0] corresponds to the first received bit of the data link message.
This register reads from the RDLC 128-byte FIFO buffer. If data is available, the FE bit in the FIFO Input Status Register is logic 0.
When an overrun is detected, an interrupt is generated and the FIFO buffer is held cleared until the RDLC Status Register is read.

Register 0x022C + 0x100*N: DS3/E3 RDLC Primary Address Match

Bit	Type	Function	Default
Bit 7	R/W	PA[7]	1
Bit 6	R/W	PA[6]	1
Bit 5	R/W	PA[5]	1
Bit 4	R/W	PA[4]	1
Bit 3	R/W	PA[3]	1
Bit 2	R/W	PA[2]	1
Bit 1	R/W	PA[1]	1
Bit 0	R/W	PA[0]	1

PA[7:0]:

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[0] corresponds to the first received bit of the data link message. The MM bit in the Configuration Register is used mask off PA[1:0] during the address comparison.

Register 0x022D + 0x100*N: DS3/E3 RDLC Secondary Address Match

Bit	Type	Function	Default
Bit 7	R/W	SA[7]	1
Bit 6	R/W	SA[6]	1
Bit 5	R/W	SA[5]	1
Bit 4	R/W	SA[4]	1
Bit 3	R/W	SA[3]	1
Bit 2	R/W	SA[2]	1
Bit 1	R/W	SA[1]	1
Bit 0	R/W	SA[0]	1

SA[7:0]:

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[0] corresponds to the first received bit data link message. The MM bit in the Configuration Register is used mask off SA[1:0] during the address comparison.

1.26 DS3/E3 PRGD Pseudo Random Pattern Generator and Detector Registers

Register 0x0230 + 0x100*N: PRGD Control

Bit	Type	Function	Default
Bit 7	R/W	PDR[1]	0
Bit 6	R/W	PDR[0]	0
Bit 5	R/W	QRSS	0
Bit 4	R/W	PS	0
Bit 3	R/W	TINV	0
Bit 2	R/W	RINV	0
Bit 1	R/W	AUTOSYNC	1
Bit 0	R/W	MANSYNC	0

PDR[1:0]:

The PDR[1:0] bits select the content of the four pattern detector registers to be any one of the pattern receive registers, the error count holding registers, or the bit count holding registers. The selection is shown in the following table:

PDR[1:0]	PDR#1	PDR#2	PDR#3	PDR#4
00, 01	Pattern Receive (LSB)	Pattern Receive	Pattern Receive	Pattern Receive (MSB)
10	Error Count (LSB)	Error Count	Error Count	Error Count (MSB)
11	Bit Count (LSB)	Bit Count	Bit Count	Bit Count (MSB)

QRSS:

The QRSS bit enables the zero suppression feature required when generating the QRSS sequence. When QRSS is a logic 1, a one is forced in the TDAT stream when the following 14 bit positions are all zeros. When QRSS is a logic 0, the zero suppression feature is disabled.

PS:

The PS bit selects the generated pattern. When PS is a logic 1, a repetitive pattern is generated. When PS is a logic 0, a pseudo-random pattern is generated. The PS bit should be set to 1 before the length, tap and pattern insertion registers are written to. If the PS logic value changes then the length, tap and pattern insertion registers must be reprogrammed.

TINV:

The TINV bit controls the logical inversion of the generated data stream. When TINV is a logic 1, the data is inverted. When TINV is a logic 0, the data is not inverted.

RINV:

The RINV bit controls the logical inversion of the receive data stream before processing. When RINV is a logic 1, the received data is inverted before being processed by the pattern detector. When RINV is a logic 0, the received data is not inverted.

AUTOSYNC:

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. The automatic resynchronization is activated when 6 or more bit errors are detected in the last 64 bit periods. When AUTOSYNC is a logic 1, the auto resync feature is enabled. When AUTO SYNC is a logic 0, the auto sync feature is disabled, and pattern resynchronization is accomplished using the MANSYNC bit.

MANSYNC:

The MANSYNC bit is used to initiate a manual resynchronization of the pattern detector. A low to high transition on MANSYNC initiates the resynchronization.

Register 0x0231 + 0x100*N: PRGD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	SYNCE	0
Bit 6	R/W	BEE	0
Bit 5	R/W	XFERE	0
Bit 4	R	SYNCV	X
Bit 3	R	SYNCI	X
Bit 2	R	BEI	X
Bit 1	R	XFERI	X
Bit 0	R	OVR	X

SYNCE:

The SYNCE bit enables the generation of an interrupt when the pattern detector changes synchronization state. When SYNCE is set to logic 1, the interrupt is enabled.

BEE:

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. When BEE is set to logic 1, the interrupt is enabled.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the receive pattern registers, the bit counter holding registers, and the error counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

SYNCV:

The SYNCV bit indicates the synchronization state of the pattern detector. When SYNCV is a logic 1 the pattern detector is synchronized (the pattern detector has observed at least 32 consecutive error free bit periods). When SYNCV is a logic 0, the pattern detector is out of sync (the pattern detector has detected 6 or more bit errors in a 64 bit period window).

SYNCI:

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic 1, the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic 0 when this register is read.

BEI:

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic 1, at least one bit error has been detected. BEI is set to logic 0 when this register is read.

XFERI:

The XFERI bit indicates that a transfer of pattern detector data has occurred. A logic 1 in this bit position indicates that the pattern receive registers, the bit counter holding registers and the error counter holding registers have been updated. This update is initiated by writing to one of the pattern detector register locations, or by writing a logic 1 to the DS3_E3 bit of the TEMUX 84 Global Performance Monitor Update Register. XFERI is set to logic 0 when this register is read.

OVR:

The OVR bit is the overrun status of the pattern detector registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the pattern receive registers, the bit counter holding registers and the error counter holding registers have been overwritten. OVR is set to logic 0 when this register is read.

Register 0x0232 + 0x100*N: PRGD Length

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PL[4]	0
Bit 3	R/W	PL[3]	0
Bit 2	R/W	PL[2]	0
Bit 1	R/W	PL[1]	0
Bit 0	R/W	PL[0]	0

PL[4:0]:

PL[4:0] determine the length of the generated pseudo random or repetitive pattern. The pattern length is equal to the value of PL[4:0] + 1.

Register 0x0233 + 0x100*N: PRGD Tap

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PT[4]	0
Bit 3	R/W	PT[3]	0
Bit 2	R/W	PT[2]	0
Bit 1	R/W	PT[1]	0
Bit 0	R/W	PT[0]	0

PT[4:0]:

PT[4:0] determine the feedback tap position of the generated pseudo random pattern. The feedback tap position is equal to the value of PT[4:0] + 1.

Register 0x0234 + 0x100*N: PRGD Error Insertion

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	EVENT	0
Bit 2	R/W	EIR[2]	0
Bit 1	R/W	EIR[1]	0
Bit 0	R/W	EIR[0]	0

EVENT:

A low to high transition on the EVENT bit causes a single bit error to be inserted in the generated pattern. This bit must be cleared and set again for a subsequent error to be inserted.

EIR[2:0]:

The EIR[2:0] bits control the insertion of a programmable bit error rate as indicated in the following table:

EIR[2:0]	Generated Bit Error Rate
000	No errors inserted
001	10^{-1}
010	10^{-2}
011	10^{-3}
100	10^{-4}
101	10^{-5}
110	10^{-6}
111	10^{-7}

Register 0x0238 + 0x100*N: PRGD Pattern Insertion #1

Bit	Type	Function	Default
Bit 7	R/W	PI[7]	0
Bit 6	R/W	PI[6]	0
Bit 5	R/W	PI[5]	0
Bit 4	R/W	PI[4]	0
Bit 3	R/W	PI[3]	0
Bit 2	R/W	PI[2]	0
Bit 1	R/W	PI[1]	0
Bit 0	R/W	PI[0]	0

Register 0x0239 + 0x100*N: PRGD Pattern Insertion #2

Bit	Type	Function	Default
Bit 7	R/W	PI[15]	0
Bit 6	R/W	PI[14]	0
Bit 5	R/W	PI[13]	0
Bit 4	R/W	PI[12]	0
Bit 3	R/W	PI[11]	0
Bit 2	R/W	PI[10]	0
Bit 1	R/W	PI[9]	0
Bit 0	R/W	PI[8]	0

Register 0x023A + 0x100*N: PRGD Pattern Insertion #3

Bit	Type	Function	Default
Bit 7	R/W	PI[23]	0
Bit 6	R/W	PI[22]	0
Bit 5	R/W	PI[21]	0
Bit 4	R/W	PI[20]	0

Bit	Type	Function	Default
Bit 3	R/W	PI[19]	0
Bit 2	R/W	PI[18]	0
Bit 1	R/W	PI[17]	0
Bit 0	R/W	PI[16]	0

Register 0x023B + 0x100*N: PRGD Pattern Insertion #4

Bit	Type	Function	Default
Bit 7	R/W	PI[31]	0
Bit 6	R/W	PI[30]	0
Bit 5	R/W	PI[29]	0
Bit 4	R/W	PI[28]	0
Bit 3	R/W	PI[27]	0
Bit 2	R/W	PI[26]	0
Bit 1	R/W	PI[25]	0
Bit 0	R/W	PI[24]	0

PI[31:0]:

PI[31:0] contain the data that is loaded in the pattern generator each time a new pattern (pseudo random or repetitive) is to be generated. When a pseudo random pattern is to be generated, PI[31:0] should be set to 0xFFFFFFFF. The data is loaded each time pattern insertion register #4 is written. Pattern insertion registers #1 - #3 should be loaded with the desired data before pattern register #4 is written. When a repetitive pattern is transmitted, PI[31], the MSB, contains the first bit transmitted, PI[0], the LSB, contains the last bit transmitted.

Note that the PI[31:0] value has no effect on the pattern detection. If a repetitive pattern is selected, the receiver will synchronize to any bit sequence that repeats with the programmed periodicity.

Register 0x023C + 0x100*N: PRGD Pattern Detector #1

Bit	Type	Function	Default
Bit 7	R	PD[7]	0
Bit 6	R	PD[6]	0
Bit 5	R	PD[5]	0
Bit 4	R	PD[4]	0
Bit 3	R	PD[3]	0
Bit 2	R	PD[2]	0
Bit 1	R	PD[1]	0
Bit 0	R	PD[0]	0

Register 0x023D + 0x100*N: PRGD Pattern Detector #2

Bit	Type	Function	Default
Bit 7	R	PD[15]	0
Bit 6	R	PD[14]	0
Bit 5	R	PD[13]	0
Bit 4	R	PD[12]	0
Bit 3	R	PD[11]	0
Bit 2	R	PD[10]	0
Bit 1	R	PD[9]	0
Bit 0	R	PD[8]	0

Register 0x023E + 0x100*N: PRGD Pattern Detector #3

Bit	Type	Function	Default
Bit 7	R	PD[23]	0
Bit 6	R	PD[22]	0
Bit 5	R	PD[21]	0
Bit 4	R	PD[20]	0

Bit	Type	Function	Default
Bit 3	R	PD[19]	0
Bit 2	R	PD[18]	0
Bit 1	R	PD[17]	0
Bit 0	R	PD[16]	0

Register 0x023F + 0x100*N: PRGD Pattern Detector #4

Bit	Type	Function	Default
Bit 7	R	PD[31]	0
Bit 6	R	PD[30]	0
Bit 5	R	PD[29]	0
Bit 4	R	PD[28]	0
Bit 3	R	PD[27]	0
Bit 2	R	PD[26]	0
Bit 1	R	PD[25]	0
Bit 0	R	PD[24]	0

PD[31:0]:

PD[31:0] contain the pattern detector data. The values contained in these registers are determined by the PDR[1:0] bits in the PRGD Control register.

When PDR[1:0] is set to 00 or 01, PD[31:0] contain the pattern receive register. The 32 bits received immediately before the last accumulation interval are present on PD[31:0]. PD[31] contains the first of the 32 received bits, PD[0] contains the last of the 32 received bits.

When PDR[1:0] is set to 10, PD[31:0] contain the error counter holding register. The value in this register represents the number of bit errors that have been accumulated since the last accumulation interval. Note that bit errors are not accumulated while the pattern detector is out of sync.

When PDR[1:0] is set to 11, PD[31:0] contain the bit counter holding register. The value in this register represents the total number of bits that have been received since the last accumulation interval. Note that the total bit count is not incremented while the pattern detector is out of sync

The PRGD Pattern Detect registers are updated by writing to any one of the Pattern Detect registers. Alternatively, the Pattern Detect registers are updated globally with all other TEMUX 84 counter registers by writing a logic 1 to the DS3_E3 bit of the Global Performance Monitor Update register.

1.27 MX23 Multiplexer Registers

Register 0x0240 + 0x100*N: MX23 Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	LBCODE[1]	0
Bit 2	R/W	LBCODE[0]	0
Bit 1	R/W	CBE	0
Bit 0	R/W	INTE	0

INTE:

When set to logic 1, the INTE bit enables the MX23 to activate the interrupt output, INTB, and set the MX23x bit of one of the Master Interrupt Source DS3 registers whenever any of the LBRI[7:1] bits are set to logic 1 in the MX23 Loopback Request Interrupt register. MX23 interrupts are masked when INTE is cleared low.

CBE:

When set to logic 1, the CBE bit enables C-bit parity operation. When CBE is low, M23 operation is enabled. While in C-bit parity mode, loopback request detection and loopback request insertion are disabled. The generated DS2 clock is nominally 6.3062723 MHz while in C-bit parity mode, received C bits are ignored, and transmitted C bits are set to 1. While in M23 mode, the generated DS2 clock is nominally 6.311993 MHz and C bit decoding and encoding is fully operational.

LBCODE[1:0]:

The LBCODE[1:0] bits select the valid state for a loopback request coded in the C-bits of the DS3 signals. Transmit and receive are not independent; the same code is expected in the receive DS3 as is inserted in the transmitted DS3. The following table gives the correspondence between LBCODE[1:0]

bits and the valid codes:

LBCODE[1:0]	Loopback Code
00	C1 = C2 and C1 = $\overline{C3}$
01	C1 = C3 and C1 = $\overline{C2}$
10	C2 = C3 and C1 = $\overline{C2}$
11	C1 = C2 and C1 = $\overline{C3}$

If LBCODE[1:0] is 'b00 or 'b11, the loopback code is as per ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7. Because TR-TSY-000233 Section 5.3.14.1 recommends compatibility with non-compliant existing equipment, the two other loopback command possibilities are also supported. The LBCODE[1:0] bits become logical 0 upon either a hardware or software reset.

Register 0x0241 + 0x100*N: MX23 Demux AIS Insert

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DAIS[7]	0
Bit 5	R/W	DAIS[6]	0
Bit 4	R/W	DAIS[5]	0
Bit 3	R/W	DAIS[4]	0
Bit 2	R/W	DAIS[3]	0
Bit 1	R/W	DAIS[2]	0
Bit 0	R/W	DAIS[1]	0

DAIS[7:1]:

Setting any of the DAIS[7:1] bits activates insertion of the alarm indication signal (all ones) into the corresponding DS2 stream demultiplexed from the DS3 signal input on RDAT. Demux AIS insertion takes place after the point where per DS2 loopback may be invoked using the Loopback Activate register thus allowing demux AIS to be inserted into the through path while a DS2 loopback is activated.

Register 0x0242 + 0x100*N: MX23 Mux AIS Insert

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	MAIS[7]	0
Bit 5	R/W	MAIS[6]	0
Bit 4	R/W	MAIS[5]	0
Bit 3	R/W	MAIS[4]	0
Bit 2	R/W	MAIS[3]	0
Bit 1	R/W	MAIS[2]	0
Bit 0	R/W	MAIS[1]	0

MAIS[7:1]:

Setting any of the MAIS[7:1] bits activates insertion of the alarm indication signal (all ones) into the corresponding DS2 stream multiplexed into the DS3 signal output on TDAT. Mux AIS insertion takes place before the point where per DS2 loopback may be invoked using the Loopback Activate register and thus mux AIS cannot be inserted while a DS2 loopback is activated.

Register 0x0243 + 0x100*N: MX23 Loopback Activate

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	LBA[7]	0
Bit 5	R/W	LBA[6]	0
Bit 4	R/W	LBA[5]	0
Bit 3	R/W	LBA[4]	0
Bit 2	R/W	LBA[3]	0
Bit 1	R/W	LBA[2]	0
Bit 0	R/W	LBA[1]	0

LBA[7:1]:

Setting any of the LBA[7:1] bits activates loopback of the corresponding DS2 stream from the input DS3 signal to the output DS3 signal.
The demultiplexed DS2 signals continue to present valid payloads while loopbacks are activated. The MX23 Demux AIS Insert Register allows insertion of DS2 AIS if required.

Register 0x0244 + 0x100*N: MX23 Loopback Request Insert

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	ILBR[7]	0
Bit 5	R/W	ILBR[6]	0
Bit 4	R/W	ILBR[5]	0
Bit 3	R/W	ILBR[4]	0
Bit 2	R/W	ILBR[3]	0
Bit 1	R/W	ILBR[2]	0
Bit 0	R/W	ILBR[1]	0

ILBR[7:1]:

Setting any of the ILBR[7:1] bits enables the insertion of a loopback request in the corresponding DS2 stream in the output DS3 signal. The format of the loopback request is determined by the LBCODE[1:0] bits in the MX23 Configuration Register.

Register 0x0245 + 0x100*N: MX23 Loopback Request Detect

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LBRD[7]	X
Bit 5	R	LBRD[6]	X
Bit 4	R	LBRD[5]	X
Bit 3	R	LBRD[4]	X
Bit 2	R	LBRD[3]	X
Bit 1	R	LBRD[2]	X
Bit 0	R	LBRD[1]	X

LBRD[7:1]:

The LBRD[7:1] bits are set to logic 1 while a loopback request is detected for the corresponding DS2 stream in the input DS3 signal. The LBRD[7:1] bits are set to logic 0 otherwise.

The format of the loopback request expected is determined by the LBCODE[1:0] bits in the MX23 Configuration Register. As per TR-TSY-000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection. Removal of the loopback request is declared when it has been absent for five successive M-frames.

Register 0x0246 + 0x100*N: MX23 Loopback Request Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LBRI[7]	X
Bit 5	R	LBRI[6]	X
Bit 4	R	LBRI[5]	X
Bit 3	R	LBRI[4]	X
Bit 2	R	LBRI[3]	X
Bit 1	R	LBRI[2]	X
Bit 0	R	LBRI[1]	X

LBRI[7:1]:

The LBRI[7:1] bits are set to logic 1 when a loopback request is asserted or deasserted for the corresponding DS2 stream in the input DS3 signal. The LBRI[7:1] bits are set to logic 1 whenever the corresponding LBRD[7:1] bits change state. If interrupts are enabled using the INTE bit in the MX23 Configuration register then the interrupt output, INTB, is activated. The LBRI[7:1] bits are SET to logic 0 immediately following a read of the register, acknowledging the interrupt and deactivating the INTB output.

1.28 DS3 FEAC Transmit Bit Oriented Code Registers

Register 0x0248 + 0x100*N: FEAC XBOC Control

Bit	Type	Function	Default
Bit 7	R	FEACSMPI	X
Bit 6	R/W	FEACSMPE	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	RPT[3]	0
Bit 2	R/W	RPT[2]	0
Bit 1	R/W	RPT[1]	0
Bit 0	R/W	RPT[0]	0

FEACSMPI:

The FEACSMPI bit is set to logic 1 when the FEAC XBOC Code register and RPT[3:0] are sampled by the FEAC XBOC, indicating that the Code Register is ready to be updated with a new FEAC code. FEACSMFPI is set to logic 0 when this register is read.

FEACSMPE:

Setting FEACSMPE to logic 1 enables a hardware interrupt on the TEMUX 84 INTB output pin when FEACSMPI is logic 1.

RPT[3:0]:

These bits contain the 4 bit repeat count used to determine the number (RPT[3:0] + 1) of consecutive, identical, 16-bit bit-oriented code patterns to be transmitted before sampling the FEAC XBOC Code Register, and FEAC XBOC Control Register again. In the event that the Code Register values do not change, the same FEAC code pattern will be repeated continuously. The RPT[3:0] bits can be changed at any time, and are sampled at the same time as the bit oriented code patterns. To obtain the maximum FEAC code modification rate, RPT[3:0] and FEAC[5:0] should be updated and stable within N*16 - 3 FEAC bit periods (approximately 16.7 ms when N is 10) of the INTB interrupt pin asserted low, where N is the number of times the FEAC code is to be repeated.

Register 0x0249 + 0x100*N: FEAC XBOC Code

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	FEAC[5]	1
Bit 4	R/W	FEAC[4]	1
Bit 3	R/W	FEAC[3]	1
Bit 2	R/W	FEAC[2]	1
Bit 1	R/W	FEAC[1]	1
Bit 0	R/W	FEAC[0]	1

FEAC[5:0]:

FEAC[5:0] contains the six bit code that is transmitted on the DS3 far end alarm and control channel (FEAC). The transmitted code consists of a sixteen bit sequence that is repeated continuously. The sequence consists of 8 ones followed by a zero, followed by the six bit code sequence transmitted in order FEAC0, FEAC1, ..., FEAC5, followed by a zero. The all ones sequence is inserted in the FEAC channel when FEAC[5:0] is written with all ones.

1.29 DS3 FEAC Receive Bit Oriented Code Registers

Register 0x024A + 0x100*N: FEAC RBOC Configuration/Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	FEACE	0

FEACE:

The FEACE bit enables the generation of an interrupt when a valid far end alarm and control (FEAC) code is detected. When a logic 1 is written to FEACE, interrupt generation is enabled; the INTB output and the DS3RBOCx bit of one of the Master Interrupt Source DS3 registers is asserted upon a valid FEAC code.

AVC:

The AVC bit position selects the validation criterion used in determining a valid FEAC code. When a logic 0 is written to AVC, a FEAC code is validated when 8 out of the last 10 received codes are identical. The FEAC code is removed when 2 out of the last 10 received codes do not match the validated code.

When a logic 1 is written to AVC, a FEAC code is validated when 4 out of the last 5 received codes are identical. The FEAC code is removed when a single received FEACs does not match the validated code.

IDLE:

The IDLE bit enables the generation of an interrupt when a validated FEAC is removed. When a logic 1 is written to IDLE, the interrupt generation is enabled; the INTB output and the INTB output and the DS3RBOCx bit of one

of the Master Interrupt Source DS3 registers is asserted upon removal of a valid FEAC code.

Register 0x024B + 0x100*N: FEAC RBOC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	IDLI	X
Bit 6	R	FEACI	X
Bit 5	R	FEAC[5]	X
Bit 4	R	FEAC[4]	X
Bit 3	R	FEAC[3]	X
Bit 2	R	FEAC[2]	X
Bit 1	R	FEAC[1]	X
Bit 0	R	FEAC[0]	X

FEAC[5:0]:

The FEAC[5:0] bits contain the received far end alarm and control channel codes. The FEAC[5:0] bits are set to all ones ("111111") when no code has been validated.

FEACI:

The FEACI bit is set to logic 1 when a new FEAC code is validated. The FEAC code value is contained in the FEAC[5:0] bits. The FEACI bit position is set to logic 0 when this register is read.

IDLI:

The IDLI bit is set to logic 1 when a validated FEAC code is removed. The FEAC[5:0] bits are set to all ones when the code is removed. The IDLI bit position is set to logic 0 when this register is read.

1.30 DS2 Framer Registers (N=0 to 2, M=1 to 7)

Registers 0x0240 + 0x100*N +0x10*M: DS2 FRMR #1-#7 Configuration

Bit	Type	Function	Default
Bit 7	R/W	G747	0
Bit 6		Unused	X
Bit 5	R/W	WORD	0
Bit 4	R/W	M2O5	0
Bit 3	R/W	MBDIS	0
Bit 2	R/W	REFR	0
Bit 1		Unused	X
Bit 0		Unused	X

REFR:

The REFR bit is used to trigger reframing. If a logic 1 is written to REFR when it was previously logic 0, the FRMR is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a low-to-high transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transition.

MBDIS:

The MBDIS bit disables the declaration of out-of-frame upon excessive M-bit errors. If MBDIS is a logic 0, out-of-frame is declared when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. If MBDIS is a logic 1, the state of the M-bits is ignored once in frame. Regardless of the state of the MBDIS bit, the F-bits are always monitored for invalid framing.

M2O5:

The M2O5 bit selects the error ratio for declaring out-of-frame (OOF) when in DS2 mode only. When a 1 is written to M2O5, the framer declares OOF when 2 F-bit errors out of 5 consecutive F-bits are observed. When a 0 is written, the framer declares OOF when 2 F-bit errors out of 4 consecutive F-bits are observed. (These two ratios are recommended in TR-TSY-000009 Section 4.1.2) When the DS2 FRMR is configured for G.747 operation (the G747 bit is set to logic 1), the OOF status is declared when 4 consecutive framing word

errors occur (as per CCITT Rec. G747 Section 4), regardless of the M2O5 bit setting.

WORD:

The WORD bit determines the method of accumulating G.747 framing errors. If the WORD bit is a logic 0, each frame alignment signal (FAS) bit error results in a single FERR count. If the WORD bit is a logic 1, one or more bit errors in a FAS word result in a single FERR count.

G747:

The G747 bit configures the DS2 FRMR for G.747 operation. If the G747 bit is a logic 1, the DS2 FRMR will process a G.747 signal. If the G747 bit is a logic 0, the DS2 FRMR will process a DS2 signal as defined in ANSI T1.107 Section 7.

Registers 0x0241 + 0x100*N +0x10*M: DS2 FRMR #1-#7 Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	COFAE	0
Bit 6		Unused	X
Bit 5	R/W	REDE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	RESE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	OOFE	0
Bit 0		Unused	X

These bits enable the propagation of interrupt statuses to the INTB output and enable the setting of the appropriate DS2FRMR bit of the Master Interrupt Source DS2 registers upon assertion of the associated interrupt status bit.

OOFE:

The OOFE bit enables interrupt generation when a DS2 out of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

AISE:

The AISE bit enables interrupt generation when the DS2 AIS maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

RESE:

The RESE bit enables interrupt generation when a change is detected in the debounced value of the reserved bit in Set II when in G.747 mode. The interrupt is enabled when the RESE bit is written with a logic 1. The debounced value of the reserved bit only changes when the reserved bit is the same for two consecutive frames. The RESE bit has no effect in DS2 mode.

FERFE:

The FERFE bit enables interrupt generation when a DS2 far end receive failure defect is declared or removed. The interrupt is enabled when a logic 1 is written.

REDE:

The REDE bit enables an interrupt to be generated when a change of state of the DS2 RED indication occurs. The DS2 RED indication is visible in the REDV bit location of the DS2 FRMR Status register. When REDE is set to logic 1, the interrupt output, INTB, is set to logic 0 when the state of the RED indication changes.

COFAE:

The COFAE bit enables interrupt generation when the TEMUX 84 detects a DS2 change of frame alignment. The interrupt is enabled when a logic 1 is written.

Registers 0x0242 + 0x100*N + 0x10*M: DS2 FRMR #1-#7 Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	X
Bit 6		Unused	X
Bit 5	R	REDI	X
Bit 4	R	FERFI	X
Bit 3	R	RESI	X
Bit 2	R	AISI	X
Bit 1	R	OOFI	X
Bit 0		Unused	X

OOFI:

The OOFI bit is set to logic 1 when an out of frame defect is detected or removed. The OOFI bit position is set to logic 0 when this register is read.

AISI:

The AISI bit is set to logic 1 when the DS2 AIS maintenance signal is detected or removed. The AISI bit position is set to logic 0 when this register is read.

RESI:

The RESI bit is set to logic 1 when the debounced value of the reserved bit in Set II in G.747 mode changes. The debounced value of the reserved bit only changes when the reserved bit is the same for two consecutive frames. This bit has no effect in DS2 mode.

FERFI:

The FERFI bit is set to logic 1 when a FERF defect is detected or removed. The FERFI bit position is set to logic 0 when this register is read.

REDI:

The REDI bit indicates that a change of state of the DS2 RED indication has occurred. The DS2 RED indication is visible in the REDV bit location of the DS2 FRMR Status register. When the REDI bit is a logic 1, a change in the RED state has occurred. When the REDI bit is logic 0, no change in the RED state has occurred.

COFAI:

The COFAI bit is set to logic 1 when a change of frame alignment is detected. A COFA is generated when a new DS2 frame alignment is determined that differs from the last known frame alignment. The COFAI bit position is set to logic 0 when this register is read.

Registers 0x0243 + 0x100*N + 0x10*M: DS2 FRMR #1-#7 Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	REDV	X
Bit 4	R	FERFV	X
Bit 3	R	RESV	X
Bit 2	R	AISV	X
Bit 1	R	OOFV	X
Bit 0		Unused	X

OOFV:

The OOFV bit indicates the current DS2 out of frame defect state. When the DS2 FRMR has lost frame alignment and is searching for the new alignment, OOFV is set to logic 1. When the DS2 FRMR has found DS2 frame alignment, the OOFV bit is set to logic 0.

AISV:

The AISV bit indicates the alarm indication signal state. When the TEMUX 84 detects the AIS maintenance signal, AISV is set to logic 1.

RESV:

The RESV bit reflects the debounced state of the reserved bit in Set II when in G.747 mode. The debounced value of the reserved bit only changes when the reserved bit is the same for two consecutive frames.

FERFV:

The FERFV bit indicates the current far end receive failure defect state.
In DS2 mode, the FERFV bit reflects the debounced state of the X bit (first bit of the M4-Subframe). If the X-bit has been a zero for two consecutive M-frames, the FERFV bit becomes a logic 1. If the X-bit has been a one for two consecutive M-frames, the FERFV bit becomes a logic 0.
In G.747 mode, FERFV bit reflects the debounced state of the Remote Alarm Indication (RAI, bit 1 of Set II) bit. If the RAI bit has been a one for two

consecutive frames, the FERFV bit becomes a logic 1. If the RAI bit has been a zero for two consecutive frames, the FERFV bit becomes a logic 0. A six frame latency of the FERFV status ensures a virtually 100% probability of freezing correctly in DS2 mode upon an out-of-frame condition and a better than 99.9% probability of freezing correctly in G.747 mode.

REDV:

The REDV bit indicates the current state of the DS2 RED indication. The REDV bit is a logic 1 if an out-of-frame condition has persisted for 9.9 ms (6.9ms in G.747 mode). This is less than 1.5 times the maximum average reframe time allowed. The REDV status will remain asserted for 9.9 ms (6.9ms in G.747 mode) after frame alignment has been declare and then become logic 0.

Registers 0x0244 + 0x100*N + 0x10*M: DS2 FRMR #1-#7 Monitor Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	0
Bit 0	R	OVR	0

INTE:

The INTE bit allows the generation of an interrupt, assertion of interrupt output signal INTB, upon transfer of the DS2 error counts into holding registers. A logic 1 in the INTE bit position enables the DS2 FRMR to generate an interrupt when the counter values are transferred to the Holding Registers. A logic 0 in the INTE bit position disables the DS2 FRMR from generating an interrupt. The interrupt is cleared when this register is read if its assertion was a result a transfer operation. Writing a logic 1 to the DS3_E3 bit of the Global Performance Monitor Update register is required to generate a transfer of the counters to the holding registers.

INTR:

The INTR bit indicates the current status of the internal interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the Holding Registers has occurred; a logic 0 indicates that no transfer has occurred. This bit is set to logic 0 when this register is read. The value of the INTR bit is not affected by the value of the INTE bit. Writing a logic 1 to the DS3_E3 bit of the Global Performance Monitor Update register is required to generate a transfer of the counters to the holding registers.

OVR:

The OVR bit indicates the overrun status of the Holding Registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the

Holding Registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

Registers 0x0245 + 0x100*N + 0x10*M: DS2 FRMR #1-#7 FERR Count

Bit	Type	Function	Default
Bit 7	R	FERR[7]	X
Bit 6	R	FERR[6]	X
Bit 5	R	FERR[5]	X
Bit 4	R	FERR[4]	X
Bit 3	R	FERR[3]	X
Bit 2	R	FERR[2]	X
Bit 1	R	FERR[1]	X
Bit 0	R	FERR[0]	X

FERR[7:0]:

This register indicates the number of DS2 framing bit error events or G.747 framing word errors that occurred during the previous accumulation interval. A DS2 framing bit error event is either an M-bit or and F-bit error. One or more bit errors in a G.747 frame alignment signal results in a single framing word error.

A transfer to the holding register can be triggered by writing a logic 1 to the DS3_E3 bit of the Global Performance Monitor Update register.

Registers 0x0246 + 0x100*N + 0x10*M: DS2 FRMR #1-#7 PERR Count (LSB)

Bit	Type	Function	Default
Bit 7	R	PERR[7]	X
Bit 6	R	PERR[6]	X
Bit 5	R	PERR[5]	X
Bit 4	R	PERR[4]	X
Bit 3	R	PERR[3]	X
Bit 2	R	PERR[2]	X
Bit 1	R	PERR[1]	X
Bit 0	R	PERR[0]	X

Registers 0x0247 + 0x100*N + 0x10*M: DS2 FRMR #1-#7 PERR Count (MSB)

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	PERR[12]	X
Bit 3	R	PERR[11]	X
Bit 2	R	PERR[10]	X
Bit 1	R	PERR[9]	X
Bit 0	R	PERR[8]	X

PERR[12:0]:

These two registers indicate the number of G.747 parity error events that occurred during the previous accumulation interval.

A transfer operation can be triggered by writing a logic 1 to the DS3_E3 bit of the Global Performance Monitor Update register.

1.31 MX12 Multiplexer Registers (N=0 to 2, M=1 to 7)

Registers 0x0248 + 0x100*N + 0x10*M: MX12 #1-#7Configuration and Control

Bit	Type	Function	Default
Bit 7	R/W	G747	0
Bit 6	R/W	PINV	0
Bit 5	R/W	MINV	0
Bit 4	R/W	FINV	0
Bit 3	R/W	XAIS	0
Bit 2	R/W	XFERF	0
Bit 1	R/W	XRES	0
Bit 0	R/W	INTE	0

INTE:

When set to logic 1, the INTE bit enables the MX12 to activate the interrupt output, INTB, whenever any of the LBRI[4:1] bits are set to logic 1 in the MX12 Loopback Request Interrupt register. MX12 interrupts are masked when INTE is cleared low.

XRES:

The XRES bit only has effect in G.747 mode. When XRES is set to logic 1 and AIS is not being transmitted, the reserved bit (Set II, bit 3) is set to 0; otherwise, the transmitted reserved bit is set to 1.

XFERF:

When set to logic 1, the XFERF bit enables the transmission of the far end receive failure (FERF) signal in the DS2 output stream when in DS2 mode (i.e. G747 bit logic 0). When XFERF is set to logic 1, the transmitted X bit is set to 0, provided that AIS is not being transmitted; otherwise the transmitted X bit is set to 1. When in G.747 mode (i.e. G747 bit high), the remote alarm indication (RAI) is set to 1 when XFERF is set to logic 1; otherwise, the transmitted RAI bit is set to 0 unless AIS is being transmitted.

XAIS:

When set to a logic 1, the XAIS bit enables the transmission of the alarm indication signal (AIS) in the DS2 stream. When XAIS is set to logic 1, the transmitted data is set to all ones; otherwise the transmitted data is not affected.

FINV:

When FINV is set to logic 1 and G747 is low, all the transmitted F bits in the DS2 output stream are logically inverted for diagnostic purposes. If G747 is high when FINV is set to logic 1, the nine bit frame alignment signal (111010000) is logically inverted (i.e. 000101111).

MINV:

When MINV is set to a logic 1, the transmitted M bits in the DS2 stream are inverted for diagnostic purposes. This only has effect when the G747 bit is low.

PINV:

When PINV is set to logic 1, the transmitted parity bit in the G.747 formatted output stream is inverted for diagnostic purposes. This only has effect when the G747 bit is high.

G747:

When G747 is high, the MX12 supports CCITT Recommendation G.747. In this mode, three 2048 kbit/s tributaries are multiplexed into and demultiplex out of an 840-bit frame. If G747 is low, the frame format is compatible with DS2 as specified in the ANSI T1.107 Standard.

Registers 0x0249 + 0x100*N + 0x10*M: MX12 #1-#7 Loopback Code Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	LBCODE[1]	0
Bit 0	R/W	LBCODE[0]	0

LBCODE[1:0]:

The LBCODE[1:0] bits select the valid state for a loopback request coded in the C-bits of the DS2 signals. Transmit and receive are not independent; the same code is expected in the receive DS2 as is inserted in the transmitted DS2. The following table gives the correspondence between LBCODE[1:0] bits and the valid codes:

LBCODE[1:0]	Loopback Code
00	C1 = C2 and C1 = $\overline{C3}$
01	C1 = C3 and C1 = $\overline{C2}$
10	C2 = C3 and C1 = $\overline{C2}$
11	C1 = C2 and C1 = $\overline{C3}$

If LBCODE[1:0] is 'b00 or 'b11, the loopback code is as per ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7

The LBCODE[1:0] bits become logical 0 upon either a hardware or software reset.

The LBCODE[1:0] bits will also select the valid state for a loopback request coded in the C-bits of the G.747 formatted signal. Again, the transmit and receive are not independent; the same code is expected in the demultiplexed

G.747 stream as is inserted in the G.747 stream to be multiplexed. The valid codes are the same as those for the DS2 formatted stream given in the table above.

Register 0x024A + 0x100*N +0x10*M: MX12 #1-#7 Mux/Demux AIS Insert

Bit	Type	Function	Default
Bit 7	R/W	MAIS[4]	0
Bit 6	R/W	MAIS[3]	0
Bit 5	R/W	MAIS[2]	0
Bit 4	R/W	MAIS[1]	0
Bit 3	R/W	DAIS[4]	0
Bit 2	R/W	DAIS[3]	0
Bit 1	R/W	DAIS[2]	0
Bit 0	R/W	DAIS[1]	0

DAIS[4:1]:

Setting any of the DAIS[4:1] bits activates insertion of the alarm indication signal (all ones) into the corresponding DS1 stream demultiplexed from the DS2 signal. Demux AIS insertion takes place after the point where remote loopback may be invoked using the Loopback Activate register, thus allowing demux AIS to be inserted into the through path while a loopback is activated.

MAIS[4:1]:

Setting any of the MAIS[4:1] bits activates insertion of the alarm indication signal (all ones) into the corresponding DS1 stream multiplexed into the DS2 signal. Mux AIS insertion takes place before the point where remote loopback may be invoked using the Loopback Activate register and thus mux AIS cannot be inserted while a loopback is activated.

Registers 0x024B + 0x100*N +0x10*M: MX12 #1-#7 Loopback Activate

Bit	Type	Function	Default
Bit 7	R/W	ILBR[4]	0
Bit 6	R/W	ILBR[3]	0
Bit 5	R/W	ILBR[2]	0
Bit 4	R/W	ILBR[1]	0
Bit 3	R/W	LBA[4]	0
Bit 2	R/W	LBA[3]	0
Bit 1	R/W	LBA[2]	0
Bit 0	R/W	LBA[1]	0

LBA[4:1]:

Setting any of the LBA[4:1] bits activates loopback of the corresponding stream from the DS2 signal received to the DS2 signal transmitted. The demultiplexed DS1 streams continue to present valid payloads while loopbacks are activated. The AIS Insert Register allows insertion of AIS if required. LBA[4] has no effect in G.747 mode, but LBA[3:1] activates the loopback of the corresponding 2048 kbit/s signal.

ILBR[4:1]:

Setting any of the ILBR[4:1] bits enables the insertion of a loopback request in the corresponding DS1 streams in the DS2 output signal. The loopback is indicated by inverting the C_{j1}, C_{j2} or C_{j3} bits according to the format of the loopback request is determined by the LBCODE[1:0] bits in the Loopback Code Select Register. In G.747 mode, ILBR[j] inverts bit C_{j1}, C_{j2} or C_{j3} in the G.747 frame in an analogous fashion.

Register 0x024C + 0x100*N + 0x10*M: MX12 #1-#7 Loopback Interrupt

Bit	Type	Function	Default
Bit 7	R	LBRI[4]	0
Bit 6	R	LBRI[3]	0
Bit 5	R	LBRI[2]	0
Bit 4	R	LBRI[1]	0
Bit 3	R	LBRD[4]	0
Bit 2	R	LBRD[3]	0
Bit 1	R	LBRD[2]	0
Bit 0	R	LBRD[1]	0

LBRD[4:1]:

The LBRD[4:1] bits are a logic 1 while a loopback request is detected for the corresponding DS1 stream in the received DS2 signal. The LBRD[4:1] bits are a logic 0 otherwise. The format of the loopback request expected is determined by the LBCODE[1:0] bits in the Loopback Code Select Register. As per TR-TSY-000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection. Removal of the loopback request is declared when it has been absent for five successive M-frames. LBRD[4] is not used in G747 mode.

LBRI[4:1]:

The LBRI[4:1] bits are a logic 1 when a loopback request is asserted or deasserted for the corresponding DS1 stream in the received DS2 signal. The LBRI[4:1] bits are set to a logic 1 whenever the corresponding LBRD[4:1] bits change state. If interrupts are enabled using the INTE bit in the Configuration register then the interrupt output, INTB, is activated. The LBRI[4:1] bits are set to a logic 0 immediately following a read of this register, acknowledging the interrupt and deactivating the INTB output. LBRI[4] is not used in G747 mode.

1.32 E3 FRMR Registers

Register 0x02C0 + 0x100*N: E3 FRMR Framing Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	UNI	0
Bit 3	R/W	FORMAT[1]	0
Bit 2	R/W	FORMAT[0]	0
Bit 1	R/W	REFRDIS	0
Bit 0	R/W	REFR	0

REFR:

A transition from logic 0 to logic 1 in the REFR bit position forces the E3 Framer to initiate a search for frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to initiate subsequent searches for frame alignment.

REFRDIS:

The REFRDIS bit disables reframing under the consecutive framing bit error condition once frame alignment has been found, leaving reframing to be initiated only by software via the REFR bit. A logic 1 in the REFRDIS bit position causes the FRMR to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur when four consecutive framing patterns are received in error.

FORMAT[1:0]:

The FORMAT[1:0] bits determine the framing mode used for pattern matching when finding frame alignment and for generating the output status signals. The FORMAT[1:0] bits select one of two framing formats:

Table 6 E3 FRMR FORMAT[1:0] Configurations

FORMAT[1]	FORMAT[0]	Framing Format Selected
0	0	G.751 E3 format
0	1	G.832 E3 format
1	0	Reserved
1	1	Reserved

UNI:

The UNI bit selects the mode of the receive data interface. When UNI is logic 1, the E3-FRMR expects unipolar data on the RDAT input and accepts line code violation indications on the RLCV input. When UNI is logic 0, the E3-FRMR expects bipolar data on the RPOS and RNEG inputs and decodes the pulses according to the HDB3 line code.

Reserved:

The Reserved bit must be programmed to logic 0 for proper operation.

Register 0x02C1 + 0x100*N: E3 FRMR Maintenance Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	WORDBIP	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	WORDERR	0
Bit 2	R/W	PYLD&JUST	0
Bit 1	R/W	FERFDET	0
Bit 0	R/W	TMARKDET	0

TMARKDET:

The TMARKDET bit determines the persistency check performed on the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte). When TMARKDET is logic 1, the Timing Marker bit must be in the same state for 5 consecutive frames before the TIMEMK status is changed to that state. When TMARKDET is logic 0, the Timing Marker bit must be in the same state for 3 consecutive frames. When a framing mode other than G.832 is selected, the setting of the TMARKDET bit is ignored.

FERFDET:

The FERFDET bit determines the persistency check performed on the Far End Receive Failure (FERF) bit (bit 1 of the G.832 Maintenance and Adaptation byte) or on the Remote Alarm indication (RAI) bit (bit 11 of the frame inG.751 mode). When FERFDET is logic 1, the FERF, or RAI, bit must be in the same state for 5 consecutive frames before the FERF/RAI status is changed to that state. When FERFDET is logic 0, the FERF, or RAI, bit must be in the same state for 3 consecutive frames.

PYLD&JUST:

The PYLD&JUST bit selects whether the justification service bits and the tributary justification bits in framing mode G.751 is indicated as overhead or payload. When PYLD&JUST is logic 1, the justification service bits and the tributary justification bits are indicated as payload by the ROVRHD outputs. When PYLD&JUST is logic 0, the justification service and tributary justification bits are indicated as overhead.

WORDERR:

The WORDERR bit selects whether the framing bit errors accumulated in PMON indicate all bit errors in the framing pattern or only one error for one or more errors in the framing pattern. When WORDERR is logic 1, one or more framing bit errors in a frame results in a single FERR increment. When WORDERR is logic 0, each framing bit error results in a FERR increment.

WORDBIP:

The WORDBIP bit selects whether the transmitted FEBEs indicate all bit errors in the BIP-8 pattern or only one error for one or more errors in the BIP-8 pattern. When WORDBIP is logic 1, one or more parity bit errors in a frame result in a single FEBE indication. When WORDBIP is logic 0, each and every parity bit error results in a FEBE indication. For G.832 applications, this bit should be set to logic 1.

Register 0x02C2 + 0x100*N: E3 FRMR Framing Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	CZDE	0
Bit 3	R/W	LOSE	0
Bit 2	R/W	LCVE	0
Bit 1	R/W	COFAE	0
Bit 0	R/W	OOFE	0

Besides allowing propagation of interrupt statuses to the INTB output, these bits also enable the setting of the E2FRMRx bit of one of the Master Interrupt Source DS3/E3 registers upon assertion of the associated interrupt status bit.

OOFE:

The OOFE bit is an interrupt enable. When OOFE is logic 1, a change of state of the OOF status generates an interrupt and sets the INTB output to logic 0. When OOFE is logic 0, changes of state of the OOF status are disabled from causing interrupts on the INTB output.

COFAE:

The COFAE bit is an interrupt enable. When COFAE is logic 1, a change of frame alignment generates an interrupt and sets the INTB output to logic 0. When COFAE is logic 0, changes of frame alignment are disabled from causing interrupts on the INTB output.

LCVE:

The LCVE bit is an interrupt enable. When LCVE is logic 1, detection of a line code violation generates an interrupt and sets the INTB output to logic 0. When LCVE is logic 0, occurrences of line code violations are disabled from causing interrupts on the INTB output.

LOSE:

The LOSE bit is an interrupt enable. When LOSE is logic 1, a change of state of the loss-of-signal generates an interrupt and sets the INTB output to logic

0. When LOSE is logic 0, occurrences of loss-of-signal are disabled from causing interrupts on the INTB output.

CZDE:

The CZDE bit is an interrupt enable. When CZDE is logic 1, detection of four consecutive zeros in the HDB3-encoded stream generates an interrupt and sets the INTB output to logic 0. When CZDE is logic 0, occurrences of consecutive zeros are disabled from causing interrupts on the INTB output.

Register 0x02C3 + 0x100*N: E3 FRMR Framing Interrupt Indication and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	CZDI	X
Bit 5	R	LOSI	X
Bit 4	R	LCVI	X
Bit 3	R	COFAI	X
Bit 2	R	OOFI	X
Bit 1	R	LOS	X
Bit 0	R	OOF	X

OOF:

The OOF bit indicates the current state of the E3-FRMR. When OOF is logic 1, the E3-FRMR is out of frame alignment and actively searching for the new alignment. While OOF is high all status indications and overhead extraction continue with the previous known alignment. When OOF is logic 0, the E3-FRMR has found a valid frame alignment and is operating in a maintenance mode, indicating framing bit errors, and extracting and processing overhead bits. During reset, OOF is set to logic 1, but the setting may change prior to the register being read.

LOS:

The LOS bit indicates the current state of the Loss-Of-Signal detector. When LOS is logic 1, the E3-FRMR has received 32 consecutive RCLK cycles with no occurrences of bipolar data on RPOS and RNEG. When LOS is logic 0, the FRMR is receiving valid bipolar data. When the E3-FRMR has declared loss of signal, the LOS indication is set to logic 0 (de-asserted) when the E3-FRMR has received 32 consecutive RCLK cycles containing no occurrences of 4 consecutive zeros. The LOS bit is forced to logic 0 if the UNI bit is logic 1. During reset, LOS is set to logic 0, but the setting may change prior to the register being read.

OOFI:

A logic 1 OOFI bit indicates a change in the OOF status. The OOFI bit is cleared to logic 0 upon the completion of the register read. When OOFI is

logic 0, it indicates that no OOF state change has occurred since the last time this register was read.

COFAI:

The COFAI bit indicates that a change of frame alignment between the previous alignment and the newly found alignment has occurred. When COFAI is logic 1, the last high-to-low transition on the OOF signal resulted in the new frame alignment differing from the previous one. The COFAI bit is cleared to logic 0 upon the completion of the register read. When COFAI is logic 0, it indicates that no change in frame alignment has occurred when OOF went low.

LCVI:

The LCVI bit indicates that a line code violation has occurred. When LCVI is logic 1, a line code violation on the RPOS and RNEG inputs was detected since the last time this register was read. The LCVI bit is cleared to logic 0 upon the completion of the register read. When LCVI is logic 0, it indicates that no line code violation was detected since the last register read. When the UNI bit in the Framing Options register is logic 1, the LCVI is forced to logic 0.

LOSI:

The LOSI bit indicates that a state transition occurred on the LOS status signal. When LOSI is logic 1, a high-to-low or low-to-high transition occurred on the LOS status signal since the last time this register was read. The LOSI bit is cleared to logic 0 upon the completion of the register read. When LOSI is logic 0, it indicates that no state change has occurred on LOS since the last time this register was read. When the UNI bit in the Framing Options register is logic 1, the LOSI is forced to logic 0.

CZDI:

The CZDI bit indicates that four consecutive zeros in the HDB3-encoded stream have been detected. CZDI is asserted to a logic 1, whenever the CZD signal is asserted. The CZDI bit is cleared to a logic 0 upon the completion of the register read. When CZDI is logic 0, it indicates that no occurrences of four consecutive zeros was detected since the last register read. When the UNI bit in the Framing Options register is logic 1, the CZDI indication is forced to logic 0.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The indication bits (bits 2,3,4,5,6 of this register) are cleared to

logic 0 after the register is read; the INTB output is also cleared to high impedance if the interrupt was generated by any of these five events.

Register 0x02C4 + 0x100*N: E3 FRMR Maintenance Event Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	FERRE	0
Bit 6	R/W	PERRE	0
Bit 5	R/W	AISDE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	FEBEE	0
Bit 2	R/W	PTYPEE	0
Bit 1	R/W	TIMEMKE	0
Bit 0	R/W	NATUSEE	0

Besides allowing propagation of interrupt statuses to the INTB output, these bits also enable the setting of the DS3E3INT bit of the Master Interrupt Source register upon assertion of the associated interrupt status bit.

NATUSEE:

The NATUSEE bit is an interrupt enable. When NATUSEE is logic 1, an interrupt is generated on the INTB output when the National Use bit (bit 12 of the frame in G.751 E3 mode) changes state. When NATUSEE is logic 0, changes in state of the National Use bit does not cause an interrupt on INTB.

TIMEMKE:

The TIMEMKE bit is an interrupt enable. When TIMEMKE is logic 1, an interrupt is generated on the INTB output when the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) changes state after the selected persistency check is applied. When TIMEMKE is logic 0, changes in state of the Timing Marker bit does not cause an interrupt on INTB.

PTYPEE:

The PTYPEE bit is an interrupt enable. When PTYPEE is logic 1, an interrupt is generated on the INTB output when the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte) change state. When PTYPEE is logic 0, changes in state of the Payload Type bits does not cause an interrupt on INTB.

FEBEE:

The FEBEE bit is an interrupt enable. When FEBEE is logic 1, an interrupt is generated on the INTB output when the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte) changes state. When FEBEE is logic 0, changes in state of the FEBE bit does not cause an interrupt on INTB.

FERFE:

The FERFE bit is an interrupt enable. When FERFE is logic 1, an interrupt is generated on the INTB output when the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or when the Remote Alarm indication bit (bit 11 of the frame in G.751) changes state after the selected persistency check is applied. When FERFE is logic 0, changes in state of the FERF or RAI bit does not cause an interrupt on INTB.

AISDE:

The AISDE bit is an interrupt enable. When AISDE is logic 1, an interrupt is generated on the INTB output when the AISD indication changes state. When AISDE is logic 0, changes in state of the AISD signal does not cause an interrupt on INTB.

PERRE:

The PERRE bit is an interrupt enable. When PERRE is logic 1, an interrupt is generated on the INTB output when a BIP-8 error (in G.832 mode) is detected. When PERRE is logic 0, occurrences of BIP-8 errors do not cause an interrupt on INTB.

FERRE:

The FERRE bit is an interrupt enable. When FERRE is logic 1, an interrupt is generated on the INTB output when a framing bit error is detected. When FERRE is logic 0, occurrences of framing bit errors do not cause an interrupt on INTB.

Register 0x02C5 + 0x100*N: E3 FRMR Maintenance Event Interrupt Indication

Bit	Type	Function	Default
Bit 7	R	FERRI	0
Bit 6	R	PERRI	0
Bit 5	R	AISDI	0
Bit 4	R	FERFI	0
Bit 3	R	FEBEI	0
Bit 2	R	PTYPEI	0
Bit 1	R	TIMEMKI	0
Bit 0	R	NATUSEI	0

NATUSEI:

The NATUSEI bit is a transition Indication. When NATUSEI is logic 1, a change of state of the National Use bit (bit 12 of the frame in G.751 E3 mode) has occurred. When NATUSEI is logic 0, no change of state of the National Use bit has occurred since the last time this register was read.

TIMEMKI:

The TIMEMKI bit is a transition indication. When TIMEMKI is logic 1, a change in state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) has occurred. When TIMEMKI is logic 0, no changes in the state of the Timing Marker bit occurred since the last time this register was read.

PTYPEI:

The PTYPEI bit is a transition indication. When PTYPEI is logic 1, a change of state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte) has occurred. When PTYPEI is logic 0, no changes in the state of the Payload Type bits has occurred since the last time this register was read.

FEBEI:

The FEBEI bit is a transition indication. When FEBEI is logic 1, a change of state of the Far End Block Error indication bit (bit 2 of the G.832 Maintenance

and Adaptation byte) has occurred. When FEBEI is logic 0, no changes in the state of the FEBE bit has occurred since the last time this register was read.

FERFI:

The FERFI bit is a transition indication. When FERFI is logic 1, a change of state of the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or when the Remote Alarm indication bit (bit 12 of the frame in G.751) has occurred. When FERFI is logic 0, no changes in the state of the FERF or RAI bit has occurred since the last time this register was read.

AISDI:

The AISDI bit is a transition indication. When AISDI is logic 1, a change in state of the AISD indication has occurred. When AISDI is logic 0, no changes in the state of the AISD signal has occurred since the last time this register was read.

PERRI:

The PERRI bit is an event indication. When PERRI is logic 1, the occurrence of one or more BIP-8 errors (in G.832 mode) has been detected. When PERRI is logic 0, no occurrences of BIP-8 errors have occurred since the last time this register was read.

FERRI:

The FERRI bit is an event indication. When FERRI is logic 1, the occurrence of one or more framing bit error has been detected. When FERRI is logic 0, no occurrences of framing bit errors have occurred since the last time this register was read.

The transition/event interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the activity of the maintenance events. The contents of this register are cleared to logic 0 after the register is read; the INTB output is also cleared to high impedance if the interrupt was generated by any of the Maintenance Event outputs.

Register 0x02C6 + 0x100*N: E3 FRMR Maintenance Event Status

Bit	Type	Function	Default
Bit 7	R	AISD	X
Bit 6	R	FERF/RAI	X
Bit 5	R	FEBE	X
Bit 4	R	PTYPE[2]	X
Bit 3	R	PTYPE[1]	X
Bit 2	R	PTYPE[0]	X
Bit 1	R	TIMEMK	X
Bit 0	R	NATUSE	X

NATUSE:

The NATUSE bit reflects the state of the extracted National Use bit (bit 12 of the frame in G.751 E3 mode).

TIMEMK:

The TIMEMK bit reflects the state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte).

PTYPE[2:0]:

The PTYPE[2:0] bits reflect the state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte). These bits are not latched and should be read 2 or 3 times in rapid succession to ensure a coherent binary value.

FEBE:

The FEBE bit reflects the state of the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte).

FERF:

The FERF bit reflects the value of the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or the value of the Remote Alarm Indication bit (bit 11 of the frame in G.751) when the value has been the same for either 3 or 5 consecutive frames.

AISD:

The AISD bit reflects the state of the AIS detection circuitry. When AISD is logic 1, less than 8 zeros (in G.832 mode), or less than 5 zeros (in G.751 mode), were detected during one complete frame period while the FRMR is out of frame alignment. When AISD is logic 0, 8 or more zeros (in G.832 mode), or 5 or more zeros (in G.751 mode), were detected during one complete frame period, or the FRMR has found frame alignment.

1.33 E3 TRAN Registers

Register 0x02C8 + 0x100*N: E3 TRAN Framing Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	FORMAT[1]	0
Bit 0	R/W	FORMAT[0]	0

FORMAT[1:0]:

The FORMAT[1:0] bits determine the framing mode used for framing pattern when generating the formatted output data stream. The FORMAT[1:0] bits select one of two framing formats:

Table 7 E3 TRAN FORMAT[1:0] Configurations

FORMAT[1]	FORMAT[0]	Framing Format Selected
0	0	G.751 E3 format
0	1	G.832 E3 format
1	0	Reserved
1	1	Reserved

Reserved:

The Reserved bits must be programmed to logic 0 for correct operation.

Register 0x02C9 + 0x100*N: E3 TRAN Status and Diagnostic Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	CPERR	0
Bit 4	R/W	DFERR	0
Bit 3	R/W	DLCV	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TAIS	0
Bit 0	R/W	NATUSE	1

NATUSE:

The NATUSE bit determines the default value of the National Use bit inserted into the G.751 E3 frame overhead. The value of the NATUSE bit is logically ORed with the bit collected once per frame from the internal HDLC transmitter (if TNETOP is set to logic 1). When TNETOP is logic 0, the NATUSE bit controls the value of the National Use bit. When NATUSE is logic 1, the National Use bit (bit 12 in G.751) is forced to logic 1 regardless of the bit input from the internal HDLC transmitter or the setting of TNETOP. When NATUSE is logic 0, the National Use bit is set to the value sampled from the internal HDLC transmitter if TNETOP is logic 0. Otherwise, the National Use bit will be set to logic 0. If the E3 TRAN is configured for G.832 mode, this bit is ignored.

TAIS:

The TAIS bit enables AIS signal transmission. When TAIS is logic 1, the all 1's AIS signal is transmitted. When TAIS is logic 0, the normal data is transmitted.

Reserved:

The Reserved bits must be programmed to logic 0 for proper operation.

DLCV:

The DLCV bit selects whether a line code violation is generated for diagnostic purposes. When DLCV changes from logic 0 to logic 1, a single LCV is

generated; in HDB3, the LCV is generated by causing a bipolar violation pulse of the same polarity to the previous bipolar violation. To generate another LCV, the DLCV register bit must be first be written to logic 0 and then to logic 1 again.

DFERR:

The DFERR bit selects whether the framing pattern is corrupted for diagnostic purposes. When DFERR is logic 1, the framing pattern inserted into the output data stream is inverted. When DFERR is logic 0, the unaltered framing pattern inserted into the output data stream.

CPERR:

The CPERR bit enables continuous generation of BIP-8 errors for diagnostic purposes. When CPERR is logic 1, the calculated BIP-8 value is continuously inverted according to the error mask specified by the BIP-8 Error Mask register and inserted into the G.832 EM byte. When CPERR is logic 0, the calculated BIP-8 value is altered only once, according to the error mask specified by the BIP-8 Error Mask register, and inserted into the EM byte.

Register 0x02CA + 0x100*N: E3 TRAN BIP-8 Error Mask

Bit	Type	Function	Default
Bit 7	R/W	MBIP[7]	0
Bit 6	R/W	MBIP[6]	0
Bit 5	R/W	MBIP[5]	0
Bit 4	R/W	MBIP[4]	0
Bit 3	R/W	MBIP[3]	0
Bit 2	R/W	MBIP[2]	0
Bit 1	R/W	MBIP[1]	0
Bit 0	R/W	MBIP[0]	0

MBIP[7:0]:

The MBIP[7:0] bits act as an error mask to cause the transmitter to insert up to 8 BIP-8 errors. The contents of this register are XORed with the calculated BIP-8 byte and inserted into the G.832 EM byte of the frame. A logic 1 in any MBIP bit position causes that bit position in the EM byte to be inverted. Writing this register with a mask value causes that mask to be applied only once; if continuous BIP-8 errors are desired, the CPERR bit in the E3 TRAN Status and Diagnostic Options register can be used.

Register 0x02CB + 0x100*N: E3 TRAN Maintenance and Adaptation Options

Bit	Type	Function	Default
Bit 7	R/W	FERF/RAI	0
Bit 6	R/W	FEBE	0
Bit 5	R/W	PTYPE[2]	0
Bit 4	R/W	PTYPE[1]	0
Bit 3	R/W	PTYPE[0]	0
Bit 2	R/W	TUMFRM[1]	0
Bit 1	R/W	TUMFRM[0]	0
Bit 0	R/W	TIMEMK	0

TIMEMK:

The TIMEMK bit determines the state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte). When TIMEMK is set to logic 1, the Timing Marker bit in the MA byte is set to logic 1. When TIMEMK is set to logic 0, the Timing Marker bit in the MA byte is set to logic 0.

TUMFRM[1:0]:

The TUMFRM[1:0] bits reflect the value to be inserted in the Tributary Unit Multiframe bits (bits 6, and 7 of the G.832 Maintenance and Adaptation byte).

PTYPE[2:0]:

The PTYPE[2:0] bits reflect the value to be inserted in the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte).

FEBE:

The FEBE bit reflects the value to be inserted in the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte). The FEBE bit value is logically ORed with the FEBE indications generated by the FRMR for any detected BIP-8 errors. When the FEBE bit is logic 1, bit 2 of the G.832 MA byte is set to logic 1; when the FEBE bit is logic 0, any BIP-8 error indications from the FRMR causes bit 2 of the MA byte to be set to logic 1.

FERF/RAI:

The FERF/RAI bit reflects the value to be inserted in the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or the value of the Remote Alarm indication bit (bit 11 of the frame in G.751). The FERF/RAI bit is logically ORed with the LOS, OOF, AIS, and LCD indications from the E3 FRMR when the LOSEN, OOFEN and AISEN register bits in the DS3/E3 Master Alarm Enable register are set to logic 1 respectively. When the OR of the two signals is logic 1, the FERF or RAI bit in the frame is set to logic 1; when neither signal is logic 1, the FERF or RAI bit is set to logic 0.

1.34 E3 Trail Trace Buffer Registers

Register 0x02D0 + 0x100*N: TTB Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

LEN16:

The path trace message length bit (LEN16) selects the length of the message to be 16 bytes or 64 bytes. The LEN16 bit must be programmed to logic 1 for proper operation in G.832 applications.

NOSYNC:

The NOSYNC bit disables synchronization to the Trail Trace message. When NOSYNC is set to logic 1, synchronization is disabled and the bytes of the Trail Trace message are captured by the TTB in a circular buffer. When NOSYNC is set to logic 0, the TTB synchronizes to the byte with the most significant bit set to logic 1 and places that byte in the first location in the capture buffer page.

TNULL:

The transmit null (TNULL) bit controls the insertion of all-zeros into the outgoing Trail Trace message. The null insertion should be used when microprocessor accesses are being performed that change the outgoing trail trace message. When TNULL is set to logic 1, an all-zeros byte is inserted into the transmit stream. When this bit is set to logic 0, the contents of the transmit trace buffer are sent.

PER5:

The receive trace identifier persistency bit (PER5) controls the number of times that persistency check is made in order to accept the received message. When this bit is set to logic 1, five identical message required in order to accept the message. When this bit set to logic 0, three unchanged consecutive messages are required.

RTIMIE:

The receive trace identifier mismatch interrupt enable (RTIMIE) controls the activation of the interrupt output when comparison between the accepted trace identifier message and the expected trace identifier message changes state from match to mismatch and vice versa. When RTIMIE is set to logic 1, changes in match state will activate the interrupt output. When RTIMIE set to logic 0, trail trace message match state changes will not affect INTB or the TTB status bit of the Master Interrupt Source DS2 register.

RTIUIE:

The receive trace identifier unstable interrupt enable (RTIUIE) control the activation of the interrupt output when the receive trace identifier message changes state from stable to unstable and vice versa. When RTIUIE is set to logic 1, changes in the state of the trail trace message unstable indication will activate the interrupt output. When RTIUIE set to logic 0, trail trace unstable state changes will not effect INTB or the TTB status bit of the Master Interrupt Source DS2 register.

RRAMACC**:**

The receive RAM access (RRAMACC) control bit is used by the microprocessor to identify that the access by the microprocessor is to the receive trace buffers or to the transmit trace buffer. When RRAMACC is set to logic 1, subsequent microprocessor read and write accesses are directed to the receive side trace buffers. When RRAMACC is set to logic 0, microprocessor accesses are directed to the transmit side trace buffer.

ZEROEN**:**

The zero enable bit (ZEROEN) enables TIM assertion and removal based on an all ZEROs path trace message string. When ZEROEN is set to logic 1, all ZEROs path trace message strings are considered when entering and exiting TIM states. When ZEROEN is set to logic 0, all ZEROs path trace message strings are ignored.

Register 0x02D1 + 0x100*N: TTB Trail Trace Identifier Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

RTIMV:

The receive trace identifier mismatch value status bit (RTIMV) is set to logic 1 when the accepted message differs from the expected message. RTIMV is set to logic 0 when the accepted message is equal to the expected message. A mismatch is not declared if the accepted trail trace message string is all-zeros.

RTIMI:

The receive trace identifier mismatch indication status bit (RTIMI) is set to logic 1 when match/mismatch status of the trace identifier framer changes state. This bit (and the interrupt) is cleared when this register is read.

RTIUV:

The receive trace identifier unstable value status bit (RTIUV) is set to logic 1 when 8 messages that differ from its immediate predecessor are received. RTIUV is set to logic 0 and the unstable message count is reset when 3 or 5 (depending on PER5 control bit) consecutive identical messages are received.

RTIUI:

The receive trace identifier unstable indication status bit (RTIUV) is set to logic 1 when the stable/unstable status of the trace identifier framer changes state. This bit (and the interrupt) is cleared when this register is read.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to the trail trace RAM has been completed. BUSY is set to logic 1 upon writing to the TTB Indirect Address register, and stays high until the access has completed. At this point, BUSY is set to logic 0. This register should be polled to determine when either new data is available in the TTB Indirect Data register after an indirect read, or when the TTB is ready to accept another write access.

Register 0x02D2 + 0x100*N: TTB Indirect Address

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

A[6:0]:

The indirect read address bits (A[6:0]) indexes into the trail trace identifier buffers. When RRAMACC is set to logic 1, decimal addresses 0 to 63 reference the receive capture page while addresses 64 to 127 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive G.832 E3 stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor. When RRAMACC is set to logic 0, decimal addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted in the TR bytes of the G.832 E3 transmit stream. In this case A[6] is a don't care (I.e., address 0 and address 64 are indexes to the same location in the buffer). Note that only the first 16 addresses need to be written with the trail trace message to be transmitted.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the static page of the trail trace message buffer. Writing to this indirect address register initiates an external microprocessor access to the static page of the trail trace message buffer. When RWB is set to logic 1, a read access is initiated. The data read is available upon completion of the access in the TTB Indirect Data register. When RWB is set to logic 0, a write access is initiated. The data in the TTB Indirect Data register will be written to the addressed location in the static page.

Register 0x02D3 + 0x100*N: TTB Indirect Data

Bit	Type	Function	Default
Bit 7	R/W	D[7]	X
Bit 6	R/W	D[6]	X
Bit 5	R/W	D[5]	X
Bit 4	R/W	D[4]	X
Bit 3	R/W	D[3]	X
Bit 2	R/W	D[2]	X
Bit 1	R/W	D[1]	X
Bit 0	R/W	D[0]	X

D[7:0]:

The indirect data bits (D[7:0]) contain either the data read from a message buffer after an indirect read operation has completed, or the data to be written to the RAM for an indirect write operation. Note that the write data must be set up in this register before an indirect write is initiated. Data read from this register reflects the value written until the completion of a subsequent indirect read operation.

Register 0x02D4 + 0x100*N: TTB Expected Payload Type Label

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	EXPLD[2]	0
Bit 1	R/W	EXPLD[1]	0
Bit 0	R/W	EXPLD[0]	0

EXPLD[2:0]:

The EXPLD[2:0] bits contain the expected payload type label bits of the G.832 E3 Maintenance and Adaptation (MA) byte. The EXPLD[2:0] bits are compared with the received payload type label extracted from the receive stream. A payload type label mismatch (PLDM) is declared if the received payload type bits differs from the expected payload type. If enabled, an interrupt is asserted upon declaration and removal of PLDM.

For compatibility with old equipment that inserts 000B for unequipped or 001B for equipped, regardless of the payload type, the receive payload type label mismatch mechanism is based on the following table:

Table 8 TTB Payload Type Match Configurations

Expected	Received	Action
000	000	Match
000	001	Mismatch
000	XXX	Mismatch
001	000	Mismatch
001	001	Match
001	XXX	Match
XXX	000	Mismatch

Expected	Received	Action
XXX	001	Match
XXX	XXX	Match
XXX	YYY	Mismatch

Note:

XXX, YYY = anything except 000B or 001B, and XXX is not equal to YYY.

Reserved:

The reserved bits must be written to logic 0 for proper operation.

Register 0x02D5 + 0x100*N: TTB Payload Type Label Control/Status

Bit	Type	Function	Default
Bit 7	R/W	RPLDUIE	0
Bit 6	R/W	RPLDMIE	0
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	RPLDUI	X
Bit 2	R	RPLDUV	X
Bit 1	R	RPLDMI	X
Bit 0	R	RPLDMV	X

RPLDMV:

The receive payload type label mismatch status bit (RPLDMV) reports the match/mismatch status between the expected and the received payload type label. RPLDMV is set to logic 1 when the received payload type bits differ from the expected payload type written to the TTB Expected Payload Type Label Register. The PLDMV bit is set to logic 0 when the received payload type matches the expected payload type.

RPLDMI:

The receive payload type label mismatch interrupt status bit (RPLDMI) is set to logic 1 when the match/mismatch status between the received and the expected payload type label changes state. This bit (and the interrupt) is cleared when this register is read.

RPLDUV:

The receive payload type label unstable status bit (RPLDUV) reports the stable/unstable status of the payload type label bits in the receive stream. RPLDUV is set to logic 1 when 5 labels that differ from its immediate predecessor are received. RPLDUV is set to logic 0 and the unstable label count is reset when 5 consecutive identical labels are received.

RPLDUI:

The receive payload type label unstable interrupt status bit (RPLDUI) is set to logic 1 when the stable/unstable status of the path signal label changes state. This bit (and the interrupt) is cleared when this register is read.

RPLDMIE:

The receive payload type label mismatch interrupt enable bit (RPLDMIE) controls the activation of the interrupt output when the comparison between received and the expected payload type label changes state from match to mismatch and vice versa. When RPLDMIE is set to logic 1, changes in match state activates the interrupt output. When RPLDMIE is set to logic 0, changes from match to mismatch or mismatch to match will not generate an interrupt.

RPLDUIE:

The receive payload type label unstable interrupt enable bit (RPLDUIE) controls the activation of the interrupt output when the received payload type label changes state from stable to unstable and vice versa. When RPLDUIE is set to logic 1, changes in stable state activates the interrupt output. When RPLDUIE is set to logic 0, changes in the stable state will not generate and interrupt.

1.35 Full Featured T1/E1 Pattern Generators and Receivers

Each of the six (N = 0 to 5) T1/E1 pattern generator and receiver pairs may be associated with a specific tributary via the T1/E1 PRGD Tributary Select registers (0x0042 to 0x0047.

The pattern receiver analyzes the data after the frame alignment block, but before the elastic store so it is not subject to frame slips.

The pattern generator inserts its data after the TPCC (thus overwrites signaling, DMW, trunk conditioning) and before the frame insertion.

1.36 T1/E1 Pattern Generator and Detector Registers

Register 0x0500 + 0x20*N: T1/E1 Pattern Generator and Detector Control

Bit	Type	Function	Default
Bit 7	R/W	PDR[1]	0
Bit 6	R/W	PDR[0]	0
Bit 5	R/W	QRSS	0
Bit 4	R/W	PS	0
Bit 3	R/W	TINV	0
Bit 2	R/W	RINV	0
Bit 1	R/W	AUTOSYNC	1
Bit 0	R/W	MANSYNC	0

PDR[1:0]:

The PDR[1:0] bits select the content of the four pattern detector registers to be any one of the pattern receive registers, the error count holding registers, or the bit count holding registers. The selection is shown in the following table:

PDR[1:0]	PDR#1	PDR#2	PDR#3	PDR#4
00, 01	Pattern Receive (LSB)	Pattern Receive	Pattern Receive	Pattern Receive (MSB)

10	Error Count (LSB)	Error Count	Error Count	Error Count (MSB)
11	Bit Count (LSB)	Bit Count	Bit Count	Bit Count (MSB)

QRSS:

The QRSS bit enables the zero suppression feature required when generating the QRSS sequence. When QRSS is a logic 1, a one is forced in the TDAT stream when the following 14 bit positions are all zeros. When QRSS is a logic 0, the zero suppression feature is disabled.

PS:

The PS bit selects the generated pattern. When PS is a logic 1, a repetitive pattern is generated. When PS is a logic 0, a pseudo-random pattern is generated. The PS bit should be set to 1 before the length, tap and pattern insertion registers are written to. If the PS logic value changes then the length, tap and pattern insertion registers must be reprogrammed.

TINV:

The TINV bit controls the logical inversion of the generated data stream. When TINV is a logic 1, the data is inverted. When TINV is a logic 0, the data is not inverted.

RINV:

The RINV bit controls the logical inversion of the receive data stream before processing. When RINV is a logic 1, the received data is inverted before being processed by the pattern detector. When RINV is a logic 0, the received data is not inverted.

AUTOSYNC:

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. The automatic resynchronization is activated when 6 or more bit errors are detected in the last 64 bit periods. When AUTOSYNC is a logic 1, the auto resync feature is enabled. When AUTOSYNC is a logic 0, the auto sync feature is disabled, and pattern resynchronization is accomplished using the MANSYNC bit.

MANSYNC:

The MANSYNC bit is used to initiate a manual resynchronization of the pattern detector. A low to high transition on MANSYNC initiates the resynchronization.

Register 0x0501 + 0x20*N: T1/E1 Pattern Generator and Detector Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	SYNCE	0
Bit 6	R/W	BEE	0
Bit 5	R/W	XFERE	0
Bit 4	R	SYNCV	X
Bit 3	R	SYNCI	X
Bit 2	R	BEI	X
Bit 1	R	XFERI	X
Bit 0	R	OVR	X

SYNCE:

The SYNCE bit enables the generation of an interrupt when the pattern detector changes synchronization state. When SYNCE is set to logic 1, the INTB output is asserted low if the SYNCI bit is logic 1.

BEE:

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. When BEE is set to logic 1, the INTB output is asserted low if the BEI bit is logic 1.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the receive pattern registers, the bit counter holding registers, and the error counter holding registers. When XFERE is set to logic 1, the INTB output is asserted low if the XFERI bit is logic 1.

SYNCV:

The SYNCV bit indicates the synchronization state of the pattern detector. When SYNCV is a logic 1 the pattern detector is synchronized (the pattern detector has observed at least 32 consecutive error free bit periods). When SYNCV is a logic 0, the pattern detector is out of sync (the pattern detector has detected 6 or more bit errors in a 64 bit period window).

SYNCI:

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic 1, the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic 0 when this register is read.

BEI:

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic 1, at least one bit error has been detected. BEI is set to logic 0 when this register is read.

XFERI:

The XFERI bit indicates that a transfer of pattern detector data has occurred. A logic 1 in this bit position indicates that the pattern receive registers, the bit counter holding registers and the error counter holding registers have been updated. This update is initiated by writing to one of the pattern detector register locations, or by writing a logic 1 to the E1T1_PRBS bit of the Global Performance Monitor Update register. XFERI is set to logic 0 when this register is read.

OVR:

The OVR bit is the overrun status of the pattern detector registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the pattern receive registers, the bit counter holding registers and the error counter holding registers have been overwritten. OVR is set to logic 0 when this register is read.

Register 0x0502 + 0x20*N: T1/E1 Pattern Generator and Detector Length

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PL[4]	0
Bit 3	R/W	PL[3]	0
Bit 2	R/W	PL[2]	0
Bit 1	R/W	PL[1]	0
Bit 0	R/W	PL[0]	0

PL[4:0]:

PL[4:0] determine the length of the generated pseudo random or repetitive pattern. The pattern length is equal to the value of PL[4:0] + 1.

Register 0x0503 + 0x20*N: T1/E1 Pattern Generator and Detector Tap

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PT[4]	0
Bit 3	R/W	PT[3]	0
Bit 2	R/W	PT[2]	0
Bit 1	R/W	PT[1]	0
Bit 0	R/W	PT[0]	0

PT[4:0]:

PT[4:0] determine the feedback tap position of the generated pseudo random pattern. The feedback tap position is equal to the value of PT[4:0] + 1.

Register 0x0504 + 0x20*N: T1/E1 Pattern Generator and Detector Error Insertion

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	EVENT	0
Bit 2	R/W	EIR[2]	0
Bit 1	R/W	EIR[1]	0
Bit 0	R/W	EIR[0]	0

EVENT:

A low to high transition on the EVENT bit causes a single bit error to be inserted in the generated pattern. This bit must be cleared and set again for a subsequent error to be inserted.

EIR[2:0]:

The EIR[2:0] bits control the insertion of a programmable bit error rate as indicated in the following table:

EIR[2:0]	Generated Bit Error Rate
000	No errors inserted
001	10^{-1}
010	10^{-2}
011	10^{-3}
100	10^{-4}
101	10^{-5}
110	10^{-6}

111	10^{-7}

Register 0x0508 + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Insertion #1

Bit	Type	Function	Default
Bit 7	R/W	PI[7]	0
Bit 6	R/W	PI[6]	0
Bit 5	R/W	PI[5]	0
Bit 4	R/W	PI[4]	0
Bit 3	R/W	PI[3]	0
Bit 2	R/W	PI[2]	0
Bit 1	R/W	PI[1]	0
Bit 0	R/W	PI[0]	0

Register 0x0509 + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Insertion #2

Bit	Type	Function	Default
Bit 7	R/W	PI[15]	0
Bit 6	R/W	PI[14]	0
Bit 5	R/W	PI[13]	0
Bit 4	R/W	PI[12]	0
Bit 3	R/W	PI[11]	0
Bit 2	R/W	PI[10]	0
Bit 1	R/W	PI[9]	0
Bit 0	R/W	PI[8]	0

Register 0x050A + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Insertion #3

Bit	Type	Function	Default
Bit 7	R/W	PI[23]	0
Bit 6	R/W	PI[22]	0

Bit	Type	Function	Default
Bit 5	R/W	PI[21]	0
Bit 4	R/W	PI[20]	0
Bit 3	R/W	PI[19]	0
Bit 2	R/W	PI[18]	0
Bit 1	R/W	PI[17]	0
Bit 0	R/W	PI[16]	0

Register 0x050B + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Insertion #4

Bit	Type	Function	Default
Bit 7	R/W	PI[31]	0
Bit 6	R/W	PI[30]	0
Bit 5	R/W	PI[29]	0
Bit 4	R/W	PI[28]	0
Bit 3	R/W	PI[27]	0
Bit 2	R/W	PI[26]	0
Bit 1	R/W	PI[25]	0
Bit 0	R/W	PI[24]	0

PI[31:0]:

PI[31:0] contain the data that is loaded in the pattern generator each time a new pattern (pseudo random or repetitive) is to be generated. When a pseudo random pattern is to be generated, PI[31:0] should be set to 0xFFFFFFFF. The data is loaded each time pattern insertion register #4 is written. Pattern insertion registers #1 - #3 should be loaded with the desired data before pattern register #4 is written. When a repetitive pattern is transmitted, PI[31], the MSB, contains the first bit transmitted, PI[0], the LSB, contains the last bit transmitted.

Note that the PI[31:0] value has no effect on the pattern detection. If a repetitive pattern is selected, the receiver will synchronize to any bit sequence that repeats with the programmed periodicity.

Register 0x050C + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Detector #1

Bit	Type	Function	Default
Bit 7	R	PD[7]	0
Bit 6	R	PD[6]	0
Bit 5	R	PD[5]	0
Bit 4	R	PD[4]	0
Bit 3	R	PD[3]	0
Bit 2	R	PD[2]	0
Bit 1	R	PD[1]	0
Bit 0	R	PD[0]	0

Register 0x050D + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Detector #2

Bit	Type	Function	Default
Bit 7	R	PD[15]	0
Bit 6	R	PD[14]	0
Bit 5	R	PD[13]	0
Bit 4	R	PD[12]	0
Bit 3	R	PD[11]	0
Bit 2	R	PD[10]	0
Bit 1	R	PD[9]	0
Bit 0	R	PD[8]	0

Register 0x050E + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Detector #3

Bit	Type	Function	Default
Bit 7	R	PD[23]	0
Bit 6	R	PD[22]	0

Bit	Type	Function	Default
Bit 5	R	PD[21]	0
Bit 4	R	PD[20]	0
Bit 3	R	PD[19]	0
Bit 2	R	PD[18]	0
Bit 1	R	PD[17]	0
Bit 0	R	PD[16]	0

Register 0x050F + 0x20*N: T1/E1 Pattern Generator and Detector Pattern Detector #4

Bit	Type	Function	Default
Bit 7	R	PD[31]	0
Bit 6	R	PD[30]	0
Bit 5	R	PD[29]	0
Bit 4	R	PD[28]	0
Bit 3	R	PD[27]	0
Bit 2	R	PD[26]	0
Bit 1	R	PD[25]	0
Bit 0	R	PD[24]	0

PD[31:0]:

PD[31:0] contain the pattern detector data. The values contained in these registers are determined by the PDR[1:0] bits in the PRGD Control register.

When PDR[1:0] is set to 00 or 01, PD[31:0] contain the pattern receive register. The 32 bits received immediately before the last accumulation interval are present on PD[31:0]. PD[31] contains the first of the 32 received bits, PD[0] contains the last of the 32 received bits.

When PDR[1:0] is set to 10, PD[31:0] contain the error counter holding register. The value in this register represents the number of bit errors that have been accumulated since the last accumulation interval. Note that bit errors are not accumulated while the pattern detector is out of sync.

When PDR[1:0] is set to 11, PD[31:0] contain the bit counter holding register. The value in this register represents the total number of bits that have been received since the last accumulation interval.

The PRGD Pattern Detect registers for a single tributary are updated by writing to any one of the associated Pattern Detect registers when the PDR[1:0] bits are 11. Alternatively, the Pattern Detect registers are updated globally with all other TEMUX 84 counter registers by writing to the Global Performance Monitor Update register (address 0x0007) with the E1T1_PRBS bit set to logic 1.

Registers 0x0510 + 0x20*N: Generator Controller Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

This register allows selection of the microprocessor read access type and output enable control for the Generator Controller.

<u>Reserved:</u>

The Reserved bit must be logic 0 for normal operation.

<u>IND:</u>

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the TEMUX 84 is reset, the IND bit is set low, disabling the indirect access mode.

<u>PCCE:</u>

The PCCE bit enables the generator when set to a logic 1. DS0s must also be enabled individually.

Registers 0x0511 + 0x20*N: Generator Controller µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

Registers 0x0512 + 0x20*N: Generator Controller Channel Indirect Address/Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A6	0
Bit 5	R/W	A5	0
Bit 4	R/W	A4	0
Bit 3	R/W	A3	0
Bit 2	R/W	A2	0
Bit 1	R/W	A1	0
Bit 0	R/W	A0	0

This register allows the µP to access the internal Generator Controller registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal Generator Controller register is requested; when R/WB is set to a logic 0, a write to the internal RPSC register is requested.

This register address is only valid when the IND bit of the associated Generator Controller Configuration register is logic 1.

Registers 0x0513 + 0x20*N: Generator Controller Channel Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D7	0
Bit 6	R/W	D6	0
Bit 5	R/W	D5	0
Bit 4	R/W	D4	0
Bit 3	R/W	D3	0
Bit 2	R/W	D2	0
Bit 1	R/W	D1	0
Bit 0	R/W	D0	0

This register contains either the data to be written into the internal Generator Controller registers when a write request is initiated or the data read from the internal Generator Controller registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The functions are allocated within the registers shown in Table 9:

Table 9 Generator Controller Indirect Register Map

Addr	Register
20H	DDS Control byte for Timeslot 0
21H	DDS Control byte for Channel 1/Timeslot 1
22H	DDS Control byte for Channel 2/Timeslot 2
.	.
.	.
37H	DDS Control byte for Channel 23/Timeslot 23
38H	DDS Control byte for Channel 24/Timeslot 24

Addr	Register
39H	DDS Control byte for Timeslot 25
.	.
.	.
3EH	DDS Control byte for Timeslot 30
3FH	DDS Control byte for Timeslot 31
40H	Bit Enable byte for Timeslot 0
41H	Bit Enable byte for Channel 1/Timeslot 1
42H	Bit Enable byte for Channel 2/Timeslot 2
. .	. .
57H	Bit Enable byte for Channel 23/Timeslot 23
58H	Bit Enable byte for Channel 24/Timeslot 24
59H	Bit Enable byte for Timeslot 25
. .	. .
5EH	Bit Enable byte for Timeslot 30
5FH	Bit Enable byte for Timeslot 31

The "Timeslot" designation refers to the E1 assignment. The "Channel" designation refers to the T1 assignment.

The bits within each control byte are allocated as follows:

Table 10 - Generator Controller Indirect Registers 0x20-0x3F: DDS Control byte

Bit	Type	Function	Default
Bit 7	R/W	Unused	X
Bit 6	R/W	Unused	X
Bit 5	R/W	Unused	X
Bit 4	R/W	SIXBITS	X

Bit	Type	Function	Default
Bit 3	R/W	DDS4	X
Bit 2	R/W	DDS3	X
Bit 1	R/W	DDS2	X
Bit 0	R/W	DDS1	X

SIXBITS:

When the SIXBITS bit is set to a logic 1, the DDS pattern is placed in the second through the seventh bit (with the first bit being the most significant, and the first bit transmitted, sequentially) of the DS0. When the SIXBITS bit is set to a logic 0, the DDS pattern is placed in the first through the seventh bit of the DS0.

DDS4:

When set to logic 1, 01000000 is continuously repeated in the first or second (depending on SIXBITS state) through the seventh bit of the DS0.

DDS3:

When set to logic 1, 00110010 is continuously repeated in the first or second (depending on SIXBITS state) through the seventh bit of the DS0.

This bit supercedes DDS4.

DDS2:

When set to logic 1, 100 octets of 01111110 followed by 100 octets of 00000000 are repeated in the first or second (depending on SIXBITS state) through the seventh bit of the DS0.

This bit supercedes DDS3 and DDS4.

DDS1:

When set to logic 1, 100 octets of 11111111 followed by 100 octets of 00000000 are repeated in the first or second (depending on SIXBITS state) through the seventh bit of the DS0.

This bit supercedes DDS2, DDS3 and DDS4.

Table 11 - Generator Controller Indirect Registers 0x40-0x5F: Bit Enable byte

Bit	Type	Function	Default
Bit 7	R/W	BE[7]	X
Bit 6	R/W	BE[6]	X
Bit 5	R/W	BE[5]	X
Bit 4	R/W	BE[4]	X
Bit 3	R/W	BE[3]	X
Bit 2	R/W	BE[2]	X
Bit 1	R/W	BE[1]	X
Bit 0	R/W	BE[0]	X

BE[7:0]:

These bits determine which individual bits are used by the Pattern Generator. If a BE bit is logic one, the corresponding bit in the T1/E1 tributary is expected to contain a bit in the sequencebeing analyzed.

These bits only control PRBS and fixed pattern insertion; the DDS codes occupy an entire DS0 regardless of the state of these bits.

BE[7] corresponds to the first bit transmitted. All channels/timeslots must be programmed before the PCCE bit is set to logic 1.

Registers 0x0514 + 0x20*N: Receiver Controller Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

This register allows selection of the microprocessor read access type and output enable control for the Receiver Controller.

Reserved:

The Reserved bit must be logic 0 for normal operation.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the TEMUX 84 is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the Pattern Receiver when set to a logic 1. DS0s must also be enabled individually.

Registers 0x0515 + 0x20*N: Receiver Controller µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

Registers 0x0516 + 0x20*N: Receiver Controller Channel Indirect Address/Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A6	0
Bit 5	R/W	A5	0
Bit 4	R/W	A4	0
Bit 3	R/W	A3	0
Bit 2	R/W	A2	0
Bit 1	R/W	A1	0
Bit 0	R/W	A0	0

This register allows the µP to access the internal Receiver Controller registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal Receiver Controller register is requested; when R/WB is set to a logic 0, an write to the internal Receiver Controller register is requested.

This register address is only valid when the IND bit of the associated Receiver Controller Configuration register is logic 1.

Registers 0x0517 + 0x20*N: Receiver Controller Channel Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D7	0
Bit 6	R/W	D6	0
Bit 5	R/W	D5	0
Bit 4	R/W	D4	0
Bit 3	R/W	D3	0
Bit 2	R/W	D2	0
Bit 1	R/W	D1	0
Bit 0	R/W	D0	0

This register contains either the data to be written into the internal Receiver Controller registers when a write request is initiated or the data read from the internal Receiver Controller registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The functions are allocated within the registers shown in Table 9:

Table 12 - Receiver Controller Indirect Register Map

Addr	Register
40H	Bit Enable byte for Timeslot 0
41H	Bit Enable byte for Channel 1/Timeslot 1
42H	Bit Enable byte for Channel 2/Timeslot 2
. . .	. . .
57H	Bit Enable byte for Channel 23/Timeslot 23
58H	Bit Enable byte for Channel 24/Timeslot 24

Addr	Register
59H	Bit Enable byte for Timeslot 25
. .	. .
5EH	Bit Enable byte for Timeslot 30
5FH	Bit Enable byte for Timeslot 31

The "Timeslot" designation refers to the E1 assignment. The "Channel" designation refers to the T1 assignment.

The bits within each control byte are allocated as follows:

Table 13 - Receiver Controller Indirect Registers 0x40-0x5F: Bit Enable byte

Bit	Type	Function	Default
Bit 7	R/W	BE[7]	X
Bit 6	R/W	BE[6]	X
Bit 5	R/W	BE[5]	X
Bit 4	R/W	BE[4]	X
Bit 3	R/W	BE[3]	X
Bit 2	R/W	BE[2]	X
Bit 1	R/W	BE[1]	X
Bit 0	R/W	BE[0]	X

BE[7:0]:

These bits determine whether individual bits are overwritten by the Pattern Receiver. If a BE bit is logic one, the corresponding bit in the T1/E1 tributary is replaced by a bit in the sequence generated by the Pattern Generator.

BE[7] corresponds to the first bit transmitted. All channels/timeslots must be programmed before the PCCE bit is set to logic 1.

1.37 SONET/SDH Mapper Master Configuration Registers

Register 0x0700: SONET/SDH Master Reset

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	VTMPRST[3]	0
Bit 5	R/W	VTMPRST[2]	0
Bit 4	R/W	VTMPRST[1]	0
Bit 3	R/W	DS3MPRST[3]	0
Bit 2	R/W	DS3MPRST[2]	0
Bit 1	R/W	DS3MPRST[1]	0
Bit 0	R/W	RESET	0

RESET:

The RESET bit allows software to hold the entire SONET/SDH mapper in a reset condition. When RESET is a logic 1 the SONET/SDH mapper will be held in a reset state which is also a low power state. This will force all registers to their default state with the exception of this register, which is not reset when this RESET bit is a logic 1. While in reset the clocks can not be guaranteed accurate or existing. When RESET is a logic 0 the SONET/SDH mapper is in normal operating mode. The SONET/SDH mapper is by default in the operational state. This register is only reset by the hardware device reset and not by this RESET register bit.

DS3MPRST[3:1]:

The DS3 mapper reset bits allow independent reset control over the DS3 mappers. The reset to the DS3 mapper blocks is the OR of this bit and the RESET bit in this register. This bit is useful for putting the DS3 mappers in a low power reset mode when the VT/TU mappers are being used. When DS3MPRST[n] is a logic 1, the DS3 mapper block associated with SPEn is held in reset. When DS3MPRST[n] is a logic 0, the DS3 mapper block associated with SPEn is in normal operating mode.

VTMPRST[3:1]:

The VT/TU mapper reset bits allow independent reset control over the VT/TU mapper blocks. The reset to the VT/TU mapper blocks is the OR of this bit and the RESET bit in this register. This bit is useful for putting the VT/TU mapper blocks in a low power reset mode when the DS3 mappers are being used. When VTMPRST[n] is a logic 1, the VT/TU mapper block associated with SPEn is held in reset. When VTMPRST[n] is a logic 0, the VT/TU mapper blocks associated with SPEn is in normal operating mode.

Reserved:

This bit is reserved and should be set to its default values.

Register 0x0701: SONET/SDH Master Ingress Configuration

Bit	Type	Function	Default
Bit 7	R/W	LDPE	0
Bit 6	R/W	ITMFEN	0
Bit 5	R/W	IVTPPBYP	0
Bit 4	R/W	ITSEN	0
Bit 3	R/W	INCLDPL	0
Bit 2	R/W	INCLDC1J1V1	0
Bit 1	R/W	LDOP	0
Bit 0	R/W	ICONCAT	0

This register configures the TEMUX 84 functionality that is related to the ingress SONET/SDH data stream.

ICONCAT:

When set to logic 1, the ICONCAT bit configures the telecom drop bus of the TEMUX 84 to operate in AU4 mode. When the ICONCAT bit is set to 0, the telecom drop bus operates in AU3 mode (or equivalently, STS-1 mode) and the LDC1J1V1 input is expected to mark every J1 byte of each SPE. When ICONCAT is set to 1, the telecom drop bus operates in AU4 mode and the LDC1J1V1 input is expected to mark the J1 of the VC4.
When ICONCAT is set to AU4 mode, the ingress VTPPs must be configured for TUG3 operation via the ITUG3 bit in the SONET/SDH Master Ingress VTPP Configuration register.

LDOP:

The LDOP bit controls the expected parity on the incoming parity signal LDDP. When LDOP is set to logic 1, the parity of the parity signal set, together with LDDP is expected to be odd. When LDOP is set to logic 0, the expected parity is even. Membership of the parity signal set always includes LDDATA[7:0], and may include input signals LDC1J1V1 and LDPL as controlled by the INCLDC1J1V1 and INCLDPL bits, respectively.

INCLDC1J1V1:

The INCLDC1J1V1 bit controls whether the LDC1J1V1 input signal participates in the incoming parity calculations. When INCLDC1J1V1 is set to

logic 1, the parity signal set includes the LDC1J1V1 input. When INCLDC1J1V1 is set to logic 0, parity is calculated without regard to the state of LDC1J1V1. Selection of odd or even parity is controlled by the LDOP bit.

If 77.76MHz operation is selected (i.e. L77 is high), INCLDC1J1V1 may only be set to logic 1 if the LSTM[1:0] register bits are binary 00.

INCLDPL:

The INCLDPL bit controls the whether the LDPL input signal participates in the incoming parity calculations. When INCLDPL is set to logic 1, the parity signal set includes the LDPL input. When INCLDPL is set to logic 0, parity is calculated without regard to the state of LDPL. Selection of odd or even parity is controlled by the LDOP bit.

ITSEN:

The Ingress Time Switch Enable register bit, ITSEN, controls the time switch function in the RTDM blocks. When ITSEN is a logic 0, the RTDMs are not enabled to perform switching of the tributaries and all tributaries are fixed in a one-to-one mapping from an STM-1 AU4 or STS-3. When ITSEN is a logic 1, the RTDM is enabled to cross-connect the tributaries.

IVTPPBYP:

The Ingress VTPP bypass select bit, IVTPPBYP, configures the Line Side Telecom Drop bus to bypass the ingress VTPP and go directly into the RTDM and byte synchronous demapper. This is possible only when the Line Side Telecom Drop bus is processed outside the TEMUX 84, such as when connecting through an external TUPP-PLUS. When IVTPPBYP is a logic 1, the ingress VTPPs will be bypassed. The data on the telecom bus must be preprocessed such that the J1 octet is in a fixed location and the LDV5, LDPL and LDTPL signals are valid. If byte synchronous demapping is active, the J1 position must correspond to a pointer of 522. When IVTPPBYP is a logic 0, the ingress VTPPs will perform pointer processing on a single STS-1 SPE, STM-1 VC3 or STM-1 TUG-3. When using the ingress VTPP the Line Side Telecom Drop bus has no restrictions on any pointer alignments. When the ingress VTPP is bypassed, the RTOP is also bypassed. When the Ingress VTPP is bypassed, the OTUG3 bit in the SONET/SDH Master Ingress VTPP Configuration register must match the external telecom bus interface.

ITMFEN:

When set to logic 1, the ITMFEN bit enables the TEMUX 84 to use the V1 pulse indications of the LDC1J1V1 to locate the V1 bytes, and hence the

tributary multiframe boundaries. If ITMFEN=1, an external tributary pointer processor, such as the TUPP-PLUS, must provide valid V1 indications on LDC1J1V1.. When ITMFEN is set to 1 the H4 bytes in the incoming data stream are ignored by the VTPP. When ITMFEN is set to 0, the ingress VTPP processes the H4 bytes to locate the multiframe boundaries and the V1 indication is ignored.

LDPE:

The LDPE bit is an active high interrupt enable. When LDPE is set to logic 1, the occurrence of a parity error on the Line Side Drop Telecom bus parity signal set (as indicated by the LDPINT bit of the Master Interrupt Source SDH #1 register) will cause an interrupt to be asserted on the interrupt (INTB) output and the SDHINT bit of the Master Interrupt Source register to be logic 1. When LDPE is set to logic 0, incoming parity errors will not cause an interrupt.

Register 0x0702: SONET/SDH Master Egress Configuration

Bit	Type	Function	Default
Bit 7	R/W	LATOHEN	0
Bit 6	R/W	ETSEN	0
Bit 5	R/W	LAJ1EN	0
Bit 4	R/W	LAV1EN	0
Bit 3	R/W	INCLAPL	0
Bit 2	R/W	INCLAC1J1V1	0
Bit 1	R/W	LAOP	0
Bit 0	R/W	ECONCAT	0

This register configures the TEMUX 84 functionality that are related to the egress data stream.

ECONCAT:

When set to logic 1, the ECONCAT bit configures the telecom add bus of the TEMUX 84 to operate in AU4 mode. When the ECONCAT bit is set to 0, the telecom add bus operates in AU3 mode (or equivalently, STS-1 mode) and the LAC1J1V1 output marks every J1 byte of each SPE. When ECONCAT is set to 1, the telecom add bus operates in AU4 mode and the LAC1J1V1 output is marks the J1 of the VC4. The TEMUX 84 stretches J1 to provide a J1 for TUG3 #1, 2 and 3.
When ECONCAT is set to AU4 mode the egress VTPP must be configured for TUG3 operation via the OTUG3 bit in the SONET/SDH Master Egress VTPP Configuration register.

LAOP:

The LAOP bit controls the parity placed on the egress parity signal LADP. When LAOP is set to logic 0, the parity of outgoing data stream LADATA[7:0], together with LADP is even. When LAOP is set to logic 1, the parity is odd.

INCLAC1J1V1:

The INCLAC1J1V1 bit controls whether the LAC1J1V1 signal participates in the egress parity calculations. When INCLAC1J1V1 is set to logic 1, the parity signal set includes the LAC1J1V1 output. When INCLAC1J1V1 is set

to logic 0, parity is calculated without regard to the state of LAC1J1V1. Selection of odd or even parity is controlled by the LAOP bit.

INCLAPL:

The INCLAPL bit controls the whether the LAPL signal participates in the egress parity calculations. When INCLAPL is set to logic 1, the parity signal set includes the LAPL output. When INCLAPL is set to logic 0, parity is calculated without regard to the state of LAPL. Selection of odd or even parity is controlled by the LAOP bit.

LAV1EN:

The Line Side Telecom Add bus V1 enable bit, LAV1EN, controls the identification of the third byte after J1. When LAV1EN is set to logic 0, the LAC1J1V1 output only indicates the C1 and optionally J1 bytes. The third byte after J1 is not indicated. When LAV1EN is set to logic 1, the LAC1J1V1 output indicates the C1, optionally J1 and the third byte after J1 every fourth frame. If the LADDOE bit of the Bus Configuration register is logic 0, the Telecom Add bus is high-impedance during the V1 byte position if this bit is logic 0.

LAJ1EN:

The Line Side Telecom Add bus J1 enable bit, LAJ1EN, controls the identification of the J1 byte in addition to the C1 byte. When LAJ1EN is set to logic 0, the LAC1J1V1 output only indicates the C1 byte and optionally the third byte after the J1 if LAV1EN is set to logic 1. When LAJ1EN is set to logic 1, the LAC1J1V1 output indicates the C1, J1 and optionally the third byte after J1. If the LADDOE bit of the Bus Configuration register is logic 0, the Telecom Add bus is high-impedance during the J1 byte position if this bit is logic 0.

ETSEN:

The Egress Time Switch Enable register bit, ETSEN, overrides the time switch function in the TTMP block. When ETSEN is a logic 0 the TTMP is not enabled to perform switching of the tributaries and all tributaries are fixed in a one-to-one mapping from a single STS-1 SPE, STM-1 VC3 or STM-1 TUG-3. When ETSEN is a logic 1 the TTMP is enabled to cross-connect the tributaries.

LATOHEN

The Line Side Telecom Add bus Transport Overhead Enable register bit, LATOHEN, controls whether the Line Add bus is driven during the transport

overhead of the SONET frame. When LATOHEN is set to 1, the Line Side Telecom Add bus signals, LADP, LAPL, LADATA, and LAV5, are all driven during the transport overhead. For 77.76 MHz Telecombus operation, the same Line Add bus signals are all driven during the transport overhead for the configured STM-1 (as per the LSTM[1:0] bits in the Bus Configuration register 0x0006). When LATOHEN is logic 0, the Line Add bus signals are held in tristate during the transport overhead (the LADDOE bit, when asserted, has precedence over this bit).

Register 0x0703: SONET/SDH Master Ingress VTPP Configuration

Bit	Type	Function	Default
Bit 7	R/W	IN_MINDELAY	0
Bit 6	R/W	SOS	0
Bit 5	R/W	MONIS	0
Bit 4	R/W	ICODE	0
Bit 3	R/W	NOFILT	0
Bit 2		Unused	X
Bit 1	R/W	ITUG3	0
Bit 0	R/W	OTUG3	0

This register is used to enable the processing of a STS-1 (TUG3) and configure the major operational modes of the ingress VTPP.

OTUG3:

When set to logic 1, the OTUG3 bit configures the ingress tributary payload processor, ingress VTPP, to process TUG2s that have been mapped into a TUG3 in the outgoing data stream connecting to the internal SONET/SDH blocks. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1. When passing transparent VTs between the line side Telecom bus and the system side SBI bus, OTUG3 must be configured for TUG2s mapped into a TUG3 by setting this bit high. When the ingress VTPP is bypassed this bit must be set to match the format of the external telecom drop bus.

When byte synchronous demapping is being performed, the OTUG3 bit must be set to logic 1.

ITUG3:

When set to logic 1, the ITUG3 bit configures the ingress tributary payload processor to process TUG2s that have been mapped into a TUG3 in the incoming data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1. When processing a TUG3 the ICONCAT bit must also be set to logic 1. . When the ingress VTPP is not

bypassed this bit must be set to match the format of the external telecom drop bus.

NOFILT:

The NOFILT bit controls the processing of incoming tributary pointers. When a logic 0 is written to this location, illegal variations from normal tributary pointer value (i.e. changes which do not correspond to pointer justification events, and are not accompanied by a new data flag) are ignored unless a consistent new value is received three times consecutively. When a logic 1 is written to this location, variations take effect immediately and are passed through the payload buffer unfiltered.

ICODE:

The ICODE bit controls the value inserted into tributary bytes when idle insertion is enabled. When a logic 0 is written to this location, the idle code is chosen to be all zeros. Setting ICODE to 1 sets the idle code to all ones. Idle insertion only affects the tributary payload bytes which are overwritten with the selected idle pattern. The outgoing pointer remains a function of the incoming pointer and the relative multiframe alignment of the incoming and outgoing streams. ICODE has no effect on pointer processing.

MONIS:

The MONIS bit controls the source of pointer justification interrupts. When MONIS is set to logic 1, the incoming stream is monitored for tributary pointer justification events. When MONIS is set to logic 0, the outgoing stream is monitored for pointer justification events. Interrupts can be optionally generated upon a pointer justification event in the monitored stream.

SOS:

The SOS bit controls the spacing between consecutive pointer justification events on the incoming stream. When SOS is set to logic 1, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred at least three frames ago. When SOS is set to logic 0, pointer justification indications in the incoming stream are followed without regard to the proximity of previous active offset change. It is recommended to set this bit to 1 for all VT/TU mapping modes where the IVTPP is not bypassed

IN_MINDELAY:

Setting this bit to logic 1 minimizes the latency through the ingress VTPP. It is recommended this bit be set to logic 1. Provided LREFCLK is within

specification and the tributaries are within network specifications, no adverse side effects will be observed.

Register 0x0704: SONET/SDH Master Egress VTPP Configuration

Bit	Type	Function	Default
Bit 7	R/W	EG_MINDELAY	0
Bit 6	R/W	LATPLSEL	0
Bit 5	R/W	EVTPPBYP	0
Bit 4	R/W	EPTRBYP[3]	0
Bit 3	R/W	EPTRBYP[2]	0
Bit 2	R/W	EPTRBYP[1]	0
Bit 1	R/W	ITUG3	0
Bit 0	R/W	OTUG3	0

This register configures additional TEMUX 84 functionality that are related to the egress data stream.

OTUG3:

When set to logic 1, the OTUG3 bit configures the egress tributary payload processor, egress VTPP, to process TUG2s that have been mapped into a TUG3 in the outgoing data stream on the telecom add bus. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1. When the egress VTPP is not bypassed this bit must be set to match the format of the external telecom add bus.

ITUG3:

When set to logic 1, the ITUG3 bit configures the egress tributary payload processor to process TUG2s that have been mapped into a TUG3 in the incoming data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1. When passing transparent VTs between the system side SBI bus and the line side Telecom bus, ITUG3 must be configured for TUG2s mapped into a TUG3 by setting this bit high. When the egress VTPP is bypassed this bit must be set to match the format of the external telecom add bus.

When byte synchronous mapping is being performed, the ITUG3 bit must be set to logic 1.

EPTRBYP[3:1]:

When set to logic 1, the EPTRBYP[n] bit configures the egress VTPP associated with SPEn to bypass pointer interpretation for all transparent and byte synchronously mapped virtual tributaries. Pointer interpretation bypass is necessary for transparent VTs which do not have valid V1,V2 pointers and for byte synchronously mapped VTs. Two types of transparent VTs are possible, those without pointers but with V5 indications and those with pointers and no V5 indications. When EPTRBYP is logic 0, the transparent VTs entering the egress VTPP must have valid pointers. When EPTRBYP is logic 1, the transparent VTs entering the egress VTPP does not need valid pointers but must have a valid V5 indication. In either pointer bypass configuration, tributaries from the TTMP tributary bit asynchronous mapper will be able to pass through the VTPP.

The pointer interpretation may be disabled on a per-tributary basis via the ETVTPTRDIS bit of the TTMP Tributary Control registers. This control is necessary if transparent VTs and byte synchronously mapped VTs are to coexist within one SPE.

EVTPPBYP:

The egress VTPP bypass select bit, EVTPPBYP, configures the TEMUX 84 to bypass the egress VTPP and connect directly to the Line Side Telecom Add bus. When EVTPPBYP is a logic 1 the egress VTPP will be bypassed. When bypassing the egress VTPP, the Line Side Telecom Add bus must be able to accept a J1 at a pointer offset of either 0 or 522. When EVTPPBYP is a logic 0 the egress VTPP will perform pointer processing on a single STS-1 SPE, STM-1 VC3 or STM-1 TUG-3. When using the egress VTPP the Line Side Telecom Add bus has no restrictions on any pointer alignments. When the egress VTPP is bypassed the ITUG3 bit in this register must be set to match the format of the external telecom add bus.

Note that the V1 and V2 bytes do not contain a valid tributary pointer for byte synchronous mapped tributaries when EVTPPBYP is logic 0. The LAV5 output must be used in lieu of pointers.

LATPLSEL:

This bit determines the function of the LAOE/LATPL output. When LATPLSEL bit is logic 1, the output is defined as LATPL. When LATPLSEL bit is logic 0, the output is defined as LAOE.

LATPLSEL should only be set to logic 1 when EVTPPBYP is logic 1.

EG_MINDELAY:

Setting this bit to logic 1 minimizes the latency through the egress VTPP. It is recommended this bit be set to logic 1. Provided LREFCLK is within specification and the tributaries are within network specifications, no adverse side effects will be observed.

Register 0x0705: SONET/SDH Master RTOP Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	RDI10	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	1

This register configures the operation of RTOP.

Reserved:

These bits are reserved and should be set to their default values.

RDI10:

The RDI10 bit controls the number of times the tributary path RDI, RFI or the extended RDI code is filtered before being accepted. When RDI10 is set to logic 1, the RDI bit, the RFI bit or the extended RDI code is filtered for ten occurrences. When RDI10 is set to logic 0, the RDI bit, the RFI bit or the extended RDI code is filtered for five occurrences.

Register 0x0706: SONET/SDH Master Tributary Alarm AIS Control

Bit	Type	Function	Default
Bit 7	R/W	LOMAIS	0
Bit 6	R/W	LOPAIS	0
Bit 5		Unused	X
Bit 4	R/W	UNEQAIS	0
Bit 3	R/W	PSLMAIS	0
Bit 2	R/W	PSLUAIS	0
Bit 1		Unused	X
Bit 0	R/W	EGRALMEN	0

This register controls the insertion of ingress tributary path AIS as a result of tributary path signal label alarms and tributary multiframe alarms. It also controls the insertion of egress tributary alarms as a result of SBI bus alarm indications.

EGRALMEN:

The EGRALMEN bit enables an egress SBI alarm indication signal to force AIS generation into the egress tributary. When EGRALMEN is a logic 1 and the SBI bus is selected, an alarm indication from the SBI bus will force the egress data stream to an all ones AIS alarm. The EGRALMEN only has effect on tributaries whose PROV bit has been set via the TTMP Tributary Control register. When EGRALMEN is a logic 0, AIS alarm generation in the egress direction will not be generated due to a SBI alarm indication. This EGRALMEN bit has priority over the EALMEN bit in the T1/E1 Master Configuration register. While the EALMEN bit can only force all ones AIS into the data stream, EGRALMEN also enables the TTOP block to handle the state associated with going in and out of AIS and the New Data Flag in the V1 byte.

PSLUAIS:

The PSLUAIS bit is an active high AIS insertion enable. When PSLUAIS is set to logic 1, AIS is automatically generated on the ingress data stream for all tributaries that are in path signal label unstable state. When PSLUAIS is set to logic 0, the generation of AIS on the ingress data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

This bit only has effect on a tributary if the TUPTE bit of the corresponding RTOP Configuration and Alarm Status register is logic 1.

PSLMAIS:

The PSLMAIS bit is an active high AIS insertion enable. When PSLMAIS is set to logic 1, AIS is automatically generated on the ingress data stream for all tributaries that are in path signal label mismatch state. When PSLMAIS is set to logic 0, the generation of AIS on the ingress data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries. Note that the generation of AIS is inhibited in the unequipped state (i.e. when UNEQ is “active”), regardless of the PSLM state.

This bit only has effect on a tributary if the TUPTE bit of the corresponding RTOP Configuration and Alarm Status register is logic 1.

UNEQAIS:

The UNEQAIS bit is an active high AIS insertion enable. When UNEQAIS is set to logic 1, AIS is automatically generated on the outgoing data stream for all tributaries that are unequipped. The only exception is when the provisioned expected path signal label is unequipped (000)". When UNEQAIS is set to logic 0, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

This bit only has effect on a tributary if the TUPTE bit of the corresponding RTOP Configuration and Alarm Status register is logic 1.

LOPAIS:

The LOPAIS bit is an active high AIS insertion enable. When LOPAIS is set to logic 1, AIS is automatically generated on the ingress data stream for all tributaries that are in loss of pointer state. When LOPAIS is set to logic 0, the generation of AIS on the ingress data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

LOMAIS:

The LOMAIS bit is an active high AIS insertion enable. When LOMAIS is set to logic 1, AIS is automatically generated on the ingress data stream for all tributaries that are in loss of tributary multiframe state. (Loss of multiframe is declared when for 9 consecutive H4 bytes, there are no 4 consecutive H4 bytes that follow in the correct sequence. Loss of multiframe is removed when multiframe boundary is re-acquired after receiving four consecutive H4

bytes following in the correct sequence.) When LOMAIS is set to logic 0, the generation of AIS on the ingress data stream is inhibited.

Register 0x0707: SONET/SDH Master Tributary Remote Defect Indication Control

Bit	Type	Function	Default
Bit 7	R/W	LOMRDI	0
Bit 6	R/W	LOPRDI	0
Bit 5	R/W	AISRDI	0
Bit 4	R/W	UNEQRDI	0
Bit 3	R/W	PSLMRDI	0
Bit 2	R/W	PSLURDI	0
Bit 1		Unused	X
Bit 0		Unused	X

This register controls the insertion into the Telecom Add bus of tributary RDI-V as a result of tributary pointer alarms, tributary path signal label alarms and tributary multiframe alarms. An enabled alarm will result in the setting of bit 8 of the V5 byte and, if extended RDI is enabled, also bit 5 of Z7. The Egress AIS registers in the TRAP module must be set correctly, in addition to setting this register, for RDI-V insertion.

PSLURDI:

The PSLURDI bit is an active high RDI insertion enable. When PSLURDI is set to logic 1, RDI is reported to TRAP and optionally in the V5 byte of the ingress data stream for all tributaries that are in path signal label unstable state. When PSLURDI is set to logic 0, reporting of RDI due to PSLU is inhibited.

PSLMRDI:

The PSLMRDI bit is an active high RDI insertion enable. When PSLMRDI is set to logic 1, RDI is reported to TRAP and optionally in the V5 byte of the ingress data stream for all tributaries that are in path signal label mismatch state. The only exception is when the provisioned expected path signal label is “Equipped – Nonspecific Payload” (001), in which case the RDI is suppressed. When PSLMRDI is set to logic 0, reporting of RDI due to PSLM is inhibited.

UNEQRDI:

The UNEQRDI bit is an active high RDI insertion enable. When UNEQRDI is set to logic 1, RDI is reported to TRAP and optionally in the V5 byte of the ingress data stream for all tributaries that are in unequipped state. The only exception is when the provisioned expected path signal label is unequipped (000). When UNEQRDI is set to logic 0, reporting of RDI due to UNEQ is inhibited.

AISRDI:

The AISRDI bit is an active high RDI insertion enable. When AISRDI is set to logic 1, RDI is reported to TRAP and optionally the V5 byte of the outgoing data stream for all tributaries that are in incoming AIS state. When AISRDI is set to logic 0, reporting of RDI due to AIS is inhibited.

LOPRDI:

The LOPRDI bit is an active high RDI insertion enable. When LOPRDI is set to logic 1, RDI is reported to TRAP and optionally the V5 byte of the outgoing data stream for all tributaries that are in loss of pointer state. When LOPRDI is set to logic 0, reporting of RDI due to LOP is inhibited.

LOMRDI:

The LOMRDI bit is an active high RDI insertion enable. When LOMRDI is set to logic 1, RDI is reported to TRAP and optionally in the V5 byte of the outgoing data stream for all tributaries that are in loss of multiframe state. When LOMRDI is set to logic 0, reporting of RDI due to LOM is inhibited.

Register 0x0708: SONET/SDH Master Tributary Auxiliary Remote Defect Indication Control

Bit	Type	Function	Default
Bit 7	R/W	NOLOMARDI	1
Bit 6	R/W	NOLOPARDI	1
Bit 5	R/W	NOAISARDI	1
Bit 4	R/W	UNEQARDI	0
Bit 3	R/W	PSLMARDI	0
Bit 2	R/W	PSLUARDI	0
Bit 1		Unused	X
Bit 0		Unused	X

This register controls the insertion into the Telecom Add bus of one bit of ERDI-V (bit 6 of Z7) if extended RDI is configured as a result of tributary pointer alarms, tributary path signal label alarms and tributary multiframe alarms. The Egress AIS registers in the TRAP module must be set correctly, in addition to setting this register, for RDI-V or ARDI-V insertion.

PSLUARDI:

The PSLUARDI bit is an active high auxiliary RDI insertion enable. When PSLUARDI is set to logic 1, ARDI is reported to TRAP for all tributaries that are in path signal label unstable state. When PSLUARDI is set to logic 0, reporting of auxiliary RDI due to PSLU is inhibited.

PSLMARDI:

The PSLMARDI bit is an active high auxiliary RDI insertion enable. When PSLMARDI is set to logic 1, ARDI is reported to TRAP for all tributaries that are in path signal label mismatch state. When PSLMARDI is set to logic 0, reporting of auxiliary RDI due to PSLM is inhibited. PSLMARDI only has effect if the ERDI bit of the TRAP Control register is logic 1.

UNEQARDI:

The UNEQARDI bit is an active high auxiliary RDI insertion enable. When UNEQARDI is set to logic 1, ARDI is reported to TRAP for all tributaries that are in unequipped state. When UNEQARDI is set to logic 0, the reporting of auxiliary RDI for unequipped tributaries is inhibited.

NOLOPARDI:

The NOLOPARDI bit is an active high auxiliary RDI insertion disable. When NOLOPARDI is set to logic 1, ARDI is not reported to TRAP for all tributaries that are in loss of pointer state. NOLOPARDI has precedence over UNEQARDI, PSLUARDI and PSLMARDI. When NOLOPARDI is set to logic 0, reporting of RDI is according to UNEQARDI, PSLUARDI and PSLMARDI and the associated alarm states.

NOAISARDI:

The NOAISARDI bit is an active high auxiliary RDI insertion disable. When NOAISARDI is set to logic 1, auxiliary RDI is not reported to TRAP for all tributaries that are in incoming AIS state. NOAISARDI has precedence over UNEQARDI, PSLUARDI and PSLMARDI. When NOAISARDI is set to logic 0, reporting of RDI is according to UNEQARDI, PSLUARDI and PSLMARDI and the associated alarm states.

NOLOMARDI:

The NOLOMARDI bit is an active high auxiliary RDI insertion disable. When NOLOMARDI is set to logic 1, ARDI is not reported to TRAP for all tributaries that are in loss of multiframe state. When NOLOMARDI is set to logic 0, reporting of RDI is according to UNEQARDI, PSLUARDI and PSLMARDI and the associated alarm states.

Register 0x0709: SONET/SDH Master DS3/E3 Clock Generation Control

Bit	Type	Function	Default
Bit 7	R/W	FASTCLKFREQ	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	SC1FPEN	0

FASTCLKFREQ:

The Fast Clock Frequency select bit indicates the frequency of the CLK52M reference clock connected to the TEMUX 84 DS3 mappers and DS3/E3 clock synthesizers. When FASTCLKFREQ is set to logic 1 the CLK52M reference clock is selected to be 51.84MHz. When FASTCLKFREQ is set to logic 0 the CLK52M reference clock is selected to be 44.928MHz.

If the E3 data rate is being supported, FASTCLKFREQ must be logic 1 and CLK52M must be 51.84MHz.

SC1FPEN:

The SC1FP enable bit controls whether the internal VT/TU mapper blocks use the SBI bus SAC1FP and SDC1FP frame pulses for synchronization or the line side telecom bus LAC1 and LDC1J1V1 signals for frame synchronization. When SC1FPEN is '0', SAC1FP and SDC1FP are not used by the VT/TU mapper. When SC1FPEN is '1', SAC1FP and SDC1FP are used by the VT/TU mapper blocks and SREFCLK must be the same as LREFCLK.

Normally the VT/TU blocks are synchronized to the telecom bus frame signals but when Transparent VT's are enabled between the SBI bus and the line side telecom bus, SREFCLK must be the same as LREFCLK and SC1FPEN should be set to “1” . This is required so that the VT/TU mapped tributaries align with the SBI bus transparent VTs.

When transparent VTs are enabled, there is no assumed relationship between

LDC1J1V1, SDC1FP, LAC1 and SAC1FP. In this case SC1FPEN must be set to “1”, the VTPPs will align the SAC1FP and SDC1FP frame alignment with LAC1 and LDC1J1V1 frame alignment.

Register 0x070A: SONET/SDH Master Loopback Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	DLOOP	0
Bit 0	R/W	LLOOP	0

LLOOP:

The LLOOP bit puts the Telecom Bus interface into Line Loopback mode. When LLOOP is a logic 1 the entire ingress STM-1/STS-3 will be looped back out the egress telecom bus. When LLOOP is a logic 0, no line loopback will be preformed.

DLOOP:

The DLOOP bit enables a diagnostic loopback at the telecom bus interface. When DLOOP is a logic 1 then entire egress STS-3 or STM-1 is looped back to the ingress data path. When DLOOP is a logic 0, no diagnostic loopback will be performed.

If performing byte synchronous mapping, the transmit pointer programmed via the SONET/SDH Transmit Pointer Configuration registers must be decimal 522 if DLOOP is logic 1 and EVTPPBYP is logic 0. Also, the OTUG3 bit of the SONET/SDH Master Egress VTPP Configuration register must be logic 1 if byte synchronously mapped tributaries are being looped back.

This bit only has effect on SPEs that are carrying VT1.5/TU11 or VT2/TU12 tributaries. DS3 payloads cannot be looped back.

Reserved:

This bit should be set to a logic 0 for correct operation of the TEMUX 84.

Register 0x070B: SONET/SDH Telecom Bus Signal Monitor, Accumulation Trigger

Bit	Type	Function	Default
Bit 7	R	RADWESTA	X
Bit 6	R	RADEASTA	X
Bit 5	R	LAC1A	X
Bit 4	R	LDDA	X
Bit 3	R	LDV5A	X
Bit 2	R	LDTPLA	X
Bit 1	R	LDPLA	X
Bit 0	R	LDC1J1V1A	X

When a monitored Telecom Bus signal makes a low to high transition, the corresponding register bit is set to logic 1. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

Writing to this register delimits the accumulation intervals in the RTOP accumulation registers. Counts accumulated in those registers are transferred to holding registers where they can be read. The counters themselves are then cleared to begin accumulating events for a new accumulation interval. To prevent loss of data, accumulation intervals must be 0.5 second or shorter. The bits in this register are not affected by write accesses.

LDC1J1V1A:

The LDC1J1V1 active, LDC1J1V1A, bit monitors for low to high transitions on the LDC1J1V1 input. LDC1J1V1A is set to logic 1 on a rising edge of LDC1J1V1, and is set to logic 0 when this register is read.

LDPLA:

The LDPL active, LDPLA, bit monitors for low to high transitions on the LDPL input. LDPLA is set to logic 1 on a rising edge of LDPL, and is set to logic 0 when this register is read.

LDTPLA:

The LDTPL active, LDTPLA, bit monitors for low to high transitions on the LDTPL input. LDTPLA is set to logic 1 on a rising edge of LDTPL, and is set to logic 0 when this register is read.

LDV5A:

The LDV5 active, LDV5A, bit monitors for low to high transitions on the LDV5 input. LDV5A is set to logic 1 on a rising edge of LDV5, and is set to logic 0 when this register is read.

LDDA:

The LDDATA bus active, LDDA, bit monitors for low to high transitions on the LDDATA[7:0] bus. LDDA is set to logic 1 when a rising edge has been observed on each signal on the LDDATA [7:0] bus with no interveaning reads of this regiater. LDDA is set to logic 0 when this register is read.

LAC1A:

The LAC1 active, LAC1A, bit monitors for low to high transitions on the LAC1 input. LAC1A is set to logic 1 on a rising edge of LAC1, and is set to logic 0 when this register is read.

RADEASTA:

The RADEASTCK active, RADEASTA, bit detects low to high transitions on the RADEASTCK input. RADEASTA is set to logic 1 on a rising edge of RADEASTCK, and is set to logic 0 when this register is read.

RADWESTA:

The RADWESTCK active, RADWESTA, bit detects low to high transitions on the RADWESTCK input. RADWESTA is set to logic 1 on a rising edge of RADWESTCK, and is set to logic 0 when this register is read.

Register 0x070C: SONET/SDH Transmit Pointer Configuration #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	TXPTR[9]	1
Bit 0	R/W	TXPTR[8]	0

Register 0x070D: SONET/SDH Transmit Pointer Configuration #2

Bit	Type	Function	Default
Bit 7	R/W	TXPTR[7]	0
Bit 6	R/W	TXPTR[6]	0
Bit 5	R/W	TXPTR[5]	0
Bit 4	R/W	TXPTR[4]	0
Bit 3	R/W	TXPTR[3]	1
Bit 2	R/W	TXPTR[2]	0
Bit 1	R/W	TXPTR[1]	1
Bit 0	R/W	TXPTR[0]	0

TXPTR[9:0]:

The transmit pointer (TXPTR[9:0]) controls the SPE payload offset of the line side Telecom Add bus. The value encodes the J1 byte position relative to the H3 bytes. A value of 0 positions the J1 byte in the egress data stream to the byte immediately following the H3 bytes. The default value of 522 decimal positions the J1 byte in the egress data stream to the byte immediately following the C1 bytes.

When the egress VTPP is bypassed, the TXPTR[9:0] value must match the

LOCK0 bit in the TTMP Telecom Interface Configuration register. When LOCK0 is logic 0, TXPTR[9:0] must be decimal 522. When LOCK0 is logic 1, TXPTR[9:0] must be decimal 0.

Register 0x073C: DLL Configuration (TelecomBus)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The DLL Configuration Register controls the basic operation of the DLL.

ERRORE:

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, the INTB output is asserted low upon assertion of the ERROR bit in the DLL Control Status register. When ERRORE is set low, changes in the ERROR bit does not generate an interrupt.

Reserved:

The reserved bits must be set low for correct operation.

Register 0x073E: DLL Delay Tap Status (TelecomBus)

Bit	Type	Function	Default
Bit 7	R	TAP[7]	X
Bit 6	R	TAP[6]	X
Bit 5	R	TAP[5]	X
Bit 4	R	TAP[4]	X
Bit 3	R	TAP[3]	X
Bit 2	R	TAP[2]	X
Bit 1	R	TAP[1]	X
Bit 0	R	TAP[0]	X

The DLL Delay Tap Status Register indicates the delay tap used by the DLL to generate the outgoing clock.

Writing to this register performs a software reset of the DLL. A software reset requires a maximum of 24*256 LREFCLK cycles for the DLL to regain lock. During this time the TelecomBus output propagation delays may vary.

TAP[7:0]:

The tap status register bits (TAP[7:0]) specifies the delay line tap the DLL is using to generate its outgoing clock. .
When TAP[7:0] is logic zero, the DLL is using the delay line tap with minimum phase delay. When TAP[7:0] is equal to 255, the DLL is using the delay line tap with maximum phase delay.

Register 0x073F: DLL Control Status (TelecomBus)

Bit	Type	Function	Default
Bit 7	R	LREFCLKI	X
Bit 6	R	DLLCLKI	X
Bit 5	R	ERRORI	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1		Unused	X
Bit 0	R	RUN	X

The DLL Control Status Register provides information of the DLL operation.

RUN:

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the variable delay clock and the rising edge of LREFCLK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.
The RUN register bit is cleared only by a hardware or a software reset.

ERROR:

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. ERROR is set low when the DLL captures lock again.
When this bit is a logic 1, it is recommended the DLL be re-initialized by writing any value to the DLL Delay Tap Status register.

ERRORI:

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one and is cleared upon read.

DLLCLKI:

The reference clock event register bit DLLCLKI provides a method to monitor activity on the variable delay clock. When the internal DLLCLK changes from a logic zero to a logic one, the DLLCLKI register bit is set to logic one and cleared upon read.

In the unlikely event this bit is logic 0, the DLL should be re-initiated by writing any value to the DLL Delay Tap Status register.

LREFCLKI:

The line clock event register bit LREFCLKI provides a method to monitor activity on the LREFCLK input clock. When the LREFCLK primary input changes from a logic zero to a logic one, the LREFCLKI register bit is set to logic one. The LREFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

1.38 VTPP Ingress Tributary Payload Processor Registers (N = 0 to 2)

There is a set of Ingress VTPP registers for each TUG3.

Register 0x0740 + 0x40*N, 0x0742 + 0x40*N, 0x0744 + 0x40*N, 0x0746 + 0x40*N, 0x0748 + 0x40*N, 0x074A + 0x40*N, 0x074C + 0x40*N: VTPP Ingress, TU #1 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #1 in TUG2 #2 to TUG2 #7.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #1 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #1 in the corresponding TUG2 . When IIDLE is set to logic 1, tributary payload bytes, except V5 is replaced by the idle code. The V5 byte is always set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is computed from the incoming pointer value and the relative frame offsets as per normal. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. The IIDLE bit has precedence over the IPAIS bit. The active offset will be forced to 0.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set to logic 1, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #1 in the corresponding TUG2 is inverted to cause downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set to logic 1.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #1 in the corresponding TUG2. When ALARME is set to logic 1, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set to logic 0.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #1 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #1 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit specifies the tributary configuration of tributary group TUG2 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0741 + 0x40*N, 0x0743 + 0x40*N, 0x0745 + 0x40*N, 0x0747 + 0x40*N, 0x0749 + 0x40*N, 0x074B + 0x40*N, 0x074D + 0x40*N: VTPP Ingress, TU #1 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #1 in TUG2 #2 to TUG2 #7.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS indications (i.e. H1 = 0xFF, H2 = 0xFF) required to enter the AIS state for tributary TU #1 in the corresponding TUG2. When RELAYAIS is set to logic 1, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set to logic 0, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #1 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #1 in the corresponding TUG2. When PEE is set to logic 1, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set to logic 1 and upon detection of outgoing pointer justification events when the MONIS bit is set to logic 0. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set to logic 0.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #1 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set to logic 1 when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #1 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set to logic 1 when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #1 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set to logic 1 when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #1 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 0x074E + 0x40*N: VTPP Ingress, TU #1 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

LOP1I:

The LOP1I bit identifies the source of loss of pointer interrupts. The LOP1I bit reports and acknowledges LOP interrupt of TU #1 in TUG2 #1. Interrupts are generated upon loss of pointer and upon re-acquisition. LOP1I is set to logic 1 when the corresponding loss of pointer event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP1I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect loss of pointer events.

LOP2I-LOP7I:

The LOP2I to LOP7I bits identify the source of loss of pointer interrupts. The LOP2I to LOP7I bits report and acknowledge LOP interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set to logic 1 when a loss of pointer event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect loss of pointer events.

Reserved:

The Reserved bit must be written with a logic 0 for proper operation of the TEMUX 84.

Register 0x074F + 0x40*N: VTPP Ingress, TU #1 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge alarm indication signal interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

AIS1I:

The AIS1I bit identifies the source of tributary path AIS interrupts. The AIS1I bit reports and acknowledges AIS interrupt of TU #1 in TUG2 #1. Interrupts are generated upon detection and removal of tributary path AIS alarm. AIS1I is set to logic 1 when the corresponding tributary path AIS event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS1I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect tributary path AIS events.

AIS2I-AIS7I:

The AIS2I to AIS7I bits identify the source of tributary path AIS interrupts. The AIS2I to AIS7I bits report and acknowledge AIS interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS. An AIS*x*I bit is set to logic 1 when a tributary path AIS event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect tributary path AIS events.

Registers 0x0750 + 0x40*N, 0x0752 + 0x40*N, 0x0754 + 0x40*N, 0x0756 + 0x40*N, 0x0758 + 0x40*N, 0x075A + 0x40*N, 0x075C + 0x40*N: VTPP Ingress, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #2 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has no effect when IIDLE is set to logic 1.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #2 in the corresponding TUG2. When IIDLE is set to logic 1, tributary payload bytes, except V5 is replaced by the idle code. The V5 byte is always set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is computed from the incoming pointer value and the relative frame offsets as per normal. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. The IIDLE bit has precedence over the IPAIS bit. The active offset will be forced to 0.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set to logic 1, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #2 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of

pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set to logic 1.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #2 in the corresponding TUG2. When ALARME is set to logic 1, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set to logic 0.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #2 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #2 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit is read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must remain at its default for proper operation of the TEMUX 84.

Register 0x0751 + 0x40*N, 0x0753 + 0x40*N, 0x0755 + 0x40*N, 0x0757 + 0x40*N, 0x0759 + 0x40*N, 0x075B + 0x40*N, 0x075D + 0x40*N: VTPP Ingress, TU #2 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #2 in TUG2 #1 to TUG2 #7.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #2 in the corresponding TUG2. When RELAYAIS is set to logic 1, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set to logic 0, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #2 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #2 in the corresponding TUG2. When PEE is set to logic 1, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set to logic 1 and upon detection of outgoing pointer justification events when the MONIS bit is set to logic 0. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set to logic 0.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #2 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set to logic 1 when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #2 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set to logic 1 when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #2 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set to logic 1 when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #2 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 0x075E + 0x40*N: VTPP Ingress, TU #2 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set to logic 1 when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect loss of pointer events.

Register 0x075F + 0x40*N: VTPP Ingress, TU #2 in TUG2 #1 to TUG2 #7 AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set to logic 1 when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect tributary path AIS events.

Register 0x0760 + 0x40*N, 0x0762 + 0x40*N, 0x0764 + 0x40*N, 0x0766 + 0x40*N, 0x0768 + 0x40*N, 0x076A + 0x40*N, 0x076C + 0x40*N: VTPP Ingress, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #3 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has no effect when IIDLE is set to logic 1.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #3 in the corresponding TUG2. When IIDLE is set to logic 1, tributary payload bytes, except V5 is replaced by the idle code. The V5 byte is always set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is computed from the incoming pointer value and the relative frame offsets as per normal. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. The IIDLE bit has precedence over the IPAIS bit. The active offset will be forced to 0.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set to logic 1, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #3 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of

pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set to logic 1.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #3 in the corresponding TUG2. When ALARME is set to logic 1, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set to logic 0.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #3 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #3 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit is read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit is read-only and reflect the values written into the corresponding register of TU #1. This bit must remain a logic 1 for proper operation of the TEMUX 84.

Register 0x0761 + 0x40*N, 0x0763 + 0x40*N, 0x0765 + 0x40*N, 0x0767 + 0x40*N, 0x0769 + 0x40*N, 0x076B + 0x40*N, 0x076D + 0x40*N: VTPP Ingress, TU #3 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #3 in the corresponding TUG2. When RELAYAIS is set to logic 1, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set to logic 0, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #3 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #3 in the corresponding TUG2. When PEE is set to logic 1, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set to logic 1 and upon detection of outgoing pointer justification events when the MONIS bit is set to logic 0. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set to logic 0.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #3 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set to logic 1 when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #3 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set to logic 1 when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #3 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set to logic 1 when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #3 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 0x076E + 0x40*N: VTPP Ingress, TU #3 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set to logic 1 when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect loss of pointer events.

Register 0x076F + 0x40*N: VTPP Ingress, TU #3 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set to logic 1 when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect tributary path AIS events.

Register 0x0770 + 0x40*N, 0x0772 + 0x40*N, 0x0774 + 0x40*N, 0x0776 + 0x40*N, 0x0778 + 0x40*N, 0x077A + 0x40*N, 0x077C + 0x40*N: VTPP Ingress, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #4 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has no effect when IIDLE is set to logic 1.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #4 in the corresponding TUG2. When IIDLE is set to logic 1, tributary payload bytes, except V5 is replaced by the idle code. The V5 byte is always set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is computed from the incoming pointer value and the relative frame offsets as per normal. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. The IIDLE bit has precedence over the IPAIS bit. The active offset will be forced to 0.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set to logic 1, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #4 in the corresponding TUG2 is

inverted, causing downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set to logic 1.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #4 in the corresponding TUG2. When ALARME is set to logic 1, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set to logic 0.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #4 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #4 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation is FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit is read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit is read-only and reflect the values written into the corresponding register of TU #1. This bit must remain a logic 1 for proper operation of the TEMUX 84.

Register 0x0771 + 0x40*N, 0x0773 + 0x40*N, 0x0775 + 0x40*N, 0x0777 + 0x40*N, 0x0779 + 0x40*N, 0x077B + 0x40*N, 0x077D + 0x40*N: VTPP Ingress, TU #4 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #4 in the corresponding TUG2. When RELAYAIS is set to logic 1, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set to logic 0, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #4 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #4 in the corresponding TUG2. When PEE is set to logic 1, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set to logic 1 and upon detection of outgoing pointer justification events when the MONIS bit is set to logic 0. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set to logic 0.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #4 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set to logic 1 when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #4 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set to logic 1 when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #4 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set to logic 1 when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #4 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 0x077E + 0x40*N: VTPP Ingress, TU #4 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. When the corresponding TUG2 tributary group is configured TU12 (VT2) mode, the associated LOP*x*I bit is unused and will return a logic 0 when read. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set to logic 1 when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect loss of pointer events.

Register 0x077F + 0x40*N: VTPP Ingress, TU #4 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated AIS*x*I bit is unused and will return a logic 0 when read. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set to logic 1 when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect tributary path AIS events.

1.39 RTDM Receive Tributary Bit Asynchronous Demapper Registers

Registers 0x0800 – 0x85E: RTDM Tributary Control

TU Address Map:

TUG3	TUG2	TU #1	TU #2	TU #3	TU #4
1	1	0x800	0x808	0x810	0x818
1	2	0x801	0x809	0x811	0x819
1	3	0x802	0x80A	0x812	0x81A
1	4	0x803	0x80B	0x813	0x81B
1	5	0x804	0x80C	0x814	0x81C
1	6	0x805	0x80D	0x815	0x81D
1	7	0x806	0x80E	0x816	0x81E
2	1	0x820	0x828	0x830	0x838
2	2	0x821	0x829	0x831	0x839
2	3	0x822	0x82A	0x832	0x83A
2	4	0x823	0x82B	0x833	0x83B
2	5	0x824	0x82C	0x834	0x83C
2	6	0x825	0x82D	0x835	0x83D
2	7	0x826	0x82E	0x836	0x83E
3	1	0x840	0x848	0x850	0x858
3	2	0x841	0x849	0x851	0x859
3	3	0x842	0x84A	0x852	0x85A
3	4	0x843	0x84B	0x853	0x85B
3	5	0x844	0x84C	0x854	0x85C
3	6	0x845	0x84D	0x855	0x85D
3	7	0x846	0x84E	0x856	0x85E

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

These registers configure the operating mode for individual tributaries.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from the tributary. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set to logic 1, all payload bits of the de-mapped T1 or E1 stream are set to logic 1 and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set to logic 0, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of the tributary. When PROV is set to logic 1, the tributary is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set to logic 0, the tributary is not processed.

The priority of the per-tributary mapping configuration bits is given below.

ITVT bit of the INSBI block	ENBL bit of the byte sync. demapper	PROV	Configuration
1	X	X	Transparent VT to the SBI DROP Bus.
0	1	0	Byte synchronously demapped VT.
0	X	1	Bit asynchronously demapped VT.
0	0	0	No demapping. The SBI columns for the tributary contain all zeros.

TU11 and T1 Bits:

When the TU11 bit is set to logic 1, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set to logic 0, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

The T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set to logic 1) or an E1 stream (if the T1 bit is set to logic 0).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the group are read-only. The T1 bit must be configured the same for all tributaries.

If at least one tributary in a TUG3 is a byte synchronously demapped T1, the combination of TU11 logic 0 with T1 logic 1 is not supported for that TUG3.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Illegal setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 0x0862: RTDM Time Switch Page Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	APAGE	0

This register allows selection of one of two pages in the time switch configuration RAM to be the active page. Neither time switch page is active when the Ingress Time Switch Enable register bit, ITSEN, in the Master SONET/SDH Ingress Configuration register is a logic 0.

APAGE:

The time switch configuration RAM active page select bit, APAGE, controls the selection of one of two pages in the time switch configuration RAM to be the active page. When APAGE is set to logic 1, the configuration in page 1 of the time switch configuration RAM is used to associate incoming tributaries to logical FIFOs in the payload buffer. When APAGE is set to logic 0, the configuration in page 0 of the time switch configuration RAM is used to associate incoming tributaries to logical FIFOs in the payload buffer. Changes of the active page as a result of write accesses to APAGE are synchronized to SCLK and effective immediately.

Register 0x0863: RTDM Indirect Time Switch Tributary RAM Status and Control

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6	R/W	RWB	1
Bit 5	R/W	PAGE	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register provides control and status for the indirect RAM containing time switch tributary information. **Writing to this register triggers an indirect time switch configuration register access**. The BUSY bit will immediately be set to logic 1 and will remain high until the write is complete. The write will only physically occur during transport overhead cycles such that writes can be safely made to the active page as well. Note that when an indirect write access is to be performed, the RTDM Indirect Ingress Tributary Data register and the RTDM Indirect Time Switch Internal Link Address register must first be setup before writing to this register. This time switch settings configured via this register are inactive when the Ingress Time Switch Enable register bit, ITSEN, in the Master SONET/SDH Ingress Configuration register is a logic 0.

PAGE:

The indirect page select bit, PAGE, selects between accesses to the two pages in the time switch configuration RAM. When PAGE is set to logic 1, page 1 of the time switch configuration RAM is accessed. When PAGE is set to logic 0, page 0 of the RAM is accessed. The PAGE bit should be different than the APAGE bit when writing to the RAM as writing to the active page is not recommended.

RWB:

The indirect access control bit, RWB, selects between a configure (write) or interrogate (read) access to the time switch configuration RAM. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is

taken from the Indirect Time Switch Tributary register. Writing a logic one to RWB triggers an indirect read operation. The read can be found in the Indirect Tributary Data register.

BUSY:

The BUSY bit reports the status of the prevailing indirect access operation. BUSY is set to logic 1 when a write to the Indirect Time Switch Tributary Address register triggers an indirect access and remains high until the access is complete. The BUSY bit should be polled until it is low to determine when data from an indirect read operation is available in the Indirect Tributary Data register or when a new indirect write operation may commence. If LREFCLK disappears during an access, the BUSY bit can stay high.

Register 0x0864: RTDM Indirect Time Switch Internal Link Address

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	INT_SPE[1]	0
Bit 5	R/W	INT_SPE[0]	1
Bit 4	R/W	INT_LINK[4]	0
Bit 3	R/W	INT_LINK[3]	0
Bit 2	R/W	INT_LINK[2]	0
Bit 1	R/W	INT_LINK[1]	0
Bit 0	R/W	INT_LINK[0]	1

The address specified by this register is the TEMUX 84 internal link number that ingress tributaries to the TEMUX 84 will be switched to when the Ingress Time Switch Enable register bit, ITSEN, in the Master SONET/SDH Ingress Configuration register is a logic 1. The ingress tributary that will be mapped to this internal link number is the Ingress tributary number specified via the RTDM Indirect Ingress Tributary Data register and is contained in the time switch RAM at the address specified by this register.

The one constraint on switch configuration is that the all the remapped tributaries for each INT_SPE[1:0] value must be of the same type (T1 or E1).

INT_LINK [4:0]:

The indirect internal link number bits (INT_LINK[4:0]) associate the specified T1 or E1 stream internal to the TEMUX 84 and matching the system side interface with the ingress tributary specified in the Indirect Ingress Tributary Data register. The internal link number that an ingress tributary will be switched to, must be set up in this register before triggering the indirect write or read via the RTDM Indirect Ingress Tributary Data register. INT_LINK [4:0] ranges from 00001b to 10101b (1 to 21) for E1 streams and from 00001b to 11100b (1 to 28) for T1 streams.

INT_SPE[1:0]:

The indirect internal synchronous payload envelope bits, INT_SPE[1:0], associate the specified T1 or E1 stream internal to the TEMUX 84 and matching the system side interface with the ingress tributary specified in the

Indirect Ingress Tributary Data register. Before triggering the indirect write operation, the internal SPE number must be set up in this register. Valid values for SPE[1:0] are 01b, 10b and 11b..

Register 0x0865: RTDM Indirect Ingress Tributary Data

Bit	Type	Function	Default
Bit 7	R/W	ING_TUG3[1]	X
Bit 6	R/W	ING_TUG3[0]	X
Bit 5	R/W	ING_TUG2[2]	X
Bit 4	R/W	ING_TUG2[1]	X
Bit 3	R/W	ING_TUG2[0]	X
Bit 2	R/W	ING_TU[2]	X
Bit 1	R/W	ING_TU[1]	X
Bit 0	R/W	ING_TU[0]	X

This register identifies an ingress tributary that will be switched to an internal link number through the time switch configuration RAM. An indirect access to the time switch configuration RAM, associates the ingress link specified in this register with the internal link number forming the RAM address as specified in the RTDM Indirect Time Switch Internal Link Address register. The time switch selection configured via this indirect data register are inactive when the Ingress Time Switch Enable register bit, ITSEN, in the Master SONET/SDH Ingress Configuration register is a logic 0.

ING_TU[2:0]:

The indirect ingress tributary unit bits (ING_TU[2:0]) indicate the tributary unit to be switched to the internal link identified in the RTDM Indirect Time Switch Internal Link Address register. Legal ING_TU[2:0] ranges are ‘b001 to ‘b100.

ING_TUG2[2:0]:

The indirect ingress tributary unit group 2 bits (ING_TUG2[2:0]) indicate the tributary unit group 2 to be switched to the internal link identified in the RTDM Indirect Time Switch Internal Link Address register. Legal ING_TUG2[2:0] ranges are ‘b001 to ‘b111.

ING_TUG3[1:0]:

The indirect ingress tributary unit group 3 bits (ING_TUG2[1:0]) indicate the tributary unit group 3 to be switched to the internal link identified in the RTDM Indirect Time Switch Internal Link Address register. Legal ING_TUG3[1:0] ranges are ‘b01 to ‘b11.

1.40 VTPP Egress Tributary Payload Processor Registers

There is a set of Egress VTPP registers for each TUG3.

Register 0x0900 + 0x40*N, 0x0902 + 0x40*N, 0x09404 + 0x40*N, 0x0906 + 0x40*N, 0x0908 + 0x40*N, 0x090A + 0x40*N, 0x090C + 0x40*N: VTPP Egress, TU #1 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #1 in TUG2 #1 to TUG2 #7.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #1 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set to logic 1, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #1 in the corresponding TUG2 is inverted to cause downstream pointer processing elements to enter a loss of pointer state. The DLOP bit has no effect when the IPAIS bit is set to logic 1.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #1 in the corresponding TUG2. When ALARME is set to logic 1, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set to logic 0.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #1 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #1 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit specifies the tributary configuration of tributary group TUG2 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

These bits must be kept at their defaults for proper operation of the TEMUX 84.

Register 0x0901 + 0x40*N, 0x0903 + 0x40*N, 0x0905 + 0x40*N, 0x0907 + 0x40*N, 0x0909 + 0x40*N, 0x090B + 0x40*N, 0x090D + 0x40*N: VTPP Egress, TU #1 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #1 in TUG2 #1 to TUG2 #7.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #1 in the corresponding TUG2. When RELAYAIS is set to logic 1, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set to logic 0, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #1 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #1 in the corresponding TUG2. When PEE is set to logic 1, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set to logic 1 and upon detection of outgoing pointer justification events when the MONIS bit is set to logic 0. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set to logic 0.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #1 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set to logic 1 when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #1 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set to logic 1 when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #1 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set to logic 1 when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #1 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 0x090E + 0x40*N: VTPP Egress, TU #1 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

LOP1I:

The LOP1I bit identifies the source of loss of pointer interrupts. The LOP1I bit reports and acknowledges LOP interrupt of TU #1 in TUG2 #1. Interrupts are generated upon loss of pointer and upon re-acquisition. LOP1I is set to logic 1 when the corresponding loss of pointer event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP1I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect loss of pointer events.

LOP2I-LOP7I:

The LOP2I to LOP7I bits identify the source of loss of pointer interrupts. The LOP2I to LOP7I bits report and acknowledge LOP interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set to logic 1 when a loss of pointer event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect loss of pointer events.

Reserved:

The Reserved bit must be written with a logic 0 for proper operation of the TEMUX 84.

Register 0x090F + 0x40*N: VTPP Egress, TU #1 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge alarm indication signal interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

AIS1I:

The AIS1I bit identifies the source of tributary path AIS interrupts. The AIS1I bit reports and acknowledges AIS interrupt of TU #1 in TUG2 #1. Interrupts are generated upon detection and removal of tributary path AIS alarm. AIS1I is set to logic 1 when the corresponding tributary path AIS event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS1I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect tributary path AIS events.

AIS2I-AIS7I:

The AIS2I to AIS7I bits identify the source of tributary path AIS interrupts. The AIS2I to AIS7I bits report and acknowledge AIS interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS. An AIS*x*I bit is set to logic 1 when a tributary path AIS event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect tributary path AIS events.

Register 0x0910 + 0x40*N, 0x0912 + 0x40*N, 0x0914 + 0x40*N, 0x0916 + 0x40*N, 0x0918 + 0x40*N, 0x091A + 0x40*N, 0x091C + 0x40*N: VTPP Egress, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #2 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set to logic 1, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #2 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of pointer state. The DLOP bit has no effect when the IPAIS bit is set to logic 1.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #2 in the corresponding TUG2. When ALARME is set to logic 1, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set to logic 0.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #2 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #2 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit is read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

Bit 7 is read-only and reflects the value written into the corresponding register of TU #1. Bit 1 must remain a logic 0 for proper operation of the TEMUX 84.

Register 0x0911 + 0x40*N, 0x0913 + 0x40*N, 0x0915 + 0x40*N, 0x0917 + 0x40*N, 0x0919 + 0x40*N, 0x091B + 0x40*N, 0x091D + 0x40*N: VTPP Egress, TU #2 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #2 in TUG2 #1 to TUG2 #7.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #2 in the corresponding TUG2. When RELAYAIS is set to logic 1, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set to logic 0, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #2 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #2 in the corresponding TUG2. When PEE is set to logic 1, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set to logic 1 and upon detection of outgoing pointer justification events when the MONIS bit is set to logic 0. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set to logic 0.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #2 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set to logic 1 when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #2 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set to logic 1 when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #2 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set to logic 1 when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #2 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 0x091E + 0x40*N: VTPP Egress, TU #2 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set to logic 1 when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect loss of pointer events.

Register 0x091F + 0x40*N: VTPP Egress, TU #2 in TUG2 #1 to TUG2 #7 AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set to logic 1 when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect tributary path AIS events.

Register 0x0920 + 0x40*N, 0x0922 + 0x40*N, 0x0924 + 0x40*N, 0x0926 + 0x40*N, 0x0928 + 0x40*N, 0x092A + 0x40*N, 0x092C + 0x40*N: VTPP Egress, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #3 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set to logic 1, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #3 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of pointer state. The DLOP bit has no effect when the IPAIS bit is set to logic 1.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #3 in the corresponding TUG2. When ALARME is set to logic 1, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set to logic 0.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #3 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #3 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit is read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

Bit 7 is read-only and reflects the value written into the corresponding register of TU #1. Bit 1 must remain a logic 0 for proper operation of the TEMUX 84.

Register 0x0921 + 0x40*N, 0x0923 + 0x40*N, 0x0925 + 0x40*N, 0x0927 + 0x40*N, 0x0929 + 0x40*N, 0x092B + 0x40*N, 0x092D + 0x40*N: VTPP Egress, TU #3 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #3 in the corresponding TUG2. When RELAYAIS is set to logic 1, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set to logic 0, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #3 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #3 in the corresponding TUG2. When PEE is set to logic 1, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set to logic 1 and upon detection of outgoing pointer justification events when the MONIS bit is set to logic 0. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set to logic 0.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #3 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set to logic 1 when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #3 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set to logic 1 when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #3 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set to logic 1 when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #3 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 0x092E + 0x40*N: VTPP Egress, TU #3 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set to logic 1 when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect loss of pointer events.

Register 0x092F + 0x40*N: VTPP Egress, TU #3 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set to logic 1 when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect tributary path AIS events.

Register 0x0930 + 0x40*N, 0x0932 + 0x40*N, 0x0934 + 0x40*N, 0x0936 + 0x40*N, 0x0938 + 0x40*N, 0x093A + 0x40*N, 0x093C + 0x40*N: VTPP Egress, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #4 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set to logic 1, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #4 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of pointer state. The DLOP bit has no effect when the IPAIS bit is set to logic 1.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #4 in the corresponding TUG2. When ALARME is set to logic 1, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set to logic 0.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #4 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #4 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation is FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit is read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

Bit 7 is read-only and reflects the value written into the corresponding register of TU #1. Bit 1 must remain a logic 0 for proper operation of the TEMUX 84.

Register 0x0931 + 0x40*N, 0x0933 + 0x40*N, 0x0935 + 0x40*N, 0x0937 + 0x40*N, 0x0939 + 0x40*N, 0x093B + 0x40*N, 0x093D + 0x40*N: VTPP Egress, TU #4 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #4 in the corresponding TUG2. When RELAYAIS is set to logic 1, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set to logic 0, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #4 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #4 in the corresponding TUG2. When PEE is set to logic 1, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set to logic 1 and upon detection of outgoing pointer justification events when the MONIS bit is set to logic 0. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set to logic 0.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #4 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set to logic 1 when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #4 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set to logic 1 when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #4 in the corresponding TUG2. When the MONIS bit is set to logic 1, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set to logic 0, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set to logic 1 when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set to logic 0) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #4 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 0x093E + 0x40*N: VTPP Egress, TU #4 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. When the corresponding TUG2 tributary group is configured TU12 (VT2) mode, the associated LOP*x*I bit is unused and will return a logic 0 when read. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set to logic 1 when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect loss of pointer events.

Register 0x093F + 0x40*N: VTPP Egress, TU #4 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated AIS*x*I bit is unused and will return a logic 0 when read. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set to logic 1 when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set to logic 0) and may be polled to detect tributary path AIS events.

1.41 Byte Synchronous Mapper Registers

Register 0x09C0: Byte Synchronous Mapping Control Register

Bit	Type	Function	Default
Bit 7	R/W	APAGE	0
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	TS_EN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	1

Reserved:

The reserved bits should be set to the default for correct operation.

TS_EN:

The TS_EN bit is used to enable the tributary to internal link mapping capability.

- When TS_EN is a ‘0’ mapping will be fixed to a one to one mapping and will not be programmable.
- When TS_EN is a ‘1’ tributary to internal link mapping is enabled and is specified by the contents of the Byte Synchronous Mapping Tributary Mapping RAM.

APAGE:

The tributary mapping RAM active page select bit (APAGE) controls the selection of one of two pages in the tributary mapping RAM to be the active page. When APAGE is set to logic 1, page one of the tributary mapping RAM is used to associate incoming tributaries to T1/E1 links. When APAGE is set to logic 0, page 0 of the tributary mapping RAM is used to associate incoming tributaries to internal links. Changes of the active page as a result of write accesses to APAGE will be synchronized to multi-frame boundaries.

Register 0x09C1 Byte Synchronous Mapping FIFO Underrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_UDRI	X

This interrupt status register is cleared when read.

If an underrun condition is reported for a link, the link should be reset by writing to the tributary control RAM location for the tributary corresponding to that link.

This Underrun interrupt register is the output of a priority encoder of the underrun history of all links. The most significant links have the highest priority and will be reported first if underruns simultaneously occur on multiple links.

If bit 0 is logic zero, no links have under since the last read, and all pending underrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is logic one, the register contents are valid, and indicate a link has underrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note that if a tributary is misbehaving so that it frequently underruns, the reporting of the multiple underruns can prevent the reporting of underruns on lower priority links. Such misbehaving links should be disabled (TRIB_ENBL=0) to obtain the complete FIFO underrun history.

FIFO_UDRI:

This bit is set when a FIFO underrun is detected.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the tributary associated with the FIFO buffer in which the underrun was detected.
Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.
LINK[4:0] and SPE[1:0] are invalid unless FIFO_UDRI is set.

Table 1 and Table 2 provide the correspondence between SPE and LINK and the Telecom bus tributaries.

Register 0x09C2 Byte Synchronous Mapping FIFO Overrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_OVRI	X

This interrupt status register is cleared when read.

If an overflow condition is reported for a link, the link should be reset by writing to the tributary control RAM location for the tributary corresponding to that link.

This Overrun interrupt register is the output of a priority encoder of the overrun history of all links. The most significant links have the highest priority and will be reported first if overruns simultaneously occur on multiple links.

If bit 0 is logic zero, no links have under/overrun since the last read, and all pending overrun notifications have been reported. Bits 1-7 should be ignored.

If bit 0 is logic one, the register contents are valid, and indicate a link has overrun since the last read, or a prior notification was still pending. Continue reading this register, recording all entries, until bit 0 is zero, indicating that no more pending entries are present.

Note that if a tributary is misbehaving so that it frequently overruns, the reporting of the multiple overruns can prevent the reporting of overruns on lower priority links. Such misbehaving links should be disabled (TRIB_ENBL=0) to obtain the complete FIFO overrun history.

FIFO_OVRI:

This bit is set when a FIFO overrun is detected.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the tributary associated with the FIFO buffer in which the overrun was detected.
Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.
LINK[4:0] and SPE[1:0] are invalid unless FIFO_OVRI is set.

Table 1 and Table 2 provide the correspondence between SPE and LINK and the Telecom bus tributaries.

Register 0x09C3: Byte Synchronous Mapping Tributary Register Indirect Access Address Register

Bit	Type	Function	Default
Bit 7	R/W	MAP_REG	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] fields are used to fully specify for which tributary the Mapping or Control RAM write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SPE as specified by the SPE[1:0] field. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.

When an SPE is configured for E1, indirect accesses are not permitted to TRIB indexes b'10110 through b'11100.

MAP_REG:

MAP_REG specifies whether the Byte Synchronous Mapping Tributary Mapping RAM or Byte Synchronous Mapping Tributary Control RAM are to be addressed by the SPE[1:0] and TRIB[4:0] fields.

When MAP_REG = '1' the Byte Synchronous Mapping Tributary Mapping RAM is addressed by the SPE[1:0] and TRIB[4:0] fields.

When MAP_REG = '0' the Byte Synchronous Mapping Tributary Control RAM is addressed by the SPE[1:0] and TRIB[4:0] fields.

Register 0x09C4: Byte Synchronous Mapping Tributary Register Indirect Access Control Register

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RWB	0
Bit 0	R/W	PAGE	0

PAGE:

The indirect page select bit (PAGE) selects between the two pages in the tributary mapping RAM. The PAGE bit should be different than the APAGE bit when writing to the RAM as writing to the active page is not recommended.

The PAGE bit has no relevance for Control RAM accesses.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary mapping or control configuration RAM. Writing a ‘0’ to RWB triggers an indirect write operation. Data to be written is taken from the Byte Synchronous Mapping Tributary Mapping Indirect Access Data Register or Byte Synchronous Mapping Tributary Control Indirect Access Data Register. Writing a ‘1’ to RWB triggers an indirect read operation. The data read can be found in the Byte Synchronous Mapping Tributary Mapping Indirect Access Data Register or Byte Synchronous Mapping Tributary Control Indirect Access Data Register.

HST_ADDR_ERR:

When set following a host read, this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when a write to the Byte Synchronous Mapping Tributary Register Indirect Access Control Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Data register or to determine when a new indirect write operation may commence. The BUSY bit is asserted for up to 4.32us after a page switch.

Register 0x09C5: Byte Synchronous Mapping Tributary Mapping Indirect Access Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SPE[1]	See Note below
Bit 5	R/W	SPE[0]	See Note below
Bit 4	R/W	LINK[4]	See Note below
Bit 3	R/W	LINK[3]	See Note below
Bit 2	R/W	LINK[2]	See Note below
Bit 1	R/W	LINK[1]	See Note below
Bit 0	R/W	LINK[0]	See Note below

LINK[4:0] and SPE[1:0]

The LINK[4:0] and SPE[1:0] fields are used to specify the internal link to tributary mapping.

LINK[4:0] specifies the internal T1/E1 link number within the SPE as specified by the SPE[1:0] field that should be used as the source for data transmitted to the tributary associated with the Byte Synchronous Mapping Tributary Register Indirect Access Address register entry.

Note: The default mapping is straight through i.e. 1:1. Therefore, SPE1, LINK 1 on the discrete T1/E1 side will be mapped by default to SPE1, LINK 1 on the mapped SONET/SDH side and so on up to SPE3, LINK 28.

The mapping of more than one tributary to a link or more than one link to a tributary is not allowed.

Register 0x09C6: Byte Synchronous Mapping Tributary Control Indirect Access Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	TRIB_TYP	0
Bit 1	R/W	RFI	0
Bit 0	R/W	ENBL	0

Reserved:

The reserved bits should be set to the default for correct operation.

ENBL

The ENBL bit is used to enable the tributary. Writing to the Byte Synchronous Mapping Tributary Register Indirect Access Control Register with the ENBL bit set enables the byte synchronous mapper to take tributary data from an T1/E1 link and transmit that data to the tributary mapped to that link.

The priority of the per-tributary mapping configuration bits is given below.

ETVT bit of the TTMP block	ENBL	PROV bit of the TTMP block	Configuration
1	X	0	Transparent VT from the SBI ADD Bus.
0	1	X	Byte synchronously mapped VT. (The PROV bit must be set to enable AIS insertion as controlled by the EGRALMEN bit.)
0	0	1	Bit asynchronously mapped VT.
0	0	0	No mapping. The VT contains valid overhead, but the payload is all zeros.

RFI:

The RFI bit controls the insertion of RFI-V. The contents of this bit are inserted into bit 4 of the V5 byte of the tributary.

TRIB_TYP:

The TRIB_TYP bit must be set to match the tributary type.

TRIB_TYP	Description
0	T1
1	E1

Note: Any write to a Tributary Control RAM location for a tributary will generate a configuration reset on that tributary, irrespective of whether the

data written to the tributary control RAM location is unchanged from the previous value.

Register 0x09C9: Byte Synchronous Mapping T1 Thresholds Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_T1[3]	0
Bit 6	R/W	MIN_THR_T1[2]	1
Bit 5	R/W	MIN_THR_T1[1]	1
Bit 4	R/W	MIN_THR_T1[0]	0
Bit 3	R/W	MAX_THR_T1[3]	1
Bit 2	R/W	MAX_THR_T1[2]	1
Bit 1	R/W	MAX_THR_T1[1]	1
Bit 0	R/W	MAX_THR_T1[0]	0

MIN_THR_T1[3:0]

Used to modify the Minimum Threshold for T1 tributaries. The Minimum threshold is the FIFO depth below which a positive justification is performed.

MAX_THR_T1[3:0]

Used to modify the Maximum Threshold for T1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a negative justification.

MAX_THR_T1 should be set to 1010 to guarantee correct operation.

Register 0x09CA: Byte Synchronous Mapping E1 Thresholds Register

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR_E1[3]	0
Bit 6	R/W	MIN_THR_E1[2]	0
Bit 5	R/W	MIN_THR_E1[1]	1
Bit 4	R/W	MIN_THR_E1[0]	0
Bit 3	R/W	MAX_THR_E1[3]	1
Bit 2	R/W	MAX_THR_E1[2]	1
Bit 1	R/W	MAX_THR_E1[1]	1
Bit 0	R/W	MAX_THR_E1[0]	0

MIN_THR_E1[3:0]

Used to modify the Minimum Threshold for E1 tributaries. The Minimum threshold is the FIFO depth below which a positive justification is performed.

MAX_THR_E1[3:0]

Used to modify the Maximum Threshold for E1 tributaries. The Maximum threshold is the FIFO depth which when exceeded will cause a negative justification.

MAX_THR_E1 should be set to 1010 to guarantee correct operation.

1.42 Byte Synchronous Demapper Registers

Register 0x09E0: Byte Synchronous Demapping Control Register

Bit	Type	Function	Default
Bit 7	R/W	APAGE	0
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	TS_EN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	1

Reserved:

The reserved bits must be set to their defaults for correct operation.

TS_EN:

The TS_EN bit is used to enable the tributary to T1/E1 link mapping capability.

- When TS_EN is ‘0’ mapping will be fixed to a one to one mapping and will not be programmable.
- When TS_EN is ‘1’ tributary to T1/E1 link mapping is enabled and is specified by the contents of the Byte Synchronous Demapping Tributary Mapping Register RAM

APAGE:

The tributary mapping RAM active page select bit (APAGE) controls the selection of one of two pages in the tributary mapping RAM to be the active page. When APAGE is set to logic 1, page one of the tributary mapping RAM is used to associate incoming tributaries to T1/E1 links. When APAGE is set to logic 0, page 0 of the tributary mapping RAM is used to associate incoming tributaries to T1/E1 links. Changes of the active page as a result of write accesses to APAGE will be synchronized to SBI multi-frame boundaries.

Register 0x09E3: Byte Synchronous Demapping Tributary RAM Indirect Access Address Register

Bit	Type	Function	Default
Bit 7	R/W	MAP_REG	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] fields are used to fully specify to which tributary the Mapping or Control register write or read operation will apply.

TRIB[4:0] specifies the SBI tributary number within the SPE as specified by the SPE[1:0] field. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.

When an SPE is configured for E1, indirect accesses are not permitted to TRIB indexes b'10110 through b'11100.

MAP_REG:

MAP_REG specifies whether the Byte Synchronous Demapping Tributary Mapping Registers or Byte Synchronous Demapping Tributary Control Registers are to be addressed by the SPE[1:0] and TRIB[4:0] fields.

When MAP_REG = '1' the Byte Synchronous Demapping Tributary Mapping Registers are addressed by by the SPE[1:0] and TRIB[4:0] fields.

When MAP_REG = '0' the Byte Synchronous Demapping Tributary Control Registers are addressed by by the SPE[1:0] and TRIB[4:0] fields.

Register 0x09E4: Byte Synchronous Demapping Tributary RAM Indirect Access Control Register

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6	R	HST_ADDR_ERR	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RWB	0
Bit 0	R/W	PAGE	0

PAGE:

The indirect page select bit (PAGE) selects between the two pages in the tributary mapping RAM. The PAGE bit should be different than the APAGE bit when writing to the RAM as writing to the active page is not recommended.

The PAGE bit has no relevance for Control RAM accesses.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary mapping or control configuration RAM. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the Byte Synchronous Demapping Tributary Mapping Indirect Access Data Register or Byte Synchronous Demapping Tributary Control Indirect Access Data Register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the Byte Synchronous Demapping Tributary Mapping Indirect Access Data Register or Byte Synchronous Demapping Tributary Control Indirect Access Data Register.

HST_ADDR_ERR:

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. For DS3 and E3 out of range tributaries are 1,2 to 1,28; 2,2 to 2,28 and 3,2 to 3,28. For E1 out of range tributaries are 1,22 to 1,28; 2,22 to 2,28 and 3,22 to 3,28.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when a write to the Byte Synchronous Demapping Tributary Register Indirect Access Control Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Data register or to determine when a new indirect write operation may commence.

Register 0x09E5: Byte Synchronous Demapping Tributary Mapping RAM Indirect Access Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SPE[1]	See Note below
Bit 5	R/W	SPE[0]	See Note below
Bit 4	R/W	LINK[4]	See Note below
Bit 3	R/W	LINK[3]	See Note below
Bit 2	R/W	LINK[2]	See Note below
Bit 1	R/W	LINK[1]	See Note below
Bit 0	R/W	LINK[0]	See Note below

LINK[4:0] and SPE[1:0]

The LINK[4:0] and SPE[1:0] fields are used to specify the system interface link to Telecom Drop bus tributary mapping.

LINK[4:0] specifies the system interface link number within the system interface SPE as specified by the SPE[1:0] field that should be used as the destination for data received from the Telecom Drop bus tributary associated with the Byte Synchronous Demapping Tributary Control and Status Register.

Note: The default mapping is straight through i.e. 1:1. Therefore, SPE1, LINK 1 on the system interface side will be mapped by default to SPE1, LINK 1 on the Telecom Drop bus side and so on up to SPE3, LINK 28.

Register 0x09E6: Byte Synchronous Demapping Tributary Control RAM Indirect Access Data Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	ENBL	0

Reserved:

The reserved bits must be logic 0 for correct operation.

ENBL

The ENBL bit is used to enable the Tributary. Writing to an Byte Synchronous Demapping Tributary RAM Indirect Access Control Register with the ENBL bit set enables the EXSBI to take tributary data from a Telecom Drop bus tributary and transmit that data to the T1/E1 link mapped to that tributary.

The priority of the per-tributary mapping configuration bits is given below.

ITVT bit of the INSBI block	ENBL	PROV bit of the RTDM block	Configuration
1	X	X	Transparent VT to the SBI DROP Bus.
0	1	0	Byte synchronously demapped VT.
0	X	1	Bit asynchronously demapped VT.
0	0	0	No demapping. The SBI columns or the H-MVIP timeslots for the tributarycontain all zeros.

Note: Any write to a Tributary Control register for a tributary will generate a configuration reset on that tributary, irrespective of whether the data written to the tributary control register is unchanged from the previous value.

Register 0x09EF: Byte Synchronous Demapping FIFO Control Register

Bit	Type	Function	Default
Bit 7	R/W	FI_EMPTY_ENBL	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

FI_EMPTY_ENBL:

This bit must be logic 1 for correct operation of the byte synchronous demapping. Setting it prevents FIFO underflows. If this bit is logic 0, tributary bits may be lost or corrupted.

1.43 RTOP Receive Tributary Path Overhead Processor Registers

There is a set of RTOP registers for each TUG3.

Register 0x0A00 + 0x100*N, 0x0A08 + 0x100*N, 0x0A10 + 0x100*N, 0x0A18 + 0x100*N, 0x0A20 + 0x100*N, 0x0A28 + 0x100*N, 0x0A30 + 0x100*N: RTOP, TU #1 in TUG2 #1 to TUG2 #7, Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

This set of registers configures the operational modes of TU #1 in TUG2 #1 to TUG2 #7.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIE is set to logic 1, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set to logic 0. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set to logic 0 and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set to logic 1.

RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIZ7EN is set to logic 0, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set to logic 1. Interrupts due to RFIV status change are masked when RFIE is set to logic 0. When RDIZ7EN is set to logic 1, RFIE is ignored.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #1 in the corresponding TUG2. When COPSLE is set to logic 1, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set to logic 0.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #1 in the corresponding TUG2. When PSLME is set to logic 1, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set to logic 0.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #1 in the corresponding TUG2. When PSLUE is set to logic 1, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set to logic 0.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #1 in the corresponding TUG2. When BLKBIP is set to logic 1, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set to logic 0, the BIP error count is incremented once for each BIP-2 bit that is in error.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0A01 + 0x100*N, 0x0A09 + 0x100*N, 0x0A11 + 0x100*N, 0x0A19 + 0x100*N, 0x0A21 + 0x100*N, 0x0A29 + 0x100*N, 0x0A31 + 0x100*N: RTOP, TU #1 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	Reserved	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

This set of registers reports alarm status and configures TU #1 in TUG2 #1 to TUG2 #7.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #1 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set to logic 1 when the RDI bit in the V5 byte is set to logic 1 for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register. RDIV is set to logic 0 when the RDI bit is set to logic 0 for five or ten consecutive multiframes as determined by the RDI10 bit

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #1 in the corresponding TUG2 when RDIZ7EN is set to logic 0. RFIV is set to logic 1 when the RFI bit in the V5 byte is set to logic 1 for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register. RFIV is set to logic 0 when the RFI bit is set to logic 0 for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #1 in the corresponding TUG2 when RDIZ7EN is set to logic 1. The ERDIV[2:0] bits are set to a new code when the same code in the

extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register.

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #1 in the corresponding TUG2. PSLMV is set to logic 1 when the accepted PSL differs from the provisioned value. PSLMV is set to logic 0 when the accepted PSL has the same value as the provisioned one. The PSL match/mismatch state is determined as follows:

Expected PSL	**Accepted PSL**	**PSLM State**
000	000	Match
000	001	Mismatch
000	XXX ≠ 000	Mismatch
001	000	Mismatch
001	001	Match
001	XXX ≠ 001	Match
XXX ≠ 000, 001	000	Mismatch
XXX ≠ 000, 001	001	Match
XXX ≠ 000, 001	XXX	Match
XXX ≠ 000, 001	YYY	Mismatch

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #1 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs form that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set to logic 1 when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set to logic 0 when the unstable counter is cleared.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #1 in the corresponding TUG2. TUPTE is set to logic 1 if tributary TU #1 is to be terminated in the network element containing this TEMUX 84 device. In this case, tributary AIS is automatically inserted based on the contents of the Master SONET/SDH Tributary Alarm AIS Control register. TUPTE is set to logic 0 if tributary TU #1 is part of the through traffic in the network element containing this TEMUX 84 device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #1 in the corresponding TUG2 . When RDIZ7EN is set to logic 0, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set to logic 1, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

Register 0x0A02 + 0x100*N, 0x0A0A + 0x100*N, 0x0A12 + 0x100*N, 0x0A1A + 0x100*N, 0x0A22 + 0x100*N, 0x0A2A + 0x100*N, 0x0A32 + 0x100*N: RTOP, TU #1 in TUG2 #1 to TUG2 #7, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This set of registers configures the expected path signal label of TU #1 in TUG2 #1 to TUG2 #7.

EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #1 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 0x0A03 + 0x100*N, 0x0A0B + 0x100*N, 0x0A13 + 0x100*N, 0x0A1B + 0x100*N, 0x0A23 + 0x100*N, 0x0A2B + 0x100*N, 0x0A33 + 0x100*N: RTOP, TU #1 in TUG2 #1 to TUG2 #7, Accepted Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	APSL[2]	X
Bit 1	R	APSL[1]	X
Bit 0	R	APSL[0]	X

This set of registers reports the accepted path signal label of TU #1 in TUG2 #1 to TUG2 #7.

APSL[2:0]:

The APSL[2:0] bits reports the accepted path signal label of tributary TU #1 in the corresponding TUG2. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

Register 0x0A04 + 0x100*N, 0x0A0C + 0x100*N, 0x0A14 + 0x100*N, 0x0A1C + 0x100*N, 0x0A24 + 0x100*N, 0x0A2C + 0x100*N, 0x0A34 + 0x100*N: RTOP, TU #1 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 0x0A05 + 0x100*N, 0x0A0D + 0x100*N, 0x0A15 + 0x100*N, 0x0A1D + 0x100*N, 0x0A25 + 0x100*N, 0x0A2D + 0x100*N, 0x0A35 + 0x100*N: RTOP, TU #1 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

These sets of registers report the number of block interleave parity (BIP-2) errors detected in TU #1 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. These registers do not saturate.

BIP[10:0]:

The BIP[10:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to any of the Master SONET/SDH Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2 registers within 10 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. BIP-2 errors may be accumulated on a nibble basis or block basis as controlled by the BLKBIP register bit.

Register 0x0A06 + 0x100*N, 0x0A0E + 0x100*N, 0x0A16 + 0x100*N, 0x0A1E + 0x100*N, 0x0A26 + 0x100*N, 0x0A2E + 0x100*N: RTOP, 0x0A36 + 0x100*N: RTOP, TU #1 in TUG2 #2 to TUG2 #7, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 0x0A07 + 0x100*N, 0x0A0F + 0x100*N, 0x0A17 + 0x100*N, 0x0A1F + 0x100*N, 0x0A27 + 0x100*N, 0x0A2F + 0x100*N, 0x0A37 + 0x100*N: RTOP, TU #1 in TUG2 #2 to TUG2 #7, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers reports the number of far end block errors (FEBE) detected in TU #1 in TUG2 #1 to TUG2 #7 in the previous accumulation interval.

FEBE[10:0]:

The FEBE[10:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by applying by writing to the Master SONET/SDH Accumulate Trigger register. The write access transfers the internally accumulated error count to the FEBE registers within 10 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 0x0A38 + 0x100*N: RTOP, TU #1 in TUG2 #1 to TUG2 #7, COPSL Interrupt

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	COPSL7I	0
Bit 5	R	COPSL6I	0
Bit 4	R	COPSL5I	0
Bit 3	R	COPSL4I	0
Bit 2	R	COPSL3I	0
Bit 1	R	COPSL2I	0
Bit 0	R	COPSL1I	0

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

COPSL1I-COPSL7I:

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. The COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #1 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSL*x*I bit is set to logic 1 when a change of PSL event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSL*x*I remains valid when interrupts are not enabled (COPSLE set to logic 0) and may be polled to detect change of path signal label events.

Reserved:

The Reserved bit must be written with a logic 0 for proper operation of the TEMUX 84.

Register 0x0A39 + 0x100*N: RTOP, TU #1 in TUG2 #1 to TUG2 #7, PSLM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLM7I	0
Bit 5	R	PSLM6I	0
Bit 4	R	PSLM5I	0
Bit 3	R	PSLM4I	0
Bit 2	R	PSLM3I	0
Bit 1	R	PSLM2I	0
Bit 0	R	PSLM1I	0

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

PSLM1I-PSLM7I:

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. The PSLM2I to PSLM7I bits report and acknowledge PSLM interrupt of TU #1 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLM*x*I bit is set to logic 1 when a change of PSL matched state on the associated tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM*x*I remains valid when interrupts are not enabled (PSLME set to logic 0) and may be polled to detect path signal label match/mismatch events.

Register 0x0A3A + 0x100*N: RTOP, TU #1 in TUG2 #1 to TUG2 #7, PSLU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLU7I	0
Bit 5	R	PSLU6I	0
Bit 4	R	PSLU5I	0
Bit 3	R	PSLU4I	0
Bit 2	R	PSLU3I	0
Bit 1	R	PSLU2I	0
Bit 0	R	PSLU1I	0

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

PSLU1I-PSLU7I:

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #1 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLU*x*I bit is set to logic 1 when a change of PSL unstable state on the associated tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLU*x*I remains valid when interrupts are not enabled (PSLUE set to logic 0) and may be polled to detect path signal label stable/unstable events.

Register 0x0A3B + 0x100*N: RTOP, TU #1 in TUG2 #1 to TUG2 #7, RDI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RDI7I	0
Bit 5	R	RDI6I	0
Bit 4	R	RDI5I	0
Bit 3	R	RDI4I	0
Bit 2	R	RDI3I	0
Bit 1	R	RDI2I	0
Bit 0	R	RDI1I	0

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

RDI1I-RDI7I:

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. The RDI2I to RDI7I bits report and acknowledge RDI interrupt of TU #1 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDI*x*I bit is set to logic 1 when a change of RDI state on the associated tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI*x*I remains valid when interrupts are not enabled (RDIE set to logic 0) and may be polled to detect change of remote defect indication events.

Register 0x0A3C + 0x100*N: RTOP, TU #1 in TUG2 #1 to TUG2 #7 RFI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RFI7I	0
Bit 5	R	RFI6I	0
Bit 4	R	RFI5I	0
Bit 3	R	RFI4I	0
Bit 2	R	RFI3I	0
Bit 1	R	RFI2I	0
Bit 0	R	RFI1I	0

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

RFI1I-RFI7I:

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #1 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFI*x*I bit is set to logic 1 when a change of RFI state on the associated tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI*x*I remains valid when interrupts are not enabled (RFIE set to logic 0) and may be polled to detect change of remote failure indication events.

Register 0x0A3D + 0x100*N: RTOP, TU #1 in TUG2 #1 to TUG2 #7, Inband Error Reporting Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	IBER7	0
Bit 5	R/W	IBER6	0
Bit 4	R/W	IBER5	0
Bit 3	R/W	IBER4	0
Bit 2	R/W	IBER3	0
Bit 1	R/W	IBER2	0
Bit 0	R/W	IBER1	0

This register enables the inband error reporting mode of the tributaries TU #1 in TUG2 #1 to TUG2 #7.

IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #1 in TUG2 #2 to TUG2 #7, respectively. Setting an IBER*x* bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #1 of the corresponding TUG2. When an IBER*x* bit is low, in band error reporting is disabled and the V5 byte of tributary TU #1 of the corresponding TUG2 is not modified as a result of ingress error events. The egress V5 byte may still be modified via the Remote Serial Alarm ports.

Register 0x0A40 + 0x100*N, 0x0A48 + 0x100*N, 0x0A50 + 0x100*N, 0x0A58 + 0x100*N, 0x0A60 + 0x100*N, 0x0A68 + 0x100*N, 0x0A70 + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, Configuration

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

This set of registers configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIE is set to logic 1, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set to logic 0. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set to logic 0 and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set to logic 1.

RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIZ7EN is set to logic 0, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set to logic 1. Interrupts due to RFIV status change are masked when RFIE is set to logic 0. When RDIZ7EN is set to logic 1, RFIE is ignored.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #2 in the corresponding TUG2. When COPSLE is set to logic 1, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set to logic 0.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #2 in the corresponding TUG2. When PSLME is set to logic 1, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set to logic 0.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #2 in the corresponding TUG2. When PSLUE is set to logic 1, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set to logic 0.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #2 in the corresponding TUG2. When BLKBIP is set to logic 1, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set to logic 0, the BIP error count is incremented once for each BIP-2 bit that is in error.

TU11:

The TU11 bit reports the tributary configuration of the corresponding TUG2. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0A41 + 0x100*N, 0x0A49 + 0x100*N, 0x0A51 + 0x100*N, 0x0A59 + 0x100*N, 0x0A61 + 0x100*N, 0x0A69 + 0x100*N, 0x0A71 + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	Reserved	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

This set of registers reports alarm status and configures TU #2 in TUG2 #1 to TUG2 #7.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #2 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set to logic 1 when the RDI bit in the V5 byte is set to logic 1 for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register. RDIV is set to logic 0 when the RDI bit is set to logic 0 for five or ten consecutive multiframes as determined by the RDI10 bit

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #2 in the corresponding TUG2 when RDIZ7EN is set to logic 0. RFIV is set to logic 1 when the RFI bit in the V5 byte is set to logic 1 for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register. RFIV is set to logic 0 when the RFI bit is set to logic 0 for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #2 in the corresponding TUG2 when RDIZ7EN is set to logic 1. The ERDIV[2:0] bits are set to a new code when the same code in the

extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration registers.

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #2 in the corresponding TUG2. PSLMV is set to logic 1 when the accepted PSL differs from the provisioned value. Note that a path signal mismatch may be declared when the provisioned value is 000 or 001; this is beyond the requirements of GR-253-CORE. PSLMV is set to logic 0 when the accepted PSL has the same value as the provisioned one. The PSL match/mismatch state is determined as follows:

Expected PSL	Accepted PSL	PSLM State
000	000	Match
000	001	Mismatch
000	XXX ≠ 000	Mismatch
001	000	Mismatch
001	001	Match
001	XXX ≠ 001	Match
XXX ≠ 000, 001	000	Mismatch
XXX ≠ 000, 001	001	Match
XXX ≠ 000, 001	XXX	Match
XXX ≠ 000, 001	YYY	Mismatch

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #2 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs form that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set to

logic 1 when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set to logic 0 when the unstable counter is cleared.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #2 in the corresponding TUG2. TUPTE is set to logic 1 if tributary TU #2 is to be terminated in the network element containing this TEMUX 84 device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register. TUPTE is set to logic 0 if tributary TU #2 is part of the through traffic in the network element containing this TEMUX 84 device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #2 in the corresponding TUG2 . When RDIZ7EN is set to logic 0, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set to logic 1, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

Register 0x0A42 + 0x100*N, 0x0A4A + 0x100*N, 0x0A52 + 0x100*N, 0x0A5A + 0x100*N, 0x0A62 + 0x100*N, 0x0A6A + 0x100*N, 0x0A72 + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This set of registers configures the expected path signal label of TU #2 in TUG2 #1 to TUG2 #7.

EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #2 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 0x0A43 + 0x100*N, 0x0A4B + 0x100*N, 0x0A53 + 0x100*N, 0x0A5B + 0x100*N, 0x0A63 + 0x100*N, 0x0A6B + 0x100*N, 0x0A73 + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, Accepted Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	APSL[2]	0
Bit 1	R	APSL[1]	0
Bit 0	R	APSL[0]	0

This set of registers reports the accepted path signal label of TU #2 in TUG2 #1 to TUG2 #7.

APSL[2:0]:

The APSL[2:0] bits reports the accepted path signal label of tributary TU #2 in TUG2 #1 to TUG2 #7. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

Register 0x0A44 + 0x100*N, 0x0A4C + 0x100*N, 0x0A54 + 0x100*N, 0x0A5C + 0x100*N, 0x0A64 + 0x100*N, 0x0A6C + 0x100*N, 0x0A74 + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 0x0A45 + 0x100*N, 0x0A4D + 0x100*N, 0x0A55 + 0x100*N, 0x0A5D + 0x100*N, 0x0A65 + 0x100*N, 0x0A6D + 0x100*N, 0x0A75 + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

These registers reports the number of block interleave parity (BIP-2) errors detected in TU #2 in TUG2 #1 to TUG2 #7 in the previous accumulation interval.

BIP[10:0]:

The BIP[10:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to the Master SONET/SDH Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2 registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 0x0A46 + 0x100*N, 0x0A4E + 0x100*N, 0x0A56 + 0x100*N, 0x0A5E + 0x100*N, 0x0A66 + 0x100*N, 0x0A6E + 0x100*N, 0x0A76 + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 0x0A47 + 0x100*N, 0x0A4F + 0x100*N, 0x0A57 + 0x100*N, 0x0A5F + 0x100*N, 0x0A67 + 0x100*N, 0x0A6F + 0x100*N, 0x0A77 + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers reports the number of far end block errors (FEBE) detected in TU #2 in TUG2 #1 to TUG2 #7 in the previous accumulation interval.

FEBE[10:0]:

The FEBE[10:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by writing to the Master SONET/SDH Accumulate Trigger registers. The write access transfers the internally accumulated error count to the FEBE registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 0x0A78 + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, COPSL Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	COPSL7I	0
Bit 5	R	COPSL6I	0
Bit 4	R	COPSL5I	0
Bit 3	R	COPSL4I	0
Bit 2	R	COPSL3I	0
Bit 1	R	COPSL2I	0
Bit 0	R	COPSL1I	0

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

COPSL1I-COPSL7I:

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. The COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSL*x*I bit is set to logic 1 when a change of PSL event on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSL*x*I remains valid when interrupts are not enabled (COPSLE set to logic 0) and may be polled to detect change of path signal label events.

Register 0x0A79 + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, PSLM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLM7I	0
Bit 5	R	PSLM6I	0
Bit 4	R	PSLM5I	0
Bit 3	R	PSLM4I	0
Bit 2	R	PSLM3I	0
Bit 1	R	PSLM2I	0
Bit 0	R	PSLM1I	0

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

PSLM1I-PSLM7I:

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. The PSLM1I to PSLM7I bits report and acknowledge PSLM interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLM*x*I bit is set to logic 1 when a change of PSL matched state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM*x*I remains valid when interrupts are not enabled (PSLME set to logic 0) and may be polled to detect path signal label match/mismatch events.

Register 0x0A7A + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, PSLU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLU7I	0
Bit 5	R	PSLU6I	0
Bit 4	R	PSLU5I	0
Bit 3	R	PSLU4I	0
Bit 2	R	PSLU3I	0
Bit 1	R	PSLU2I	0
Bit 0	R	PSLU1I	0

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

PSLU1I-PSLU7I:

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. The PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLU*x*I bit is set to logic 1 when a change of PSL unstable state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLU*x*I remains valid when interrupts are not enabled (PSLUE set to logic 0) and may be polled to detect path signal label stable/unstable events.

Register 0x0A7B + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, RDI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RDI7I	0
Bit 5	R	RDI6I	0
Bit 4	R	RDI5I	0
Bit 3	R	RDI4I	0
Bit 2	R	RDI3I	0
Bit 1	R	RDI2I	0
Bit 0	R	RDI1I	0

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

RDI1I-RDI7I:

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. The RDI1I to RDI7I bits report and acknowledge RDI interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDI*x*I bit is set to logic 1 when a change of RDI state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI*x*I remains valid when interrupts are not enabled (RDIE set to logic 0) and may be polled to detect change of remote defect indication events.

Register 0x0A7C + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, RFI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RFI7I	0
Bit 5	R	RFI6I	0
Bit 4	R	RFI5I	0
Bit 3	R	RFI4I	0
Bit 2	R	RFI3I	0
Bit 1	R	RFI2I	0
Bit 0	R	RFI1I	0

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

RFI1I-RFI7I:

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. The RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFI*x*I bit is set to logic 1 when a change of RFI state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI*x*I remains valid when interrupts are not enabled (RFIE set to logic 0) and may be polled to detect change of remote failure indication events.

Register 0x0A7D + 0x100*N: RTOP, TU #2 in TUG2 #1 to TUG2 #7, Inband Error Reporting Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	IBER7	0
Bit 5	R/W	IBER6	0
Bit 4	R/W	IBER5	0
Bit 3	R/W	IBER4	0
Bit 2	R/W	IBER3	0
Bit 1	R/W	IBER2	0
Bit 0	R/W	IBER1	0

This register enables the inband error reporting mode for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #2 in TUG2 #1 to TUG2 #7, respectively. Setting an IBER*x* bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #2 of the corresponding TUG2. When an IBER*x* bit is low, in band error reporting is disabled and the V5 byte of tributary TU #2 of the corresponding TUG2 is not modified.

Register 0x0A80 + 0x100*N, 0x0A88 + 0x100*N, 0x0A90 + 0x100*N, 0x0A98 + 0x100*N, 0x0AA0 + 0x100*N, 0x0AA8 + 0x100*N, 0x0AB0 + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, Configuration

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

This set of registers configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIE is set to logic 1, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set to logic 0. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set to logic 0 and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set to logic 1.

RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIZ7EN is set to logic 0, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set to logic 1. Interrupts due to RFIV status change are masked when RFIE is set to logic 0. When RDIZ7EN is set to logic 1, RFIE is ignored.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #3 in the corresponding TUG2. When COPSLE is set to logic 1, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set to logic 0.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #3 in the corresponding TUG2. When PSLME is set to logic 1, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set to logic 0.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #3 in the corresponding TUG2. When PSLUE is set to logic 1, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set to logic 0.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #3 in the corresponding TUG2. When BLKBIP is set to logic 1, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set to logic 0, the BIP error count is incremented once for each BIP-2 bit that is in error.

TU11:

The TU11 bit reports the tributary configuration of the corresponding TUG2. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0A81 + 0x100*N, 0x0A89 + 0x100*N, 0x0A91 + 0x100*N, 0x0A99 + 0x100*N, 0x0AA1 + 0x100*N, 0x0AA9 + 0x100*N, 0x0AB1 + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	Reserved	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

This set of registers reports alarm status and configures TU #3 in TUG2 #1 to TUG2 #7.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #3 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set to logic 1 when the RDI bit in the V5 byte is set to logic 1 for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register. RDIV is set to logic 0 when the RDI bit is set to logic 0 for five or ten consecutive multiframes as determined by the RDI10 bit

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #3 in the corresponding TUG2 when RDIZ7EN is set to logic 0. RFIV is set to logic 1 when the RFI bit in the V5 byte is set to logic 1 for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register. RFIV is set to logic 0 when the RFI bit is set to logic 0 for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #3 in the corresponding TUG2 when RDIZ7EN is set to logic 1. The ERDIV[2:0] bits are set to a new code when the same code in the

extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register.

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #3 in the corresponding TUG2. PSLMV is set to logic 1 when the accepted PSL differs from the provisioned value. PSLMV is set to logic 0 when the accepted PSL has the same value as the provisioned one. The PSL match/mismatch state is determined as follows:

Expected PSL	Accepted PSL	PSLM State
000	000	Match
000	001	Mismatch
000	XXX ≠ 000	Mismatch
001	000	Mismatch
001	001	Match
001	XXX ≠ 001	Match
XXX ≠ 000, 001	000	Mismatch
XXX ≠ 000, 001	001	Match
XXX ≠ 000, 001	XXX	Match
XXX ≠ 000, 001	YYY	Mismatch

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #3 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs form that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set to logic 1 when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set to logic 0 when the unstable counter is cleared.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #3 in the corresponding TUG2. TUPTE is set to logic 1 if tributary TU #3 is to be terminated in the network element containing this TEMUX 84 device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register. TUPTE is set to logic 0 if tributary TU #3 is part of the through traffic in the network element containing this TEMUX 84 device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #3 in the corresponding TUG2 . When RDIZ7EN is set to logic 0, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set to logic 1, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

Register 0x0A82 + 0x100*N, 0x0A8A + 0x100*N, 0x0A92 + 0x100*N, 0x0A9A + 0x100*N, 0x0AA2 + 0x100*N, 0x0AAA + 0x100*N, 0x0AB2 + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This set of registers configures the expected the path signal label of TU #3 in TUG2 #1 to TUG2 #7.

EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #3 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 0x0A83 + 0x100*N, 0x0A8B + 0x100*N, 0x0A93 + 0x100*N, 0x0A9B + 0x100*N, 0x0AA3 + 0x100*N, 0x0AAB + 0x100*N, 0x0AB3 + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, Accepted Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	APSL[2]	0
Bit 1	R	APSL[1]	0
Bit 0	R	APSL[0]	0

This set of registers reports the accepted the path signal label of TU #3 in TUG2 #1 to TUG2 #7.

APSL[2:0]:

The APSL[2:0] bits reports the accepted path signal label of tributary TU #3 in the corresponding TUG2. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

Register 0x0A84 + 0x100*N, 0x0A8C + 0x100*N, 0x0A94 + 0x100*N, 0x0A9C + 0x100*N, 0x0AA4 + 0x100*N, 0x0AAC + 0x100*N, 0x0AB4 + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 0x0A85 + 0x100*N, 0x0A8D + 0x100*N, 0x0A95 + 0x100*N, 0x0A9D + 0x100*N, 0x0AA5 + 0x100*N, 0x0AAD + 0x100*N, 0x0AB5 + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

These registers reports the number of block interleave parity (BIP-2) errors detected in TU #3 in TUG2 #1 to TUG2 #7 in the previous accumulation interval.

BIP[10:0]:

The BIP[10:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to the Master SONET/SDH Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2 registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 0x0A86 + 0x100*N, 0x0A8E + 0x100*N, 0x0A96 + 0x100*N, 0x0A9E + 0x100*N, 0x0AA6 + 0x100*N, 0x0AAE + 0x100*N, 0x0AB6 + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 0x0A87 + 0x100*N, 0x0A8F + 0x100*N, 0x0A97 + 0x100*N, 0x0A9F + 0x100*N, 0x0AA7 + 0x100*N, 0x0AAF + 0x100*N, 0x0AB7 + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers reports the number of far end block errors (FEBE) detected in TU #3 in TUG2 #1 to TUG2 #7 in the previous accumulation interval.

FEBE[10:0]:

The FEBE[10:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by writing to the Master SONET/SDH Accumulate Trigger register. The write access transfers the internally accumulated error count to the FEBE registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 0x0AB8 + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, COPSL Interrupt

Bit	Type	Function	Default
Bit 7		Reserved	X
Bit 6	R	COPSL7I	0
Bit 5	R	COPSL6I	0
Bit 4	R	COPSL5I	0
Bit 3	R	COPSL4I	0
Bit 2	R	COPSL3I	0
Bit 1	R	COPSL2I	0
Bit 0	R	COPSL1I	0

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

COPSL1I-COPSL7I:

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. The COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSL*x*I bit is set to logic 1 when a change of PSL event on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSL*x*I remains valid when interrupts are not enabled (COPSLE set to logic 0) and may be polled to detect change of path signal label events.

Reserved:

The Reserved bits must be written with a logic 0 for proper operation of the TUPP-PLUS.

Register 0x0AB9 + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, PSLM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLM7I	0
Bit 5	R	PSLM6I	0
Bit 4	R	PSLM5I	0
Bit 3	R	PSLM4I	0
Bit 2	R	PSLM3I	0
Bit 1	R	PSLM2I	0
Bit 0	R	PSLM1I	0

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

PSLM1I-PSLM7I:

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. The PSLM1I to PSLM7I bits report and acknowledge PSLM interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLM*x*I bit is set to logic 1 when a change of PSL matched state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM*x*I remains valid when interrupts are not enabled (PSLME set to logic 0) and may be polled to detect path signal label match/mismatch events.

Register 0x0ABA + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, PSLU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLU7I	0
Bit 5	R	PSLU6I	0
Bit 4	R	PSLU5I	0
Bit 3	R	PSLU4I	0
Bit 2	R	PSLU3I	0
Bit 1	R	PSLU2I	0
Bit 0	R	PSLU1I	0

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

PSLU1I-PSLU7I:

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. The PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLU*x*I bit is set to logic 1 when a change of PSL unstable state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLU*x*I remains valid when interrupts are not enabled (PSLUE set to logic 0) and may be polled to detect path signal label stable/unstable events.

Register 0x0ABB + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, RDI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RDI7I	0
Bit 5	R	RDI6I	0
Bit 4	R	RDI5I	0
Bit 3	R	RDI4I	0
Bit 2	R	RDI3I	0
Bit 1	R	RDI2I	0
Bit 0	R	RDI1I	0

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

RDI1I-RDI7I:

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. The RDI1I to RDI7I bits report and acknowledge RDI interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDI*x*I bit is set to logic 1 when a change of RDI state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI*x*I remains valid when interrupts are not enabled (RDIE set to logic 0) and may be polled to detect change of remote defect indication events.

Register 0x0ABC + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, RFI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RFI7I	0
Bit 5	R	RFI6I	0
Bit 4	R	RFI5I	0
Bit 3	R	RFI4I	0
Bit 2	R	RFI3I	0
Bit 1	R	RFI2I	0
Bit 0	R	RFI1I	0

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

RFI1I-RFI7I:

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. The RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFI*x*I bit is set to logic 1 when a change of RFI state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI*x*I remains valid when interrupts are not enabled (RFIE set to logic 0) and may be polled to detect change of remote failure indication events.

Register 0x0ABD + 0x100*N: RTOP, TU #3 in TUG2 #1 to TUG2 #7, Inband Error Reporting Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	IBER7	0
Bit 5	R/W	IBER6	0
Bit 4	R/W	IBER5	0
Bit 3	R/W	IBER4	0
Bit 2	R/W	IBER3	0
Bit 1	R/W	IBER2	0
Bit 0	R/W	IBER1	0

This register enables the inband error reporting mode for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #3 in TUG2 #1 to TUG2 #7, respectively. Setting an IBER*x* bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #3 of the corresponding TUG2. When an IBER*x* bit is low, in band error reporting is disabled and the V5 byte of tributary TU #3 of the corresponding TUG2 is not modified.

Register 0x0AC0 + 0x100*N, 0x0AC8 + 0x100*N, 0x0AD0 + 0x100*N, 0x0AD8 + 0x100*N, 0x0AE0 + 0x100*N, 0x0AE8 + 0x100*N, 0x0AF0 + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, Configuration

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

This set of registers configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #4 in the corresponding TUG2. When RDIZ7EN is set to logic 0, an interrupt is generated upon assertion and negation events of the RDIV bit when RDIE is set to logic 1. Interrupts due to RDIV status change are masked when RDIE is set to logic 0.

When RDIZ7EN is set to logic 1, an interrupt is generated upon assertion or negation events of the ERDIV[2:0] bits when RDIE is set to logic 1. Interrupts due to ERDIV[2:0] status change are masked when RDIE is set to logic 0.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #4 in the corresponding TUG2. When COPSLE is set to logic 1, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set to logic 0.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #4 in the corresponding TUG2. When PSLME is set to logic 1, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set to logic 0.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #4 in the corresponding TUG2. When PSLUE is set to logic 1, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set to logic 0.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #4 in the corresponding TUG2. When BLKBIP is set to logic 1, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set to logic 0, the BIP error count is incremented once for each BIP-2 bit that is in error.

TU11:

The TU11 bit reports the tributary configuration of the corresponding TUG2. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0AC1 + 0x100*N, 0x0AC9 + 0x100*N, 0x0AD1 + 0x100*N, 0x0AD9 + 0x100*N, 0x0AE1 + 0x100*N, 0x0AE9 + 0x100*N, 0x0AF1 + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	Reserved	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

This set of registers configures and reports the alarm status of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #4 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set to logic 1 when the RDI bit in the V5 byte is set to logic 1 for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register. RDIV is set to logic 0 when the RDI bit is set to logic 0 for five or ten consecutive multiframes as determined by the RDI10 bit

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #4 in the corresponding TUG2 when RDIZ7EN is set to logic 0. RFIV is set to logic 1 when the RFI bit in the V5 byte is set to logic 1 for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register. RFIV is set to logic 0 when the RFI bit is set to logic 0 for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #4 in the corresponding TUG2 when RDIZ7EN is set to logic 1.

The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register.

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #4 in the corresponding TUG2. PSLMV is set to logic 1 when the accepted PSL differs from the provisioned value. PSLMV is set to logic 0 when the accepted PSL has the same value as the provisioned one. The PSL match/mismatch state is determined as follows:

Expected PSL	Accepted PSL	PSLM State
000	000	Match
000	001	Mismatch
000	XXX ≠ 000	Mismatch
001	000	Mismatch
001	001	Match
001	XXX ≠ 001	Match
XXX ≠ 000, 001	000	Mismatch
XXX ≠ 000, 001	001	Match
XXX ≠ 000, 001	XXX	Match
XXX ≠ 000, 001	YYY	Mismatch

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #4 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs form that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set to logic 1 when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set to logic 0 when the unstable counter is cleared.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #4 in the corresponding TUG2. TUPTE is set to logic 1 if tributary TU #4 is to be terminated in the network element containing this TEMUX 84 device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register. TUPTE is set to logic 0 if tributary TU #4 is part of the through traffic in the network element containing this TEMUX 84 device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #4 in the corresponding TUG2 . When RDIZ7EN is set to logic 0, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set to logic 1, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

Register 0x0AC2 + 0x100*N, 0x0ACA + 0x100*N, 0x0AD2 + 0x100*N, 0x0ADA + 0x100*N, 0x0AE2 + 0x100*N, 0x0AEA + 0x100*N, 0x0AF2 + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This set of registers configures the expected path signal label of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #4 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 0x0AC3 + 0x100*N, 0x0ACB + 0x100*N, 0x0AD3 + 0x100*N, 0x0ADB + 0x100*N, 0x0AE3 + 0x100*N, 0x0AEB + 0x100*N, 0x0AF3 + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	APSL[2]	0
Bit 1	R	APSL[1]	0
Bit 0	R	APSL[0]	0

This set of register reports the accepted path signal label of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

APSL[2:0]:

The APSL[2:0] bits reports the accepted path signal label of tributary TU #4 in the corresponding TUG2. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

Register 0x0AC4 + 0x100*N, 0x0ACC + 0x100*N, 0x0AD4 + 0x100*N, 0x0ADC + 0x100*N, 0x0AE4 + 0x100*N, 0x0AEC + 0x100*N, 0x0AF4 + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 0x0AC5 + 0x100*N, 0x0ACD + 0x100*N, 0x0AD5 + 0x100*N, 0x0ADD + 0x100*N, 0x0AE5 + 0x100*N, 0x0AED + 0x100*N, 0x0AF5 + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

These registers reports the number of block interleave parity (BIP-2) errors detected in TU #4 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated registers in this set contain invalid data. These registers do not saturate.

BIP[10:0]:

The BIP[10:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2 registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 0x0AC6 + 0x100*N, 0x0ACE + 0x100*N, 0x0AD6 + 0x100*N, 0x0ADE + 0x100*N, 0x0AE6 + 0x100*N, 0x0AEE + 0x100*N, 0x0AF6 + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 0x0AC7 + 0x100*N, 0x0ACF + 0x100*N, 0x0AD7 + 0x100*N, 0x0ADF + 0x100*N, 0x0AE7 + 0x100*N, 0x0AEF + 0x100*N, 0x0AF7 + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers reports the number of far end block errors (FEBE) detected in TU #4 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated registers in this set contain invalid data.

FEBE[10:0]:

The FEBE[10:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the FEBE registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 0x0AF8 + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, COPSL Interrupt

Bit	Type	Function	Default
Bit 7		Unused	0
Bit 6	R	COPSL7I	0
Bit 5	R	COPSL6I	0
Bit 4	R	COPSL5I	0
Bit 3	R	COPSL4I	0
Bit 2	R	COPSL3I	0
Bit 1	R	COPSL2I	0
Bit 0	R	COPSL1I	0

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

COPSL1I-COPSL7I:

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated COPSL*x*I bit is unused and will return a logic 0 when read. When operational, the COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSL*x*I bit is set to logic 1 when a change of PSL event on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSL*x*I remains valid when interrupts are not enabled (COPSLE set to logic 0) and may be polled to detect change of path signal label events.

Register 0x0AF9 + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, PSLM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLM7I	0
Bit 5	R	PSLM6I	0
Bit 4	R	PSLM5I	0
Bit 3	R	PSLM4I	0
Bit 2	R	PSLM3I	0
Bit 1	R	PSLM2I	0
Bit 0	R	PSLM1I	0

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

PSLM1I-PSLM7I:

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated PSLM*x*I bit is unused and will return a logic 0 when read. When operational, the PSLM1I to PSLM7I bits report and acknowledge PSLM interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLM*x*I bit is set to logic 1 when a change of PSL matched state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM*x*I remains valid when interrupts are not enabled (PSLME set to logic 0) and may be polled to detect path signal label match/mismatch events.

Register 0x0AFA + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, PSLU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLU7I	0
Bit 5	R	PSLU6I	0
Bit 4	R	PSLU5I	0
Bit 3	R	PSLU4I	0
Bit 2	R	PSLU3I	0
Bit 1	R	PSLU2I	0
Bit 0	R	PSLU1I	0

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

PSLU1I-PSLU7I:

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated PSLU*x*I bit is unused and will return a logic 0 when read. When operational, the PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLU*x*I bit is set to logic 1 when a change of PSL unstable state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLU*x*I remains valid when interrupts are not enabled (PSLUE set to logic 0) and may be polled to detect path signal label stable/unstable events.

Register 0x0AFB + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, RDI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RDI7I	0
Bit 5	R	RDI6I	0
Bit 4	R	RDI5I	0
Bit 3	R	RDI4I	0
Bit 2	R	RDI3I	0
Bit 1	R	RDI2I	0
Bit 0	R	RDI1I	0

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

RDI1I-RDI7I:

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated RDI*x*I bit is unused and will return a logic 0 when read. When operational, the RDI1I to RDI7I bits report and acknowledge RDI interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDI*x*I bit is set to logic 1 when a change of RDI state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI*x*I remains valid when interrupts are not enabled (RDIE set to logic 0) and may be polled to detect change of remote defect indication events.

Register 0x0AFC + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, RFI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RFI7I	0
Bit 5	R	RFI6I	0
Bit 4	R	RFI5I	0
Bit 3	R	RFI4I	0
Bit 2	R	RFI3I	0
Bit 1	R	RFI2I	0
Bit 0	R	RFI1I	0

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

RFI1I-RFI7I:

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated RFI*x*I bit is unused and will return a logic 0 when read. When operational, the RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFI*x*I bit is set to logic 1 when a change of RFI state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI*x*I remains valid when interrupts are not enabled (RFIE set to logic 0) and may be polled to detect change of remote failure indication events.

Register 0x0AFD + 0x100*N: RTOP, TU #4 in TUG2 #1 to TUG2 #7, Inband Error Reporting Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	IBER7	0
Bit 5	R/W	IBER6	0
Bit 4	R/W	IBER5	0
Bit 3	R/W	IBER4	0
Bit 2	R/W	IBER3	0
Bit 1	R/W	IBER2	0
Bit 0	R/W	IBER1	0

This register enables the inband error reporting mode for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #4 in TUG2 #1 to TUG2 #7, respectively. Setting an IBER*x* bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #4 of the corresponding TUG2. When an IBER*x* bit is low, in band error reporting is disabled and the V5 byte of tributary TU #4 of the corresponding TUG2 is not modified.

1.44 TRAP Transmit Alarm Processor Registers

TRAP Control Registers

TU Address Map:

TUG3	TUG2	TU #1	TU #2	TU #3	TU #4
1	1	0xD00	0xD08	0xD10	0xD18
1	2	0xD01	0xD09	0xD11	0xD19
1	3	0xD02	0xD0A	0xD12	0xD1A
1	4	0xD03	0xD0B	0xD13	0xD1B
1	5	0xD04	0xD0C	0xD14	0xD1C
1	6	0xD05	0xD0D	0xD15	0xD1D
1	7	0xD06	0xD0E	0xD16	0xD1E
2	1	0xD20	0xD28	0xD30	0xD38
2	2	0xD21	0xD29	0xD31	0xD39
2	3	0xD22	0xD2A	0xD32	0xD3A
2	4	0xD23	0xD2B	0xD33	0xD3B
2	5	0xD24	0xD2C	0xD34	0xD3C
2	6	0xD25	0xD2D	0xD35	0xD3D
2	7	0xD26	0xD2E	0xD36	0xD3E
3	1	0xD40	0xD48	0xD50	0xD58
3	2	0xD41	0xD49	0xD51	0xD59
3	3	0xD42	0xD4A	0xD52	0xD5A
3	4	0xD43	0xD4B	0xD53	0xD5B
3	5	0xD44	0xD4C	0xD54	0xD5C
3	6	0xD45	0xD4D	0xD55	0xD5D
3	7	0xD46	0xD4E	0xD56	0xD5E

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	ARDI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of the incoming/outgoing egress data stream.

POHDIS:

The POHDIS bit controls the modification of the egress tributary path overhead bytes. When POHDIS is set to logic 1, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set to logic 0, the tributary path overhead is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding. When ERDI is set to logic 1, extended RDI is selected. The RDI and ARDI indications are treated as a 2-bit codepoint. The RDI indication will be inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte and the ARDI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set to logic 0, normal RDI is selected. The RDI bit value will be inserted into bit 8 of the V5 byte and the ARDI bit will be ignored. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the egress RDI indication. When FORCEEN is set to logic 1, the RDI and ARDI indications are controlled directly by the RDI and ARDI register bits. When FORCEEN is set to logic 0, the RDI and ARDI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

ARDI:

The ARDI bit controls the value of the egress Auxiliary RDI indication. When FORCEEN is set to logic 1, the RDI and ARDI indications are controlled directly by the RDI and ARDI register bits. When FORCEEN is set to logic 0, the RDI and ARDI Indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the ARDI and RDI register bits controls the RDI and ARDI indications. When FORCEEN is high the RDI and ARDI indications are controlled directly by the RDI and ARDI register bits. When FORCEEN is set to logic 0 the RDI and ARDI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

TRAP Egress AIS Control Registers

TU Address Map:

TUG3	TUG2	TU #1	TU #2	TU #3	TU #4
1	1-7	0xD07	0xD0F	0xD17	0xD1F
2	1-7	0xD27	0xD2F	0xD37	0xD3F
3	1-7	0xD47	0xD4F	0xD57	0xD5F

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EAIS7	0
Bit 5	R/W	EAIS6	0
Bit 4	R/W	EAIS5	0
Bit 3	R/W	EAIS4	0
Bit 2	R/W	EAIS3	0
Bit 1	R/W	EAIS2	0
Bit 0	R/W	EAIS1	0

EAIS7 – EAIS1:

The EAIS1 to EAIS7 bits control the state of the AIS insertion when tributary TUG2 #1 to TUG2 #7, respectively, are on the egress data stream. When EAIS*x* is set to logic 1, tributary path AIS is inserted in the associated tributary of the egress data stream. When EAIS*x* is set to logic 0, tributary path AIS is not forced in the associated tributary of the egress data stream although tributary path AIS may still be inserted due to other alarm conditions.

Register 0x0D60: TRAP Indirect Remote Alarm Page Address

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6	R/W	RWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RASEL[1]	0
Bit 0	R/W	RASEL[0]	0

This register selects the remote alarm port page used to access the ARBITER look-up table used to select which incoming alarm source is used to generate an egress RDI, ERDI or REI. **Writing to this register triggers an indirect look-up table access.**

RASEL[1:0]:

The RASEL[1:0] bits indexes into one of three pages in the ARBITER look-up table. The pages specified by the RASEL[1:0] bits are selected as follows:

RASEL[1]	RASEL[0]	Remote Alarm Source
0	0	Reserved
0	1	RADEAST Serial Alarm Port
1	0	RADWEST Serial Alarm Port
1	1	RTOP Ingress Data

The priority of the remote alarm source when mapping to an egress alarm indication is the RTOP Ingress data then RADEAST followed by RADWEST. In order for a lower priority alarm source to be selected over a higher priority alarm, the higher priority alarm port entry must be disabled by writing an invalid entry via the TRAP Indirect Datapath Tributary Data register.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the ARBITER look-up table. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the Indirect Datapath Tributary Data register. Writing a logic one to RWB triggers an indirect read operation. The read can be found in the Indirect Datapath Tributary Data register.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when a write to the Indirect Remote Alarm Port Select register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Datapath Tributary Select Data register or to determine when a new indirect write operation may commence. If LREFCLK disappears during an access, the BUSY bit can stay high.

Register 0x0D61: TRAP Indirect Remote Alarm Tributary Address

Bit	Type	Function	Default
Bit 7	R/W	RTUG3[1]	0
Bit 6	R/W	RTUG3[0]	0
Bit 5	R/W	RTUG2[2]	0
Bit 4	R/W	RTUG2[1]	0
Bit 3	R/W	RTUG2[0]	0
Bit 2	R/W	RTU[2]	0
Bit 1	R/W	RTU[1]	0
Bit 0	R/W	RTU[0]	0

This register provides the remote alarm tributary number used to access the ARBITER look-up table.

RTU[2:0]:

The indirect remote alarm tributary unit bits (RTU[2:0]) indicate the tributary unit to be configured or interrogated in the indirect access. Legal RTU[2:0] ranges are ‘b001 to ‘b100.

RTUG2[2:0]:

The indirect remote alarm tributary unit group 2 bits (RTUG2[2:0]) indicate the tributary unit group 2 to be configured or interrogated in the indirect access. Legal RTUG2[2:0] ranges are ‘b001 to ‘b111.

RTUG3[1:0]:

The indirect remote alarm tributary unit group 3 bits (RTUG2[1:0]) indicate the tributary unit group 3 to be configured or interrogated in the indirect access. Legal RTUG3[1:0] ranges are ‘b01 to ‘b11.

Register 0x0D62: TRAP Indirect Datapath Tributary Data

Bit	Type	Function	Default
Bit 7	R/W	DTUG3[1]	0
Bit 6	R/W	DTUG3[0]	0
Bit 5	R/W	DTUG2[2]	0
Bit 4	R/W	DTUG2[1]	0
Bit 3	R/W	DTUG2[0]	0
Bit 2	R/W	DTU[2]	0
Bit 1	R/W	DTU[1]	0
Bit 0	R/W	DTU[0]	0

This register contains data read from the ARBITER look-up tables after an indirect channel read operation or data to be inserted into the ARBITER look-up table in an indirect channel write operation.

Please note that if a particular datapath tributary is not mapped to a remote alarm tributary, as set by via Register D61H: TRAP Indirect Remote Alarm Tributary, it is recommended the desired alarm values be set manually. This can be accomplished using the FORCEEN bit in theTRAP TU Control registers.

DTU[1:0]:

The indirect datapath tributary unit bits (DTU[2:0]) specifies the tributary number of the datapath tributary that is associated with the remote alarm tributary specified in the Indirect Remote Alarm Page Address register and the Indirect Remote Alarm Tributary Address register. In an indirect write operation, the datapath tributary number to be written to the ARBITER look-up table must be set up in this register before triggering the indirect write. When read back, DTU[2:0] reflects the value written until the completion of a subsequent indirect channel read operation. Normal DTU[2:0] ranges are ‘b001 to ‘b100. Values outside of this range disable the remote alarm tributary specified in the Indirect Remote Alarm Page Address register and the Indirect Remote Alarm Tributary Address register from being associated with a datapath tributary.

DTUG2[2:0]:

The indirect datapath tributary unit group 2 bits (DTUG2[2:0]) specifies the tributary unit group 2 number of the datapath tributary that is associated with the remote alarm tributary specified in the Indirect Remote Alarm Page Address register and the Indirect Remote Alarm Tributary Address register. In an indirect write operation, the datapath tributary unit 2 number to be written to the ARBITER look-up table must be set up in this register before triggering the indirect write. When read back, DTUG2[2:0] reflects the value written until the completion of a subsequent indirect channel read operation. Legal DTUG2[2:0] ranges are ‘b001 to ‘b111.

DTUG3[1:0]:

The indirect datapath tributary unit group 3 bits (DTUG3[2:0]) specifies the tributary unit group 3 number of the datapath tributary that is associated with the remote alarm tributary specified in the Indirect Remote Alarm Page Address register and the Indirect Remote Alarm Tributary Address register. In an indirect write operation, the datapath tributary unit 3 number to be written to the ARBITER look-up table must be set up in this register before triggering the indirect write. When read back, DTUG2[1:0] reflects the value written until the completion of a subsequent indirect channel read operation. Legal DTUG3[1:0] ranges are ‘b01 to ‘b11.

Register 0x0D63: TRAP RDI Control

Bit	Type	Function	Default
Bit 7	R/W	RDIPRIA[1]	0
Bit 6	R/W	RDIPRIA[0]	0
Bit 5	R/W	RDIPRIB[1]	0
Bit 4	R/W	RDIPRIB[0]	0
Bit 3		Unused	X
Bit 2	R/W	RDI20MF[3]	0
Bit 1	R/W	RDI20MF[2]	0
Bit 0	R/W	RDI20MF[1]	0

This register allows configuration of two-bit alarm code point priority in ERDI for all tributaries. Also configures the maintenance of RDI for each TUG3.

RDI20MF[3:1]

The RDI20MF[3:1] bits specify the configuration of RDI maintenance duration for each of the three TUG3s. The standard required duration is 10 multiframes. The GR-253 objective duration is 20 multiframes. RDI20MF[X] controls the configuration of TUG3 #X. The two options for each TUG3 specified by the RDI20MF[3:1] bits are selected as follows:

RDI20MF[X]	Configuration
0	A particular RDI value for TUG3 #X will be maintained for the required 10 multiframes.
1	A particular RDI value for TUG3 #X will be maintained for the GR-253 objective 20 multiframes.

RDIPRIA[1:0]

The RDIPRIA[1:0] bits specify which two-bit alarm code point will be treated as the highest priority code. High priority codes will replace low priority codes at the next V5 byte, instead of allowing 10/20 copies to be sent. The highest priority alarm is sent 10/20 times before replacement is allowed.

RDIPRIB[1:0]

The RDIPRIB[1:0] bits specify which two-bit alarm code point will be treated as the second highest priority code. These bits combined with the RDIPRIA[1:0] bits allow almost any priority scheme to be specified. The bits are interpreted as follows:

RDIPRIA[1:0]	RDIPRIB[1:0]	Priority of Codes (3 = highest)	
		Code	Priority
00	00	11	1
00	00	10	1
00	00	01	1
00	00	00	0
00	01	01	2
01	00	11	1
01	01	10	1
01	01	00	0
00	10	10	2
10	00	11	1
10	10	01	1
10	10	00	0
00	11	11	2
11	00	10	1
11	11	01	1
11	11	00	0
11	01	11	3
11	01	01	2
11	01	10	1
11	01	00	0
11	10	11	3
11	10	10	2
11	10	01	1
11	10	00	0

RDIPRIA[1:0]	RDIPRIB[1:0]	Priority of Codes (3 = highest)	
		Code	Priority
10	11	10	3
10	11	11	2
10	11	01	1
10	11	00	0
10	01	10	3
10	01	01	2
10	01	10	1
10	01	00	0
01	11	01	3
01	11	11	2
01	11	10	1
01	11	00	0
01	10	01	3
01	10	10	2
01	10	01	1
01	10	00	0

Register 0x0D68: TRAP Remote Parallel Alarm Port TUG2 #1 of TUG3 #1 Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register configures the operational modes of TUG2 #1, TUG3 #1 in the RTOP ingress data alarm port.

TU11:

The TU11 bit specifies the tributary configuration of tributary group TUG2 #1, TUG3 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0D69, 0x0D6A, 0x0D6B, 0x0D6C, 0x0D6D, 0x0D6E: TRAP Remote Parallel Alarm Port TUG2 #2 to TUG2 #7 of TUG3 #1 Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register configures the operational modes of TUG2 #2, TUG3 #1 to TUG2 #7, TUG3 #1 in the RTOP ingress data alarm port.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0D70, 0x0D71, 0x0D72, 0x0D73, 0x0D74, 0x0D75, 0x0D76: TRAP Remote Parallel Alarm Port TUG2 #1 to TUG2 #7 of TUG3 #2 Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register configures the operational modes of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2 in the RTOP ingress data alarm port.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #2. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0D78, 0x0D79, 0x0D7A, 0x0D7B, 0x0D7C, 0x0D7D, 0x0D7E: TRAP Remote Parallel Alarm Port TUG2 #1 to TUG2 #7 of TUG3 #3 Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register configures the operational modes of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3 in the RTOP ingress data alarm port.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #3. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

1.45 TTOP Transmit Tributary Path Overhead Processor Registers

Register 0x0D80: TTOP TU #1 in TUG2 #1 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #1 of TUG2 #1, TUG3 #1.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #1 of TUG2 #1, TUG3 #1. When IDLE is set to logic 1, the egress tributary payload bytes (excludes V1-V5, J2, Z6 and Z7) are set to all-zeros or all-ones as selected by the ICODE register bit in the TTOP TUG3 #1 Control register at address 0x0DE0. The outgoing active offset is forced to zero. When IDLE is set to logic 0, tributary TU #1 of TUG2 #1, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #1 of TUG2 #1, TUG3 #1. When ERDI is set to logic 1, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value of the ARDI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set to logic 0. When ERDI is set to logic 0, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. Bit 4 of the V5 byte is set to logic 0.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #1 of TUG2 #1, TUG3 #1. When TTIEN is set to logic 1, trail trace identifier

insertion is enabled. When TTIEN is set to logic 0, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #1 of TUG2 #1, TUG3 #1. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of ‘b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 bit specifies the tributary configuration of tributary group TUG2 #1, TUG3 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0D81, 0x0D82, 0x0D83, 0x0D84, 0x0D85, 0x0D86: TTOP TU #1 in TUG2 #2 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #1 of TUG2 #2, TUG3 #1 to TU #1 of TUG2 #7, TUG3 #1.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #1 in the corresponding TUG2, TUG3 #1. When IDLE is set to logic 1, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set to logic 0, tributary TU #1 in the corresponding TUG2, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #1 in the corresponding TUG2, TUG3 #1. When ERDI is set to logic 1, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the ARDI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set to logic 0. When ERDI is set to logic 0, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. Bit 4 of the V5 byte is set to logic 0.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #1 in the corresponding TUG2, TUG3 #1. When TTIEN is set to logic 1, trail trace identifier insertion is enabled. When TTIEN is set to logic 0, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #1 in the corresponding TUG2, TUG3 #1. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0D87: TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #1 BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #1 of TUG2 #1, TUG3 #1 to TU#1 of TUG2 #7, TUG3 #1.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #1 of TUG2 #1, TUG3 #1 to TUG2 #7, TUG3 #1, respectively. When DBIP*x* is set to logic 1, the inverted BIP-2 code will be inserted into the V5 byte of TU #1 of the corresponding TUG2. When DBIP*x* is set to logic 0, the normal BIP-2 code will be inserted.

Register 0x0D88, 0x0D89, 0x0D8A, 0x0D8B, 0x0D8C, 0x0D8D, 0x0D8E: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #2 of TUG2 #1, TUG3 #1 to TU #2 of TUG2 #7, TUG3 #1.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #2 in the corresponding TUG2, TUG3 #1. When IDLE is set to logic 1, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set to logic 0, tributary TU #2 in the corresponding TUG2, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #2 in the corresponding TUG2, TUG3 #1. When ERDI is set to logic 1, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the ARDI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set to logic 0. When ERDI is set to logic 0, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. Bit 4 of the V5 byte is set to logic 0.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #2 in the corresponding TUG2, TUG3 #1. When TTIEN is set to logic 1, trail trace identifier insertion is enabled. When TTIEN is set to logic 0, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #2 in the corresponding TUG2, TUG3 #1. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0D8F: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1 BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #2 of TUG2 #1, TUG3 #1 to TU#2 of TUG2 #7, TUG3 #1.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #2 of TUG2 #1, TUG3 #1 to TUG2 #7, TUG3 #1, respectively. When DBIP*x* is set to logic 1, the inverted BIP-2 code will be inserted into the V5 byte of TU #2 of the corresponding TUG2. When DBIP*x* is set to logic 0, the normal BIP-2 code will be inserted.

Register 0x0D90, 0x0D91, 0x0D92, 0x0D93, 0x0D94, 0x0D95, 0x0D96: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #3 of TUG2 #1, TUG3 #1 to TU #3 of TUG2 #7, TUG3 #1.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #3 in the corresponding TUG2, TUG3 #1. When IDLE is set to logic 1, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set to logic 0, tributary TU #3 in the corresponding TUG2, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #3 in the corresponding TUG2, TUG3 #1. When ERDI is set to logic 1, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the ARDI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set to logic 0. When ERDI is set to logic 0, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. Bit 4 of the V5 byte is set to logic 0.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #3 in the corresponding TUG2, TUG3 #1. When TTIEN is set to logic 1, trail trace identifier insertion is enabled. When TTIEN is set to logic 0, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #3 in the corresponding TUG2, TUG3 #1. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0D97: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #3 of TUG2 #1, TUG3 #1 to TU#3 of TUG2 #7, TUG3 #1.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #3 of TUG2 #1, TUG3 #1 to TUG2 #7, TUG3 #1, respectively. When DBIP*x* is set to logic 1, the inverted BIP-2 code will be inserted into the V5 byte of TU #3 of the corresponding TUG2. When DBIP*x* is set to logic 0, the normal BIP-2 code will be inserted.

Register 0x0D98, 0x0D99, 0x0D9A, 0x0D9B, 0x0D9C, 0x0D9D, 0x0D9E: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #4 of TUG2 #1, TUG3 #1 to TU #4 of TUG2 #7, TUG3 #1. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #4 in the corresponding TUG2, TUG3 #1. When IDLE is set to logic 1, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set to logic 0, tributary TU #4 in the corresponding TUG2, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #4 in the corresponding TUG2, TUG3 #1. When ERDI is set to logic 1, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the ARDI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set to logic 0. When ERDI is set to logic 0, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. Bit 4 of the V5 byte is set to logic 0.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #4 in the corresponding TUG2, TUG3 #1. When TTIEN is set to logic 1, trail trace identifier insertion is enabled. When TTIEN is set to logic 0, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #4 in the corresponding TUG2, TUG3 #1. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0D9F: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #4 of TUG2 #1, TUG3 #1 to TU#4 of TUG2 #7, TUG3 #1. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, this register has no effect.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #4 of TUG2 #1, TUG3 #1 to TUG2 #7, TUG3 #1, respectively. When DBIP*x* is set to logic 1, the inverted BIP-2 code will be inserted into the V5 byte of TU #4 of the corresponding TUG2. When DBIP*x* is set to logic 0, the normal BIP-2 code will be inserted.

Register 0x0DA0, 0x0DA1, 0x0DA2, 0x0DA3, 0x0DA4, 0x0DA5, 0x0DA6: TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #1 of TUG2 #2, TUG3 #2 to TU #1 of TUG2 #7, TUG3 #2.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #1 in the corresponding TUG2, TUG3 #2. When IDLE is set to logic 1, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set to logic 0, tributary TU #1 in the corresponding TUG2, TUG3 #2 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #1 in the corresponding TUG2, TUG3 #2. When ERDI is set to logic 1, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the ARDI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set to logic 0. When ERDI is set to logic 0, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. Bit 4 of the V5 byte is set to logic 0.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #1 in the corresponding TUG2, TUG3 #2. When TTIEN is set to logic 1, trail trace identifier insertion is enabled. When TTIEN is set to logic 0, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #1 in the corresponding TUG2, TUG3 #2. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #2. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0DA7: TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #1 of TUG2 #1, TUG3 #2 to TU#1 of TUG2 #7, TUG3 #2.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #1 of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2, respectively. When DBIP*x* is set to logic 1, the inverted BIP-2 code will be inserted into the V5 byte of TU #1 of the corresponding TUG2. When DBIP*x* is set to logic 0, the normal BIP-2 code will be inserted.

Register 0x0DA8, 0x0DA9, 0x0DAA, 0x0DAB, 0x0DAC, 0x0DAD, 0x0DAE: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #2 of TUG2 #1, TUG3 #2 to TU #2 of TUG2 #7, TUG3 #2.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #2 in the corresponding TUG2, TUG3 #2. When IDLE is set to logic 1, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set to logic 0, tributary TU #2 in the corresponding TUG2, TUG3 #2 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #2 in the corresponding TUG2, TUG3 #2. When ERDI is set to logic 1, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the ARDI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set to logic 0. When ERDI is set to logic 0, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. Bit 4 of the V5 byte is set to logic 0.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #2 in the corresponding TUG2, TUG3 #2. When TTIEN is set to logic 1, trail trace identifier insertion is enabled. When TTIEN is set to logic 0, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #2 in the corresponding TUG2, TUG3 #2. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0DAF: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #2 of TUG2 #1, TUG3 #2 to TU#1 of TUG2 #7, TUG3 #2.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #2 of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2, respectively. When DBIP*x* is set to logic 1, the inverted BIP-2 code will be inserted into the V5 byte of TU #2 of the corresponding TUG2. When DBIP*x* is set to logic 0, the normal BIP-2 code will be inserted.

Register 0x0DB0, 0x0DB1, 0x0DB2, 0x0DB3, 0x0DB4, 0x0DB5, 0x0DB6: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #3 of TUG2 #1, TUG3 #2 to TU #3 of TUG2 #7, TUG3 #2.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #3 in the corresponding TUG2, TUG3 #2. When IDLE is set to logic 1, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set to logic 0, tributary TU #3 in the corresponding TUG2, TUG3 #2 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #3 in the corresponding TUG2, TUG3 #2. When ERDI is set to logic 1, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the ARDI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set to logic 0. When ERDI is set to logic 0, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. Bit 4 of the V5 byte is set to logic 0.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #3 in the corresponding TUG2, TUG3 #2. When TTIEN is set to logic 1, trail trace identifier insertion is enabled. When TTIEN is set to logic 0, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #3 in the corresponding TUG2, TUG3 #2. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0DB7: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #3 of TUG2 #1, TUG3 #2 to TU#1 of TUG2 #7, TUG3 #2.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #3 of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2, respectively. When DBIP*x* is set to logic 1, the inverted BIP-2 code will be inserted into the V5 byte of TU #3 of the corresponding TUG2. When DBIP*x* is set to logic 0, the normal BIP-2 code will be inserted.

Register 0x0DB8, 0x0DB9, 0x0DBA, 0x0DBB, 0x0DBC, 0x0DBD, 0x0DBE: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #4 of TUG2 #1, TUG3 #2 to TU #4 of TUG2 #7, TUG3 #2. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #4 in the corresponding TUG2, TUG3 #2. When IDLE is set to logic 1, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set to logic 0, tributary TU #4 in the corresponding TUG2, TUG3 #2 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #4 in the corresponding TUG2, TUG3 #2. When ERDI is set to logic 1, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the ARDI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set to logic 0. When ERDI is set to logic 0, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. Bit 4 of the V5 byte is set to logic 0.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #4 in the corresponding TUG2, TUG3 #2. When TTIEN is set to logic 1, trail trace identifier insertion is enabled. When TTIEN is set to logic 0, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #4 in the corresponding TUG2, TUG3 #2. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0DBF: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #4 of TUG2 #1, TUG3 #2 to TU#1 of TUG2 #7, TUG3 #2. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, this register has no effect.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #4 of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2, respectively. When DBIP*x* is set to logic 1, the inverted BIP-2 code will be inserted into the V5 byte of TU #4 of the corresponding TUG2. When DBIP*x* is set to logic 0, the normal BIP-2 code will be inserted.

Register 0x0DC0, 0x0DC1, 0x0DC2, 0x0DC3, 0x0DC4, 0x0DC5, 0x0DC6: TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #1 of TUG2 #2, TUG3 #3 to TU #1 of TUG2 #7, TUG3 #3.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #1 in the corresponding TUG2, TUG3 #3. When IDLE is set to logic 1, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set to logic 0, tributary TU #1 in the corresponding TUG2, TUG3 #3 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #1 in the corresponding TUG2, TUG3 #3. When ERDI is set to logic 1, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the ARDI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set to logic 0. When ERDI is set to logic 0, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. Bit 4 of the V5 byte is set to logic 0.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #1 in the corresponding TUG2, TUG3 #3. When TTIEN is set to logic 1, trail trace identifier insertion is enabled. When TTIEN is set to logic 0, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #1 in the corresponding TUG2, TUG3 #3. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #3. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0DC7: TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #1 of TUG2 #1, TUG3 #3 to TU#1 of TUG2 #7, TUG3 #3.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #1 of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3, respectively. When DBIP*x* is set to logic 1, the inverted BIP-2 code will be inserted into the V5 byte of TU #1 of the corresponding TUG2. When DBIP*x* is set to logic 0, the normal BIP-2 code will be inserted.

Register 0x0DC8, 0x0DC9, 0x0DCA, 0x0DCB, 0x0DCC, 0x0DCD, 0x0DCE: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #2 of TUG2 #1, TUG3 #3 to TU #2 of TUG2 #7, TUG3 #3.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #2 in the corresponding TUG2, TUG3 #3. When IDLE is set to logic 1, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set to logic 0, tributary TU #2 in the corresponding TUG2, TUG3 #3 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #2 in the corresponding TUG2, TUG3 #3. When ERDI is set to logic 1, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the ARDI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set to logic 0. When ERDI is set to logic 0, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. Bit 4 of the V5 byte is set to logic 0.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #2 in the corresponding TUG2, TUG3 #3. When TTIEN is set to logic 1, trail trace identifier insertion is enabled. When TTIEN is set to logic 0, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #2 in the corresponding TUG2, TUG3 #3. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0DCF: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #2 of TUG2 #1, TUG3 #3 to TU#1 of TUG2 #7, TUG3 #3.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #2 of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3, respectively. When DBIP*x* is set to logic 1, the inverted BIP-2 code will be inserted into the V5 byte of TU #2 of the corresponding TUG2. When DBIP*x* is set to logic 0, the normal BIP-2 code will be inserted.

Register 0x0DD0, 0x0DD1, 0x0DD2, 0x0DD3, 0x0DD4, 0x0DD5, 0x0DD6: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #3 of TUG2 #1, TUG3 #3 to TU #3 of TUG2 #7, TUG3 #3.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #3 in the corresponding TUG2, TUG3 #3. When IDLE is set to logic 1, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set to logic 0, tributary TU #3 in the corresponding TUG2, TUG3 #3 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #3 in the corresponding TUG2, TUG3 #3. When ERDI is set to logic 1, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the ARDI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set to logic 0. When ERDI is set to logic 0, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. Bit 4 of the V5 byte is set to logic 0.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #3 in the corresponding TUG2, TUG3 #3. When TTIEN is set to logic 1, trail trace identifier insertion is enabled. When TTIEN is set to logic 0, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #3 in the corresponding TUG2, TUG3 #3. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0DD7: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #3 of TUG2 #1, TUG3 #3 to TU#1 of TUG2 #7, TUG3 #3

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #3 of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3, respectively. When DBIP*x* is set to logic 1, the inverted BIP-2 code will be inserted into the V5 byte of TU #3 of the corresponding TUG2. When DBIP*x* is set to logic 0, the normal BIP-2 code will be inserted.

Register 0x0DD8, 0x0DD9, 0x0DDA, 0x0DDB, 0x0DDC, 0x0DDD, 0x0DDE: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #4 of TUG2 #1, TUG3 #3 to TU #4 of TUG2 #7, TUG3 #3. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #4 in the corresponding TUG2, TUG3 #3. When IDLE is set to logic 1, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set to logic 0, tributary TU #4 in the corresponding TUG2, TUG3 #3 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #4 in the corresponding TUG2, TUG3 #3. When ERDI is set to logic 1, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the ARDI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set to logic 0. When ERDI is set to logic 0, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. Bit 4 of the V5 byte is set to logic 0.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #4 in the corresponding TUG2, TUG3 #3. When TTIEN is set to logic 1, trail trace identifier insertion is enabled. When TTIEN is set to logic 0, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #4 in the corresponding TUG2, TUG3 #3. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMUX 84.

Register 0x0DDF: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #4 of TUG2 #1, TUG3 #3 to TU#1 of TUG2 #7, TUG3 #3. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, this register has no effect

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #4 of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3, respectively. When DBIP*x* is set to logic 1, the inverted BIP-2 code will be inserted into the V5 byte of TU #4 of the corresponding TUG2. When DBIP*x* is set to logic 0, the normal BIP-2 code will be inserted.

Register 0x0DE0: TTOP TUG3 #1 Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	UPOHV	0
Bit 0	R/W	ICODE	0

This register contains control bits that are applicable to all tributaries in TUG3 #1.

ICODE:

The ICODE bit controls the value of the tributary payload bytes inserted into payload bytes of idle tributaries in TUG3 #1. When ICODE is set to logic 1, the tributary payload of an idle tributary (the corresponding IDLE bit set to logic 1) is set to all-ones. When ICODE is set to logic 0, the tributary payload is set to all-zeros.

UPOHV:

The UPOHV bit controls the value inserted into unused bits in tributary path overhead bytes of tributaries in TUG3 #1. When UPOHV is set to logic 1, unused tributary path overhead bits are set to logic 1. When UPOHV is set to logic 0, unused tributary path overhead bits are set to logic 0. Unused tributary POH bits include the J2 byte when trail trace identifier insertion is disabled (TTIEN set to logic 0), all bits in the Z6 byte, and bits 1, 2, 3, and 4 and 8 of the Z7 byte when extended RDI is enabled (ERDI set to logic 1) and all the bits of the Z7 byte when extended RDI is disabled (ERDI set to logic 0).

Register 0x0DE1: TTOP TUG3 #2 Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	UPOHV	0
Bit 0	R/W	ICODE	0

This register contains control bits that are applicable to all tributaries in TUG3 #2.

ICODE:

The ICODE bit controls the value of the tributary payload bytes inserted into payload bytes of idle tributaries in TUG3 #1. When ICODE is set to logic 1, the tributary payload of an idle tributary (the corresponding IDLE bit set to logic 1) is set to all-ones. When ICODE is set to logic 0, the tributary payload is set to all-zeros.

UPOHV:

The UPOHV bit controls the value inserted into unused bits in tributary path overhead bytes of tributaries in TUG3 #2. When UPOHV is set to logic 1, unused tributary path overhead bits are set to logic 1. When UPOHV is set to logic 0, unused tributary path overhead bits are set to logic 0. Unused tributary POH bits include the J2 byte when trail trace identifier insertion is disabled (TTIEN set to logic 0), all bits in the Z6 byte, bits 1, 2, 3, and 4 of the Z7 byte when extended RDI is enabled (ERDI set to logic 1) and all the bits of the Z7 byte when extended RDI is disabled (ERDI set to logic 0).

Register 0x0DE2: TTOP TUG3 #3 Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	UPOHV	0
Bit 0	R/W	ICODE	0

This register contains control bits that are applicable to all tributaries in TUG3 #3.

ICODE:

The ICODE bit controls the value of the tributary payload bytes inserted into payload bytes of idle tributaries in TUG3 #3. When ICODE is set to logic 1, the tributary payload of an idle tributary (the corresponding IDLE bit set to logic 1) is set to all-ones. When ICODE is set to logic 0, the tributary payload is set to all-zeros.

UPOHV:

The UPOHV bit controls the value inserted into unused bits in tributary path overhead bytes of tributaries in TUG3 #3. When UPOHV is set to logic 1, unused tributary path overhead bits are set to logic 1. When UPOHV is set to logic 0, unused tributary path overhead bits are set to logic 0. Unused tributary POH bits include the J2 byte when trail trace identifier insertion is disabled (TTIEN set to logic 0), all bits in the Z6 byte, bits 1, 2, 3, and 4 of the Z7 byte when extended RDI is enabled (ERDI set to logic 1) and all the bits of the Z7 byte when extended RDI is disabled (ERDI set to logic 0).

Register 0x0DE4: TTOP Trail Trace Identifier Page Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	SBUFINUSE	0
Bit 0	R/W	USESB	0

This register allows the selection of one of either the primary RAM bank or the shadow buffer to be accessed in indirect operations. This register also triggers a shadow RAM use request for the tributary specified in the Indirect Trail Trace Identifier Buffer Address register. Active use of the shadow RAM by any tributary is also indicated within this register.

SBUFINUSE:

The shadow buffer RAM in use, SBUFINUSE, bit is a read only bit that identifies when the shadow buffer RAM is selected for use by one of the virtual tributaries. Use of the shadow buffer RAM is under explicit control of the USESB bit described below. When SBUFINUSE is logic 1, the shadow RAM is in use for the tributary designated at the time the USESB bit was set to logic 1. The trail trace identifier for the designated tributary can at this point be modified through an indirect access to the tributary trail trace identifier buffer RAM. When SBUFINUSE is low the shadow buffer RAM is not being used by any of the tributaries.

When USESB changes state, the transmission of the current tributary trail trace identifier completes before SBUFINUSE takes on the same state. Once SBUFINUSE equals USESB, one may then write to the buffer RAM currently not being used to insert the tributary trace identifier.

USESB:

The request shadow buffer RAM use bit, USESB, directs the TTOP block to begin using the shadow RAM for retrieval of the tributary trail trace identifier for the tributary specified in the TTOP Indirect Trail Trace Identifier Tributary Select register at the time the USESB bit is set. When USESB is set to logic 1, the trail trace identifier stored in the shadow RAM is read sequentially and inserted into the J2 byte of the corresponding tributary. When USESB is set to logic 0, the trail trace identifiers stored in the tributary trail trace identifier buffer RAM are read sequentially and inserted into the J2 byte of the corresponding tributary. When setting the USESB bit from low to high or high to low, the corresponding tributary must be identified in the TTOP Indirect Trail Trace Identifier Tributary Select register. Upon selecting a new tributary, the USESB value is updated to reflect the state of the tributary. Switches between the RAM to be accessed, as a result of write accesses to USESB, are synchronized to the start of the trail trace identifier of each tributary. In other words, the requested change will not occur until after the last byte of the trail trace identifier in the current RAM is written out.

Register 0x0DE5: TTOP Indirect Trail Trace Identifier Tributary Select

Bit	Type	Function	Default
Bit 7	R/W	TUG3[1]	0
Bit 6	R/W	TUG3[0]	0
Bit 5	R/W	TUG2[2]	0
Bit 4	R/W	TUG2[1]	0
Bit 3	R/W	TUG2[0]	0
Bit 2	R/W	TU[2]	0
Bit 1	R/W	TU[1]	0
Bit 0	R/W	TU[0]	0

This register provides the tributary number used to access the tributary trail trace identifier buffer RAM. Writing to this register does not trigger an indirect time switch configuration register access.

In order to access the buffered RAM of the TTOP Trail Trace Message, one must set all bits of this register to logic 0. Then the trail trace message can be written into RAM via the TTOP Indirect Trail Trace Identifier Buffer Address and TTOP Indirect Trail Trace Identifier Buffer Data registers.

The Indirect Trail Trace Identifier Buffer Address register must be written to in order to trigger an indirect tributary trail trace identifier buffer register access. In order to obtain predictable indirect access results, the Indirect Trail Trace Identifier Tributary Select register should be modified (if necessary) prior to writing to the Indirect Trail Trace Identifier Buffer Address register.

The buffered RAM can then be used by setting USESB the TTOP Trail Trace Identifier Page Select register to logic 1.

TU[2:0]:

The indirect tributary unit bits (TU[2:0]) indicate the tributary unit to be configured or interrogated in the indirect access. Legal TU[2:0] ranges are ‘b001 to ‘b100. Out of range values will result in undefined results during indirect access operations.

TUG2[2:0]:

The indirect tributary unit group 2 bits (TUG2[2:0]) indicate the tributary unit group 2 to be configured or interrogated in the indirect access. Legal TUG2[2:0] ranges are ‘b001 to ‘b111. Out of range values will result in undefined results during indirect access operations.

TUG3[1:0]:

The indirect tributary unit group 3 bits (TUG2[1:0]) indicate the tributary unit group 3 to be configured or interrogated in the indirect access. Legal TUG3[1:0] ranges are ‘b01 to ‘b11. Out of range values will result in undefined results during indirect access operations.

Register 0x0DE6: TTOP Indirect Trail Trace Identifier Buffer Address

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6	R/W	RWB	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register provides the buffer location used to access the trail trace identifier buffer RAM. Writing to this register triggers an indirect time trail trace buffer access.

A[5:0]:

The A[5:0] indexes into the trail trace identifier buffer associated with the tributary specified by the Trail Trace Identifier Tributary Select register. Selection between the trail trace identifier buffer and the shadow buffer of the trail trace identifier buffer RAM is controlled by the USESB register bit.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the trial trace identifier buffer of the associated tributary. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the Indirect Tributary Data register. Writing a logic one to RWB triggers an indirect read operation. The read can be found in the Indirect Tributary Data register.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when a write to the Indirect Trail trace Identifier Buffer Address register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Trail trace Identifier Buffer Data register or to determine when a new indirect write

operation may commence. If LREFCLK disappears during an access, the BUSY bit can stay high.

Register 0x0DE7: TTOP Indirect Trail Trace Identifier Buffer Data

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains data read from the TTOP tributary trail trace identifier buffer RAM after an indirect channel read operation or it contains data to be inserted into the tributary trail trace identifier buffer RAM in an indirect channel write operation.

D[7:0]:

The D[7:0] bits reports the data read from the trail trace identifier buffer associated with the tributary specified by the Trail Trace Identifier Tributary Select register after an indirect read operation has completed. Data to be written to the associated tributary buffer in an indirect write operation must be set up in this register before triggering the write operation. Data in this register reflects the value written until the completion of the subsequent indirect read operation.

1.46 TTMP Transmit Tributary Mapper Registers

Registers 0x0E00 - 0x0E5E: TTMP Tributary Control

TU Address Map:

TUG3	TUG2	TU #1	TU #2	TU #3	TU #4
1	1	0xE00	0xE08	0xE10	0xE18
1	2	0xE01	0xE09	0xE11	0xE19
1	3	0xE02	0xE0A	0xE12	0xE1A
1	4	0xE03	0xE0B	0xE13	0xE1B
1	5	0xE04	0xE0C	0xE14	0xE1C
1	6	0xE05	0xE0D	0xE15	0xE1D
1	7	0xE06	0xE0E	0xE16	0xE1E
2	1	0xE20	0xE28	0xE30	0xE38
2	2	0xE21	0xE29	0xE31	0xE39
2	3	0xE22	0xE2A	0xE32	0xE3A
2	4	0xE23	0xE2B	0xE33	0xE3B
2	5	0xE24	0xE2C	0xE34	0xE3C
2	6	0xE25	0xE2D	0xE35	0xE3D
2	7	0xE26	0xE2E	0xE36	0xE3E
3	1	0xE40	0xE48	0xE50	0xE58
3	2	0xE41	0xE49	0xE51	0xE59
3	3	0xE42	0xE4A	0xE52	0xE5A
3	4	0xE43	0xE4B	0xE53	0xE5B
3	5	0xE44	0xE4C	0xE54	0xE5C
3	6	0xE45	0xE4D	0xE55	0xE5D
3	7	0xE46	0xE4E	0xE56	0xE5E

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ETVTPTRDIS	0
Bit 1	R/W	ETVT	0
Bit 0	R/W	LAOE	0

LAOE:

The Line Add Bus Output Enable bit, LAOE, enables individual tributaries to be output on the line side telecom bus. When LAOE is a logic 0, the tributary's columns will be high impedance on the Line Add bus. When LAOE is a logic 1, the tributary will be output on the Line Add bus. The state of this bit is also reflected in the tributary's columns on the LAOE (Line Add Bus Output Enable) output.

ETVT:

The Egress Transparent Virtual Tributary control bit, ETVT, selects a Transparent VT from the SBI bus interface in place of a T1 or E1 mapped into a VT1.5 or VT2. When ETVT is a logic 0 the T1 or E1 will be asynchronous mapped into a virtual tributary in the egress direction. When ETVT is a logic 1, the transparent virtual tributary from the SBI bus will be output in the egress direction. The TU11 bit in this register controls whether the tributary is a TU-11/VT1.5 or a TU-12/VT2.

The Egress VTPPs must not be bypassed when TVTs exist; the EVTPPBYP bit of the SONET/SDH Master Egress VTPP Configuration register must be logic 0.

ETVTPTRDIS:

The Egress Transparent Virtual Tributary pointer disable bit, ETVTPTRDIS, selects whether the V1,V2 pointers with the egress transparent virtual tributary, enabled via the ETVT register bit, are valid. Transparent virtual tributaries from the SBI can be configured to have valid pointers or can use the SBI V5 signal to indicate transparent VT alignment. When the egress

transparent VT has a valid pointer, the ETVTPTRDIS bit should be set to 0 so that the egress VTPP will process the pointer and if required align the TVT to the telecom Add bus. When the egress transparent virtual tributary does not have valid pointer the ETVTPTRDIS bit must be set to 1 so that the egress VTPP does not attempt to interpret the V1 and V2 pointers and instead uses the V5 indicator to align the transparent VT.

Pointer interpretation may be globally disabled via the EPTRBYP bits of the SONET/SDH Master Egress VTPP Configuration register. Setting EPTRBYP to logic 1, is the same as setting all ETVTPTRDIS bits for an SPE to logic 1.

ETVTPTRDIS or EPTRBYP must be logic 1 for byte synchronously mapped tributaries.

PROV:

The Provisioned, PROV, bit enables processing of this tributary. When PROV is set to logic 1, this tributary is mapped normally into either a VT1.5 Payload or VT2 Payload as controlled by the TU11 and T1 bits. When PROV is set to logic 0, this tributary is not processed.

The priority of the per-tributary mapping configuration bits is given below.

ETVT	ENBL bit of the Byte Synch. Mapper	PROV	Configuration
1	X	0	Transparent VT from the SBI ADD Bus.
0	1	X	Byte synchronously mapped VT. (The PROV bit must be set to enable AIS insertion as controlled by the EGRALMEN bit.)
0	0	1	Bit asynchronously mapped VT.
0	0	0	No mapping. The VT contains valid overhead, but the payload is all zeros.

TU11 and T1 Bits:

The TU11 and T1 bits specify the configuration of this tributary.

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	X	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

All tributaries in each VT Group must be configured to the same tributary type (i.e. VT1.5 or VT2). In fact, for each VT Group, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the VT Group are read-only. The T1 bit must be configured the same for each individual tributary.

Register 0x0E61: TTMP Time Switch Page Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	APAGE	0

This register allows selection of one of two pages in the time switch configuration RAM to be the active page.

APAGE:

The time switch configuration RAM active page select bit, APAGE, controls the selection of one of two pages in the time switch configuration RAM to be the active page. When APAGE is set to logic 1, the configuration in page 1 of the time switch configuration RAM is used to associate outgoing VT Payloads to logical FIFOs in the payload buffer. When APAGE is set to logic 0, the configuration in page 0 of the time switch configuration RAM is used to associate outgoing VT Payloads to logical FIFOs in the payload buffer.

Register 0x0E62: TTMP Indirect Time Switch RAM Control and Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6	R/W	RWB	1
Bit 5	R/W	PAGE	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register provides control and status for the indirect RAM containing time switch tributary information. **Writing to this register triggers an indirect time switch configuration register access.** Note that when an indirect write access is to be performed, the Indirect Time Switch Internal Link Data register and the Indirect Egress Tributary Address register must first be setup before writing to this register.

PAGE:

The indirect page select bit, PAGE, selects between accesses to the two pages in the time switch configuration RAM. When PAGE is set to logic 1, page 1 of the time switch configuration RAM is accessed. When PAGE is set to logic 0, page 0 of the RAM is accessed. The PAGE bit should be different than the APAGE bit (register 0x0E61) when writing to the RAM as writing to the active page is not recommended.

RWB:

The indirect access control bit, RWB, selects between a configure (write) or interrogate (read) access to the time switch configuration RAM. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the Indirect Time Switch Tributary register. Writing a logic one to RWB triggers an indirect read operation. The read can be found in the Indirect Tributary Data register.

BUSY:

The BUSY bit reports the status of the prevailing indirect access operation. BUSY is set to logic 1 when a write to the Indirect Time Switch Tributary Address register triggers an indirect access and remains high until the access is complete. The BUSY bit should be polled until it is low to determine when data from an indirect read operation is available in the Indirect Tributary Data register or when a new indirect write operation may commence. If LREFCLK disappears during an access, the BUSY bit can stay high.

Register 0x0E63: TTMP Indirect Egress Tributary Address

Bit	Type	Function	Default
Bit 7	R/W	EGR_TUG3[1]	0
Bit 6	R/W	EGR_TUG3[0]	1
Bit 5	R/W	EGR_TUG2[2]	0
Bit 4	R/W	EGR_TUG2[1]	0
Bit 3	R/W	EGR_TUG2[0]	1
Bit 2	R/W	EGR_TU[2]	0
Bit 1	R/W	EGR_TU[1]	0
Bit 0	R/W	EGR_TU[0]	1

The address specified by this register is the tributary identifier for egress tributaries out of the TEMUX 84 that are switched from internal links when the Egress Time Switch Enable register bit, ETSEN, in the Master SONET/SDH Master Egress Configuration register is a logic 1. The internal link that will be switched to the egress tributary is the internal link specified in the TTMP Indirect Time Switch Internal Link Data register and is indirectly accessed in the time switch RAM at the address specified by this register.

EGR_TU[2:0]:

The indirect egress tributary unit bits, EGR_TU[2:0], indicate the tributary unit that internal links identified in the TTMP Indirect Time Switch Internal Link Data register will be switched to. Legal EGR_TU[2:0] ranges are ‘b001 to ‘b100.

EGR_TUG2[2:0]:

The indirect egress tributary unit group 2 bits, EGR_TUG2[2:0], indicate the tributary unit group 2 that internal links identified in the TTMP Indirect Time Switch Internal Link Data register will be switched to. Legal EGR_TUG2[2:0] ranges are ‘b001 to ‘b111.

EGR_TUG3[1:0]:

The indirect egress tributary unit group 3 bits, EGR_TUG2[1:0], indicate the tributary unit group 3 that internal links identified in the TTMP Indirect Time Switch Internal Link Data register will be switched to. Legal EGR_TUG3[1:0] ranges are ‘b01 to ‘b11.

Register 0x0E64: TTMP Indirect Time Switch Internal Link Data

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	INT_SPE[1]	X
Bit 5	R/W	INT_SPE[0]	X
Bit 4	R/W	INT_LINK[4]	X
Bit 3	R/W	INT_LINK[3]	X
Bit 2	R/W	INT_LINK[2]	X
Bit 1	R/W	INT_LINK[1]	X
Bit 0	R/W	INT_LINK[0]	X

This register identifies an internal link that will be switched to an egress tributary through the egress time switch RAM. An indirect access to the TTMP egress time switch RAM associates the internal link specified in this register with the egress link specified as the time switch address in the TTMP Indirect Egress Tributary Address register. The time switch configuration via this indirect register are inactive when the Egress Time Switch Enable register bit, ETSEN, in the Master SONET/SDH Egress Configuration register is a logic 0.

INT_LINK [4:0]:

The indirect internal link number bits, INT_LINK[4:0], associate the specified T1 or E1 internal link with the egress tributary specified in the TTMP Indirect Egress Tributary Address register. In an indirect write operation, the internal link number to be written to the time switch configuration RAM at the egress tributary address must be set up in this register before triggering the indirect write. When read back, INT_LINK[4:0] reflects the value written until the completion of a subsequent indirect channel read operation. INT_LINK[4:0] ranges from 00001b to 10101b (1 to 21) for E1 streams and from 00001b to 11100b (1 to 28) for T1 streams.

INT_SPE[1:0]:

The indirect internal synchronous payload envelope bits, INT_ SPE[1:0], associate the specified T1 or E1 internal link with the tributary specified in the TTMP Indirect Egress Tributary Address register. In an indirect write operation, the internal SPE number to be written to the time switch configuration RAM at the egress tributary address must be set up in this

register before triggering the indirect write. INT_SPE[1:0] reflects the value written until the completion of a subsequent indirect channel read operation.

Register 0x0E65: TTMP Telecom Interface Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	LOCK0	0

LOCK0:

LOCK0 configures the position of the SPE in the egress direction when the egress VTPP is bypassed. When LOCK0 is logic 1 the H1,H2 pointer is set to zero and the first byte of the SPE (J1) will occur immediately after H3. When LOCK0 is a logic 0 the H1,H2 pointer is set to 522 and the first byte of the SPE will occur immediately after C1. (Note: A valid H1,H2 pointer is only encoded when the EVTPPBYP register bit is logic 1.)

When using the TEMUX 84 with Transparent VTs between the SBI bus and the line side telecom bus LOCK0 must be set to 0 such that J1 immediately follows C1.

1.47 D3MD DS3 Drop Side Mapper Registers (N = 0 to 2)

There is a set of D3MD registers for each TUG3.

Register 0x0E80 + 0x4*N: D3MD Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AISGEN	0

AISGEN:

The active high DS3 Alarm Indication Signal enable bit, AISGEN, configures the TEMUX 84 to generate a DS3 AIS signal in the ingress data stream. Any data on the STS-1 SPE is lost due to the assertion of AISGEN.

Register 0x0E81 + 0x4*N: D3MD Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OFLI	0
Bit 0	R	UFLI	0

The OFLI and UFLI bits and the interrupt are cleared when this register is read.

OFLI:

When a logic 1, this bit indicates that an overflow condition has occurred in the elastic store. This error resets the elastic store's read and write addresses to 180° apart.

UFLI:

When a logic 1, this bit indicates that an underflow condition has occurred in the elastic store. This error resets the elastic store's read and write addresses to 180° apart.

Register 0x0E82 + 0x4*N: D3MD Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	OFLIEN	0
Bit 0	R/W	UFLIEN	0

OFLIEN:

When set to logic 1, this bit enables generation of an interrupt if an elastic store overflow condition, OFLI, occurs.

UFLIEN:

When set to logic 1, this bit enables generation of an interrupt if an elastic store underflow condition, UFLI, occurs.

1.48 D3MA DS3 Add Side Mapper Registers (N = 0 to 2)

There is a set of D3MA registers for each TUG3.

Register 0x0E8C + 0x4*N: D3MA Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RBSO	0
Bit 0	R/W	AISGEN	0

AISGEN:

The active high DS3 Alarm Indication Signal enable bit, AISGEN, configures the TEMUX 84 to generate a DS3 AIS signal in the egress data stream. Any data on the STS-1 SPE is lost due to the assertion of AISGEN.

RBSO:

When RBSO is a logic 1, R bits are set to ‘1’s. If RBSO bit is a logic 0, R bits are set to ‘0’s.

Register 0x0E8D + 0x4*N: D3MA Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OFLI	0
Bit 0	R	UFLI	0

The OFLI and UFLI bits and the interrupt are cleared when this register is read.

OFLI:

When set to logic 1, this bit indicates that an overflow condition has occurred in the elastic store. This error resets the elastic store's read and write addresses to 180° apart.

UFLI:

When set to logic 1, this bit indicates that an underflow condition has occurred in the elastic store. This error resets the elastic store's read and write addresses to 180° apart.

Register 0x0E8E + 0x4*N: D3MA Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	OFLIEN	0
Bit 0	R/W	UFLIEN	0

OFLIEN:

When set to a logic 1, this bit enables generation of an interrupt if an elastic store overflow condition, OFLI, occurs.

UFLIEN:

When set to logic 1, this bit enables generation of an interrupt if an elastic store underflow condition, UFLI, occurs.

1.49 RTTB Receive Tributary Trail Trace Registers (N = 0 to 2)

There is a set of RTTB registers for each TUG3.

Register 0x0F00 + 0x40*N: RTTB TU3 or TU #1 in TUG2 #1, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	CONFIG[1]	1
Bit 6	R/W	CONFIG[0]	1
Bit 5	R/W	NOSYNC	0
Bit 4	R/W	LEN16	0
Bit 3	R	TIMV	X
Bit 2	R/W	TIME	0
Bit 1	R	TIUV	X
Bit 0	R/W	TIUE	0

In TU3 mode, this register reports the status and configures operational modes of the TU3 mapped into a TUG3. Out of TU3 mode, this register reports the status and configures the operational modes of TU #1 in TUG2 #1.

TIUE:

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #1 in TUG2 #1 or TU3 depending on whether the RTTB is operating in TU3 mode. When TIUE is set to logic 1, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set to logic 0.

TIUV:

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #1 in TUG2 #1 or TU3 depending on whether the RTTB is operating in TU3 mode.

TIME:

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #1 in TUG2 #1 or TU3 depending on whether the RTTB is operating in TU3 mode. When TIME is set to logic 1, an interrupt is generated upon

detection of a mismatched identifier and upon return to a matched identifier. Interrupts due to TIM status change are masked when TIME is set to logic 0.

TIMV:

The TIUV bit indicates the trail trace identifier mismatch status of tributary TU #1 in TUG2 #1 or TU3 depending on whether the RTTB is operating in TU3 mode.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #1 in TUG2 #1 or TU3 depending on whether the RTTB is operating in TU3 mode. When LEN16 is set to logic 1, the message length is set to 16 bytes. When LEN16 is set to logic 0, the message length is set to 64 bytes.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #1 in TUG2 #1 or TU3 depending on whether the RTTB is operating in TU3 mode. When LEN16 is set to logic 1 and NOSYNC is set to logic 0, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set to logic 0, and NOSYNC is also set to logic 0, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set to logic 1, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of tributary group TUG2 #1. The CONFIG[1:0] bits have no effect in TU3 mode. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	Reserved	
0	1	Reserved	
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 0x0F01 to 0x0F06 + 0x40*N: RTTB TU #1 in TUG2 #2 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	CONFIG[1]	1
Bit 6	R/W	CONFIG[0]	1
Bit 5	R/W	NOSYNC	0
Bit 4	R/W	LEN16	0
Bit 3	R	TIMV	X
Bit 2	R/W	TIME	0
Bit 1	R	TIUV	X
Bit 0	R/W	TIUE	0

This set of registers reports the status and configures the operational modes of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

TIUE:

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #1 in the corresponding TUG2. When TIUE is set to logic 1, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set to logic 0.

TIUV:

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #1 in the corresponding TUG2.

TIME:

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #1 in the corresponding TUG2. When TIME is set to logic 1, an interrupt is generated upon detection of a mismatched identifier and upon return to a matched identifier. Interrupts due to TIM status change are masked when TIME is set to logic 0.

TIMV:

The TIMV bit indicates the trail trace identifier mismatch status of tributary TU #1 in the corresponding TUG2.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #1 in the corresponding TUG2. When LEN16 is set to logic 1, the message length is set to 16 bytes. When LEN16 is set to logic 0, the message length is set to 64 bytes.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #1 in the corresponing TUG2. When LEN16 is set to logic 1 and NOSYNC is set to logic 0, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set to logic 0, and NOSYNC is also set to logic 0, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set to logic 1, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding tributary group TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	Reserved	
0	1	Reserved	
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 0x0F08 to 0x0F0E + 0x40*N: RTTB TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	NOSYNC	0
Bit 4	R/W	LEN16	0
Bit 3	R	TIMV	X
Bit 2	R/W	TIME	0
Bit 1	R	TIUV	X
Bit 0	R/W	TIUE	0

This set of registers reports the status and configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode.

TIUE:

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #2 in the corresponding TUG2. When TIUE is set to logic 1, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set to logic 0.

TIUV:

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #2 in the corresponding TUG2.

TIME:

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #2 in the corresponding TUG2. When TIME is set to logic 1, an interrupt is generated upon detection of a mismatched identifier and upon return to a matched identifier. Interrupts due to TIM status change are masked when TIME is set to logic 0.

TIMV:

The TIMV bit indicates the trail trace identifier mismatch status of tributary TU #2 in the corresponding TUG2.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #2 in the corresponding TUG2. When LEN16 is set to logic 1, the message length is set to 16 bytes. When LEN16 is set to logic 0, the message length is set to 64 bytes.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #2 in the corresponding TUG2. When LEN16 is set to logic 1 and NOSYNC is set to logic 0, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set to logic 0, and NOSYNC is also set to logic 0, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set to logic 1, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding tributary group TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	Reserved	
0	1	Reserved	
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 0x0F10H to 0x0F16 + 0x40*N: RTTB TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	NOSYNC	0
Bit 4	R/W	LEN16	0
Bit 3	R	TIMV	X
Bit 2	R/W	TIME	0
Bit 1	R	TIUV	X
Bit 0	R/W	TIUE	0

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode.

TIUE:

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #3 in the corresponding TUG2. When TIUE is set to logic 1, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set to logic 0.

TIUV:

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #3 in the corresponding TUG2.

TIME:

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #3 in the corresponding TUG2. When TIME is set to logic 1, an interrupt is generated upon detection of a mismatched identifier and upon return to a matched identifier. Interrupts due to TIM status change are masked when TIME is set to logic 0.

TIMV:

The TIMV bit indicates the trail trace identifier mismatch status of tributary TU #3 in the corresponding TUG2.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #3 in the corresponding TUG2. When LEN16 is set to logic 1, the message length is set to 16 bytes. When LEN16 is set to logic 0, the message length is set to 64 bytes.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #3 in the corresponding TUG2. When LEN16 is set to logic 1 and NOSYNC is set to logic 0, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set to logic 0, and NOSYNC is also set to logic 0, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set to logic 1, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding tributary group TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	Reserved	
0	1	Reserved	
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Registers 0x0F18 to 0x0F1E + 0x40*N: RTTB TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	NOSYNC	0
Bit 4	R/W	LEN16	0
Bit 3	R	TIMV	X
Bit 2	R/W	TIME	0
Bit 1	R	TIUV	X
Bit 0	R/W	TIUE	0

This set of registers reports the status and configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

TIUE:

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #4 in the corresponding TUG2. When TIUE is set to logic 1, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set to logic 0.

TIUV:

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #4 in the corresponding TUG2.

TIME:

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #4 in the corresponding TUG2. When TIME is set to logic 1, an interrupt is generated upon detection of a mismatched identifier and upon return to a matched identifier. Interrupts due to TIM status change are masked when TIME is set to logic 0.

TIMV:

The TIUV bit indicates the trail trace identifier mismatch status of tributary TU #4 in the corresponding TUG2.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #4 in the corresponding TUG2. When LEN16 is set to logic 1, the message length is set to 16 bytes. When LEN16 is set to logic 0, the message length is set to 64 bytes.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #4 in the corresponding TUG2. When LEN16 is set to logic 1 and NOSYNC is set to logic 0, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set to logic 0, and NOSYNC is also set to logic 0, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set to logic 1, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding tributary group TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	Reserved	
0	1	Reserved	
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 0x0F20 + 0x40*N: RTTB TU3 or TU #1 in TUG2 #1 to TUG2 #7, TIM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIM7I	0
Bit 5	R	TIM6I	0
Bit 4	R	TIM5I	0
Bit 3	R	TIM4I	0
Bit 2	R	TIM3I	0
Bit 1	R	TIM2I	0
Bit 0	R	TIM1I	0

This register is used to identify and acknowledge trail trace identifier mismatch interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 trail trace identifier mismatch interrupts.

TIM1I:

The TIM1I bit identifies the source of trail trace identifier mismatch interrupts. In TU3 mode, The TIM1I bit reports and acknowledges TIM interrupt of the TU3 trail trace identifier. Out of TU3 mode, TIM1I bit reports and acknowledges TIM interrupt of TU #1 in TUG2 #1. Interrupts are generated upon change of identifier mismatch state. The TIM1I bit is set to logic 1 when a trail trace identifier mismatch event and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. the TIM1I bit remains valid when interrupts are not enabled (TIME set to logic 0) and may be polled to detect trail trace identifier mismatch events.

TIM2I-TIM7I:

The TIM2I to TIM7I bits identify the source of trail trace identifier mismatch interrupts. TIM2I to TIM7I bits report and acknowledge TIM interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon change of identifier mismatch state. An TIM*x*I bit is set to logic 1 when a trail trace identifier mismatch event on the corresponding tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIM*x*I remains valid when

interrupts are not enabled (TIME set to logic 0) and may be polled to detect trail trace identifier mismatch events.

Register 0x0F21 + 0x40*N: RTTB TU #2 in TUG2 #1 to TUG2 #7, TIM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIM7I	0
Bit 5	R	TIM6I	0
Bit 4	R	TIM5I	0
Bit 3	R	TIM4I	0
Bit 2	R	TIM3I	0
Bit 1	R	TIM2I	0
Bit 0	R	TIM1I	0

This register is used to identify and acknowledge trail trace identifier mismatch interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

TIM1I-TIM7I:

The TIM1I to TIM7I bits identify the source of trail trace identifier mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When operational, the TIM1I to TIM7I bits report and acknowledge TIM interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier mismatch state. An TIM*x*I bit is set to logic 1 when a trail trace identifier mismatch event on the corresponding tributary (TU #2 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIM*x*I remains valid when interrupts are not enabled (TIME set to logic 0) and may be polled to detect trail trace identifier mismatch events.

Register 0x0F22 + 0x40*N: RTTB TU #3 in TUG2 #1 to TUG2 #7, TIM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIM7I	0
Bit 5	R	TIM6I	0
Bit 4	R	TIM5I	0
Bit 3	R	TIM4I	0
Bit 2	R	TIM3I	0
Bit 1	R	TIM2I	0
Bit 0	R	TIM1I	0

This register is used to identify and acknowledge trail trace identifier mismatch interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

TIM1I-TIM7I:

The TIM1I to TIM7I bits identify the source of trail trace identifier mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When operational, the TIM1I to TIM7I bits report and acknowledge TIM interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier mismatch state. An TIM*x*I bit is set to logic 1 when a trail trace identifier mismatch event on the corresponding tributary (TU #3 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIM*x*I remains valid when interrupts are not enabled (TIME set to logic 0) and may be polled to detect trail trace identifier mismatch events.

Register 0x0F23 + 0x40*N: RTTB TU #4 in TUG2 #1 to TUG2 #7, TIM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIM7I	0
Bit 5	R	TIM6I	0
Bit 4	R	TIM5I	0
Bit 3	R	TIM4I	0
Bit 2	R	TIM3I	0
Bit 1	R	TIM2I	0
Bit 0	R	TIM1I	0

This register is used to identify and acknowledge trail trace identifier mismatch interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

TIM1I-TIM7I:

The TIM1I to TIM7I bits identify the source of trail trace identifier mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated TIM*x*I bit is unused and will return a logic 0 when read. When operational, the TIM1I to TIM7I bits report and acknowledge TIM interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier mismatch state. An TIM*x*I bit is set to logic 1 when a trail trace identifier mismatch event on the corresponding tributary (TU #4 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIM*x*I remains valid when interrupts are not enabled (TIME set to logic 0) and may be polled to detect trail trace identifier mismatch events.

Register 0x0F24 + 0x40*N: RTTB TU3 or TU #1 in TUG2 #1 to TUG2 #7, TIU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIU7I	0
Bit 5	R	TIU6I	0
Bit 4	R	TIU5I	0
Bit 3	R	TIU4I	0
Bit 2	R	TIU3I	0
Bit 1	R	TIU2I	0
Bit 0	R	TIU1I	0

This register is used to identify and acknowledge trail trace identifier unstable interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 trail trace identifier unstable interrupts.

TIU1I:

The TIU1I bit identifies the source of trail trace identifier unstable interrupts. In TU3 mode, The TIU1I bit reports and acknowledges TIU interrupt of the TU3 trail trace identifier. Out of TU3 mode, TIU1I bit reports and acknowledges TIU interrupt of TU #1 in TUG2 #1. Interrupts are generated upon change of identifier unstable state. The TIU1I bit is set to logic 1 when a trail trace identifier unstable event and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. the TIU1I bit remains valid when interrupts are not enabled (TIUE set to logic 0) and may be polled to detect trail trace identifier unstable events.

TIU2I-TIU7I:

The TIU2I to TIU7I bits identify the source of trail trace identifier unstable interrupts. TIU2I to TIU7I bits report and acknowledge TIU interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon change of identifier unstable state. An TIU*x*I bit is set to logic 1 when a trail trace identifier unstable event on the corresponding tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIU*x*I remains valid when

interrupts are not enabled (TIUE set to logic 0) and may be polled to detect trail trace identifier unstable events.

Register 0x0F25 + 0x40*N: RTTB TU #2 in TUG2 #1 to TUG2 #7, TIU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIU7I	0
Bit 5	R	TIU6I	0
Bit 4	R	TIU5I	0
Bit 3	R	TIU4I	0
Bit 2	R	TIU3I	0
Bit 1	R	TIU2I	0
Bit 0	R	TIU1I	0

This register is used to identify and acknowledge trail trace identifier unstable interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

TIU1I-TIU7I:

The TIU1I to TIU7I bits identify the source of trail trace identifier unstable interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When operational, the TIU1I to TIU7I bits report and acknowledge TIU interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier unstable state. An TIU*x*I bit is set to logic 1 when a trail trace identifier unstable event on the corresponding tributary (TU #2 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIU*x*I remains valid when interrupts are not enabled (TIUE set to logic 0) and may be polled to detect trail trace identifier unstable events.

Register 0x0F26 + 0x40*N: RTTB TU #3 in TUG2 #1 to TUG2 #7, TIU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIU7I	0
Bit 5	R	TIU6I	0
Bit 4	R	TIU5I	0
Bit 3	R	TIU4I	0
Bit 2	R	TIU3I	0
Bit 1	R	TIU2I	0
Bit 0	R	TIU1I	0

This register is used to identify and acknowledge trail trace identifier unstable interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

TIU1I-TIU7I:

The TIU1I to TIU7I bits identify the source of trail trace identifier unstable interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When operational, the TIU1I to TIU7I bits report and acknowledge TIU interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier unstable state. An TIU*x*I bit is set to logic 1 when a trail trace identifier unstable event on the corresponding tributary (TU #3 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIU*x*I remains valid when interrupts are not enabled (TIUE set to logic 0) and may be polled to detect trail trace identifier unstable events.

Register 0x0F27 + 0x40*N: RTTB TU #4 in TUG2 #1 to TUG2 #7, TIU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIU7I	0
Bit 5	R	TIU6I	0
Bit 4	R	TIU5I	0
Bit 3	R	TIU4I	0
Bit 2	R	TIU3I	0
Bit 1	R	TIU2I	0
Bit 0	R	TIU1I	0

This register is used to identify and acknowledge trail trace identifier unstable interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

TIU1I-TIU7I:

The TIU1I to TIU7I bits identify the source of trail trace identifier unstable interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated TIM*x*I bit is unused and will return a logic 0 when read. When operational, the TIU1I to TIU7I bits report and acknowledge TIU interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier unstable state. An TIU*x*I bit is set to logic 1 when a trail trace identifier unstable event on the corresponding tributary (TU #4 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIU*x*I remains valid when interrupts are not enabled (TIUE set to logic 0) and may be polled to detect trail trace identifier unstable events.

Register 0x0F28 + 0x40*N: RTTB TIU Threshold

Bit	Type	Function	Default
Bit 7	R/W	TIU64[3]	0
Bit 6	R/W	TIU64[2]	1
Bit 5	R/W	TIU64[1]	1
Bit 4	R/W	TIU64[0]	1
Bit 3	R/W	TIU16[3]	0
Bit 2	R/W	TIU16[2]	1
Bit 1	R/W	TIU16[1]	1
Bit 0	R/W	TIU16[0]	1

This register contains threshold for declaration of the trail trace identifier unstable alarm (TIU) for 16-byte and 64-byte tributary path trace messages.

TIU16[3:0]:

The 16-byte message trail trace identifier unstable threshold bits (TIU16[3:0]) controls the number of dissimilar tributary path trace messages needed to declare TIU. Each time a received message differs from the previous message, an unstable counter is incremented. When the count exceeds TIU16, the TIU alarm is declared. TIU is negated when a consistent message is repeated three times to become the accepted message.

TIU64[3:0]:

The 64-byte message trail trace identifier unstable threshold bits (TIU64[3:0]) controls the number of dissimilar tributary path trace messages needed to declare TIU. Each time a received message differs from the previous message, an unstable counter is incremented. When the count exceeds TIU64, the TIU alarm is declared. TIU is negated when a consistent message is repeated three times to become the accepted message.

Register 0x0F29 + 0x40*N: RTTB Indirect Tributary Select

Bit	Type	Function	Default
Bit 7	R/W	CPAGE	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4	R/W	TUG2[2]	0
Bit 3	R/W	TUG2[1]	0
Bit 2	R/W	TUG2[0]	0
Bit 1	R/W	TU[1]	0
Bit 0	R/W	TU[0]	0

This register contains the identity of the tributary buffer to be accessed in an indirect read or write operation.

TU[1:0]:

The tributary unit address bits (TU[1:0]) identifies the tributary within the tributary unit group which is identified by the TUG2[2:0] bits. The combination of TUG2[2:0] and TU[1:0] identifies the tributary buffer to be accessed indirectly. A value of 00 corresponds to the first tributary of the group.

TUG2[2:0]:

The tributary unit group address bits (TUG2[2:0]) identifies the tributary unit group. The combination of TUG2[2:0] and TU[1:0] identifies the tributary buffer to be accessed indirectly. The valid range of TUG2[2:0] is 0 to 6.

CPAGE:

The capture page control bit (CPAGE) selects between accessing the capture page and the expected page of the tributary buffer. When CPAGE is set to logic 1, the indirect register access is targeted at the capture page. Reading from the capture page returns the most recent tributary path trace message received from the incoming stream. No de-bouncing is provided. When CPAGE is set to logic 0, the indirect register access is targeted at the expected page. An expected trace message can be provisioned by writing to the expected page. Both the capture and expected pages may be read from or written to.

Register 0x0F2A + 0x40*N: RTTB Indirect Address Select

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6	R/W	RWB	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register provides the byte address within the tributary buffer addressed by the Indirect Tributary Select register. Writing to this register triggers an indirect register access.

A[5:0]:

The indirect address bits (A[5:0]) index into the receive and expected pages of the tributary buffers.

RWB:

The indirect access control bit (RWB) selects between a read and write operation into the tributary buffers. Writing a logic zero to RWB triggers an indirect write operation. The tributary buffer is selected by the TUG2[2:0] and TU[1:0] bits in the Indirect Tributary register. Selection between the capture page and the expected page is controlled by the RPAGE bit also in the Indirect Tributary register. Bytes within the tributary buffer is indexed by A[5:0]. Data to be written is taken from D[7:0] of the Indirect Data register. Writing a logic one to RWB triggers an indirect read operation. Tributary buffer, page, and byte addressing is the same as in an indirect write operation. The data read can be found in D[7:0] of the Indirect Data register.

BUSY:

The indirect access status but (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written to trigger an indirect access and will stay high until the access is complete. At which point, BUSY will be set to logic 0. This register should be polled to determine when

data from an indirect read operation is available in the Indirect Data register or to determine when a new indirect write operation may commence.

Register 0x0F2B + 0x40*N: RTTB Indirect Data Select

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from a tributary buffer after an indirect read operation or the data to be inserted into a tributary buffer in an indirect write operation. The data written is for comparison against received and validated messages.

D[7:0]:

The indirect data bits (D[7:0]) reports the data read from a tributary buffer after an indirect read operation has complete. Data to be written to a tributary buffer in an indirect write operation must be set up in this register before triggering the write. Data in this register reflects the value written until the completion of a subsequent indirect read operation.

NOTES

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